Ordering number : ENA1853A

SANYO Semiconductors
DATA SHEET

LC88F40H0PA/PAU
LC88F40F0PA/PAU
LC88F40D0PA/PAU

CMOS LSI
For Car Audio Systems
16-bit ETR Microcontroller
(ALL FLASH)

Overview

The LC88F40H0PA/PAU, LC88F40F0PA/PAU and LC88F40D0PA/PAU are 16-bit microcontrollers which are ideally suited as a system controller in car audio applications for the control of "MP3 and WMA and other compression decoders through CD/USB," "CD mechanisms and CD DSPs," "displays," and "DSP tuners." They are configured around a CPU that operates at a high speed, and incorporate an internal flash ROM (All Flash, onboard programmable) and RAM. These 16-bit microcontrollers integrate on a single chip such principal functions as on-chip debugging, 16-bit timer/counter (may be divided into 8-bit timers/counters), synchronous SIO (also used as the I^2C bus interface), UART (full duplex), 12-bit PWM, 12-bit resolution (8-bit resolution selectable) × 13-channel A/D converter, and 16 vector interrupts.

Microcontroller model line-up (list of ROM and RAM sizes)

Type No.	Flash ROM (byte)	RAM (byte)
LC88F40H0PA/PAU	512K	30K
LC88F40F0PA/PAU	384K	20K
LC88F40D0PA/PAU	256K	12K

Features

■Power supply voltage

- Main power supply voltage (V_{DD}CPU) 3.3V±0.3V
- I/O power supply (V_{DD}PORT) V_{DD}CPU to 5.5V

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■Flash ROM (ALL FLASH)
- Single 3.3V power supply, on-board writeable
- Block erase in 512 byte units

■Minimum instruction cycle time (Tcyc)
- 83.3ns

■Ports
- Normal withstand voltage I/O ports
  Ports whose I/O direction can be designated in 1 bit units : 86 (P0n, P1n, P2n, P3n, P4n, P5n, P6n, P7n
  PAn, PB0 to PB6, PC0, PD0 to PD5)
- Dedicated pin for low-pass filter connection : 1 (LPFO)
- Regulator pins : 1 (VREG)
- Reset pins : 1 (RESB)
- TEST pins : 1 (TEST)
- Dedicated pins for crystal oscillator : 2 (XT1, XT2)
- Power pins : 2 (V_{DD}CPU, V_{SS}1: Main power, I/O power supply)
  : 4 (V_{DD}PORT1 to 2, V_{SS}2 to 3: I/O power supply)
  : 2 (V_{DD}PLL, V_{SS}4: PLLVCO power)

■SIO: 6 channels (4 channels are also used as I^2C bus.)
- SIO0: 8 bit synchronous SIO
  1) LSB first/MSB first mode selectable
  2) Built-in 8-bit baudrate generator (4 to 512 transfer clock cycle)
  3) Automatic and continuous data transfer function to and from the RAM (max. 4096 bytes)
- SIO1: 8 bit synchronous SIO
  1) LSB first/MSB first mode selectable
  2) Built-in 8-bit baudrate generator (4 to 512 transfer clock cycle)
  3) Automatic and continuous data transfer function to and from the RAM (max. 4096 bytes)
- SMIIC0: Single master I^2C/8-bit synchronous SIO
  Mode 0: Single-master mode communication
  Mode 1: Synchronous 8-bit serial I/O (MSB first)
- SMIIC1: Single master I^2C/8-bit synchronous SIO
  Mode 0: Single-master mode communication
  Mode 1: Synchronous 8-bit serial I/O (MSB first)
- SMIIC2: Single master I^2C/8-bit synchronous SIO
  Mode 0: Single-master mode communication
  Mode 1: Synchronous 8-bit serial I/O (MSB first)
- SMIIC3: Single master I^2C/8-bit synchronous SIO
  Mode 0: Single-master mode communication
  Mode 1: Synchronous 8-bit serial I/O (MSB first)

■UART: 4 channels
  1) Data length : 8 bits (LSB first)
  2) Stop bits : 1 bit
  3) Parity bits : None/even parity/odd parity
  4) Transfer rate : 8 to 4096 cycle
  5) Baudrate source clock : System clock/XT clock/VCO clock
  5) Wakeup function
  6) Full duplex communication

■Timers

- Timer 0: 16-bit timer that supports PWM/toggle outputs
  1) 5-bit prescaler
  2) 8-bit PWM × 2, 8-bit timer + 8-bit PWM mode selectable
  3) Clock source selectable from system clock, XT clock, VCO clock, and internal RC oscillator
- Timer 1: 16-bit timer with capture registers
  1) 5-bit prescaler
  2) May be divided into 2 channels of 8-bit timer
  3) Clock source selectable from system clock, XT clock, VCO clock, and internal RC oscillator
- Timer 2: 16-bit timer with capture registers
  1) 4-bit prescaler
  2) May be divided into 2 channels of 8-bit timer
  3) Clock source selectable from system clock, XT clock, VCO clock, and external events
- Timer 3: 16-bit timer that supports PWM/toggle outputs
  1) 8-bit prescaler
  2) 8-bit PWM × 2ch or 8-bit timer + 8-bit PWM mode selectable
  3) Clock source selectable from system clock, XT clock, VCO clock, and external events
- Timer 4: 16-bit timer that supports toggle outputs
  1) Clock source selectable from system clock and prescaler 0
- Timer 5: 16-bit timer that supports toggle outputs
  1) Clock source selectable from system clock and prescaler 0
- Timer 6: 16-bit timer that supports toggle outputs
  1) Clock source selectable from system clock and prescaler 1
- Timer 7: 16-bit timer that supports toggle outputs
  1) Clock source selectable from system clock and prescaler 1

* Prescaler 0 and 1 are consisted of 4 bits and can choose their clock source from XT clock or VCO clock.

- Timer 8
  1) Clock source may be selected from XT clock (32.768kHz) and frequency-divided output of clock.
  2) Interrupts can be generated in 8 timing schemes.

- Watch timer
  1) Clock may be selected from XT clock (32.768kHz)
  2) Interrupts can be generated in 4 timing schemes.

■Day, minute and second counters

1) Count-up of clocks output from watch timer
2) Configured with day counter, minute counter, second counter
3) Continues operation when in HOLDX mode.

■AD converter

1) 12/8 bits resolution selectable
2) Analog input: 13 channels
3) Comparator mode
4) Automatic reference voltage generation

■PWM: Multifrequency 12-bit PWM × 4 channels
- PWM0: Multifrequency 12-bit PWM × 2 channels (PWM0A and PWM0B)
- PWM1: Multifrequency 12-bit PWM × 2 channels (PWM1A and PWM1B)

1) 2-channel pairs controlled independently of one another
2) Clock source selectable from system clock or VCO clock
3) 8-bit prescaler: TPWMR0 = (prescaler value + 1) × clock period
4) 8-bit fundamental wave PWM generator circuit + 4-bit additional pulse generator circuit
5) Fundamental wave PWM mode
   Fundamental wave period : 16 TPWMR0 to 256 TPWR0
   High pulse width : 0 to (Fundamental wave period - TPWMR0)
6) Fundamental wave + additional pulse mode
   Fundamental wave period : 16 TPWR0 to 256 TPWR0
   Overall period : Fundamental wave period × 16
   High pulse width : 0 to (Overall period - TPWR0)

■Watchdog Timer: 1 channel
- Driven by the timer 8 + internal watchdog timer dedicated counter
- Interrupt or reset mode selectable

■Interrupts
- 63 sources, 16 vector addresses

1) Provides three levels of multiplex interrupt control. Any interrupt requests of the level equal to or lower than the current interrupt are not accepted.
2) When interrupt requests to two or more vector addresses occur at the same time, the interrupt of the highest level takes precedence over the other interrupts. For interrupts of the same level, the interrupt into the smallest vector address takes precedence.

No.	Vector Address	Interrupt Source
1	08000H	WDT (1)
2	08004H	Timer 8 (2)/Watch timer (1)
3	08008H	Timer 0 (2)
4	0800CH	INT0 (1)
5	08010H	
6	08014H	INT1 (1)
7	08018H	INT2 (1)/timer 1 (2)/UART 2 (3)
8	0801CH	INT3 (1)/timer 2 (3)/SMIIC0 (1)
9	08020H	INT4 (1)/timer 3 (2)/SMIIC1 (1)/IR Remote control receive (4)
10	08024H	INT5 (1)/timer 4 (1)/SIO1 (2)
11	08028H	
12	0802CH	PWM0 (1)/PWM1 (1)/SMIIC2 (1)
13	08030H	ADC (1)/timer 5 (1)/SMIIC3 (1)
14	08034H	INT6 (1)/timer 6 (1)/UART 3 (3)
15	08038H	INT7 (1)/timer 7 (1)/SIO0 (2)/UART 4 (3)
16	0803CH	Port 0 (3)/Port 5 (8)/UART 5 (3)

- 3 priority levels selectable.
- Of interrupts of the same level, the one with the smallest vector address takes precedence.
- A number enclosed in parentheses denotes the number of sources.

■Subroutine Stack: Entire maximum RAM space (The stack is allocated in RAM.)
- Subroutine calls that automatically save PSW, interrupt vector calls: 6 bytes
- Subroutine calls that do not automatically save PSW: 4 bytes

■High-speed Multiplication/division instructions
- 16 bits × 16 bits
- 16 bits ÷ 16 bits
- 32 bits ÷ 16 bits

■Infrared remote controller receive functions

1) Noise rejection function
2) PPM(Pulse Position Modulation), compatible with Manchester and other data encoding systems.
3) HOLDX mode release function

■Oscillation circuits

- RC oscillator circuit (internal): For system clock
- XT oscillator circuit: For system clock
- VCO oscillator circuit (internal): For system clock

■Low power consumption

- HALT mode: Halts instruction execution while allowing the peripheral circuits to continue operation.
- HOLD mode: Suspends instruction execution and the operation of the peripheral circuits.
- HOLDX mode: Suspends instruction execution and operation of all the peripheral circuits except the modules run on the XT clock.

■System clock divider function

- Can run on low current.
- 1/1 to 1/128 of the system clock frequency can be set.

■Standby Function

- HALT mode: Halts instruction execution while allowing the peripheral circuits to continue operation.
  1) Both the XT oscillator and internal RC oscillator retain the state established when the standby mode is entered.
  2) Both the XT and VCO clocks retain the state established when the standby mode is entered.
  3) There are the two ways of releasing the HALT mode.
     (1) Generating a reset condition
     (2) Generating an interrupt

- HOLD mode: Suspends instruction execution and the operation of the peripheral circuits.
  1) Both the XT oscillator and internal RC oscillator automatically stop operation.
  2) XT clock and VCO clock oscillators automatically stop.
  3) There are the six ways of releasing the HOLD mode.
     (1) Generating a reset condition
     (2) Setting at least one of the INT0, INT1, INT2, INT4, INT5, INT6, and INT7 pins to the specified level
     (3) Having an interrupt source established at port 0
     (4) Having an interrupt source established at port 5
     (5) Having an interrupt request generated in UART2, UART3, UART4, or UART5
     (6) Having an interrupt request generated in SIO0 or SIO1

- HOLDX mode: Suspends instruction execution and operation of all the peripheral circuits except the modules run on the XT clock.
  1) The internal RC oscillator automatically stops operation.
  2) The XT clock retains the state established when the HOLDX mode is entered and the VCO clock automatically stops.
  3) There are nine ways of resetting the HOLDX mode.
     (1) Generating a reset condition
     (2) Setting at least one of the INT0, INT1, INT2, INT4, INT5, INT6, and INT7 pins to the specified level
     (3) Having an interrupt source established at port 0
     (4) Having an interrupt source established at port 5
     (5) Having an interrupt request generated in UART2, UART3, UART4, or UART5
     (6) Having an interrupt request generated in SIO0 or SIO1
     (7) Having an interrupt source established in the timer 8 circuit
     (8) Having an interrupt source established in the infrared remote controller receive circuit
     (9) Having an interrupt source established in the clock timer circuit

■Reset

- External reset
- Voltage drop detection type of reset circuit (VDET circuit) incorporated
  1) Normal mode detection voltage: 2.85V ±0.15V
  2) HOLD mode detection voltage: 1.42V ±0.15V

■On-chip debugger function

- Supports software debugging with the IC mounted on the target board.
- Supports source line debugging and tracing functions, and breakpoint setting and real time monitor.
- Single-wire communication

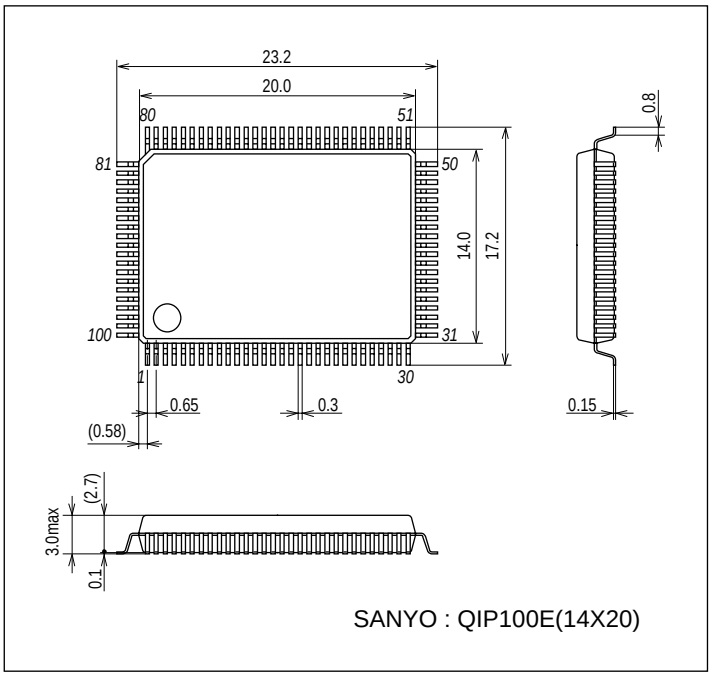
■Shipping Form

- QIP100E (Lead free product)

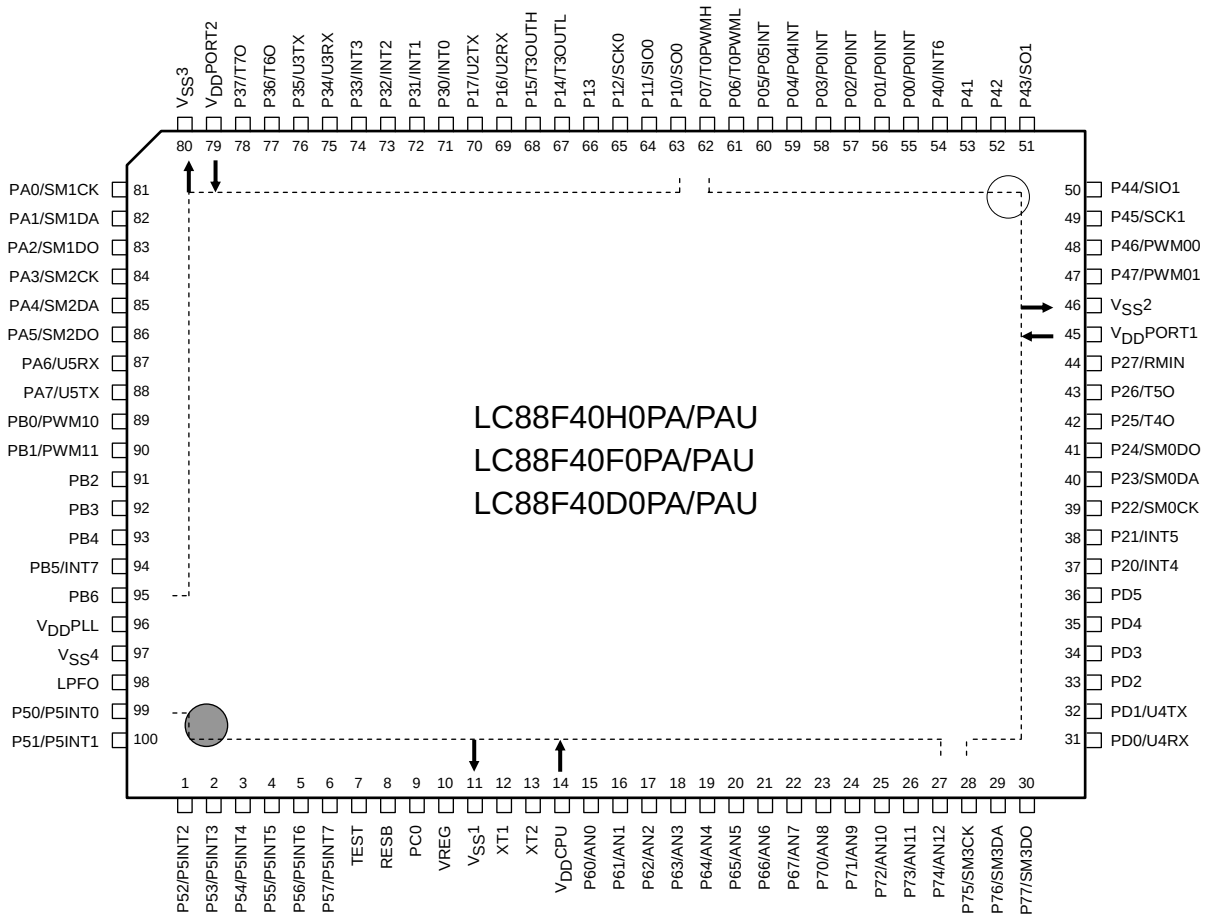
Package Dimensions

unit : mm (typ)

3151A

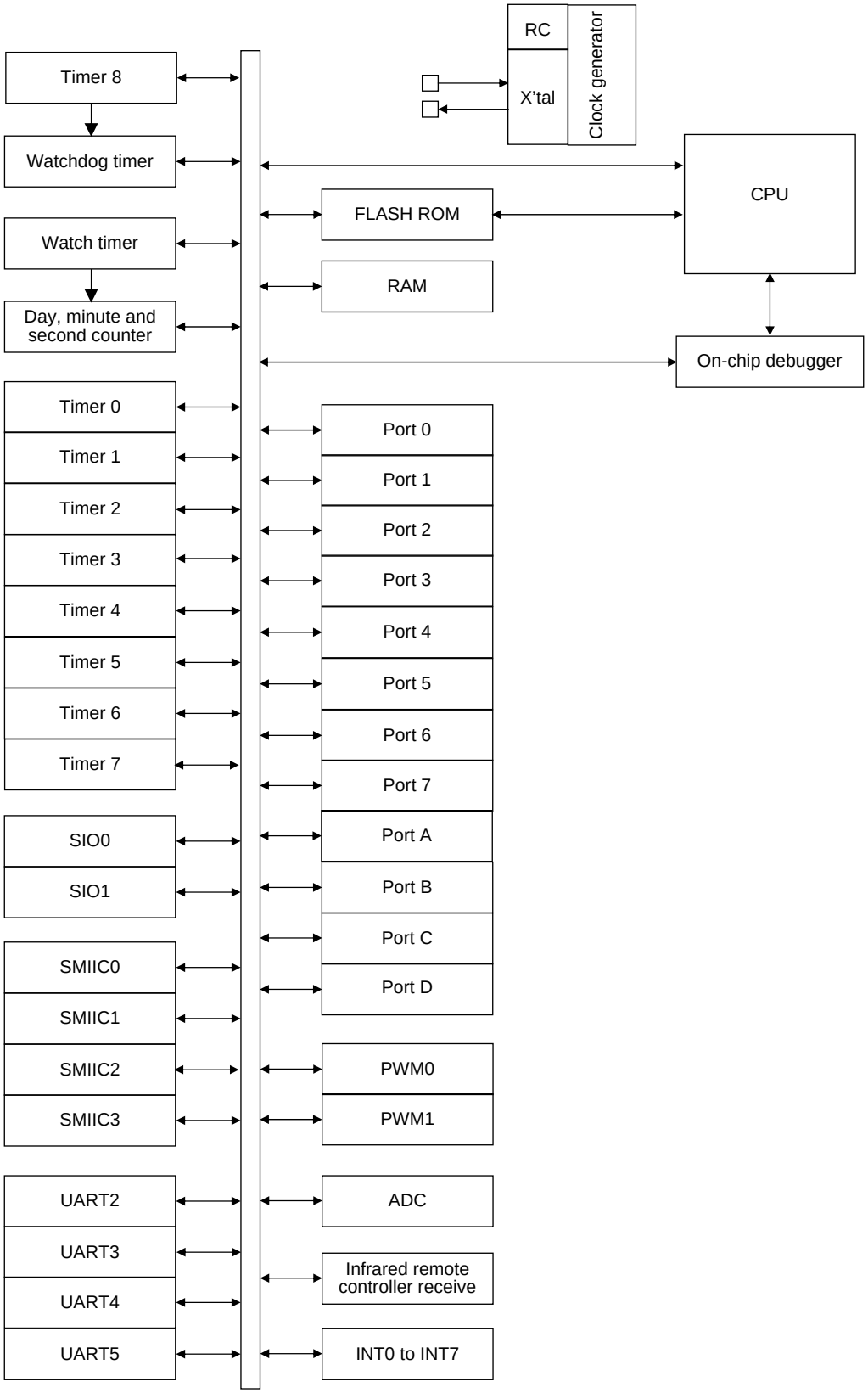


Pin Assignment



Top view

System Block Diagram



Pin Description

Name	I/O	Description	
V_{DD}CPU	-	+ Power sources 3.3V power supply (3.0 to 3.6V)	
V_{DD}PORT1	-	+ Power sources I/O power supply (V_{DD}CPU to 5.5V)	
V_{DD}PORT2	-	+ Power sources I/O power supply (V_{DD}CPU to 5.5V)	
V_{DD}PLL	-	+ Power sources PLLVCO power supply (3.0 to 3.6V)	
V_{SS}1	-	- Power sources	
V_{SS}2	-	- Power sources	
V_{SS}3	-	- Power sources	
V_{SS}4	-	- Power sources	
Port 0 P00 to P07	I/O	• 8-bit I/O port • I/O specifiable in 1-bit units • Pull-up resistors can be turned on and off in 1 bit units • Port 0 interrupt input (P00 to P05) • HOLD release input (P00 to P05) • Pin functions P06: Timer 0L output P07: Timer 0H output	Supply voltage from V_{DD}PORT1 used (V_{DD}CPU to 5.5V)
Port 1 P10 to P17	I/O	• 8-bit I/O port • I/O specifiable in 1-bit units • Pull-up resistors can be turned on and off in 1 bit units • Pin functions P10: SIO0 data output P11: SIO0 data input/output P12: SIO0 clock input/output P14: Timer 3L output P15: Timer 3H output P16: UART2 receive P17: UART2 transmit	Supply voltage from V_{DD}PORT2 used (V_{DD}CPU to 5.5V)
Port 2 P20 to P27	I/O	• 8-bit I/O port • I/O specifiable in 1-bit units • Pull-up resistors can be turned on and off in 1 bit units • Pin functions P20: INT4 input/HOLD release input/timer 3 event input/timer 2L capture input/ timer 2H capture input P21: INT5 input/HOLD release input/timer 3 event input/timer 2L capture input/ timer 2H capture input P22: SMIIC0 clock input/output P23: SMIIC0 data bus input/output P24: SMIIC0 data (used in 3-wire SIO mode) P25: Timer 4 output P26: Timer 5 output P27: Remote control receive • Interrupt acknowledge type INT4, INT5: H level, L level, H edge, L edge, both edges	Supply voltage from V_{DD}PORT1 used (V_{DD}CPU to 5.5V)
Port 3 P30 to P37	I/O	• 8-bit I/O port • I/O specifiable in 1-bit units • Pull-up resistors can be turned on and off in 1 bit units • Pin functions P30: INT0 input/HOLD release input/timer 2L capture input P31: INT1 input/HOLD release input/timer 2H capture input P32: INT2 input/HOLD release input/timer 2 event input/timer 2L capture input P33: INT3 input/HOLD release input/timer 2 event input/timer 2H capture input P34: UART3 receive P35: UART3 transmit P36: Timer 6 output P37: Timer 7 output • Interrupt acknowledge type INT0 to INT3: H level, L level, H edge, L edge, both edges	Supply voltage from V_{DD}PORT2 used (V_{DD}CPU to 5.5V)

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Name	I/O	Description	
Port 4 P40 to P47	I/O	• 8-bit I/O port • I/O specifiable in 1-bit units • Pull-up resistors can be turned on and off in 1 bit units • Pin functions P40: INT6 input/HOLD release input P43: SIO1 data output P44: SIO1 data input/output P45: SIO1 clock input/output P46: PWM00 output P47: PWM01 output • Interrupt acknowledge type INT6: H level, L level, H edge, L edge, both edges	Supply voltage from V_{DD}PORT1 used (V_{DD}CPU to 5.5V)
Port 5 P50 to P57	I/O	• 8-bit I/O port • I/O specifiable in 1-bit units • Pull-up resistors can be turned on and off in 1 bit units • Pin functions • Port 5 interrupt function • HOLD release input	Supply voltage from V_{DD}CPU used (3.0 to 3.6V)
Port 6 P60 to P67	I/O	• 8-bit I/O port • I/O specifiable in 1-bit units • Pull-up resistors can be turned on and off in 1 bit units • Pin functions AN0 (P60) to AN7 (P67): AD converter input port	Supply voltage from V_{DD}CPU used (3.0 to 3.6V)
Port 7 P70 to P77	I/O	• 8-bit I/O port • I/O specifiable in 1-bit units • Pull-up resistors can be turned on and off in 1 bit units • Pin functions AN8 (P70) to AN12 (P74): AD converter input port	Supply voltage from V_{DD}CPU used (3.0 to 3.6V)
		P75: SMIIC3 clock input/output P76: SMIIC3 data bus input/output P77: SMIIC3 data (used in 3-wire SIO mode)	Supply voltage from V_{DD}PORT1 used (V_{DD}CPU to 5.5V)
Port A PA0 to PA7	I/O	• 8-bit I/O port • I/O specifiable in 1-bit units • Pull-up resistors can be turned on and off in 1 bit units • Pin functions PA0: SMIIC1 clock input/output PA1: SMIIC1 data bus input/output PA2: SMIIC1 data (used in 3-wire SIO mode) PA3: SMIIC2 clock input/output PA4: SMIIC2 data bus input/output PA5: SMIIC2 data (used in 3-wire SIO mode) PA6: UART5 receive PA7: UART5 transmit	Supply voltage from V_{DD}PORT2 used (V_{DD}CPU to 5.5V)
Port B PB0 to PB6	I/O	• 7-bit I/O port • I/O specifiable in 1-bit units • Pull-up resistors can be turned on and off in 1 bit units • Pin functions PB0: PWM10 output PB1: PWM11 output PB5: INT7 input/HOLD release input • Interrupt acknowledge type INT7: H level, L level, H edge, L edge, both edges	Supply voltage from V_{DD}PORT2 used (V_{DD}CPU to 5.5V)
Port C PC0	I/O	• 1-bit I/O port • I/O specifiable in 1-bit units • Pull-up resistors can be turned on and off in 1 bit units	Supply voltage from V_{DD}CPU used (3.0 to 3.6V)
Port D PD0 to PD5	I/O	• 6-bit I/O port • I/O specifiable in 1-bit units • Pull-up resistors can be turned on and off in 1 bit units • Pin functions PD0: UART4 receive PD1: UART4 transmit	Supply voltage from V_{DD}PORT1 used (V_{DD}CPU to 5.5V)

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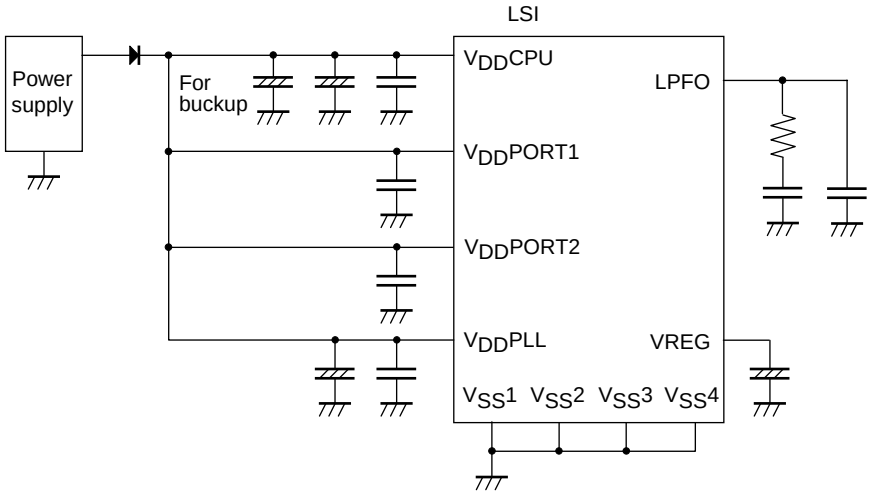
Name	I/O	Description
XT1	I	• Input terminal for 32.768kHz X'tal oscillation
XT2	O	• Output terminal for 32.768kHz X'tal oscillation
RESB	I	• Reset pin • This must be set to low for 50μs or longer when the power is turned on and when a reset is required.
TEST	I/O	• TEST pin • Used to communicate with on-chip debugger • 100kΩ pull-down
LPFO	O	• LPF connection pin for PLLVCO
VREG	O	• Regulator output pin Connect a bypass capacitor to this pin

Port Output Types

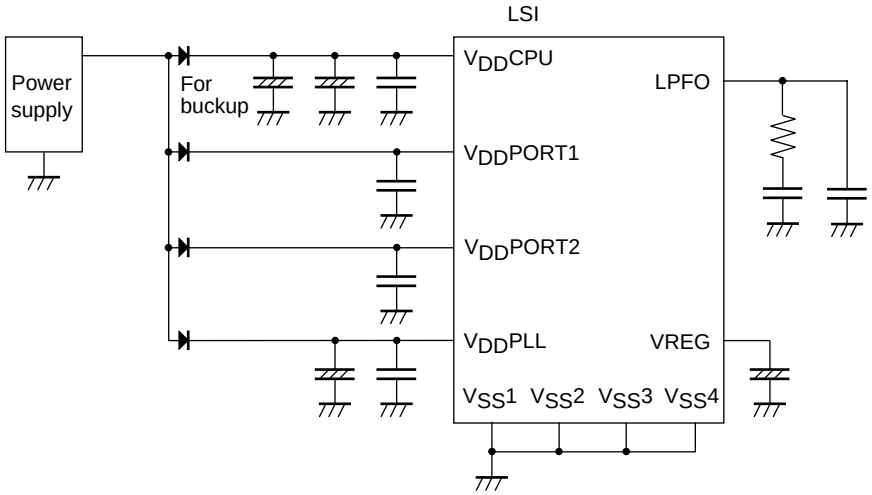
The port output type and pull-up resistance must be set using the registers.
The pin data can be read regardless of the I/O setting of the port.
The port output type (CMOS output or N-channel open drain output) and use/disuse of the pull-up resistor can be configured separately for each port.

* Make the following connection to minimize the noise input to the V_{DD}CPU pin and prolong the backup time.
  Be sure to electrically short the $V_{SS}1$, $V_{SS}2$, $V_{SS}3$ and $V_{SS}4$ pins.

Example 1: When data is being backed up in the HOLD mode, the H level signals to the output ports are fed by the backup capacitors. (V_{DD}CPU = V_{DD}PORT1 = V_{DD}PORT2 = V_{DD}PLL)



Example 2: When data is being backed up in the HOLD mode, the H level output at any ports is not sustained and is unpredictable. (V_{DD}CPU = V_{DD}PORT1 = V_{DD}PORT2 = V_{DD}PLL)



Absolute Maximum Ratings at Ta = 25°C, $V_{SS}1 = V_{SS}2 = V_{SS}3 = V_{SS}4 = 0V$

Parameter		Symbol	Applicable Pin /Remarks	Conditions	Specification			
					min	typ	max	unit
Maximum Supply voltage		V_{DD} max(1)	V_{DD}CPU V_{DD}PLL	V_{DD}CPU=V_{DD}PORT1 =V_{DD}PORT2=V_{DD}PLL	-0.3		+4.6	V
		V_{DD} max(2)	V_{DD}PORT1 V_{DD}PORT2	V_{DD}PORT1=V_{DD}PORT2	-0.3		+6.5	
Input voltage		V_I(1)	RESB, XT1		-0.3		V_{DD}(1)+0.3	
Input/Output voltage		V_{IO}(1)	Ports 5, 6 P70 to 74 Ports C XT2		-0.3		V_{DD}(1)+0.3	
		V_{IO}(2)	Ports 0, 1, 2, 3, 4 P75 to P77 Ports A, B, D		-0.3		V_{DD}(2)+0.3	
High level output current	Peak output current	IOPH(1)	Ports 0, 1, 2, 3, 5 Ports 6, 7, A, C, D P40 to P45 PB2 to PB6	CMOS output selected Per 1 application pin	-10			mA
		IOPH(2)	P46, P47 PB0, PB1	Per 1 application pin	-20			
	Average output current (Note 1-1)	IOMH(1)	Ports 0, 1, 2, 3, 5 Ports 6, 7, A, C, D P40 to P45 PB2 to PB6	CMOS output selected Per 1 application pin	-7.5			
		IOMH(2)	P46, P47 PB0, PB1	Per 1 application pin	-10			
	Total output current	ΣIOAH(1)	Ports 5 Ports C	Total of all applicable pins	-15			
		ΣIOAH(2)	Ports 6 P70 to P74	Total of all applicable pins	-15			
		ΣIOAH(3)	Ports 5, 6 P70 to P74 Ports C	Total of all applicable pins	-20			
		ΣIOAH(4)	Ports 2, D P75 to P77	Total of all applicable pins	-25			
		ΣIOAH(5)	Ports 0, 4	Total of all applicable pins	-25			
		ΣIOAH(6)	Ports 0, 2, 4, D P75 to P77	Total of all applicable pins	-45			
		ΣIOAH(7)	Ports 1, 3	Total of all applicable pins	-25			
		ΣIOAH(8)	Ports A, B	Total of all applicable pins	-25			
		ΣIOAH(9)	Ports 1, 3, A, B	Total of all applicable pins	-45			

Note 1-1: Average output current is average of current in 100ms interval.

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Parameter		Symbol	Applicable Pin /Remarks	Conditions	Specification			
					min	typ	max	unit
Low level output current	Peak output current	IOPL(1)	Ports 0, 1, 3 Ports 4, 5, 6 Ports B, C, D P20, P21 P24 to P27 P70 to P74, P77 PA2, PA5 to PA7	Per 1 application pin.			20	mA
		IOPL(2)	P22, P23 P75, P76 PA0, PA1 PA3, PA4	Per 1 application pin.			25	
	Average output current (Note 1-1)	IOML(1)	Ports 0, 1, 3 Ports 4, 5, 6 Ports B, C, D P20, P21 P24 to P27 P70 to P74, P77 PA2, PA5 to PA7	Per 1 application pin.			10	
		IOML(2)	P22, P23 P75, P76 PA0, PA1 PA3, PA4	Per 1 application pin.			15	
	Total output current	ΣIOAL(1)	Ports 5 Ports C	Total of all applicable pins			15	
		ΣIOAL(2)	Ports 6 P70 to P74	Total of all applicable pins			15	
		ΣIOAL(3)	Ports 5, 6 P70 to P74 Ports C	Total of all applicable pins			20	
		ΣIOAL(4)	Ports 2, D P75 to P77	Total of all applicable pins			25	
		ΣIOAL(5)	Ports 0, 4	Total of all applicable pins			25	
		ΣIOAL(6)	Ports 0, 2, 4, D P75 to P77	Total of all applicable pins			45	
		ΣIOAL(7)	Ports 1, 3	Total of all applicable pins			25	
		ΣIOAL(8)	Ports A, B	Total of all applicable pins			25	
		ΣIOAL(9)	Ports 1, 3, A, B	Total of all applicable pins			45	
Allowable power dissipation		Pd max	QIP100E	Ta = -40 to +85°C			400	mW
Operating temperature range		Topr			-40		+85	°C
Storage temperature range		Tstg			-45		+125	°C

Note 1-1: Average output current is average of current in 100ms interval.

Allowable Operating Conditions at Ta = -40°C to +85°C, $V_{SS}1 = V_{SS}2 = V_{SS}3 = V_{SS}4 = 0V$

Parameter	Symbol	Applicable Pin /Remarks	Conditions	Specification			
				min	typ	max	unit
Operating supply voltage	$V_{DD}(1)$	V_{DD}CPU=V_{DD}PLL		3.0		3.6	V
	$V_{DD}(2)$	V_{DD}PORT1 V_{DD}PORT2		$V_{DD}(1)$		5.5	
Memory sustaining supply voltage	VHD	V_{DD}CPU=V_{DD}PORT1 =V_{DD}PORT2=V_{DD}PLL	RAM and register contents in HOLD mode.	1.2			
High level input voltage	$V_{IH}(1)$	Ports 0, 1, 2, 3, 4 P75 to P77 Ports A, B, D	V_{DD}PORT=$V_{DD}(2)$	$0.3\times V_{DD}(2)$ +0.7		$V_{DD}(2)$	
	$V_{IH}(2)$	Ports 5, 6, C P70 to P74	V_{DD}CPU=$V_{DD}(1)$	$0.3\times V_{DD}(1)$ +0.7		$V_{DD}(1)$	
	$V_{IH}(3)$	RESB	V_{DD}CPU=$V_{DD}(1)$	$0.75\times V_{DD}(1)$		$V_{DD}(1)$	
	$V_{IH}(4)$	P22, P23, P75, P76 PA0, PA1, PA3, PA4 I^2C side	V_{DD}PORT=$V_{DD}(2)$	$0.7\times V_{DD}(2)$		$V_{DD}(2)$	
Low level input voltage	$V_{IL}(1)$	Ports 0, 1, 2, 3, 4 P75 to P77 Ports A, B, D	V_{DD}PORT=$V_{DD}(2)$	V_{SS}		$0.1\times V_{DD}(2)$ +0.4	
	$V_{IL}(2)$	Ports 5, 6, C P70 to P74	V_{DD}CPU=$V_{DD}(1)$	V_{SS}		$0.1\times V_{DD}(1)$ +0.4	
	$V_{IL}(3)$	RESB	V_{DD}CPU=$V_{DD}(1)$	V_{SS}		$0.25\times V_{DD}(1)$	
	$V_{IL}(4)$	P22, P23, P75, P76 PA0, PA1, PA3, PA4 I^2C side	V_{DD}PORT=$V_{DD}(2)$	V_{SS}		$0.3\times V_{DD}(2)$	
Instruction cycle time	tCYC		V_{DD}CPU=$V_{DD}(1)$	83.3			µs
Supply voltage rise time	Tpup	V_{DD}CPU		1		100	ms
Oscillation frequency range	FmRC		Internal RC oscillation	0.5	1.0	2.0	MHz
	FmX'tal	XT1, XT2	32.768kHz crystal oscillation.		32.768		kHz

Electrical Characteristics at Ta = -40°C to +85°C, $V_{SS}1 = V_{SS}2 = V_{SS}3 = V_{SS}4 = 0V$

Parameter	Symbol	Applicable Pin /Remarks	Conditions		Specification			
				V_{DD}[V]	min	typ	max	unit
High level input current	$I_{IH}(1)$	Ports 0, 1, 2, 3, 4 P75 to P77 Ports A, B, D	Output disable Pull-up resistor OFF $V_{IN}=V_{DD}(2)$ (including the off-leak current of the output Tr.)	V_{DD}PORT= $V_{DD}(1)$ to 5.5			1	μA
	$I_{IH}(2)$	Ports 5, 6, C P70 to P74 RESB	Output disable Pull-up resistor OFF $V_{IN}=V_{DD}(1)$ (including the off-leak current of the output Tr.)	V_{DD}CPU= 3.0 to 3.6			1	
	$I_{IH}(3)$	XT1	$V_{IN}=V_{DD}(1)$	V_{DD}CPU= 3.0 to 3.6		0.18		
Low level input current	$I_{IL}(1)$	Ports 0, 1, 2, 3, 4 P75 to P77 Ports A, B, D	Output disable Pull-up resistor OFF $V_{IN}=V_{SS}$ (including the off-leak current of the output Tr.)	V_{DD}PORT= $V_{DD}(1)$ to 5.5	-1			
	$I_{IL}(2)$	Ports 5, 6, C P70 to P74 RESB	Output disable Pull-up resistor OFF $V_{IN}=V_{SS}$ (including the off-leak current of the output Tr.)	V_{DD}CPU= 3.0 to 3.6	-1			
	$I_{IL}(3)$	XT1	$V_{IN}=V_{SS}$	V_{DD}CPU= 3.0 to 3.6		-0.18		
High level output voltage	$V_{OH}(1)$	Ports 0, 1, 2, 3 P40 to P45 P75 to P77 Ports A, D PB2 to PB6	I_{OH}=-1.0mA, $V_{DD}(2)$	V_{DD}PORT= 4.5 to 5.5	$V_{DD}(2)$ -1.0			V
	$V_{OH}(2)$		I_{OH}=-0.4mA, $V_{DD}(2)$	V_{DD}PORT= $V_{DD}(1)$ to 5.5	$V_{DD}(2)$ -0.4			
	$V_{OH}(3)$	Ports 5, 6, C P70 to P74	I_{OH}=-1.0mA, $V_{DD}(1)$	V_{DD}CPU= 3.0 to 3.6	$V_{DD}(1)$ -1.0			
	$V_{OH}(4)$		I_{OH}=-0.4mA, $V_{DD}(1)$	V_{DD}CPU= 3.0 to 3.6	$V_{DD}(1)$ -0.4			
	$V_{OH}(5)$	P46, P47 PB0, PB1	I_{OH}=-10mA, $V_{DD}(2)$	V_{DD}PORT= 4.5 to 5.5	$V_{DD}(2)$ -1.5			
	$V_{OH}(6)$		I_{OH}=-1.6mA, $V_{DD}(2)$	V_{DD}PORT= $V_{DD}(1)$ to 5.5	$V_{DD}(2)$ -0.4			
Low level output voltage	$V_{OL}(1)$	Ports 0, 1, 3, 4 P20, P21	I_{OL}=10mA	V_{DD}PORT= 4.5 to 5.5			1.5	
	$V_{OL}(2)$	P24 to P27, P77 PA2, PA5 to PA7 Ports B, D	I_{OL}=1.6mA	V_{DD}PORT= $V_{DD}(1)$ to 5.5			0.4	
	$V_{OL}(3)$	Ports 5, 6, C P70 to P74	I_{OL}=1.6mA	V_{DD}CPU= 3.0 to 3.6			0.4	
	$V_{OL}(4)$	P22, P23 P75, P76	I_{OL}=11mA	V_{DD}PORT= 4.5 to 5.5			1.5	
	$V_{OL}(5)$	PA0, PA1 PA3, PA4	I_{OL}=3.0mA	V_{DD}PORT= $V_{DD}(1)$ to 5.5			0.4	
Pull-up resistor	Rpu(1)	Ports 0, 1, 2, 3, 4 P75 to P77 Ports A, B, D	$V_{OH}=0.9V_{DD}$	V_{DD}PORT= 4.5 to 5.5	15	35	80	kΩ
	Rpu(2)			V_{DD}PORT= $V_{DD}(1)$ to 5.5	15	35	150	
	Rpu(3)	Ports 5, 6, C P70 to P74		V_{DD}CPU= 3.0 to 3.6	15	35	150	
Hysteresis voltage	VHYS	RESB Ports 1, 2, 3, 4, 5 Ports 7, A, B, C, D	Ports 1 to 5, 7, A to D PnFSAn=1			$0.1V_{DD}$		V

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Parameter	Symbol	Applicable Pin /Remarks	Conditions		Specification			
				V_{DD}[V]	min	typ	max	unit
Pin capacitance	CP	All pins	• For pins other than that under test: V_{IN}=V_{SS} • f=1MHz • Ta=25°C			10		pF
Low voltage circuit detection voltage	VDET(1)	V_{DD}CPU	On low voltage detection circuit Excluding the HOLD mode		2.7	2.85	3.0	V
	VDET(2)	V_{DD}CPU	On low voltage detection circuit HOLD mode		1.27	1.42	1.57	V

Serial I/O Characteristics at Ta = -40°C to +85°C, $V_{SS}1$ = $V_{SS}2$ = $V_{SS}3$ = $V_{SS}4$ = 0V

1. SIO0, SIO1 Serial I/O Characteristics (Wakeup Function Disabled) (Note 4-1-1)

Parameter			Symbol	Applicable Pin /Remarks	Conditions		Specification			
						V_{DD}[V]	min	typ	max	unit
Serial clock	Input clock	Period	tSCK(1)	SCK0(P12) SCK1(P45)	• See Fig. 1.	V_{DD}PORT= V_{DD}(1) to 5.5	4			tCYC
		Low level pulse width	tSCKL(1)				2			
		High level pulse width	tSCKH(1)				2			
			tSCKHA(1)		• Automatic communication mode • See Fig. 1.		6			
			tSCKHBSY (1a)		• Automatic communication mode • See Fig. 1.		23			
			tSCKHBSY (1b)		• Modes other than automatic communication mode • See Fig. 1.		4			
	Output clock	Period	tSCK(2)	SCK0(P12) SCK1(P45)	• CMOS output selected • See Fig. 1.		4			
		Low level pulse width	tSCKL(2)				1/2			tSCK
		High level pulse width	tSCKH(2)				1/2			
			tSCKHA(2)		• Automatic communication mode • CMOS output selected • See Fig. 1.	V_{DD}PORT= V_{DD}(1) to 5.5	6			tCYC
			tSCKHBSY (2a)		• Automatic communication mode • CMOS output selected • See Fig. 1.		4		23	
			tSCKHBSY (2b)		• Modes other than automatic communication mode • See Fig. 1.		4			
Serial input	Data setup time		tsDI(1)	SIO0(P11), SIO1(P44)	• Specified with respect to rising edge of SIOCLK • See fig. 1.	V_{DD}PORT= V_{DD}(1) to 5.5	0.03			µs
	Data hold time		thDI(1)				0.03			
Serial output	Input clock	Output delay time	tdD0(1)	SO0(P10), SO1(P43), SIO0(P11), SIO1(P44)	• (Note 4-1-2)	V_{DD}PORT= V_{DD}(1) to 5.5			1tCYC +0.05	
	Output clock		tdD0(2)		• (Note 4-1-2)				1tCYC +0.05	

Note 4-1-1: These specifications are theoretical values. Add margin depending on its use.

Note 4-1-2: Specified with respect to falling edge of SIOCLK. Specified as the time to the beginning of output state change in open drain output mode. See Fig. 1.

2. SIO0, SIO1 Serial Input/Output Characteristics (Wakeup Function Enabled) (Note 4-2-1)

Parameter			Symbol	Applicable Pin /Remarks	Conditions		Specification			
						V_{DD}[V]	min	typ	max	unit
Serial clock	Input clock	Period	tSCK(3)	SCK0(P12) SCK1(P45)	• See Fig. 1.	V_{DD}PORT= V_{DD}(1) to 5.5	2			tCYC
		Low level pulse width	tSCKL(3)				1			
		High level pulse width	tSCKH(3)				1			
			tSCKHBSY(3)				2			
Serial input	Data setup time		tsDI(2)	SIO0(P11), SIO1(P44)	• Specified with respect to rising edge of SIOCLK • See fig. 1.	V_{DD}PORT= V_{DD}(1) to 5.5	0.03			µs
	Data hold time		thDI(2)				0.03			
Serial output	Input clock	Output delay time	tdD0(3)	SO0(P10), SO1(P43), SIO0(P11), SIO1(P44)	• (Note 4-2-2)	V_{DD}PORT= V_{DD}(1) to 5.5			1tCYC +0.05	

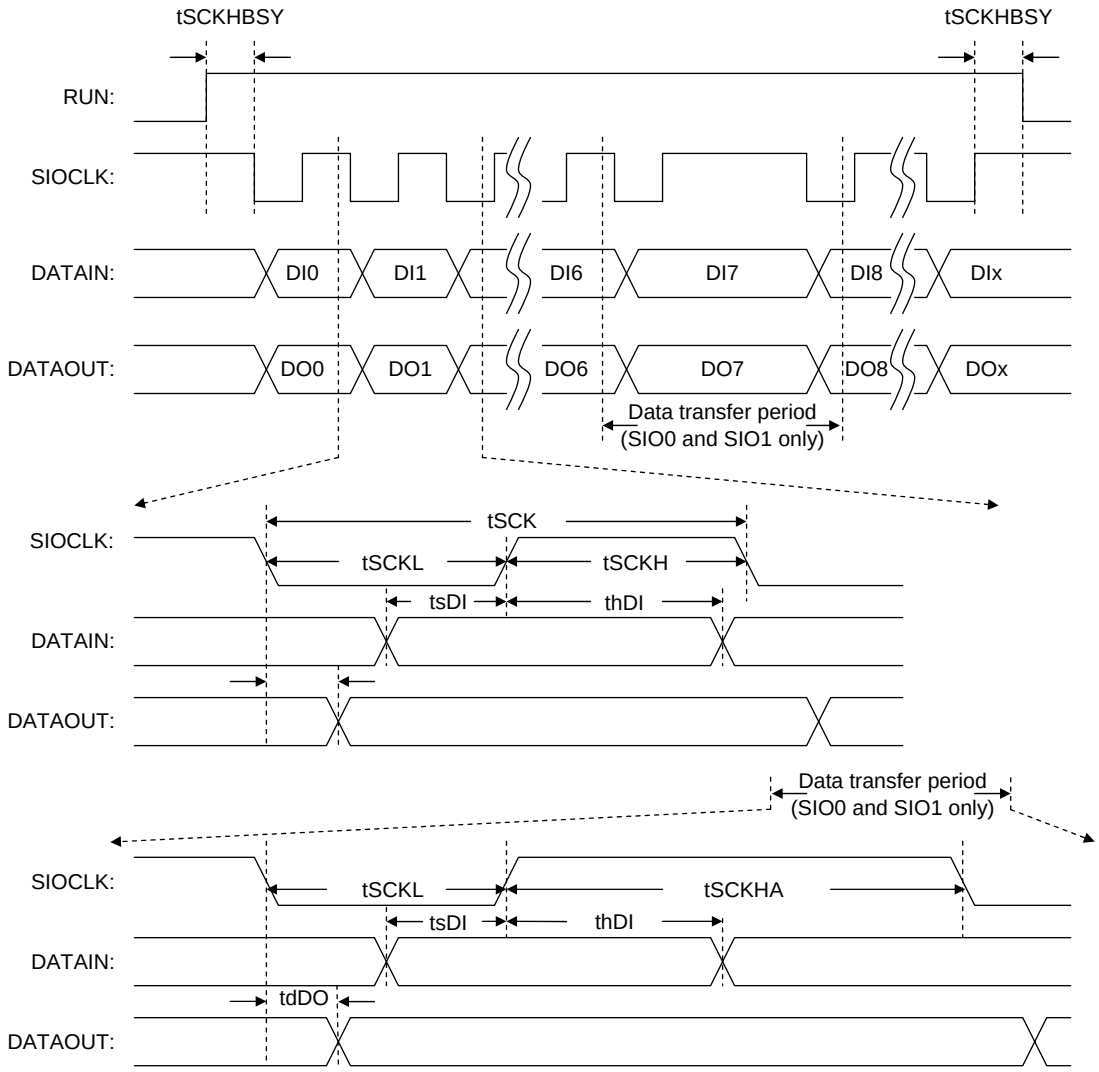
Note 4-2-1: These specifications are theoretical values. Add margin depending on its use.

Note 4-2-2: Specified with respect to falling edge of SIOCLK. Specified as the time to the beginning of output state change in open drain output mode. See Fig. 1.

3. SMIIC0 to SMIIC3 Simple SIO Mode Input/Output Characteristics

Parameter			Symbol	Applicable Pin /Remarks	Conditions		Specification			
						V_{DD}[V]	min	typ	max	unit
Serial clock	Input clock	Period	tSCK(4)	SM0CK(P22) SM1CK(PA0) SM2CK(PA3) SM3CK(P75)	• See Fig. 1.	V_{DD}PORT= V_{DD}(1) to 5.5	4			tCYC
		Low level pulse width	tSCKL(4)				2			
		High level pulse width	tSCKH(4)				2			
	Output clock	Period	tSCK(5)	SM0CK(P22) SM1CK(PA0) SM2CK(PA3) SM3CK(P75)	• CMOS output selected • See Fig. 1.		8			
		Low level pulse width	tSCKL(5)				1/2			tSCK
		High level pulse width	tSCKH(5)				1/2			
Serial input	Data setup time		tsDI(3)	SM0DA(P23) SM1DA(PA1) SM2DA(PA4) SM3DA(P76)	• Specified with respect to rising edge of SIOCLK • See fig. 1.	V_{DD}PORT= V_{DD}(1) to 5.5	0.03			µs
	Data hold time		thDI(3)				0.03			
Serial output	Output delay time		tdD0(4)	SM0DO(P24) SM0D1(PA2) SM0D2(PA5) SM0D3(P77) SM0DA(P23) SM1DA(PA1) SM2DA(PA4) SM3DA(P76)	• Specified with respect to falling edge of SIOCLK • Specified as interval up to time when output state starts changing. • See Fig. 1.	V_{DD}PORT= V_{DD}(1) to 5.5			1tCYC +0.05	

Note 4-5-1: These specifications are theoretical values. Add margin depending on its use.



* Remarks: DIx and DOx denote the last bits communicated; x = 0 to 32768

Figure 1 Serial I/O Waveforms

4. SMIIC0 to SMIIC3 I²C Mode Input/Output Characteristics

Parameter			Symbol	Applicable Pin /Remarks	Conditions		Specification			
						V_{DD}[V]	min	typ	max	unit
Serial clock	Input clock	Period	tSCL	SM0CK(P22) SM1CK(PA0) SM2CK(PA3) SM3CK(P75)	• See Fig. 2.	V_{DD}PORT= V_{DD}(1) to 5.5	5			Tfilt
		Low level pulse width	tSCLL				2.5			
		High level pulse width	tSCLH				2			
	Output clock	Period	tSCLx	SM0CK(P22) SM1CK(PA0) SM2CK(PA3) SM3CK(P75)	• Specified as interval up to time when output state starts changing.	V_{DD}PORT= V_{DD}(1) to 5.5	10			
		Low level pulse width	tSCLLx				1/2			tSCL
		High level pulse width	tSCLHx				1/2			
SM0C and SM0DA pins input spike suppression time			tsp	SM0CK(P22) SM1CK(PA0) SM2CK(PA3) SM3CK(P75) SM0DA(P23) SM1DA(PA1) SM2DA(PA4) SM3DA(P76)	• See fig. 2.				1	Tfilt
Bus release time between start and stop	Input		tBUF	SM0CK(P22) SM1CK(PA0) SM2CK(PA3) SM3CK(P75) SM0DA(P23) SM1DA(PA1) SM2DA(PA4) SM3DA(P76)	• See fig. 2.	V_{DD}PORT= V_{DD}(1) to 5.5	2.5			µs
	Output		tBUFx		• Standard-mode • Specified as interval up to time when output state starts changing.		5.5			
					• Fast-mode • Specified as interval up to time when output state starts changing.		1.6			
Start/restart condition hold time	Input		tHD; STA	SM0CK(P22) SM1CK(PA0) SM2CK(PA3) SM3CK(P75) SM0DA(P23) SM1DA(PA1) SM2DA(PA4) SM3DA(P76)	• When SMIIC register control bit, I2CSHDS=0 • See fig. 2.	V_{DD}PORT= V_{DD}(1) to 5.5	2.0			Tfilt
					• When SMIIC register control bit, I2CSHDS=1 • See fig. 2.		2.5			
	Output		tHD; STAx		• Standard-mode • Specified as interval up to time when output state starts changing.		4.1			µs
					• Fast-mode • Specified as interval up to time when output state starts changing.		1.0			
Restart condition setup time	Input		tSU; STA	SM0CK(P22) SM1CK(PA0) SM2CK(PA3) SM3CK(P75) SM0DA(P23) SM1DA(PA1) SM2DA(PA4) SM3DA(P76)	• See fig. 2.	V_{DD}PORT= V_{DD}(1) to 5.5	1.0			Tfilt
	Output		tSU; STAx		• Standard-mode • Specified as interval up to time when output state starts changing.		5.5			µs
					• Fast-mode • Specified as interval up to time when output state starts changing.		1.6			
Stop condition setup time	Input		tSU; STO	SM0CK(P22) SM1CK(PA0) SM2CK(PA3) SM3CK(P75) SM0DA(P23) SM1DA(PA1) SM2DA(PA4) SM3DA(P76)	• See fig. 2.	V_{DD}PORT= V_{DD}(1) to 5.5	1.0			Tfilt
	Output		tSU; STOx		• Standard-mode • Specified as interval up to time when output state starts changing.		4.9			µs
					• Fast-mode • Specified as interval up to time when output state starts changing.		1.1			

Note 4-6-1: These specifications are theoretical values. Add margin depending on its use.

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Parameter		Symbol	Applicable Pin /Remarks	Conditions		Specification			
					V_{DD}[V]	min	typ	max	unit
Data hold time	Input	tHD; DAT	SM0CK(P22) SM1CK(PA0) SM2CK(PA3) SM3CK(P75) SM0DA(P23) SM1DA(PA1) SM2DA(PA4) SM3DA(P76)	• See fig. 2.	V_{DD}PORT= V_{DD}(1) to 5.5	0			Tfilt
	Output	tHD; DATx		• Specified as interval up to time when output state starts changing.		1		1.5	
Data setup time	Input	tSU; DAT	SM0CK(P22) SM1CK(PA0) SM2CK(PA3) SM3CK(P75) SM0DA(P23) SM1DA(PA1) SM2DA(PA4) SM3DA(P76)	• See fig. 2.	V_{DD}PORT= V_{DD}(1) to 5.5	1			Tfilt
	Output	tSU; DATx		• Specified as interval up to time when output state starts changing.		1tSCL -1.5Tfilt			
Fall time	Input	tF	SM0CK(P22) SM1CK(PA0) SM2CK(PA3) SM3CK(P75) SM0DA(P23) SM1DA(PA1) SM2DA(PA4) SM3DA(P76)	• See fig. 2.	V_{DD}PORT= V_{DD}(1) to 5.5			300	ns
	Output	tF		• When SMIIC register control bits, PSLW=1, P5V=1	V_{DD}PORT=5	20+0.1Cb		250	
				• When SMIIC register control bits, PSLW=1, P5V=0	V_{DD}PORT=3	20+0.1Cb		250	
				• When SMIIC register control bits, PSLW=0 • Cb ≤ 400pF	V_{DD}PORT= V_{DD}(1) to 5.5			100	

Note 4-6-1: These specifications are theoretical values. Add margin depending on its use.

Note 4-6-2: The value of Tfilt is determined by the values of the register SMICnBRG (n=0, 1, 2, 3), bits 7 and 6 (BRP1, BRP0) and the system clock frequency.

BRP1	BRP0	Tfilt
0	0	tCYC × 1
0	1	tCYC × 2
1	0	tCYC × 3
1	1	tCYC × 4

Set bits (BPR1, BPR0) so that the value of Tfilt falls between the following range:

250ns ≥ Tfilt > 140ns

Note 4-6-3: Cb represents the total loads (in pF) connected to the bus pins. Cb ≤ 400pF

Note 4-6-4: The standard-mode refers to a mode that is entered by configuring SMICnBRG (n=0, 1, 2, 3) as follows:

250ns ≥ Tfilt > 140ns

BRDQ (bit5) = 1

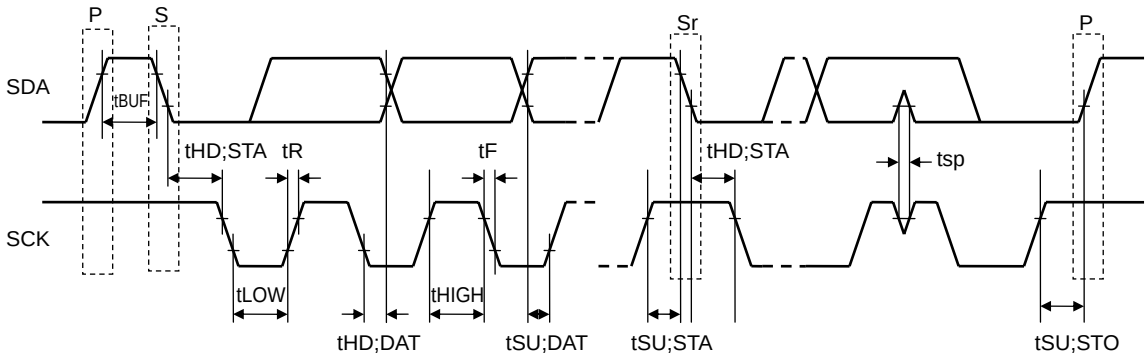
SCL frequency setting ≤ 100kHz

The fast-mode refers to a mode that is entered by configuring SMICnBRG (n=0, 1, 2, 3) as follows:

250ns ≥ Tfilt > 140ns

BRDQ (bit5) = 0

SCL frequency setting ≤ 400kHz



S: Start condition
P: Stop condition
Sr: Restart condition

Figure 2 I^2C Timing

5. UART2 to UART5 Operating Conditions at Ta = -40°C to +85°C, $V_{SS}1 = V_{SS}2 = V_{SS}3 = V_{SS}4 = 0V$

Parameter	Symbol	Applicable Pin /Remarks	Conditions	Specification				
				V_{DD}[V]	min	typ	max	unit
Transfer rate	UBR	U2RX(P16), U3RX(P34), U4RX(PD0), U5RX(PA6), U2TX(P17), U3TX(P35), U4TX(PD1), U5TX(PA7)		V_{DD}PORT= V_{DD}(1) to 5.5	8		4096	tBGCYC

Note 4-7: tBGCYC denotes one cycle of the baudrate clock source.

Pulse Input Conditions at Ta = -40°C to +85°C, $V_{SS}1 = V_{SS}2 = V_{SS}3 = V_{SS}4 = 0V$

Parameter	Symbol	Applicable Pin /Remarks	Conditions	Specification				
				V_{DD}[V]	min	typ	max	unit
High/low level minimum pulse width	tPIH(1) tPIL(1)	INT0(P30), INT1(P31), INT2(P32), INT3(P33), INT4(P20), INT5(P21), INT6(P40), INT7(PB5)	• Interrupt source flag can be set. • Event inputs for timers 2 and 3 are enabled.	V_{DD}PORT= V_{DD}(1) to 5.5	2			tCYC
	tPIL(2)	RESB	Can be reset via the external reset pin. (Note 5-1)	V_{DD}CPU= 3.0 to 3.6	50			µs
	tPIL(3)	V_{DD}CPU	Can be reset by the low voltage detection circuit. (Note 5-1)	(Note 5-2)	50			µs

Note 5-1: This parameter specifies the time required to ensure that the reset sequence is carried out without fail. The reset may be applied even if this time specification is not satisfied.
Note 5-2: (V_{DD}CPU voltage) ≤ (Low voltage circuit detection voltage)

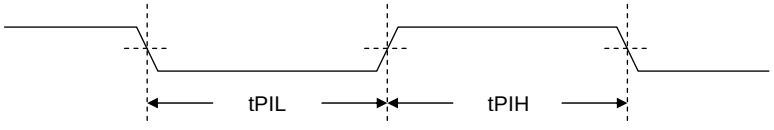


Figure 3 Pulse Input Timing Signal Waveform

AD Converter Characteristics at Ta = -40°C to +85°C, $V_{SS}1 = V_{SS}2 = V_{SS}3 = V_{SS}4 = 0V$

1. 12-bit AD Conversion Mode

Parameter	Symbol	Applicable Pin /Remarks	Conditions		Specification			
				V_{DD}CPU[V]	min	typ	max	unit
Resolution	NAD	AN0(P60) to AN7(P67), AN8(P70) to AN12(P74)		3.0 to 3.6		12		bit
Absolute accuracy	ETAD		(Note 6-1)	3.0 to 3.6			±16	LSB
Conversion time	TCAD12		Conversion time calculated	3.0 to 3.6	102			µs
Analog input voltage range	VAIN			3.0 to 3.6	V_{SS}		V_{DD}CPU	V
Analog port input current	IAINH		VAIN=V_{DD}CPU	3.0 to 3.6			1	µA
	IAINL		VAIN=V_{SS}	3.0 to 3.6	-1			

Conversion time calculation formula: TCAD12= ((52/(AD division ratio))+2) × tCYC

2. 8-bit AD Conversion Mode

Parameter	Symbol	Applicable Pin /Remarks	Conditions		Specification			
				V_{DD}CPU[V]	min	typ	max	unit
Resolution	NAD	AN0(P60) to AN7(P67), AN8(P70) to AN12(P74)		3.0 to 3.6		8		bit
Absolute accuracy	ETAD		(Note 6-1)	3.0 to 3.6			±1.5	LSB
Conversion time	TCAD8		Conversion time calculated	3.0 to 3.6	32			µs
Analog input voltage range	VAIN			3.0 to 3.6	V_{SS}		V_{DD}CPU	V
Analog port input current	IAINH		VAIN=V_{DD}CPU	3.0 to 3.6			1	µA
	IAINL		VAIN=V_{SS}	3.0 to 3.6	-1			

Conversion time calculation formula: TCAD8= ((32/(AD division ratio))+2) × tCYC

Note 6-1: The quantization error (±1/2LSB) is excluded from the absolute accuracy.

Note 6-2: The conversion time refers to the interval from the time a conversion starting instruction is issued till the time the complete digital value against the analog input value is loaded in the result register.
The conversion time is twice the normal value when one of the following conditions occurs:
- The first AD conversion is executed in the 12-bit AD conversion mode after a system reset.
- The first AD conversion is executed after the AD conversion mode is switched from 8-bit to 12-bit AD conversion mode.

Consumption Current Characteristics at Ta = -40°C to +85°C, $V_{SS}1 = V_{SS}2 = V_{SS}3 = V_{SS}4 = 0V$

Parameter	Symbol	Applicable Pin /Remarks	Conditions	V_{DD}[V]	Specification min	typ	max	unit
Normal mode consumption current (Note 7-1)	IDDOP(1)	V_{DD}CPU =V_{DD}PORT1 =V_{DD}PORT2 =V_{DD}PLL	• FmX'tal=32.768kHz crystal oscillation mode • System clock set to VCO (12MHz) • Internal RC oscillation stopped • 1/1 frequency division mode	3.0 to 3.6		10	15	mA
	IDDOP(2)		• FmX'tal=32.768kHz crystal oscillation mode • System clock set to VCO (8MHz) • Internal RC oscillation stopped • 1/1 frequency division mode	3.0 to 3.6		8	12	
	IDDOP(3)		• FmX'tal=32.768kHz crystal oscillation mode • System clock set to VCO (4MHz) • Internal RC oscillation stopped • 1/1 frequency division mode	3.0 to 3.6		6	9	
	IDDOP(4)		• FmX'tal=0kHz (oscillation stopped) • System clock set to internal RC oscillation • 1/1 frequency division mode	3.0 to 3.6		3.5	5	
	IDDOP(5)		• FmX'tal=32.768kHz crystal oscillation mode • System clock set to 32.768kHz • Internal RC oscillation stopped • 1/1 frequency division mode	3.0 to 3.6		35	150	µA
HALT mode consumption current (Note 7-1)	IDDHALT(1)	V_{DD}CPU =V_{DD}PORT1 =V_{DD}PORT2 =V_{DD}PLL	HALT mode • FmX'tal=32.768kHz crystal oscillation mode • System clock set to VCO (12MHz) • Internal RC oscillation stopped • 1/1 frequency division mode	3.0 to 3.6		3.5	5	mA
	IDDHALT(2)		HALT mode • FmX'tal=32.768kHz crystal oscillation mode • System clock set to VCO (8MHz) • Internal RC oscillation stopped • 1/1 frequency division mode	3.0 to 3.6		2.5	4	
	IDDHALT(3)		HALT mode • FmX'tal=32.768kHz crystal oscillation mode • System clock set to VCO (4MHz) • Internal RC oscillation stopped • 1/1 frequency division mode	3.0 to 3.6		1.5	3	
	IDDHALT(4)		HALT mode • FmX'tal=0kHz (oscillation stopped) • System clock set to internal RC oscillation • 1/1 frequency division mode	3.0 to 3.6		0.2	1	
	IDDHALT(5)		HALT mode • FmX'tal=32.768kHz crystal oscillation mode • System clock set to 32.768kHz • Internal RC oscillation stopped • 1/1 frequency division mode	3.0 to 3.6		15	100	µA
HOLD mode consumption current	IDDHOLD(1)	V_{DD}CPU	HOLD mode	3.0 to 3.6		1	30	
HOLDX mode consumption current	IDDHOLD(2)	V_{DD}CPU	HOLDX mode • FmX'tal=32.768kHz crystal oscillation mode	3.0 to 3.6		15	50	

Note 7-1: The consumption current value includes none of the currents that flow into the output transistor and internal pull-up resistors.

F-ROM Programming Characteristics at Ta = +10°C to +55°C, $V_{SS}1 = V_{SS}2 = V_{SS}3 = V_{SS}4 = 0V$

Parameter	Symbol	Applicable Pin /Remarks	Conditions		Specification			
				V_{DD}CPU[V]	min	typ	max	unit
Onboard programming current	I_{DD}FW(1)	V_{DD}CPU	• Microcontroller erase consumption current is excluded.	3.0 to 3.6		10	20	mA
Onboard programming time	tFW(1)		• 512-byte erase operation	3.0 to 3.6		20	30	ms
	tFW(2)		• 2-byte programming operation	3.0 to 3.6		40	60	µs

Power Pin Treatment Condition 1 (V_{DD}CPU, V_{SS}1)

Connect capacitors that meet the following conditions between the V_{DD}1 and V_{SS}1 pins:

- Connect among the V_{DD}CPU and V_{SS}1 pins and the capacitors C1 and C2 with the shortest possible lead wires, of the same length (L1=L1', L2=L2') wherever possible.
- Connect a large-capacity capacitor C1 and a small-capacity capacitor C2 in parallel.
- The capacitance of C2 should be approximately 0.1µF or larger.
- Please mount a suitable capacitor about C1.
- The V_{DD}CPU and V_{SS}1 traces must be thicker than the other traces.

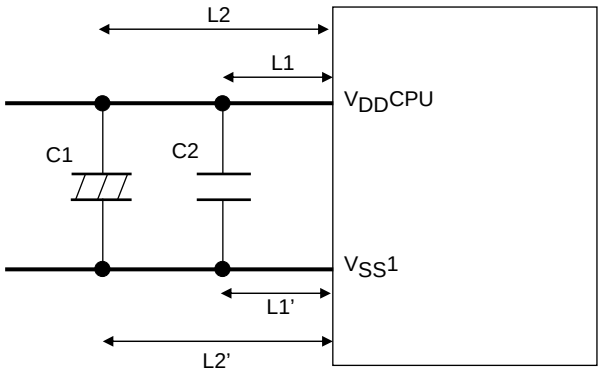


Figure 4

Power Pin Treatment Condition 2 (V_{DD}PORT1 to 2, V_{SS}2 to 3)

Connect capacitors that meet the following conditions between the V_{DD}PORT1 to V_{SS}2 and V_{DD}PORT2 to V_{SS}3 pins:

- Connect among the V_{DD}PORT1 to 2 and V_{SS}2 to 3 pins and the capacitor C3 with the shortest possible lead wires, of the same length (L3=L3') wherever possible.
- The capacitance of C3 should be approximately 0.1µF or larger.
- The V_{DD}PORT1 to 2 and V_{SS}2 to 3 traces must be thicker than the other traces.

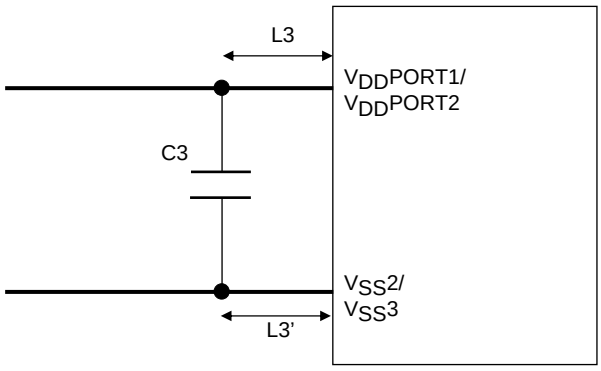


Figure 5

Power Pin Treatment Condition 3 (V_{DD}PLL, V_{SS}4)

Connect capacitors that meet the following conditions between the V_{DD}PLL and V_{SS}4 pins:

- Connect among the V_{DD}PLL and V_{SS}4 pins and the capacitors C4 and C5 with the shortest possible lead wires, of the same length (L4=L4', L5=L5') wherever possible.
- Connect a large-capacity capacitor C4 and a small-capacity capacitor C5 in parallel.
- The capacitance of C4 should be approximately 10μF.
- The capacitance of C5 should be approximately 0.1μF.
- The V_{DD}PLL and V_{SS}4 traces must be thicker than the other traces.

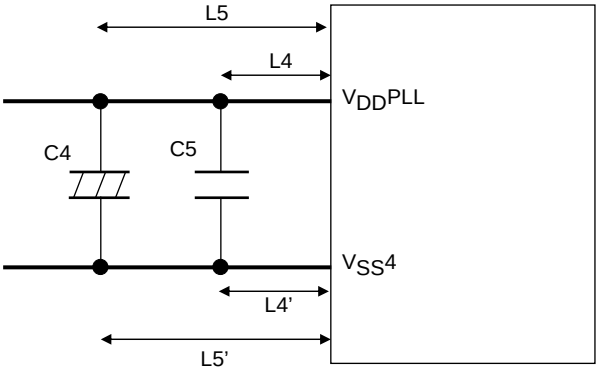


Figure 6

Power Pin Treatment Condition 4 (VREG, V_{SS}1)

Connect capacitors that meet the following conditions between the VREG and V_{SS}1 pins:

- Connect among the VREG and V_{SS}1 pins and the capacitors C6 with the shortest possible lead wires, of the same length (L6=L6') wherever possible.
- The capacitance of C6 should be approximately 1μF.
- The VREG and V_{SS}1 traces must be thicker than the other traces.

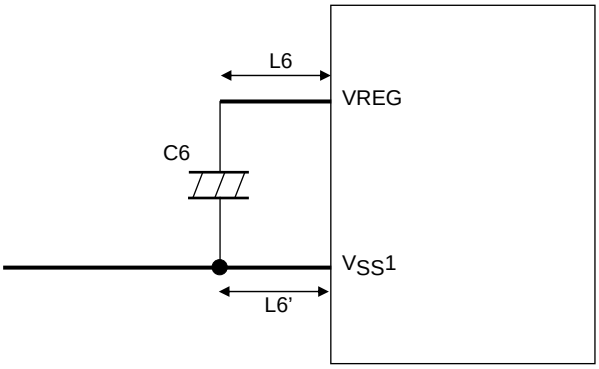


Figure 7

LPF Pin Treatment Condition (LPFO)

Insert a resistor and capacitors that meet the following conditions between the LPFO and $V_{SS}4$ pins.

R1 = 3.3kΩ
C7 = 0.068μF
C8 = 0.0039μF

• Routing traces between the LPFO and $V_{SS}4$ pins and the resistor and capacitors, and between R1 and C7 must be as short as possible.

* After the PLL circuit is activated, 50ms or more is required for stabilizing oscillation.

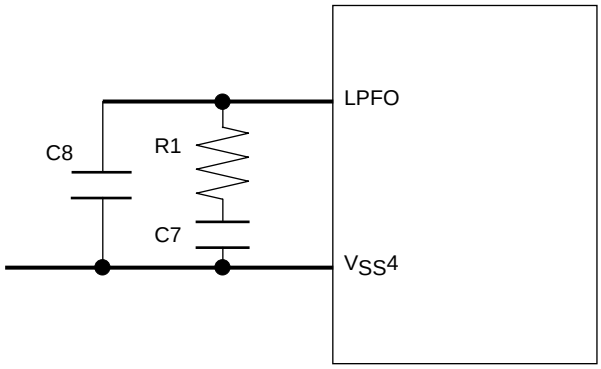


Figure 8

TEST Pin Treatment Condition (TEST)

Insert a resistor that meets the following condition between the TEST and $V_{SS}1$ pins.

R_{TEST} = 100kΩ

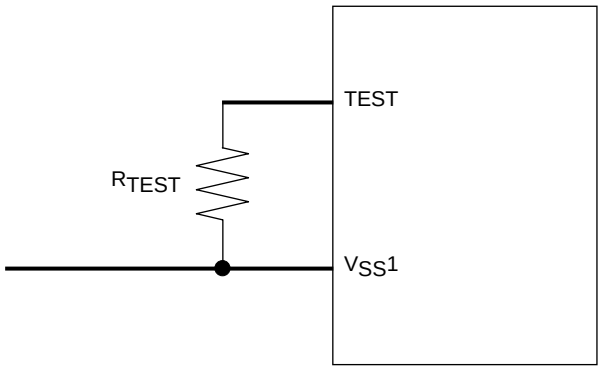


Figure 9

Example of Crystal Oscillator Circuit Characteristics

Given below are the characteristics of a sample crystal oscillator circuit that were measured using a SANYO-designated oscillation characteristics evaluation board and external components with circuit constant values with which the oscillator vendor confirmed normal and stable oscillation.

Table 1 Example of Crystal Oscillator Circuit Characteristics with a Crystal Resonator

Nominal Frequency	Vendor Name	Oscillator Name	Circuit Constant			Operating Voltage Range [V]	Oscillator Stabilization Time $tms^{X'tal}$(typ) [s]	Remarks
			C1 [pF]	C2 [pF]	Rd [Ω]			
32.768kHz	RIVER ELETEC	TFX-03 (CL=12.5pF)	15	15	680k	V_{DD}CPU= 3.0 to 3.6		

The oscillation stabilization time refers to the time interval that is required for the oscillation to get stabilized after the instruction for starting the XT oscillator circuit is executed plus the time interval that is required for the oscillation to get stabilized after the HOLD mode is released (see Figure 11).

Note: The traces to and from the components that are involved in oscillation should be kept as short as possible as the oscillation characteristics are affected by their trace pattern.

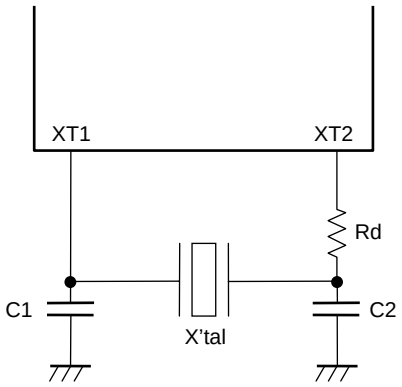


Figure 10 XT Oscillator Circuit

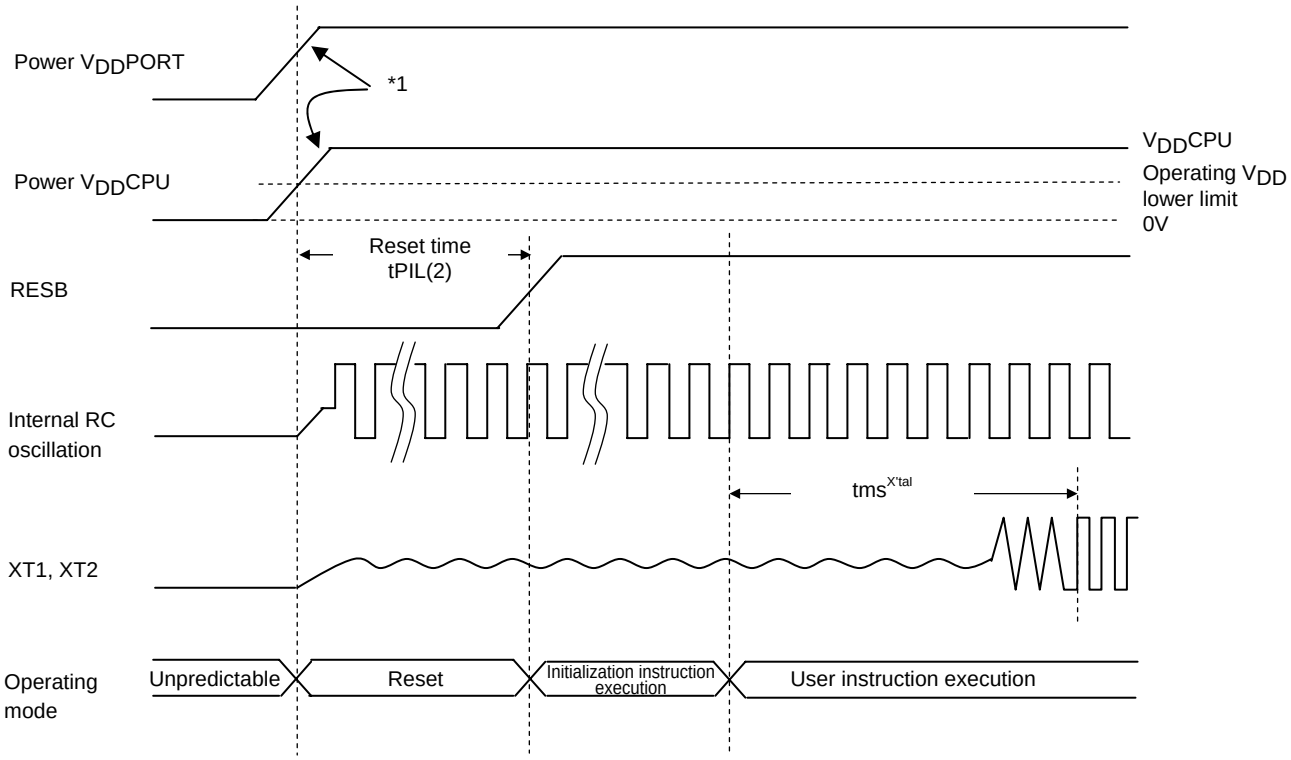


Figure 11 Reset Time and Oscillation Stabilization Time

*1: The voltage when the power is turned on and off must stand in the following relationship: V_{DD}PORT ≥ V_{DD}CPU. It should be noted that, while the V_{DD}PORT power is supplied, the I/O pin remains in an undefined state until the V_{DD}CPU voltage reaches the allowable operation range.

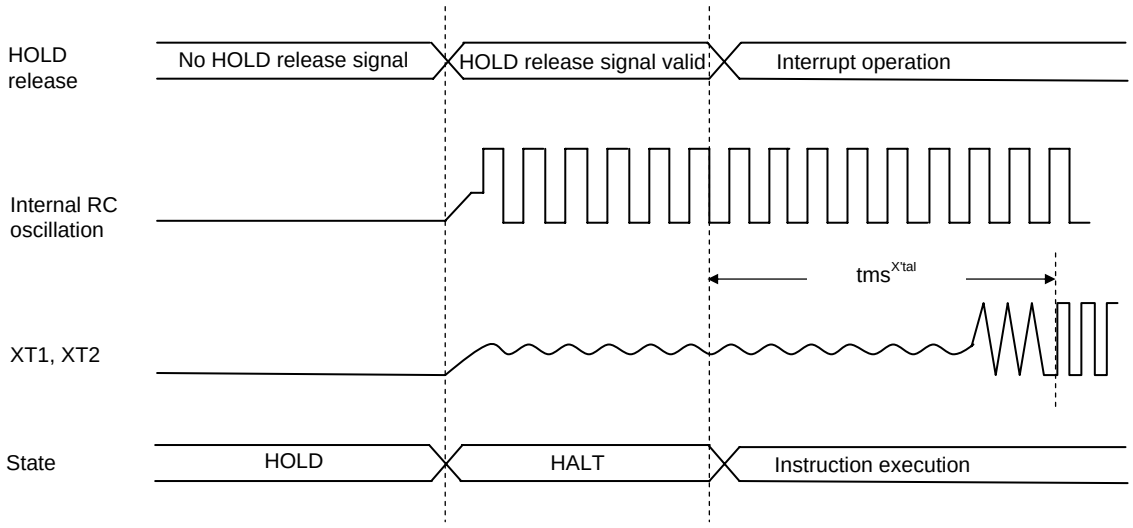
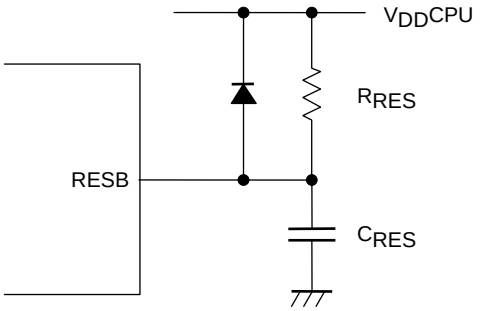


Figure 12 HOLD Release and Oscillation Stabilization Time

Reset Pin Treatment Condition (RESB)



(Note)
When the power is turned on, the RESB pin must be set to the low level.
(A reset period of 50μs or longer is required after the power has stabilized.)

Recommended value
R_{RES}: 100kΩ
C_{RES}: 0.033μF

Figure 13 Reset Circuit

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