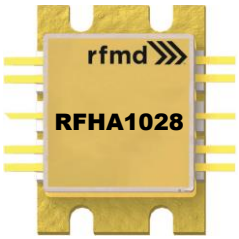
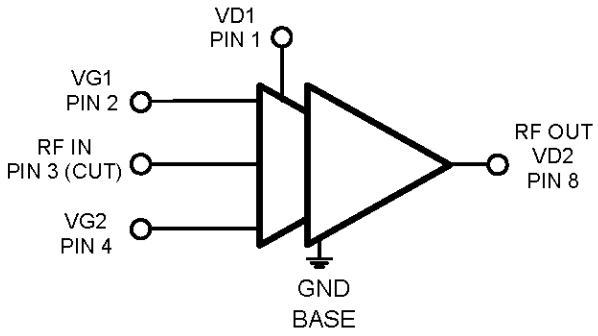
RFHA1028

160W GaN Wide-Band Pulsed Power Amplifier



Package: Flanged Ceramic, 10 pin

The RFHA1028 is a 45V 160W two-stage high power amplifier designed for L-Band pulsed radar, air traffic control and surveillance and general purpose broadband amplifiers applications. Using an advanced high power density gallium nitride (GaN) semiconductor process, these high performance amplifiers achieve high output power, high efficiency and flat gain over a broad frequency range in a single package. The RFHA1028 is an input matched power GaN transistor with 30dB small signal gain packaged in a ceramic package. The package provides excellent thermal stability through the use of advanced heat sink and power dissipation technologies. Ease of integration is accomplished through the incorporation of single, optimized matching networks that provide wideband gain and power performance in a single amplifier.



Functional Block Diagram

Features

- Wideband Operation: 1.2GHz to 1.4GHz
- Advanced GaN HEMT Technology
- Input Optimized Evaluation Board Layout for 50Ω Operation
- Integrated Matching Components for High Terminal Impedances at Input
- 45V Operation Typical Performance
  - Output Pulsed Power 160W
  - Pulse Width 1ms, Duty Cycle 10%
  - Small Signal Gain 26.5dB
  - High Efficiency 48%
  - -40°C to 85°C Operation

Applications

- Radar
- Air Traffic Control and Surveillance
- General Purpose Broadband Amplifiers

Ordering Information

RFHA1028S2	Sample bag with 2 pieces
RFHA1028SB	Bag with 5 pieces
RFHA1028SQ	Bag with 25 pieces
RFHA1028SR	7” Short reel with 50 pieces
RFHA1028TR13	13” Reel with 250 pieces
RFHA1028PCBA-410	Fully Assembled Evaluation Board Optimized for 1.2GHz to 1.4GHz; 45V

RF Micro Devices Inc. 7628 Thorndike Road, Greensboro, NC 27409-9421
For sales or technical support, contact RFMD at +1.336.678.5570 or customerservice@rfmd.com.

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Absolute Maximum Ratings

Parameter	Rating	Unit
Drain Voltage Output Stage (V_{D2})	150	V
Drain Voltage Input Stage (V_{D1})	100	V
Gate Voltage (V_G)	-6 to 2	V
Operating Voltage	45	V
Ruggedness (VSWR)	10:1	
Storage Temperature Range	-55 to +125	°C
Operating Temperature Range (T_C)	-40 to +85	°C
Operating Junction Temperature (T_J)	250	°C
Human Body Model	Class 1A	
MTTF (T_J < 200°C, 95% Confidence Limits)* MTTF (T_J < 250°C, 95% Confidence Limits)*	3.0E + 06 1.4E + 05	Hours
Thermal Resistance, R_{TH} (Junction to Case) T_C =85°C, DC Bias Only** T_C =85°C, 1ms Pulse, 10% Duty Cycle	 R_{TH1} = 3.5, R_{TH2} = 1.1 TBD	°C/W

Caution! ESD sensitive device.

RoHS (Restriction of Hazardous Substances): Compliant per EU Directive 2011/65/EU.

Exceeding any one or a combination of the Absolute Maximum Rating conditions may cause permanent damage to the device. Extended application of Absolute Maximum Rating conditions to the device may reduce device reliability. Specified typical performance or functional operation of the device under Absolute Maximum Rating conditions is not implied.

* MTTF – median time to failure for wear-out failure mode (30% I_{DSS} degradation) which is determined by the technology process reliability. Refer to product qualification report for FIT(random) failure rate.

Operation of this device beyond any one of these limits may cause permanent damage. For reliable continuous operation, the device voltage and current must not exceed the maximum operating values specified in the table above.

Bias Conditions should also satisfy the following expression: $P_{DISS} < (T_J - T_C) / R_{TH\ J\text{-}C}$ and $T_C = T_{CASE}$

** R_{th1} (driver stage) and R_{th2} (output stage) – estimated R_{th} data

Nominal Operating Parameters

Parameter	Specification			Unit	Condition
	Min	Typ	Max		
Recommended Operating Conditions					
Drain Voltage (V_{DSQ})		45		V	
Gate Voltage (V_{GSQ})	-5	-3	-2	V	
Drain Bias Current		350		mA	Stage 1 = 50mA, Stage 2 = 300mA
Gate Current Input Stage (I_{G1})		TBD			
Gate Current Output Stage (I_{G2})		TBD			
Frequency of Operation	1200		1400	MHz	
DC Functional Test					
V_{GSQ} Stage 1		-3.2		V	V_D = 45V, I_D Stage 1 = 50mA
V_{GSQ} Stage 2		-3.2		V	V_D = 45V, I_D Stage 2 = 300mA
$V_{DS(ON)}$ – Stage 2		0.25		V	V_G = 0V, I_D = 1.0A, Wafer level test

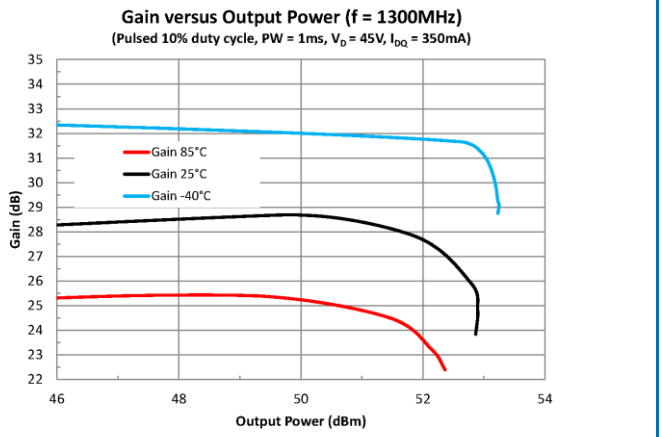
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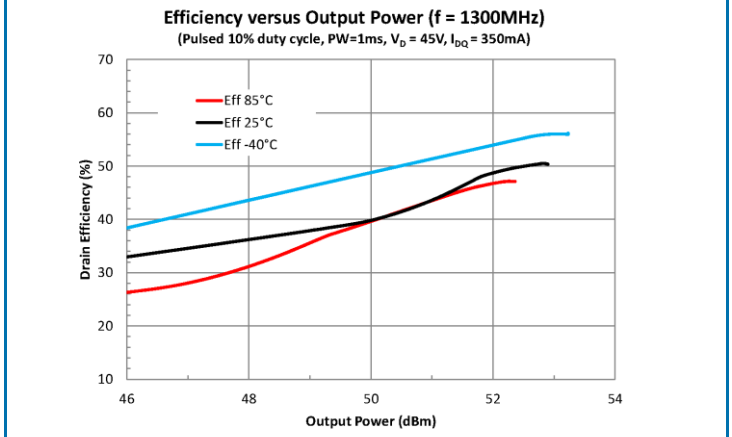
Parameter	Specification			Unit	Condition
	Min	Typ	Max		
RF Functional Test					
Small Signal Gain		23		dB	f = 1.2GHz, P_{IN} = 0dBm [1, 2]
Output Power	51	52		dBm	f = 1.2GHz, P_{IN} = 27dBm [1, 2]
Power Gain	24.5	25		dB	
Drain Efficiency	38	42		%	
Input Return Loss		-15	-10	dB	
2nd Harmonic		-33.5		dBc	
3rd Harmonic		-20.5		dBc	
Small Signal Gain		25.5		dB	f = 1.3GHz, P_{IN} = 0dBm [1, 2]
Output Power	51	52.5		dBm	f = 1.3GHz, P_{IN} = 27dBm [1, 2]
Power Gain	25	25.6		dB	
Drain Efficiency	45	50		%	
Input Return Loss		-14.5	-10	dB	
2nd Harmonic		-35		dBc	
3rd Harmonic		-25.5		dBc	
Small Signal Gain		28.5		dB	f = 1.4GHz, P_{IN} = 0dBm [1, 2]
Output Power	51	51.7		dBm	f = 1.4GHz, P_{IN} = 27dBm [1, 2]
Power Gain	24.5	25.2		dB	
Drain Efficiency	45	52		%	
Input Return Loss		-17	-10	dB	
2nd Harmonic		-27.5		dBc	
3rd Harmonic		-25		dBc	
RF Typical Performance					
Small Signal Gain		26.5		dB	P_{IN} = 0dBm [1, 2]
Gain Variation with Temperature		0.02		dB/°C	At peak output power [1, 2]
Output Power (P_{SAT})		52.5		dBm	P_{IN} = 27dBm [1, 2]
		178		W	
Drain Efficiency		48.0		%	At peak output power [1, 2]
Power Gain		25		dB	
Efficiency		50		%	
Input Return Loss		-15		dB	

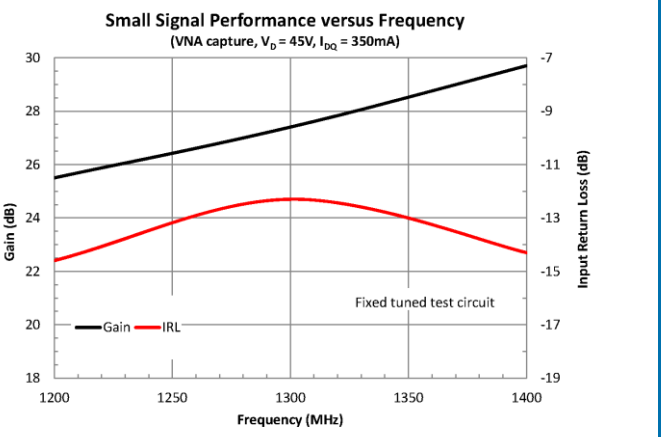
[1] Test Conditions: PW = 1ms,DC = 10%, V_{DSQ} = 45V, I_{DQ1} = 50mA, I_{DQ2} = 300mA, T = 25ºC.
[2] Performance in a standard tuned test fixture.

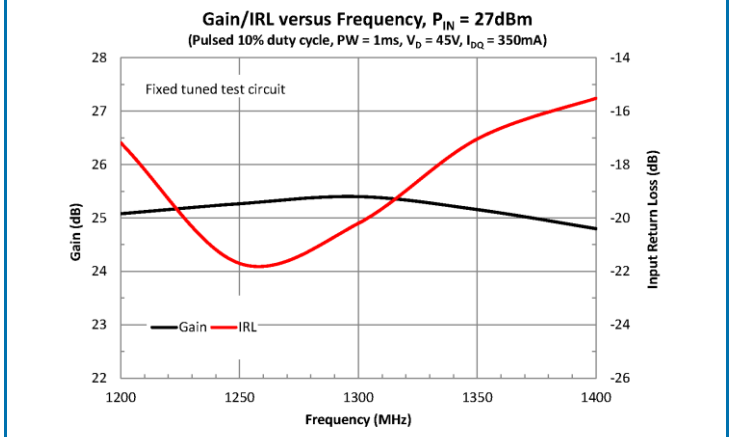
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Typical Performance in Standard Fixed Tuned Test Fixture: (T = 25°C unless noted)



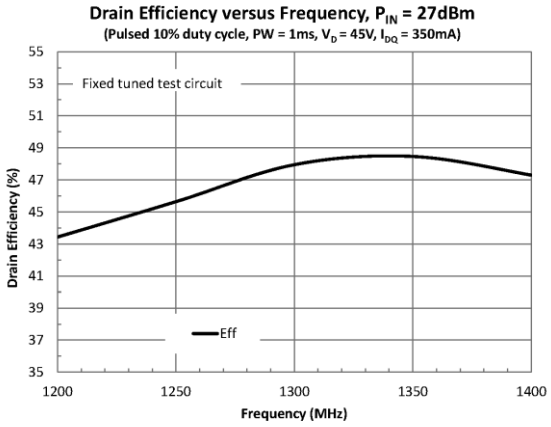


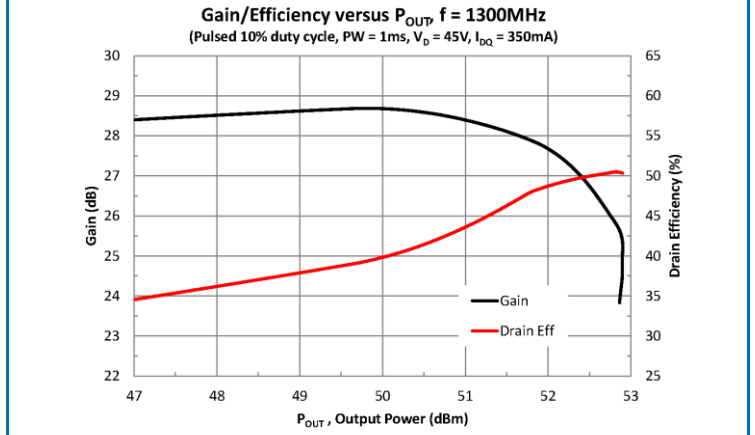


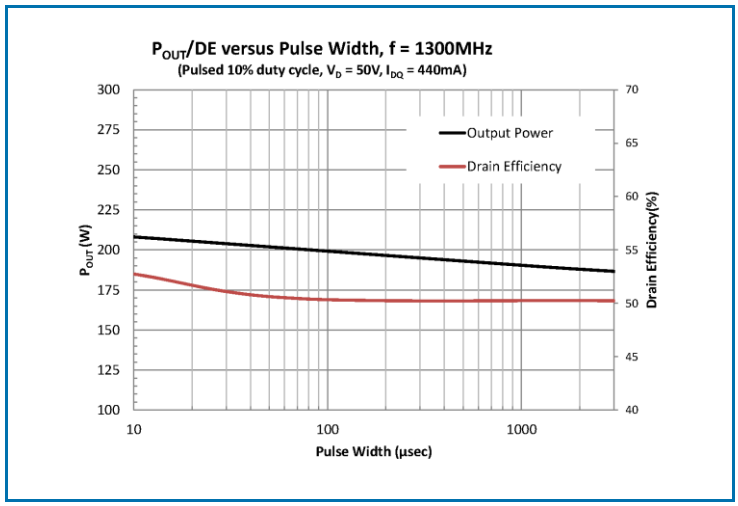


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Typical Performance in Standard Fixed Tuned Test Fixture: (T = 25°C unless noted) (continued)

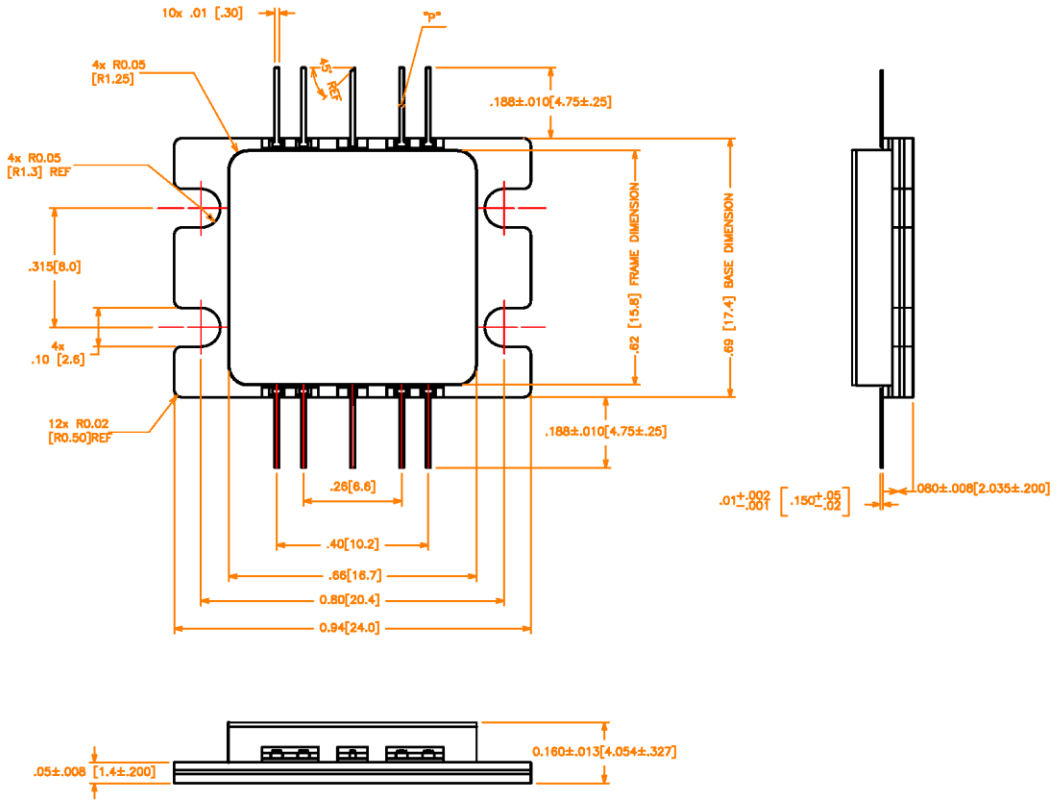






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Package Drawing (Dimensions in millimeters)



Note:
FINISH: Au PLATE 1.0µm MIN. THICKNESS OVER Ni BASE.
PLATING THICKNESS MEASURED ON POINT 'P'.

Pin Names and Descriptions

Pin	Name	Description
1	DRAIN 1	Drain - V_D First Stage
2	GATE 1	Gate - V_G First Stage
3	GATE	RF Input
4	GATE 2	Gate - V_G Output Stage
5	NC	No Connect
6	NC	No Connect
7	NC	No Connect
8	DRAIN	V_D and RF Output
9	NC	No Connect
10	NC	No Connect

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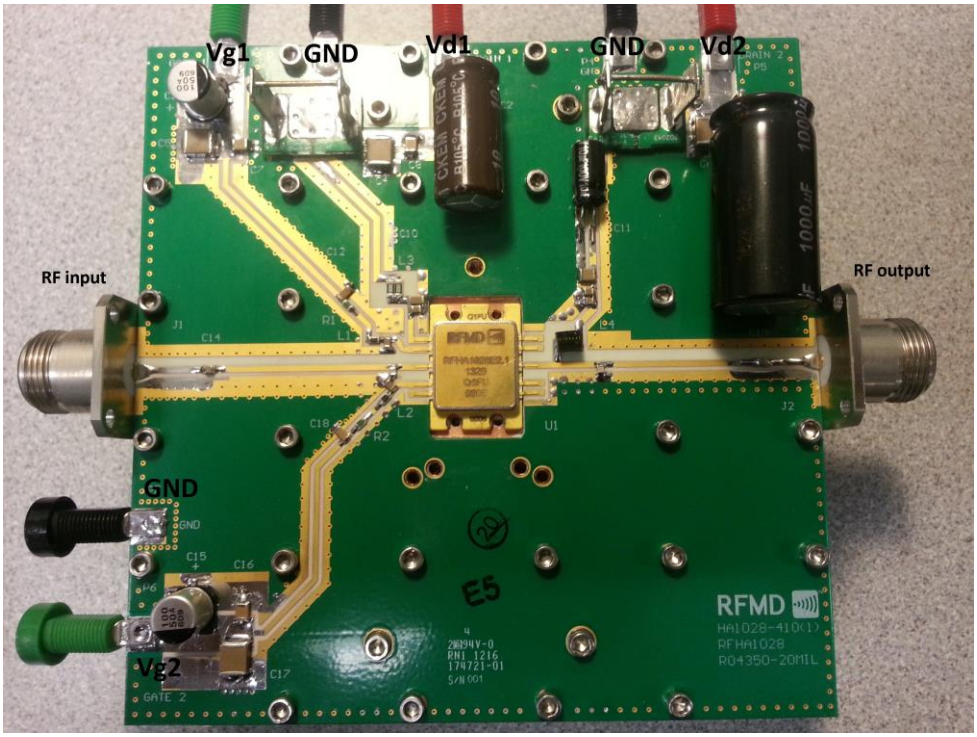
Bias Instruction for RFHA1028 1.2GHz to 1.4GHz Evaluation Board

ESD Sensitive Material. Please use proper ESD precautions when handling devices of evaluation board.
Evaluation board requires additional external fan cooling.
Connect all supplies before powering evaluation board.

1. Connect RF cables at RFIN and RFOUT.
2. Connect ground to the ground supply terminal, and ensure that both the VG and VD grounds are also connected to this ground terminal.
3. Apply -5V to VG1 and VG2.
4. Apply 45V to VD1 and VD2.
5. Increase V_{G1} until drain current for VD1 reaches 50mA or desired bias point.
6. Increase V_{G2} until drain current for VD2 reaches 300mA or desired bias point.
7. Turn on the RF input.

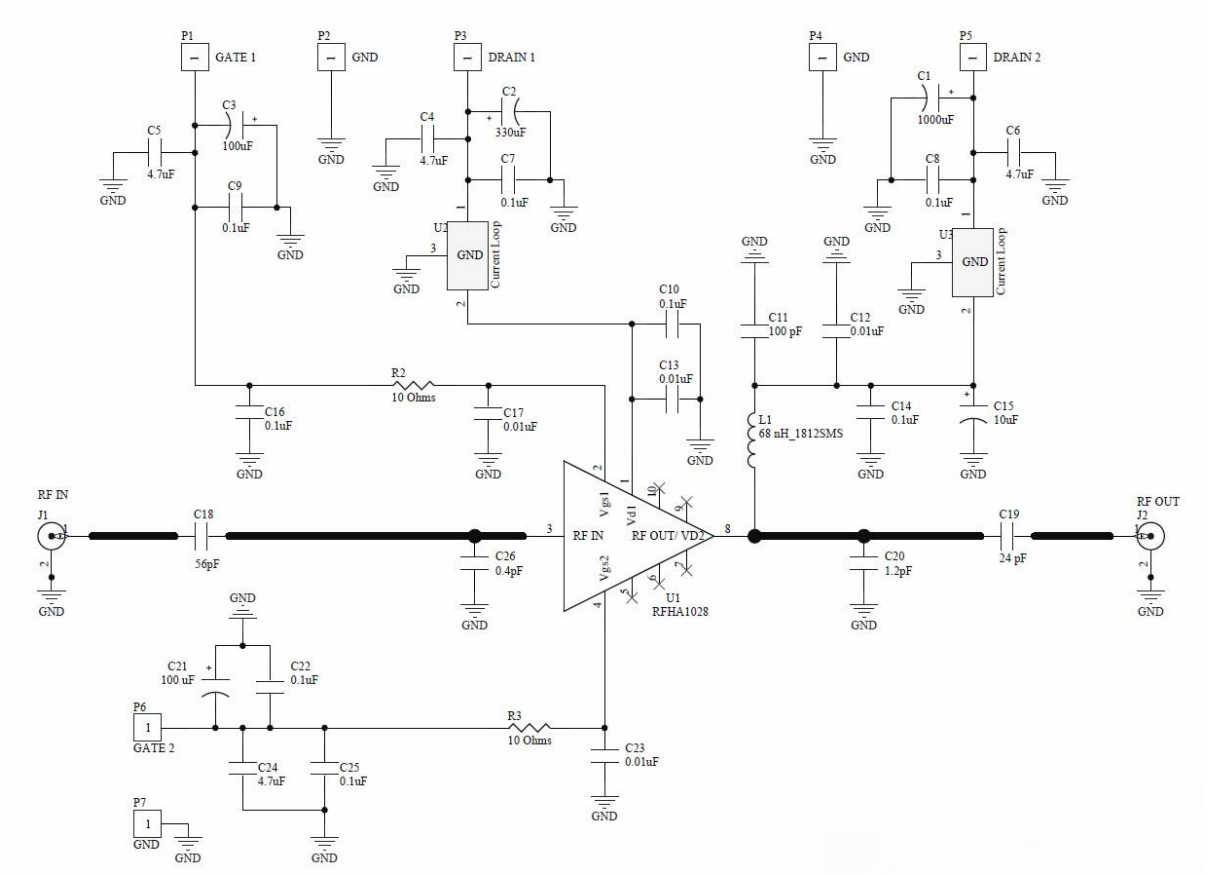
IMPORTANT NOTE: Depletion mode device - when biasing the device V_G must be applied BEFORE V_D. When removing bias V_D must be removed BEFORE V_G is removed. Failure to follow sequencing will cause the device to fail.

Note: For optimal RF performance, consistent and optimal heat removal from the base of the package is required. A thin layer of thermal grease should be applied to the interface between the base of the package and the equipment chassis. It is recommended a small amount of thermal grease is applied to the underside of the device package. Even application and removal of excess thermal grease can be achieved by spreading the thermal grease using a razor blade. The package should then be bolted to the chassis and input and output leads soldered to the circuit board.



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Proposed Evaluation Board Schematic



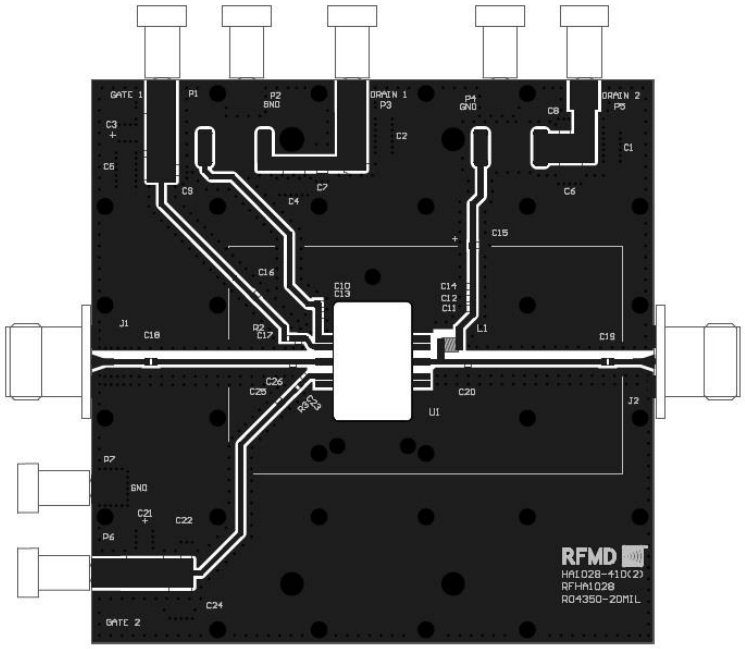
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Proposed Evaluation Board Bill of Materials

Component	Value	Manufacturer	Part Number
C3, C21	100µF	Panasonic	ECE-V1HA101UP
C2	330µF	Panasonic	EEU-FC2A331
C1	1000µF	Panasonic	ECA-2AHG102
C4, C5, C6, C24	4.7µF	Murata	GRM55ER72A475KA01L
C7, C8, C9, C22	0.1µF	Murata	GRM32NR72A104KA01L
C11	100pF	ATC	ATC800A101JT
C10, C14, C16, C25	0.1µF	Panasonic	ECJ-2VB2A104K
C19	24pF	ATC	ATC800A240JT
C18	56pF	ATC	ATC800A560JT
C12, C13, C17, C23	0.01µF	Panasonic	ECJ-2VB2A103K
C15	10µF	Panasonic	ECA-2AM100
C20	1.2pF	ATC	ATC800A1R2BT
C26	0.4pF	ATC	ATC800A0R4BT
L1	68nH	Coilcraft	1812SMS-68NJLB
R2, R3	10Ω	Panasonic	ERJ-8GEYJ100V

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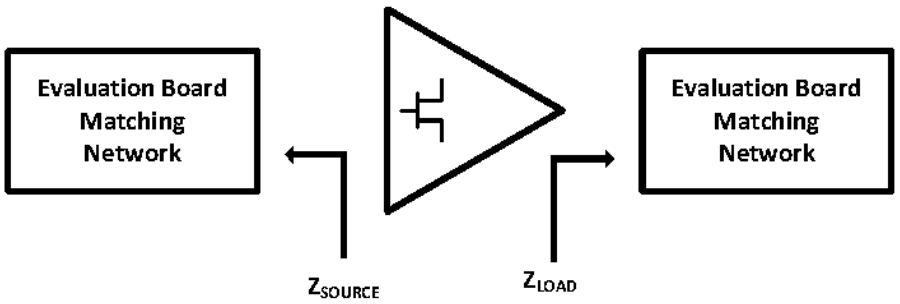
Evaluation Board Layout



Simulated Evaluation Board Impedances

Frequency	Z Source (Ω)	Z Load (Ω)
1200MHz	TBD	TBD
1300MHz	TBD	TBD
1400MHz	TBD	TBD

Device impedances reported are the simulated evaluation board impedances chosen for a tradeoff of efficiency, peak power, and linearity performance across the entire frequency bandwidth.



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Device Handling/Environmental Conditions

GaN HEMT devices are ESD sensitive materials. Please use proper ESD precautions when handling devices or evaluation boards.

DC Bias

The GaN HEMT device is a depletion mode high electron mobility transistor (HEMT). At zero volts V_{GS} the drain of the device is saturated and uncontrolled drain current will destroy the transistor. The gate voltage must be taken to a potential lower than the source voltage to pinch off the device prior to applying the drain voltage, taking care not to exceed the gate voltage maximum limits. RFMD recommends applying V_{GS} = -5V before applying any V_{DS}.

RF Power transistor performance capabilities are determined by the applied quiescent drain current. This drain current can be adjusted to trade off power, linearity, and efficiency characteristics of the device. The recommended quiescent drain current (I_{DQ}) shown in the RF typical performance table is chosen to best represent the operational characteristics for this device, considering manufacturing variations and expected performance. The user may choose alternate conditions for biasing this device based on performance tradeoffs.

Mounting and Thermal Considerations

The thermal resistance provided as R_{TH} (junction to case) represents only the packaged device thermal characteristics. This is measured using IR microscopy capturing the device under test temperature at the hottest spot of the die. At the same time, the package temperature is measured using a thermocouple touching the backside of the die embedded in the device heatsink but sized to prevent the measurement system from impacting the results. Knowing the dissipated power at the time of the measurement, the thermal resistance is calculated.

In order to achieve the advertised MTTF, proper heat removal must be considered to maintain the junction at or below the maximum of 200°C. Proper thermal design includes consideration of ambient temperature and the thermal resistance from ambient to the back of the package including heatsinking systems and air flow mechanisms. Incorporating the dissipated DC power, it is possible to calculate the junction temperature of the device.

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