

MAX17502

60V, 1A, Ultra-Small, High-Efficiency, Synchronous Step-Down DC-DC Converter

General Description

The MAX17502 high-efficiency, high-voltage, synchronous step-down DC-DC converter operates over a 4.5V to 60V input voltage range and is designed for a wide range of applications. The ultra-wide-input operation makes it ideal for not only industrial control and building automation, but also base stations, telecom, home entertainment, and automotive applications. It delivers output currents up to 1A, at output voltages of 3.3V and 5V. The output voltage is accurate within $\pm 1.6\%$ over temperature. The device operates over the -40°C to $+125^{\circ}\text{C}$ industrial temperature range and is available in a tiny, 10-pin (3mm x 2mm) TDFN lead(Pb)-free package with an exposed pad.

The device features peak-current-mode control with pulse-width modulation (PWM). The PWM operation ensures constant switching frequency at all operating conditions. The low-resistance, on-chip, pMOS/nMOS switches ensure high efficiency at full load while minimizing the critical inductances, making the layout a much simpler task compared to discrete solutions.

The device offers fixed switching frequency of 600kHz. To reduce input inrush current, the device offers an adjustable voltage soft-start feature with an external capacitor from the SS pin to ground. The device also incorporates an output enable/undervoltage lockout pin (EN/UVLO) that allows the user to turn on the part at the desired input-voltage level. An open-drain RESET pin provides a delayed power-good signal to the system upon achieving successful regulation of the output voltage. The device supports hiccup-mode current-limit protection for low power dissipation under overload and output short-circuit conditions.

Applications

- Industrial Process Control
- HVAC and Building Control
- General-Purpose Point-of-Load
- Base Station, VOIP, Telecom
- Home Theater
- Automotive
- Battery-Powered Equipment

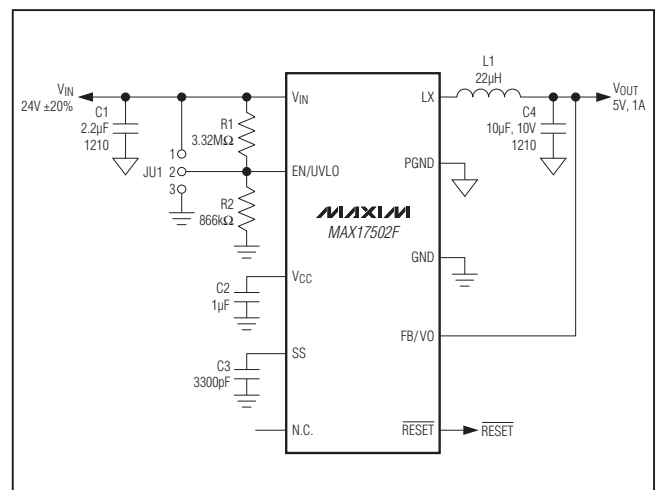
Ordering Information appears at end of data sheet.

For related parts and recommended products to use with this part, refer to www.maxim-ic.com/MAX17502.related

Benefits and Features

- ◆ **Eliminate External Components and Reduce Total Cost**
 - ◇ No Schottky-Synchronous Operation for High Efficiency and Reduced Cost
 - ◇ Internal Compensation for Ultra-Compact Layout
 - ◇ All-Ceramic Capacitors
- ◆ **Reduce Number of DC-DC Regulators to Stock**
 - ◇ Wide 4.5V to 60V Operating-Voltage Range
 - ◇ Fixed 3.3V and 5V Output
 - ◇ Delivers Up to 1A Over Temperature
 - ◇ 600kHz Switching Frequency
- ◆ **Reduce Power Dissipation**
 - ◇ Peak Efficiency > 90%
 - ◇ Shutdown Current = 1 μA (typ)
- ◆ **Operate Reliably in Adverse Industrial Environments**
 - ◇ Hiccup-Mode Current Limit and Autoretry Startup
 - ◇ Built-In Output-Voltage Monitoring (Open-Drain RESET Pin)
 - ◇ Resistor-Programmable UVLO Threshold
 - ◇ Increased Safety with Adjustable Soft-Start and Prebiased Power-Up
 - ◇ Optional Adjustable Output and PFM (Available Upon Factory Request)
 - ◇ -40°C to $+125^{\circ}\text{C}$ Industrial Temperature Range

Typical Operating Circuit



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ABSOLUTE MAXIMUM RATINGS

V_{IN} to GND	-0.3V to +70V	Continuous Power Dissipation ($T_A = +70^\circ\text{C}$)
EN/UVLO to GND	-0.3V to $V_{IN} + 0.3\text{V}$	10-Pin TDFN (derate 14.9mW/ $^\circ\text{C}$ above $+70^\circ\text{C}$)
LX to PGND	-0.3V to +70V	(multilayer board)
FB, RESET, COMP, SS to GND.....	-0.3V to 6V	1188.7mW
V_{CC} to GND.....	-0.3V to +6V	Operating Temperature Range.....
GND to PGND	-0.3V to +0.3V	-40 $^\circ\text{C}$ to +125 $^\circ\text{C}$
LX Total RMS Current.....	$\pm 1.6\text{A}$	Junction Temperature
Output Short-Circuit Duration.....	Continuous	+150 $^\circ\text{C}$
		Storage Temperature Range.....
		-65 $^\circ\text{C}$ to +160 $^\circ\text{C}$
		Lead Temperature (soldering, 10s)
		+300 $^\circ\text{C}$
		Soldering Temperature (reflow)
		+260 $^\circ\text{C}$

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PACKAGE THERMAL CHARACTERISTICS (Note 1)

Thermal Resistance

TDFN

Junction-to-Ambient Thermal Resistance (θ_{JA})	67.3 $^\circ\text{C}/\text{W}$	Junction-to-Case Thermal Resistance (θ_{JC})	18.2 $^\circ\text{C}/\text{W}$
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Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to www.maxim-ic.com/thermal-tutorial.

ELECTRICAL CHARACTERISTICS

($V_{IN} = 24\text{V}$, $V_{GND} = V_{PGND} = 0\text{V}$, $C_{VIN} = 2.2\mu\text{F}$, $C_{VCC} = 1\mu\text{F}$, $V_{EN} = 1.5\text{V}$, $C_{SS} = 3300\text{pF}$, $V_{FB} = 0.98 \times V_{OUT}$, LX = unconnected, RESET = unconnected. $T_A = T_J = -40^\circ\text{C}$ to $+125^\circ\text{C}$, unless otherwise noted. Typical values are at $T_A = +25^\circ\text{C}$. All voltages are referenced to GND, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
INPUT SUPPLY (V_{IN})						
Input Voltage Range	V_{IN}		4.5		60	V
Input Supply Current	I_{IN-SH}	$V_{EN} = 0\text{V}$, shutdown mode		0.9	3.5	μA
	I_{IN-SW}	Normal switching mode, $V_{COMP} = 0.8\text{V}$	$V_{IN} = 12\text{V}$	3.7	5.2	mA
$V_{IN} = 24\text{V}$			5	6.75		
ENABLE/UVLO (EN/UVLO)						
EN Threshold	V_{ENR}	V_{EN} rising	1.194	1.218	1.236	V
	V_{ENF}	V_{EN} falling	1.114	1.135	1.156	
	$V_{EN-TRUESD}$	V_{EN} falling, true shutdown		0.75		
EN Input Leakage Current	I_{EN}	$V_{EN} = V_{IN} = 60\text{V}$, $T_A = +25^\circ\text{C}$		7	200	nA
LDO						
V_{CC} Output Voltage Range	V_{CC}	$6\text{V} < V_{IN} < 12\text{V}$, $0\text{mA} < I_{VCC} < 10\text{mA}$, $12\text{V} < V_{IN} < 60\text{V}$, $0\text{mA} < I_{VCC} < 2\text{mA}$	4.65	5	5.35	V
V_{CC} Current Limit	$I_{VCC-MAX}$	$V_{CC} = 4.3\text{V}$, $V_{IN} = 12\text{V}$	17	40	80	mA
V_{CC} Dropout	V_{CC-DO}	$V_{IN} = 4.5\text{V}$, $I_{VCC} = 5\text{mA}$	4.1			V
V_{CC} UVLO	V_{CC-UVR}	V_{CC} rising	3.85	4	4.15	V
	V_{CC-UVF}	V_{CC} falling	3.55	3.7	3.85	

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ELECTRICAL CHARACTERISTICS (continued)

($V_{IN} = 24V$, $V_{GND} = V_{PGND} = 0V$, $C_{VIN} = 2.2\mu F$, $C_{VCC} = 1\mu F$, $V_{EN} = 1.5V$, $C_{SS} = 3300pF$, $V_{FB} = 0.98 \times V_{OUT}$, LX = unconnected, RESET = unconnected. $T_A = T_J = -40^\circ C$ to $+125^\circ C$, unless otherwise noted. Typical values are at $T_A = +25^\circ C$. All voltages are referenced to GND, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
LX							
LX Leakage Current	I_{LX_LKG}	$V_{EN} = 0V$, $T_A = +25^\circ C$, $V_{LX} = (V_{PGND} + 1V)$ to $(V_{IN} - 1V)$				1	μA
SOFT-START (SS)							
Switchover to Internal Reference Voltage Threshold	V_{SS-TH}			863	880	898	mV
Charging Current	I_{SS}	$V_{SS} = 0.5V$		4.7	5	5.3	μA
FEEDBACK (FB)							
FB Input Bias Current	I_{FB}	$T_A = +25^\circ C$	MAX17502E, $V_{FB} = 3.3V$	6.8	12	17	μA
			MAX17502F, $V_{FB} = 5V$	6.8	12	17	μA
OUTPUT VOLTAGE (V_{OUT})							
Output Voltage Range	V_{OUT}	MAX17502E only		3.248	3.3	3.352	V
		MAX17502F only		4.922	5	5.08	
CURRENT LIMIT							
Peak-Current-Limit Threshold	$I_{PEAK-LIMIT}$			1.35	1.6	1.85	A
Runaway-Current-Limit Threshold	$I_{RUNAWAY-LIMIT}$			1.55	1.8	2.05	A
Valley Current-Limit Threshold	$I_{SINK-LIMIT}$			0.56	0.65	0.74	A
TIMING							
Switching Frequency	f_{SW}	$V_{FB} > V_{OUT-HICF}$	MAX17502E/F	560	600	640	kHz
		$V_{FB} < V_{OUT-HICF}$		280	300	320	
Events to Hiccup After Crossing Runaway Current Limit					1		

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ELECTRICAL CHARACTERISTICS (continued)

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PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OUT} Undervoltage Trip Level to Cause Hiccup	$V_{OUT-HICF}$	$V_{SS} > 0.95V$ (soft-start is done)		69.14	71.14	73.14	%
Hiccup Timeout					32,768		Cycles
Minimum On-Time	t_{ON_MIN}				85	120	ns
Maximum Duty Cycle	D_{MAX}	$V_{FB} = 0.98 \times V_{FB-REG}$	MAX17502E/F	92	94	96	%
LX Dead Time					5		ns
RESET							
\overline{RESET} Output Level Low		$I_{\overline{RESET}} = 1mA$				0.02	V
\overline{RESET} Output Leakage Current High		$V_{FB} = 1.01 \times V_{OUT}$, $T_A = +25^\circ C$				0.45	μA
V_{OUT} Threshold for \overline{RESET} Assertion	$V_{OUT-OKF}$	V_{FB} falling		90.5	92.5	94.5	%
V_{OUT} Threshold for \overline{RESET} Deassertion	$V_{OUT-OKR}$	V_{FB} rising		93.5	95.5	97.5	%
\overline{RESET} Deassertion Delay after FB Reaches 95% Regulation					1024		Cycles
THERMAL SHUTDOWN							
Thermal-Shutdown Threshold		Temperature rising			165		$^\circ C$
Thermal-Shutdown Hysteresis					10		$^\circ C$

Note 2: All limits are 100% tested at $+25^\circ C$. Limits over temperature are guaranteed by design.

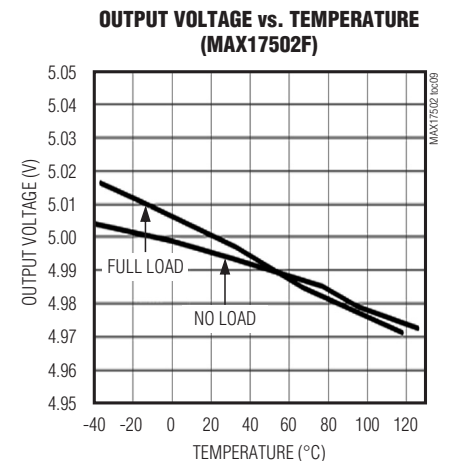
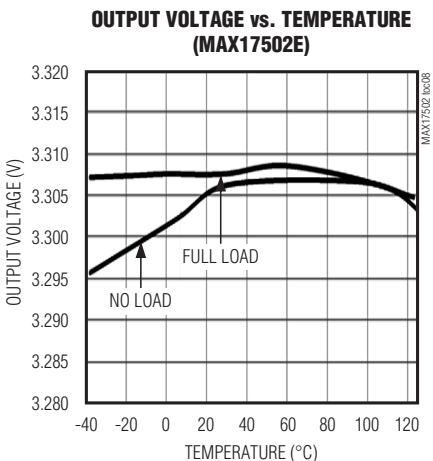
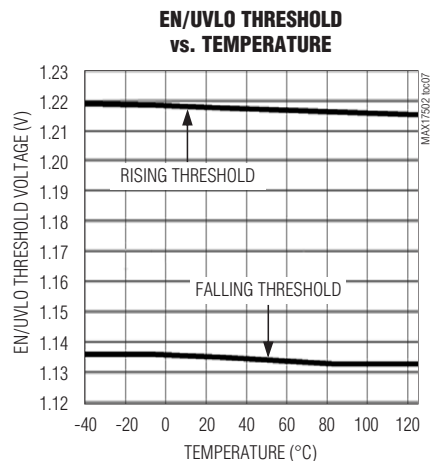
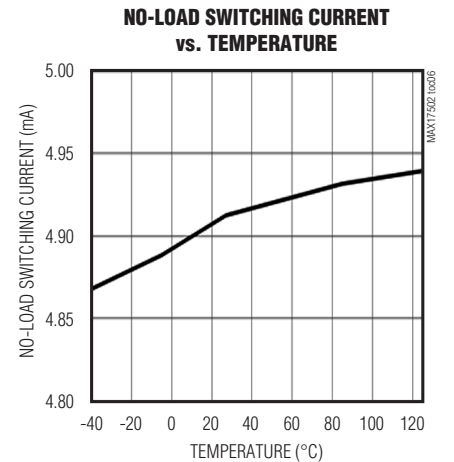
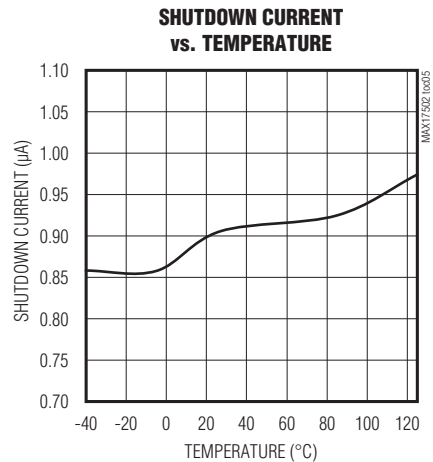
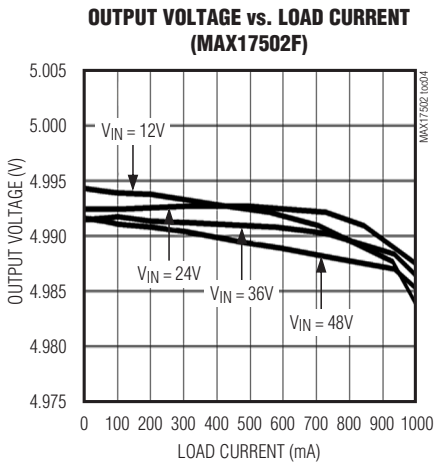
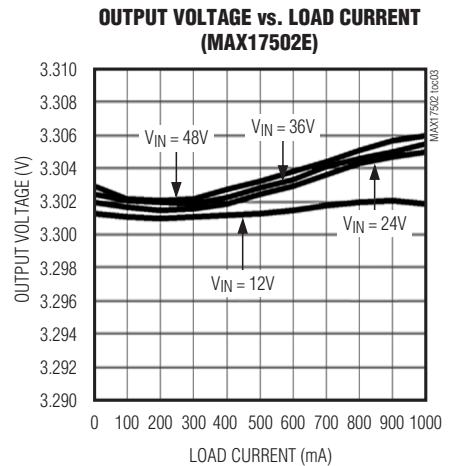
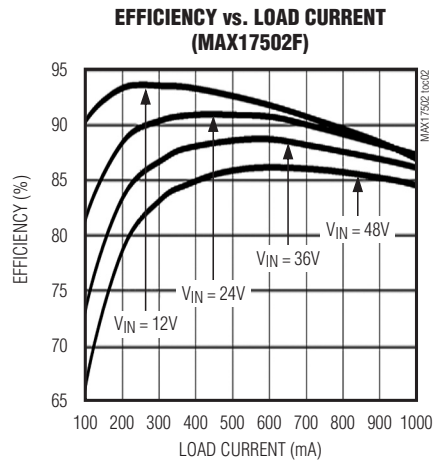
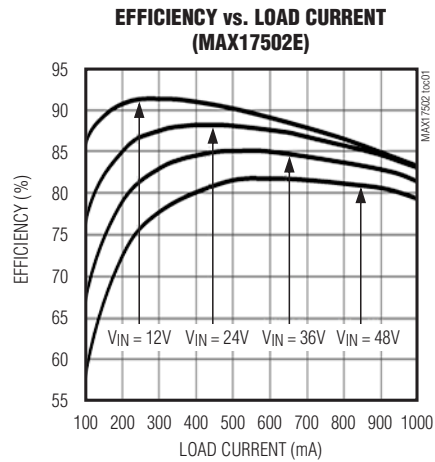
Note 3: Guaranteed by design, not production tested.

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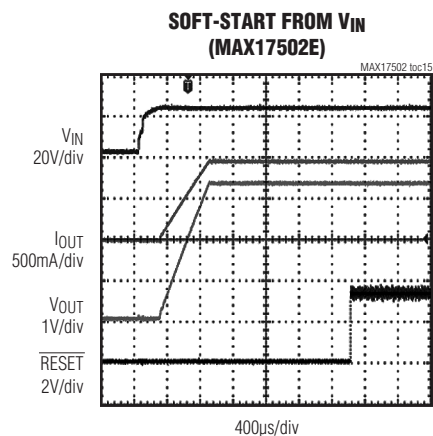
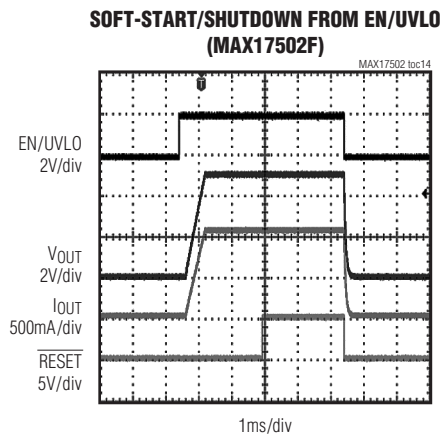
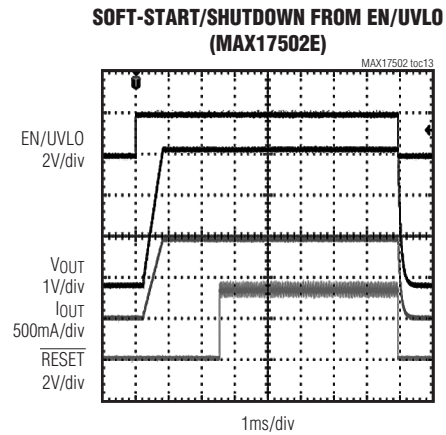
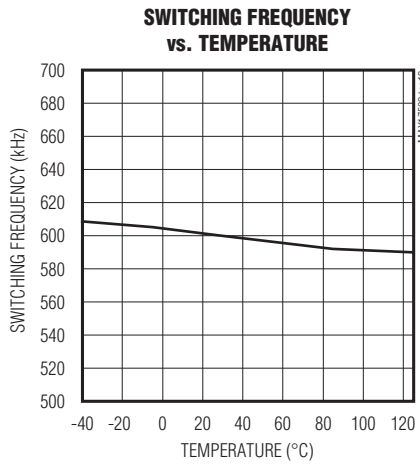
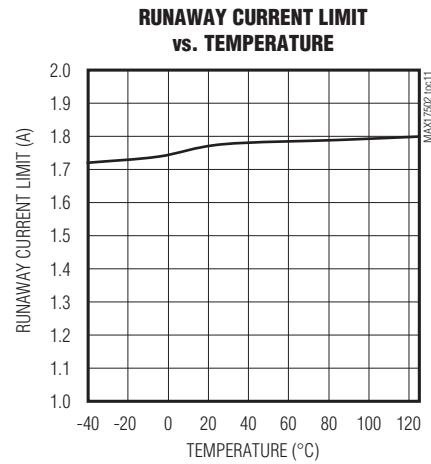
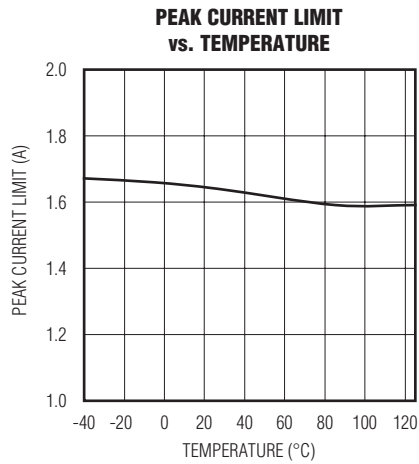


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Typical Operating Characteristics (continued)

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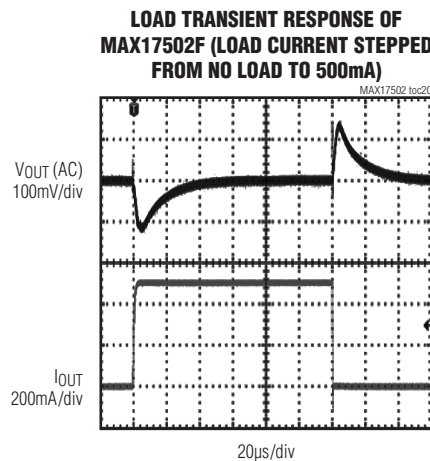
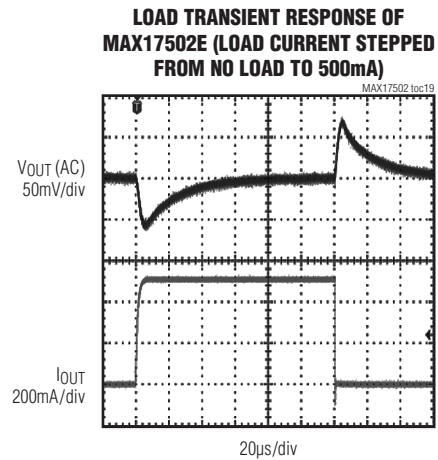
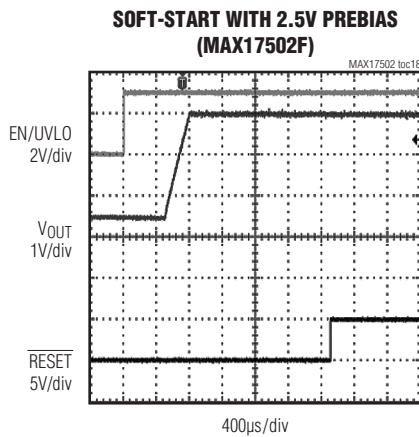
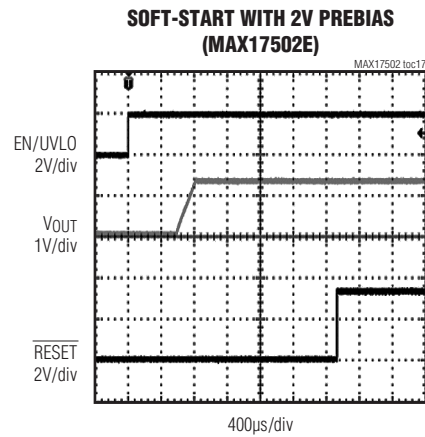
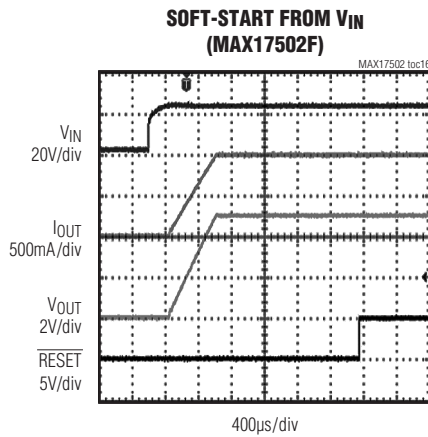


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Typical Operating Characteristics (continued)

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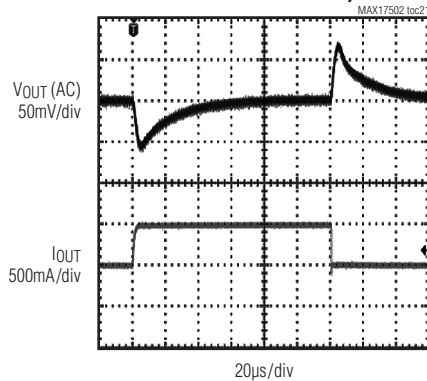
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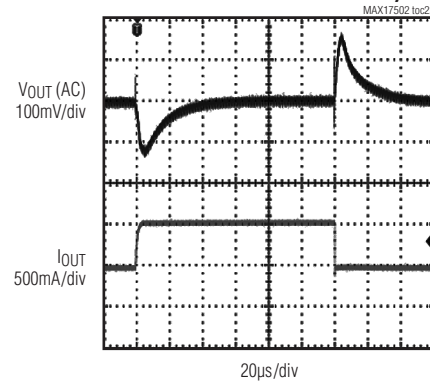
Typical Operating Characteristics (continued)

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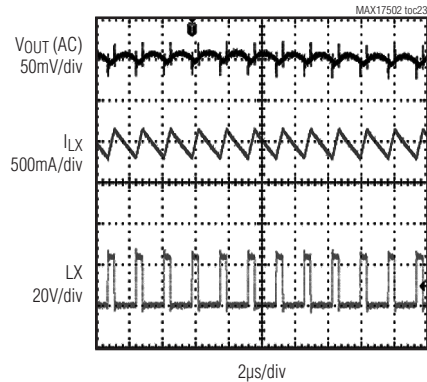
**LOAD TRANSIENT RESPONSE OF
MAX17502F (LOAD CURRENT STEPPED
FROM 500mA TO 1A)**



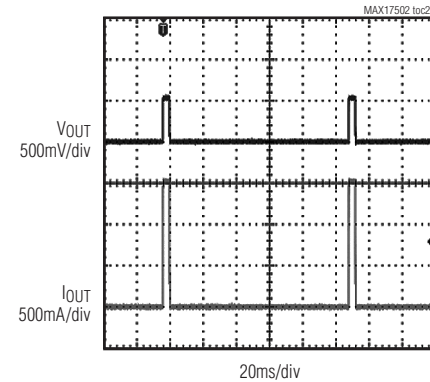
**LOAD TRANSIENT RESPONSE OF
MAX17502E (LOAD CURRENT STEPPED
FROM 500mA TO 1A)**



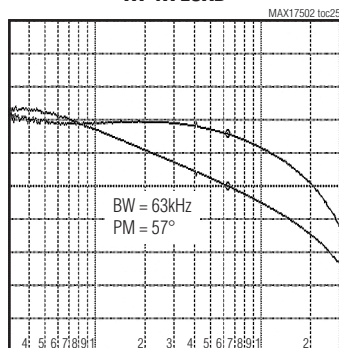
**SWITCHING WAVEFORMS OF
MAX17502F AT 1A LOAD**



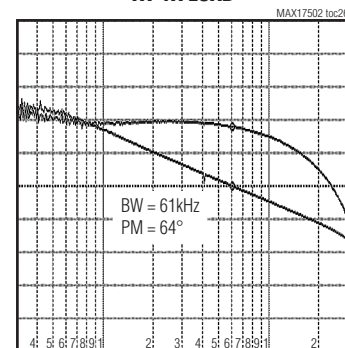
**OUTPUT OVERLOAD
PROTECTION OF MAX17502F**



**BODE PLOT OF MAX17502E
AT 1A LOAD**



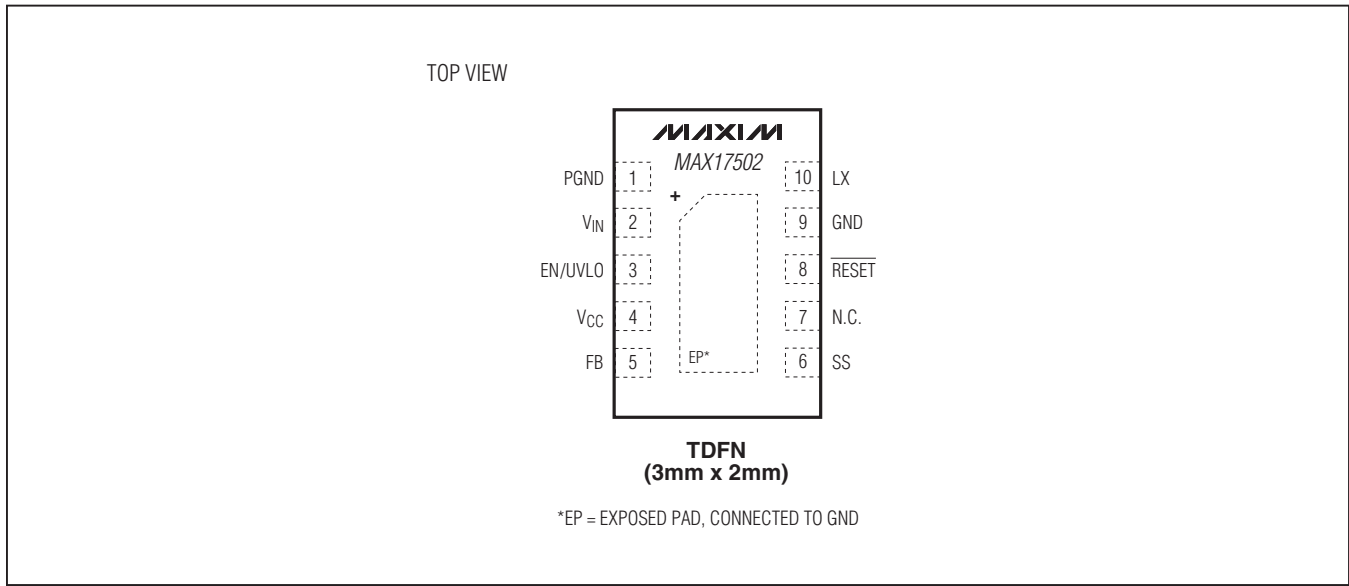
**BODE PLOT OF MAX17502F
AT 1A LOAD**



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Pin Configuration



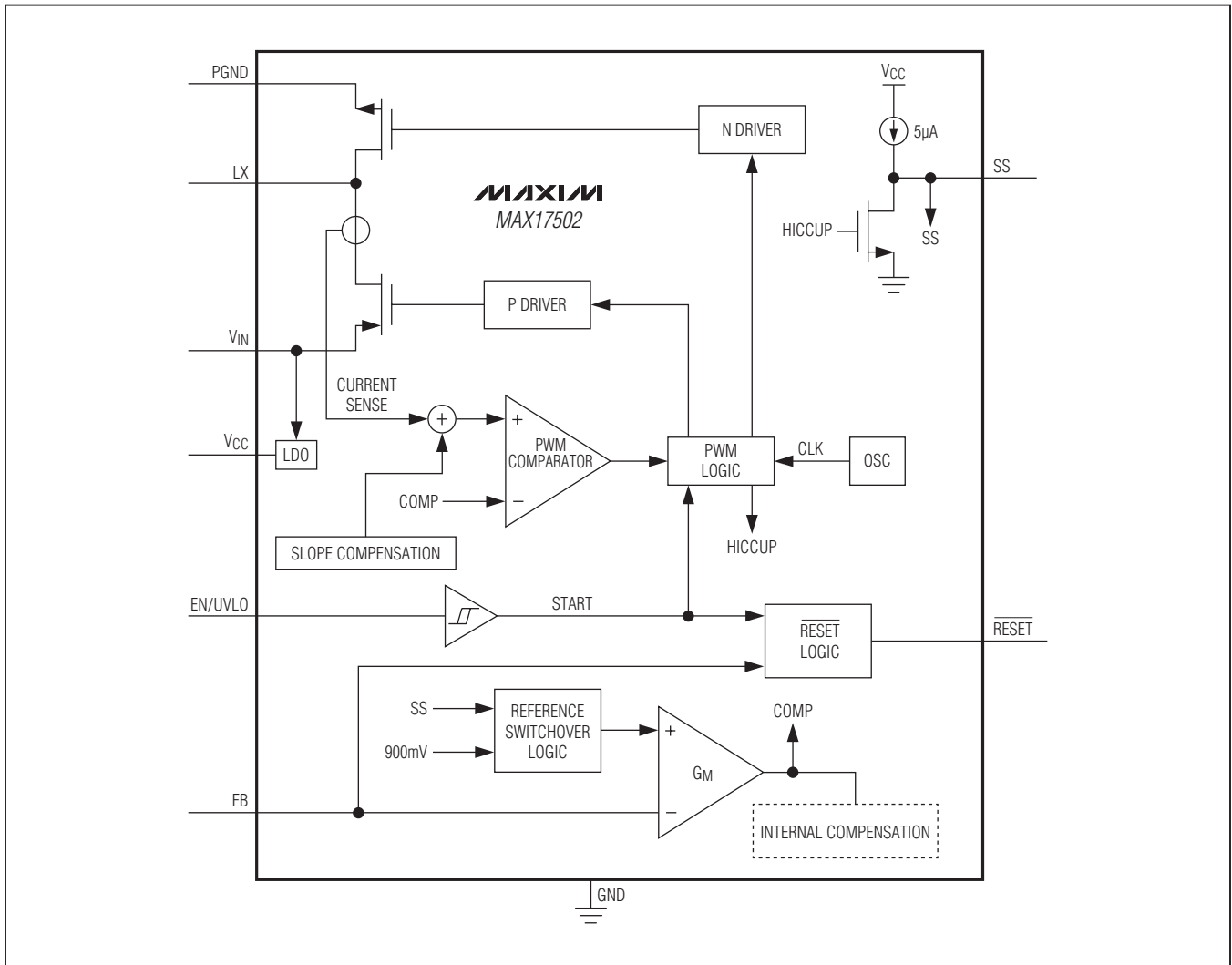
Pin Description

PIN	NAME	FUNCTION
1	PGND	Power Ground. Connect PGND externally to the power ground plane. Connect GND and PGND pins together at the ground return path of the V_{CC} bypass capacitor.
2	V_{IN}	Power-Supply Input. The input supply range is from 4.5V to 60V.
3	EN/UVLO	Enable/Undervoltage Lockout Input. Drive EN/UVLO high to enable the output voltage. Connect to the center of resistive divider between V_{IN} and GND to set the input voltage (undervoltage threshold) at which the device turns on. Pull up to V_{IN} for always on.
4	V_{CC}	5V LDO Output. Bypass V_{CC} with 1 μ F ceramic capacitance to GND.
5	FB	Feedback Input. Directly connect FB to the output.
6	SS	Soft-Start Input. Connect a capacitor from SS to GND to set the soft-start time.
7	N.C	No Connection. Leave unconnected.
8	$\overline{\text{RESET}}$	Open-Drain $\overline{\text{RESET}}$ Output. The $\overline{\text{RESET}}$ output is driven low if FB drops below 92.5% of its set value. $\overline{\text{RESET}}$ goes high 1024 clock cycles after FB rises above 95.5% of its set value.
9	GND	Analog Ground
10	LX	Switching Node. Connect LX to the switching side of the inductor. LX is high impedance when the device is in shutdown mode.
—	EP	Exposed Pad. Connect to GND pin of the IC. Connect to a large copper plane below the IC to improve heat dissipation capability.

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Block Diagram



60V, 1A, Ultra-Small, High-Efficiency, Synchronous Step-Down DC-DC Converter

Detailed Description

The MAX17502 step-down regulator operates from 4.5V to 60V and delivers up to 1A load current. Output voltage regulation accuracy meets $\pm 1.6\%$ over temperature.

The device uses a peak-current-mode-control scheme. It employs synchronous rectification. An internal transconductance error amplifier produces an integrated error voltage. The error voltage sets the duty cycle using a PWM comparator, a high-side current-sense amplifier, and a slope-compensation generator. At each rising edge of the clock, the high-side p-channel MOSFET turns on and remains on until either the appropriate or maximum duty cycle is reached, or the peak-current limit is detected.

During the high-side MOSFET's on-time, the inductor current ramps up. During the second half of the switching cycle, the high-side MOSFET turns off and the low-side n-channel MOSFET turns on. The inductor releases the stored energy as its current ramps down, and provides current to the output (the internal low $R_{DS(on)}$ pMOS/nMOS switches ensure high efficiency at full load).

This device also integrates enable/undervoltage lockout (EN/UVLO), adjustable soft-start time (SS), and open-drain reset output (RESET) functionality.

Linear Regulator (V_{CC})

An internal linear regulator (V_{CC}) provides a 5V nominal supply to power the internal blocks and the low-side MOSFET driver. The output of the V_{CC} linear regulator should be bypassed with a 1 μ F ceramic capacitor to GND. The device employs an undervoltage-lockout circuit that disables the internal linear regulator when V_{CC} falls below 3.7V (typ). The 300mV UVLO hysteresis prevents chattering on power-up/power-down. The internal V_{CC} linear regulator can source up to 40mA (typ) to supply the device and to power the low-side gate driver.

Switching Frequency

The device has a fixed 600kHz switching frequency. The minimum duty ratio at which the device can operate is 7.7%.

Overcurrent Protection/Hiccup Mode

The device is provided with a robust overcurrent-protection scheme that protects the device under overload and output short-circuit conditions. A cycle-by-cycle peak-current limit turns off the high-side MOSFET

whenever the high-side switch current exceeds an internal limit of 1.6A (typ). A runaway-current limit on the high-side switch current at 1.8A (typ) protects the device under high input voltage, short-circuit conditions when there is insufficient output voltage available to restore the inductor current that built up during the on period of the step-down converter. One occurrence of the runaway-current limit triggers a hiccup mode. In addition, if due to a fault condition, output voltage drops to 71.1% (typ) of its nominal value any time after soft-start is complete, and hiccup mode is triggered. In hiccup mode, the converter is protected by suspending switching for a hiccup timeout period of 32,768 clock cycles. Once the hiccup timeout period expires, soft-start is attempted again.

RESET Output

The device includes a $\overline{\text{RESET}}$ comparator to monitor the output voltage. The open-drain $\overline{\text{RESET}}$ output requires an external pullup resistor. $\overline{\text{RESET}}$ can sink 2mA of current while low. $\overline{\text{RESET}}$ goes high (high impedance) 1024 switching cycles after the regulator output increases above 95.5% of the designed nominal regulated voltage. $\overline{\text{RESET}}$ goes low when the regulator output voltage drops to below 92.5% of the nominal regulated voltage. $\overline{\text{RESET}}$ goes low during thermal shutdown.

Prebiased Output

When the device starts into a prebiased output, both the high-side and low-side switches are turned off so that the converter does not sink current from the output. High-side and low-side switches do not start switching until the PWM comparator commands the first PWM pulse, at which point switching commences first with the high-side switch. The output voltage is then smoothly ramped up to the target value in alignment with the internal reference.

Thermal-Overload Protection

Thermal-overload protection limits total power dissipation in the device. When the junction temperature of the device exceeds +165°C, an on-chip thermal sensor shuts down the device, allowing the device to cool. The thermal sensor turns the device on again after the junction temperature cools by 10°C. Soft-start resets during thermal shutdown. Carefully evaluate the total power dissipation (see the *Power Dissipation* section) to avoid unwanted triggering of the thermal-overload protection in normal operation.

60V, 1A, Ultra-Small, High-Efficiency, Synchronous Step-Down DC-DC Converter

Applications Information

Input Capacitor Selection

The discontinuous input-current waveform of the buck converter causes large ripple currents in the input capacitor. The switching frequency, peak inductor current, and the allowable peak-to-peak voltage ripple that reflects back to the source dictate the capacitance requirement. The device's high switching frequency allows the use of smaller value input capacitors. X7R capacitors are recommended in industrial applications for their temperature stability. A minimum value of 2.2μF should be used for the input capacitor. Higher values help reduce the ripple on the input DC bus further. In applications where the source is located distant from the device input, an electrolytic capacitor should be added in parallel to the 2.2μF ceramic capacitor to provide necessary damping for potential oscillations caused by the longer input power path and input ceramic capacitor.

Inductor Selection

Three key inductor parameters must be specified for operation with the device: inductance value (L), inductor saturation current (I_{SAT}), and DC resistance (R_{DCR}). To determine the inductance value, select the ratio of inductor peak-to-peak ripple current to the DC average current (LIR). For LIR values that are too high, the RMS currents are high, and therefore the inductor I²R losses are high. For LIR values that are too low, the inductance values are high and consequently the inductor DC resistance is also high, and therefore inductor I²R losses are high as well. A good compromise between size and loss is a 30% peak-to-peak ripple current to average-current ratio (LIR = 0.3). The switching frequency, input voltage, output voltage, and selected LIR determine the inductor value as follows:

$$L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_{SW} \times I_{OUT} \times LIR}$$

where V_{IN}, V_{OUT}, and I_{OUT} are nominal values. The switching frequency is 600kHz for the device. Select a low-loss inductor closest to the calculated value with acceptable dimensions and having the lowest possible DC resistance.

The saturation current rating (I_{SAT}) of the inductor must be high enough to ensure that saturation can occur only above the peak current-limit value (I_{PEAK-LIMIT} (typ) = 1.6A for the device). A variety of inductors from different suppliers are available to meet this requirement (e.g., inductors from the Coilcraft LPS6235 series).

See Table 1 to select inductors for 5V and 3.3V fixed output-voltage applications based on the MAX17502E/MAX17502F.

Output Capacitor Selection

X7R ceramic output capacitors are preferred due to their stability over temperature in industrial applications. The output capacitor is usually sized to support a step load of 50% of the maximum output current in the application, such that the output-voltage deviation is contained to 3% of the output-voltage change. The output capacitance can be calculated as follows:

$$C_{OUT} = \frac{1}{2} \times \frac{I_{STEP} \times t_{RESPONSE}}{\Delta V_{OUT}}$$

$$t_{RESPONSE} \cong \left(\frac{0.33}{f_C} + \frac{1}{f_{SW}} \right)$$

where I_{STEP} is the load current step, t_{RESPONSE} is the response time of the controller, ΔV_{OUT} is the allowable output-voltage deviation, and f_C is the target closed-loop crossover frequency. f_C is generally chosen to be 1/8 to 1/10 of f_{SW}.

Use Table 2 to select output capacitors for fixed 5V and 3.3V output-voltage applications based on the MAX17502E/MAX17502F.

Table 1. Inductor Selection

V _{OUT} (V)	I _{OUT} (max) (mA)	L (μH)	MINIMUM I _{SAT} (A)	SUGGESTED PART
5	1	22	1.6	Coilcraft LPS6235-223ML_
3.3	1	15	1.6	Coilcraft LPS6235-153ML_

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Table 2. Output Capacitor Selection

V _{OUT} (V)	I _{OUT} (max) (A)	TYPE	VOLTAGE RATING (V)	SUGGESTED PART
5	1	10μF/1210/X7R	10	Murata GRM32DR71A106KA01L
3.3	1	22μF/1210/X7R	10	Murata GRM32ER71A226KE20L

Soft-Start Capacitor Selection

The device implements adjustable soft-start operation for the synchronous step-down converter. A capacitor connected from the SS pin to GND programs the soft-start period.

The soft-start time (t_{SS}) is related to the capacitor connected at SS (C_{SS}) by the following equation:

$$C_{SS} = 5.55 \times t_{SS}$$

where t_{SS} is in milliseconds and C_{SS} is in nanofarads. For example, to have a 1.8ms soft-start time, a 10nF capacitor should be connected from the SS pin to GND.

Setting the Input Undervoltage-Lockout Level

The device offers an adjustable input undervoltage-lockout level. Set the voltage at which the device turns on, with a resistive voltage-divider connected from V_{IN} to GND (see Figure 1). Connect the center node of the divider to EN/UVLO.

Choose R1 to be 3.3MΩ and then calculate R2 as follows:

$$R2 = \frac{R1 \times 1.218}{(V_{INU} - 1.218)}$$

where V_{INU} is the voltage at which the device is required to turn on.

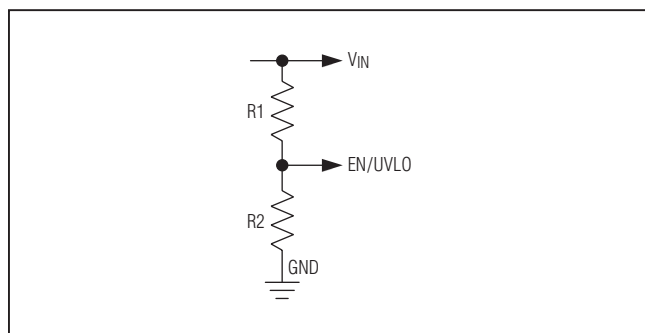


Figure 1. Adjustable UVLO Network

Power Dissipation

It should be ensured that the junction temperature of the device does not exceed 125°C under the operating conditions specified for the power supply.

At a particular operating condition, the power losses that lead to temperature rise of the part are estimated as follows:

$$P_{LOSS} = \left(P_{OUT} \times \left(\frac{1}{\eta} - 1 \right) \right) + (I_{OUT}^2 \times R_{DCR})$$

$$P_{OUT} = V_{OUT} \times I_{OUT}$$

where P_{OUT} is the output power, η is the efficiency of the device, and R_{DCR} is the DC resistance of the output inductor (see the *Typical Operating Characteristics* for more information on efficiency at typical operating conditions).

The maximum power that can be dissipated in the device's 10-pin TDFN-EP package is 1188.7mW at +70°C temperature. The power dissipation capability should be derated as the temperature goes above +70°C at 14.9mW/°C. For a multilayer board, the thermal performance metrics for the package are given below:

$$\theta_{JA} = 67.3^\circ\text{C/W}$$

$$\theta_{JC} = 18.2^\circ\text{C/W}$$

The junction temperature of the device can be estimated at any given maximum ambient temperature (T_{A_MAX}) from the following equation:

$$T_{J_MAX} = T_{A_MAX} + (\theta_{JA} \times P_{LOSS})$$

If the application has a thermal-management system that ensures that the exposed pad of the device is maintained at a given temperature (T_{EP_MAX}) by using proper heat sinks, then the junction temperature of the device can be estimated at any given maximum ambient temperature from the following equation:

$$T_{J_MAX} = T_{EP_MAX} + (\theta_{JC} \times P_{LOSS})$$

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PCB Layout Guidelines

All connections carrying pulsed currents must be very short and as wide as possible. The inductance of these connections must be kept to an absolute minimum due to the high di/dt of the currents. Since inductance of a current-carrying loop is proportional to the area enclosed by the loop, if the loop area is made very small, inductance is reduced. Additionally, small-current loop areas reduce radiated EMI.

A ceramic input filter capacitor should be placed close to the V_{IN} pin of the device. This eliminates as much trace inductance effects as possible and gives the device a cleaner voltage supply. The bypass capacitor for the V_{CC} pin should also be placed close to the pin to reduce effects of trace impedance. The feedback trace should be routed as far as possible from the inductor.

When routing the circuitry around the device, the analog small-signal ground and the power ground for switching currents must be kept separate. They should be connected together at a point where switching activity

is at minimum, typically the return terminal of the V_{CC} bypass capacitor. This helps to keep the analog ground quiet. The ground plane should be kept continuous/unbroken as much as possible. No trace carrying high switching current should be placed directly over any ground plane discontinuity.

PCB layout also affects the thermal performance of the design. A number of thermal vias that connect to a large ground plane should be provided under the exposed pad of the device, for efficient heat dissipation. Several vias in parallel have lower impedance than a single via.

For a sample layout that ensures first-pass success, refer to the MAX17502 evaluation kit layout available at www.maxim-ic.com.

MAX17502

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Typical Applications Circuits

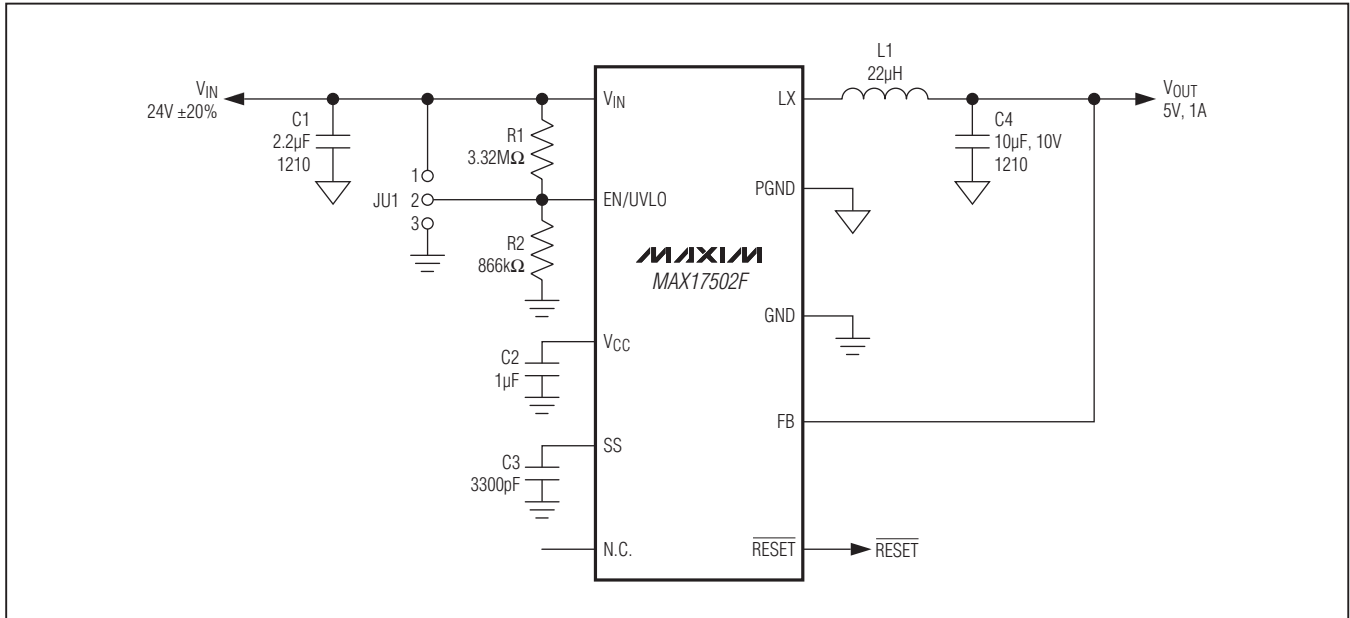


Figure 2. MAX17502F Application Circuit (5V Output, 1A Maximum Load Current, 600kHz Switching Frequency)

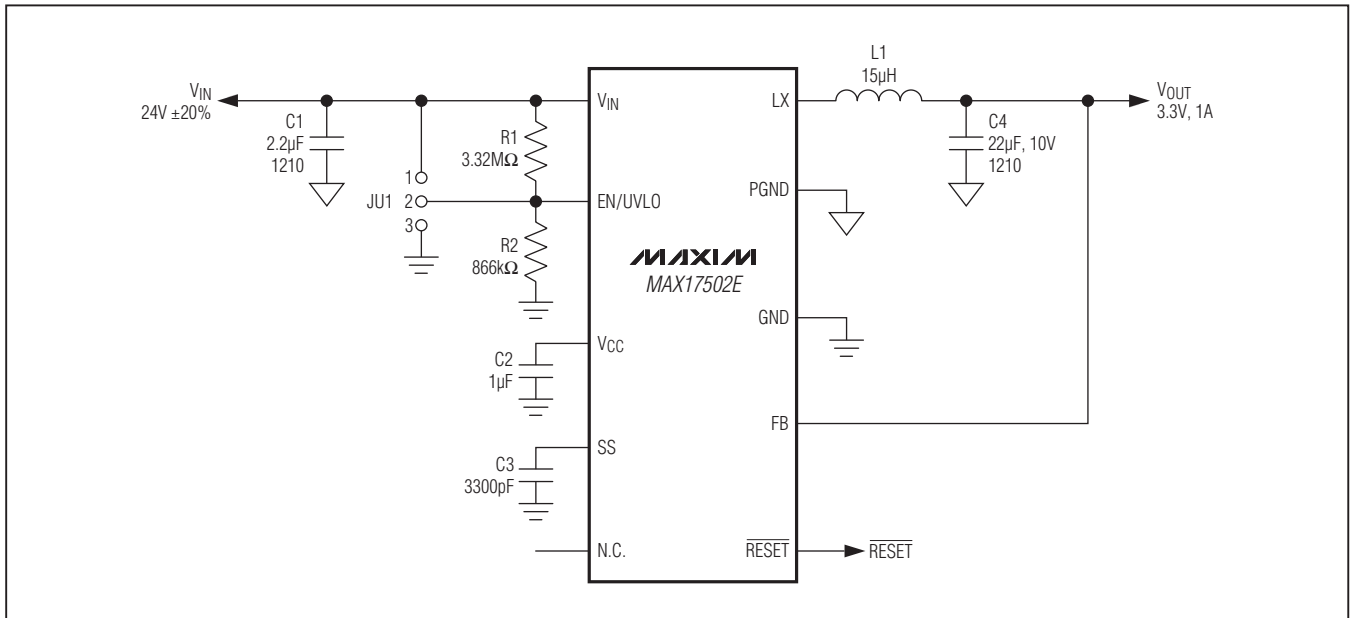


Figure 3. MAX17502E Application Circuit (3.3V Output, 1A Maximum Load Current, 600kHz Switching Frequency)

MAX17502

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Ordering Information/Selector Guide

PART	PIN-PACKAGE	OUTPUT VOLTAGE	SWITCHING FREQUENCY	PEAK-CURRENT- MODE CONTROL SCHEME	OUTPUT CURRENT
MAX17502EATB+	10 TDFN-EP*	3.3V	600kHz	Forced PWM	1A
MAX17502FATB+	10 TDFN-EP*	5V	600kHz	Forced PWM	1A

Note: All devices are specified over the -40°C to +125°C operating temperature range. Optional variants available to support adjustable output and PFM. Contact your Maxim sales representative for more information.

+Denotes a lead(Pb)-free/RoHS-compliant package.

*EP = Exposed pad.

Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns (footprints), go to www.maxim-ic.com/packages. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
10 TDFN-EP	T1032N+1	21-0429	90-0082

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Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	5/12	Initial release	—

Maxim cannot assume responsibility for use of any circuitry other than circuitry entirely embodied in a Maxim product. No circuit patent licenses are implied. Maxim reserves the right to change the circuitry and specifications without notice at any time. The parametric values (min and max limits) shown in the Electrical Characteristics table are guaranteed. Other parametric values quoted in this data sheet are provided for guidance.

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