ISL6257

Highly Integrated Narrow VDC Battery Charger for Notebook Computers

FN9288
Rev 2.00
Jan 17, 2007

The ISL6257 is a highly integrated battery charger controller for Li-Ion/Li-Ion polymer batteries. ISL6257 is designed for Narrow VDC applications where the system power source is either the battery pack or the regulated output of the charger. This makes the max voltage to the system equal to the max battery voltage instead of the max adapter voltage. Operating at lower system voltage can improve overall efficiency. High efficiency is achieved in the charger with a synchronous buck topology. The low-side MOSFET emulates a diode at light loads to improve the light load efficiency and prevent system bus boosting.

The constant output voltage can be selected for 2, 3 and 4 series Li-Ion cells with ±0.5% accuracy over temperature. It can also be programmed between 4.2V + 5% per cell and 4.2V - 5% per cell to optimize battery capacity. When supplying the load and battery charger simultaneously, the input current limit for the AC adapter is programmable to within ±3% accuracy to avoid overloading the AC adapter and to allow the system to make efficient use of available adapter power for charging. It also has a wide range of programmable charging current. The ISL6257 automatically transitions from regulating current mode to regulating voltage mode.

Ordering Information

PART NUMBER (Notes 1, 2)	PART MARKING	TEMP RANGE (°C)	PACKAGE (Pb-free)	PKG. DWG. #
ISL6257HRZ	ISL6257HRZ	-10 to +100	28 Ld 5x5 QFN	L28.5×5
ISL6257HRZ-T	ISL6257HRZ	-10 to +100	28 Ld 5x5 QFN Tape & Reel	L28.5×5

NOTE: Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Features

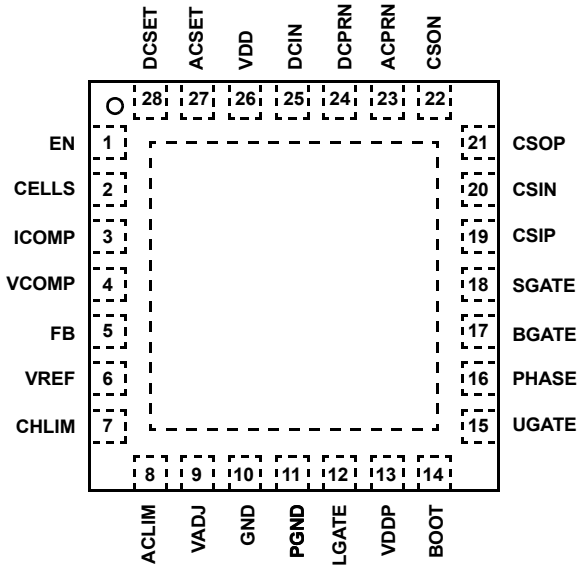
- ±0.5% Charge Voltage Accuracy (-10°C to +100°C)
- ±3% Accurate Input Current Limit
- ±3% Accurate Battery Charge Current Limit
- ±25% Accurate Battery Trickle Charge Current Limit
- Programmable Charge Current Limit, Adapter Current Limit and Charge Voltage
- Fixed 300kHz PWM Synchronous Buck Controller with Diode Emulation at Light Load
- AC Adapter Present Indicator
- Fast Input Current Limit Response
- Input Voltage Range 7V to 25V
- Support 2, 3 and 4 Cells Battery Pack
- Up to 17.64V Battery-Voltage Set Point
- Control Adapter Power Source Select MOSFET
- Thermal Shutdown
- Aircraft Power Capable
- DC Adapter Present Indicator
- Battery Discharge MOSFET Control
- Less than 10µA Battery Leakage Current
- Support Pulse Charging
- Charge any Battery Chemistry: Li-Ion, NiCd, NiMH, etc.
- Pb-Free Plus Anneal Available (RoHS Compliant)

Applications

- Notebook, Desknote and Sub-notebook Computers
- Personal Digital Assistant

Pinout

ISL6257 (28 LD QFN)
TOP VIEW



Absolute Maximum Ratings

DCIN, CSIP, CSON to GND . . . . . -0.3V to +28V
CSIP-CSIN, CSOP-CSON . . . . . -0.3V to +0.3V
CSIP-SGATE, CSIP-BGATE . . . . . -0.3V to 16V
PHASE to GND . . . . . -7V to 30V
BOOT to GND . . . . . -0.3V to +35V
BOOT to VDDP . . . . . -2V to 28V
ACLIM, ACPRN, CHLIM, DCPRN, VDD to GND . . . . . -0.3V to 7V
BOOT-PHASE, VDDP-PGND . . . . . -0.3V to 7V
ACSET and DCSET to GND (Note 1) . . . . . -0.3V to VDD + 0.3V
FB, ICOMP, VCOMP to GND . . . . . -0.3V to VDD + 0.3V
VREF, CELLS to GND . . . . . -0.3V to VDD + 0.3V
EN, VADJ, PGND to GND . . . . . -0.3V to VDD + 0.3V
UGATE . . . . . PHASE-0.3V to BOOT + 0.3V
LGATE . . . . . PGND-0.3V to VDDP + 0.3V
PGND to GND . . . . . -0.3V to +0.3V

Thermal Information

Thermal Resistance	θ_{JA} (°C/W)	θ_{JC} (°C/W)
QFN Package (Notes 2, 3)	39	9.5
QSOP Package (Note 2)	80	NA

Junction Temperature Range . . . . . -10°C to +150°C
Operating Temperature Range . . . . . -10°C to +100°C
Storage Temperature . . . . . -65°C to +150°C
Lead Temperature (soldering, 10s) . . . . . +300°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. ACSET and DCSET may be operated 1V below GND if the current through ACSET and DCSET is limited to less than 1mA.
2. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with "direct attach" features. See Tech Brief TB379.
3. For θ_{JC}, the "case temp" location is the center of the exposed metal pad on the package underside.

Electrical Specifications

DCIN = CSIP = CSIN = 18V, CSOP = CSON = 12V, ACSET = DCSET = 1.5V, ACLIM = VREF, VADJ = Floating, EN = VDD = 5V, BOOT - PHASE = 5.0V, GND = PGND = 0V, C_{VDD} = 1µF, I_{VDD} = 0mA, T_A = -10°C to +100°C, $T_J \leq +125$°C, unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
SUPPLY AND BIAS REGULATOR					
DCIN Input Voltage Range		7		25	V
DCIN Quiescent Current	EN = VDD or GND, 7V ≤ DCIN ≤ 25V		1.4	3	mA
Battery Leakage Current (Note 4)	DCIN = 0, no load		3	10	µA
VDD Output Voltage/Regulation	7V ≤ DCIN ≤ 25V, 0 ≤ I_{VDD} ≤ 30mA	4.925	5.075	5.225	V
VDD Undervoltage Lockout Trip Point	VDD Rising	4.0	4.4	4.6	V
	Hysteresis	150	250	400	mV
Reference Output Voltage VREF	0 ≤ I_{VREF} ≤ 300µA	2.365	2.39	2.415	V
FB Feedback Voltage		2.065	2.1	2.12	V
Battery Charge Voltage Accuracy	CSON = 16.8V, CELLS = VDD, VADJ = Float	-0.5		0.5	%
	CSON = 12.6V, CELLS = GND, VADJ = Float	-0.5		0.5	%
	CSON = 8.4V, CELLS = Float, VADJ = Float	-0.5		0.5	%
	CSON = 17.64V, CELLS = VDD, VADJ = VREF	-0.5		0.5	%
	CSON = 13.23V, CELLS = GND, VADJ = VREF	-0.5		0.5	%
	CSON = 8.82V, CELLS = Float, VADJ = VREF	-0.5		0.5	%
	CSON = 15.96V, CELLS = VDD, VADJ = GND	-0.5		0.5	%
	CSON = 11.97V, CELLS = GND, VADJ = GND	-0.5		0.5	%
	CSON = 7.98V, CELLS = Float, VADJ = GND	-0.5		0.5	%
TRIP POINTS					
ACSET Threshold		1.24	1.26	1.28	V
ACSET Input Bias Current Hysteresis		2.2	3.4	4.4	µA
ACSET Input Bias Current	ACSET ≥ 1.26V	2.2	3.4	4.4	µA

Electrical Specifications DCIN = CSIP = CSIN = 18V, CSOP = CSON = 12V, ACSET = DCSET = 1.5V, ACLIM = VREF, VADJ = Floating, EN = VDD = 5V, BOOT - PHASE = 5.0V, GND = PGND = 0V, C_{VDD} = 1µF, I_{VDD} = 0mA, T_A = -10°C to +100°C, $T_J \leq +125°C$, unless otherwise noted. **(Continued)**

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
ACSET Input Bias Current	ACSET < 1.26V	-1	0	1	µA
DCSET Threshold		1.24	1.26	1.28	V
DCSET Input Bias Current Hysteresis		2.2	3.4	4.4	µA
DCSET Input Bias Current	DCSET ≥ 1.26V	2.2	3.4	4.4	µA
DCSET Input Bias Current	DCSET < 1.26V	-1	0	1	µA
OSCILLATOR					
Frequency		245	300	355	kHz
PWM Ramp Voltage (peak-peak)	CSIP = 18V		1.6		V
	CSIP = 11V		1		V
SYNCHRONOUS BUCK REGULATOR					
Maximum Duty Cycle		97	99	99.6	%
UGATE Pull-Up Resistance	BOOT - PHASE = 5V, 500mA source current		1.8	3.0	Ω
UGATE Source Current	BOOT - PHASE = 5V, BOOT-UGATE = 2.5V		1.0		A
UGATE Pull-Down Resistance	BOOT - PHASE = 5V, 500mA sink current		1.0	1.8	Ω
UGATE Sink Current	BOOT - PHASE = 5V, UGATE - PHASE = 2.5V		1.8		A
LGATE Pull-Up Resistance	VDDP - PGND = 5V, 500mA source current		1.8	3.0	Ω
LGATE Source Current	VDDP - PGND = 5V, VDDP - LGATE = 2.5V		1.0		A
LGATE Pull-Down Resistance	VDDP - PGND = 5V, 500mA sink current		1.0	1.8	Ω
LGATE Sink Current	VDDP - PGND = 5V, LGATE = 2.5V		1.8		A
Dead Time	Falling UGATE to rising LGATE or falling LGATE to rising UGATE	10		30	ns
CHARGING CURRENT SENSING AMPLIFIER					
Input Common-Mode Range		0		18	V
Input Offset Voltage	Guaranteed by design	-1.5	0	1.5	mV
Input Bias Current at CSOP	5 < CSOP < 18V		0.25	2	µA
Input Bias Current at CSON	5 < CSON < 18V		50	100	µA
CHLIM Input Voltage Range		0		3.6	V
CSOP to CSON Full-Scale Current Sense Voltage	CHLIM = 3.3V (4V<CSON<16.8V)	160	165	170	mV
	CHLIM = 2.0V (4V<CSON<16.8V)	97	100	103	mV
	CHLIM = 0.6V (4V<CSON<16.8V)	28.5	30.0	31.5	mV
	CHLIM = 0.2V (4V<CSON<16.8V)	7.5	10	12.5	mV
CHLIM Input Bias Current	CHLIM = GND or 3.3V, DCIN = 0V	-1		1	µA
CHLIM Power-Down Mode Threshold Voltage	CHLIM rising	80	88	95	mV
CHLIM Power-Down Mode Hysteresis Voltage		15	25	40	mV
ADAPTER CURRENT SENSING AMPLIFIER					
Input Common-Mode Range		7		25	V
Input Offset Voltage	Guaranteed by design	-1.5		1.5	mV
Input Bias Current at CSIP and CSIN Combined	CSIP = CSIN = 25V		100	130	µA

Electrical Specifications DCIN = CSIP = CSIN = 18V, CSOP = CSON = 12V, ACSET = DCSET = 1.5V, ACLIM = VREF, VADJ = Floating, EN = VDD = 5V, BOOT - PHASE = 5.0V, GND = PGND = 0V, C_{VDD} = 1µF, I_{VDD} = 0mA, T_A = -10°C to +100°C, $T_J \leq +125$°C, unless otherwise noted. **(Continued)**

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Bias Current at CSIN	0 < CSIN < DCIN, Guaranteed by design		0.10	1	µA
ADAPTER CURRENT LIMIT THRESHOLD					
CSIP to CSIN Full-Scale Current Sense Voltage	ACLIM = VREF	97	100	103	mV
	ACLIM = Float	72	75	78	mV
	ACLIM = GND	47	50	53	mV
ACLIM Input Bias Current	ACLIM = VREF	10	16	20	µA
	ACLIM = GND	-20	-16	-10	µA
VOLTAGE REGULATION ERROR AMPLIFIER					
Error Amplifier Transconductance from VFB to VCOMP			240		µA/V
CURRENT REGULATION ERROR AMPLIFIER					
Charging Current Error Amplifier Transconductance	from V_{CA2} to ICOMP		50		µA/V
Adapter Current Error Amplifier Transconductance	from V_{CA1} to ICOMP		50		µA/V
BATTERY CELL SELECTOR					
CELLS Input Voltage for 4 Cell Select		4.3			V
CELLS Input Voltage for 3 Cell Select				2	V
CELLS Input Voltage for 2 Cell Select		2.1		4.2	V
MOSFET DRIVER					
BGATE Pull-Up Current	CSIP - BGATE = 3V	10	30	45	mA
BGATE Pull-Down Current	CSIP - BGATE = 5V	2.7	4.0	5.0	mA
CSIP - BGATE Voltage High		8	9.6	11	V
CSIP - BGATE Voltage Low		-50	0	50	mV
DCIN - CSON Threshold for CSIP-BGATE Going High	DCIN = 12V, CSON Rising	-100	0	100	mV
DCIN - CSON Threshold Hysteresis		250	300	400	mV
SGATE Pull-Up Current	CSIP - SGATE = 3V	7	12	15	mA
SGATE Pull-Down Current	CSIP - SGATE = 5V	50	160	370	µA
CSIP - SGATE Voltage High		8	9	11	V
CSIP - SGATE Voltage Low		-50	0	50	mV
CSIP - CSIN Threshold for CSIP - SGATE Going High		2.5	8	13	mV
CSIP - CSIN Threshold Hysteresis		1.3	5	8	mV
LOGIC INTERFACE					
EN Input Voltage Range		0		VDD	V
EN Threshold Voltage	Rising	1.030	1.06	1.100	V
	Falling	0.985	1.000	1.025	V
	Hysteresis	30	60	90	mV
EN Input Bias Current	EN = 2.5V	1.8	2.0	2.2	µA
ACPRN Sink Current	ACPRN = 0.4V	3	8	11	mA
ACPRN Leakage Current	ACPRN = 5V	-0.5		0.5	µA

Electrical Specifications DCIN = CSIP = CSIN = 18V, CSOP = CSON = 12V, ACSET = DCSET = 1.5V, ACLIM = VREF, VADJ = Floating, EN = VDD = 5V, BOOT - PHASE = 5.0V, GND = PGND = 0V, C_{VDD} = 1µF, I_{VDD} = 0mA, T_A = -10°C to +100°C, $T_J \leq +125°C$, unless otherwise noted. **(Continued)**

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
DCPRN Sink Current	DCPRN = 0.4V	3	8	11	mA
DCPRN Leakage Current	DCPRN = 5V	-0.5		0.5	µA
CSON to GND resistance	CSON = 12.6V	315	380	485	kΩ
Thermal Shutdown Temperature			150		°C
Thermal Shutdown Temperature Hysteresis			25		°C

NOTE:

4. This is the sum of currents in these pins (CSIP, CSIN, BGATE, BOOT, UGATE, PHASE, CSOP, CSON) all tied to 16.8V. No current in pins EN, ACSET, DCSET, VADJ, CELLS, ACLIM, CHLIM.

Typical Operating Performance

DCIN = 20V, 4S2P Li-Battery, T_A = +25°C, unless otherwise noted.

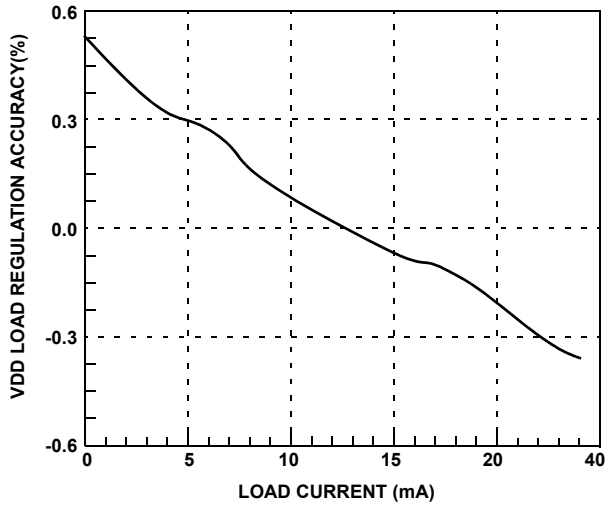


FIGURE 1. VDD LOAD REGULATION

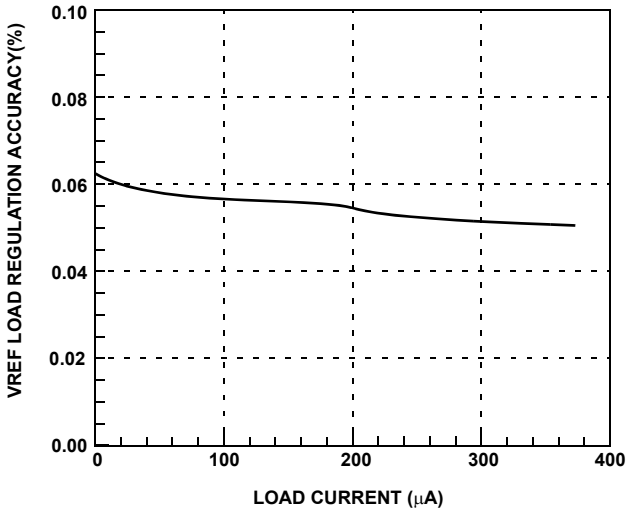


FIGURE 2. VREF LOAD REGULATION

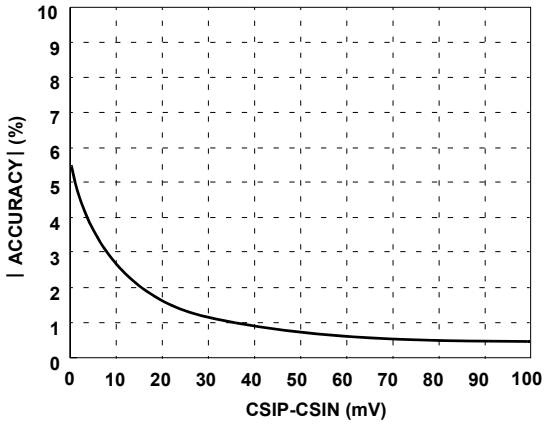


FIGURE 3. ACCURACY vs AC ADAPTER CURRENT

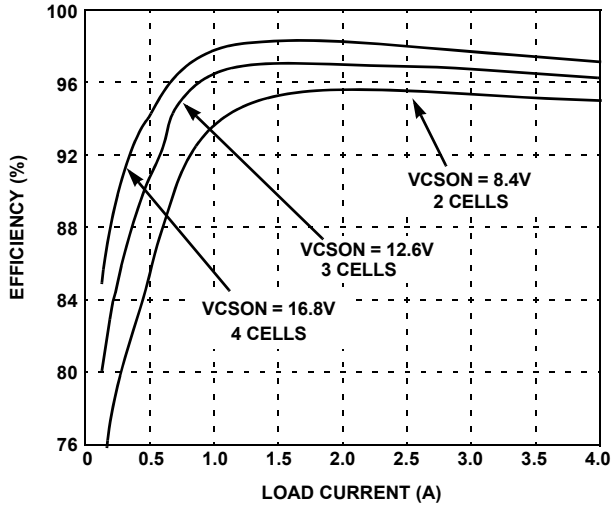


FIGURE 4. SYSTEM EFFICIENCY vs CHARGE CURRENT

Typical Operating Performance DCIN = 20V, 4S2P Li-Battery, T_A = +25°C, unless otherwise noted. **(Continued)**

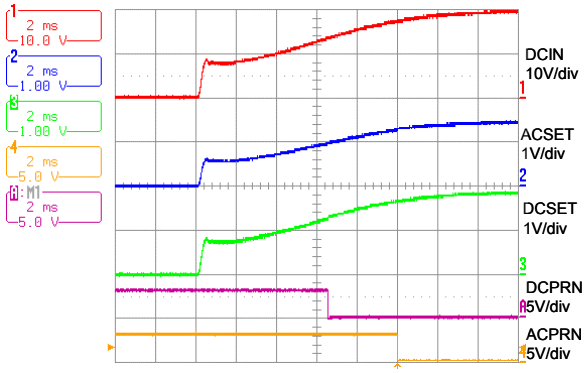


FIGURE 5. AC AND DC ADAPTER DETECTION

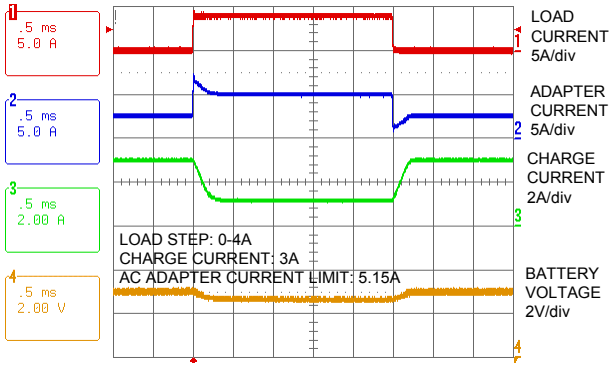


FIGURE 6. LOAD TRANSIENT RESPONSE

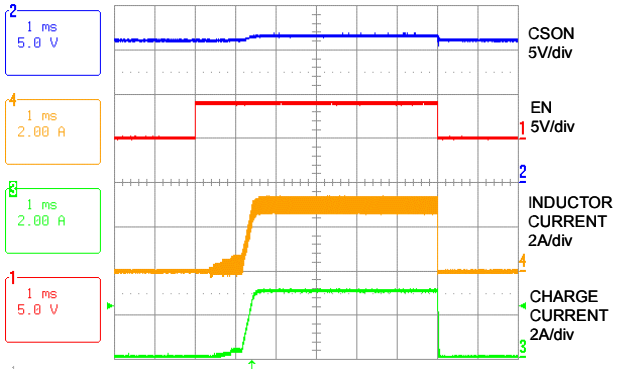


FIGURE 7. CHARGE ENABLE AND SHUTDOWN

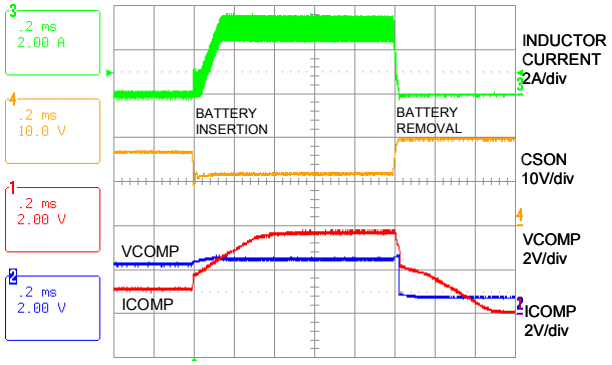


FIGURE 8. BATTERY INSERTION AND REMOVAL

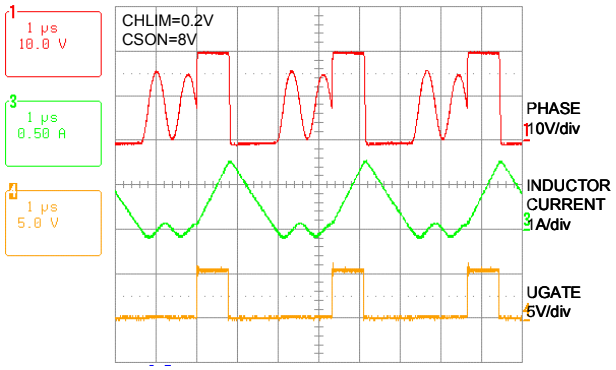


FIGURE 9. SWITCHING WAVE FORMS IN DISCONTINUOUS CONDUCTION MODE (DIODE EMULATION)

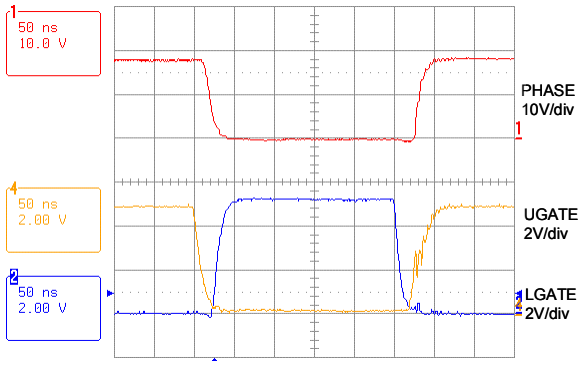


FIGURE 10. SWITCHING WAVE FORMS IN CONTINUOUS CONDUCTION MODE

Typical Operating Performance DCIN = 20V, 4S2P Li-Battery, T_A = +25°C, unless otherwise noted. **(Continued)**

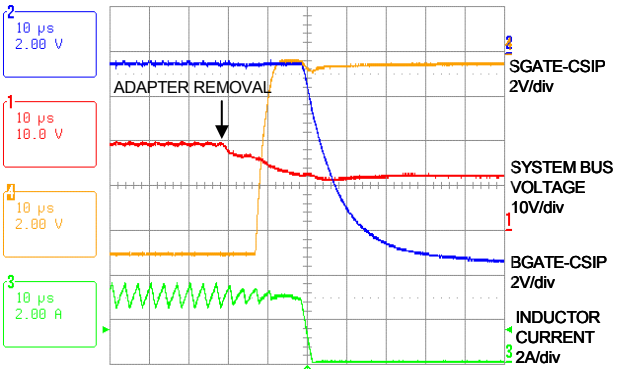


FIGURE 11. ADAPTER REMOVAL

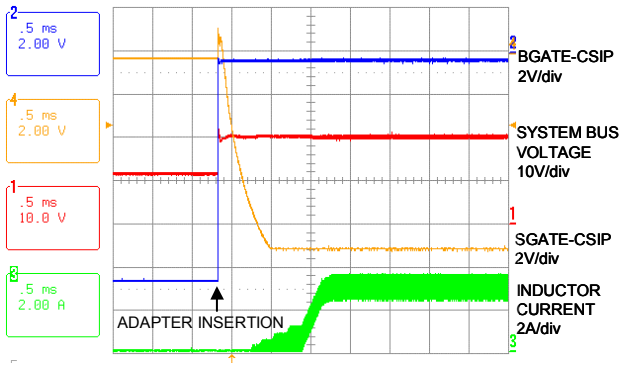


FIGURE 12. ADAPTER INSERTION

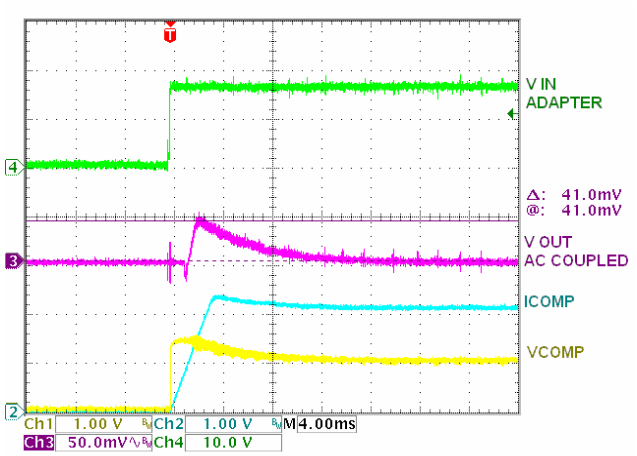


FIGURE 13. ADAPTER INSERTION WITH A CHARGED BATTERY

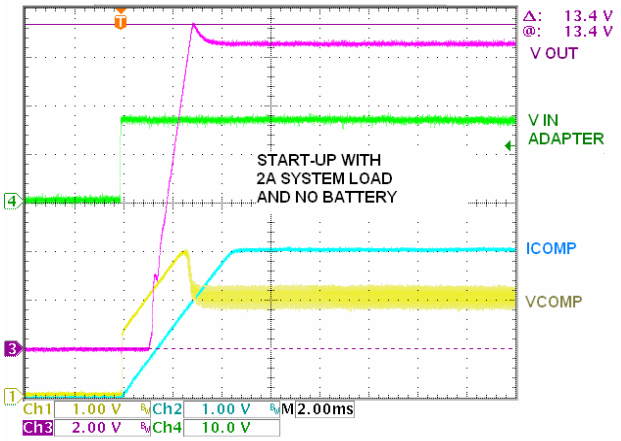


FIGURE 14. ADAPTER INSERTION WITH NO BATTERY AND A 2A SYSTEM LOAD

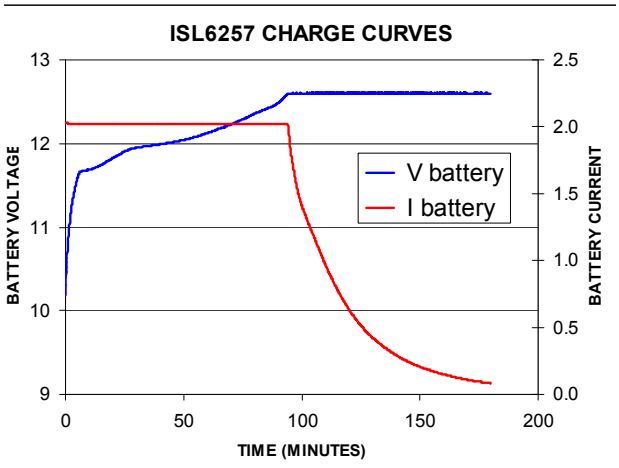


FIGURE 15. BATTERY CHARGE VOLTAGE AND CURRENT

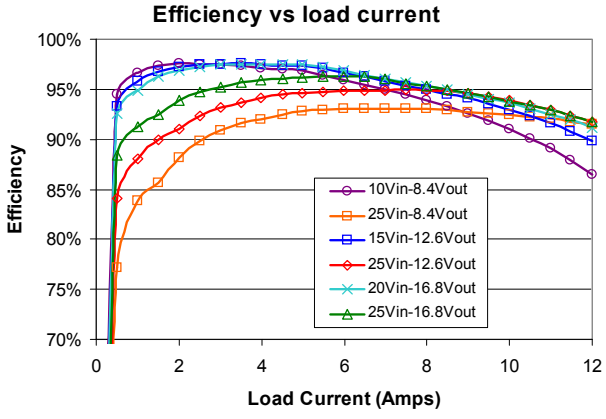


FIGURE 16. EFFICIENCY VS LOAD CURRENT

Typical Operating Performance

DCIN = 20V, 4S2P Li-Battery, T_A = +25°C, unless otherwise noted. **(Continued)**

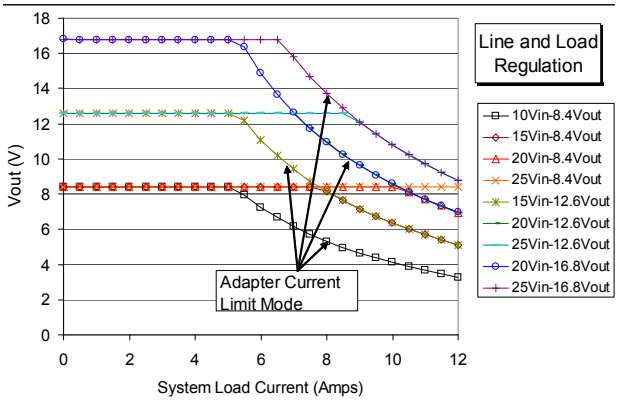


FIGURE 17. LINE AND LOAD REGULATION IN NVDC MODE

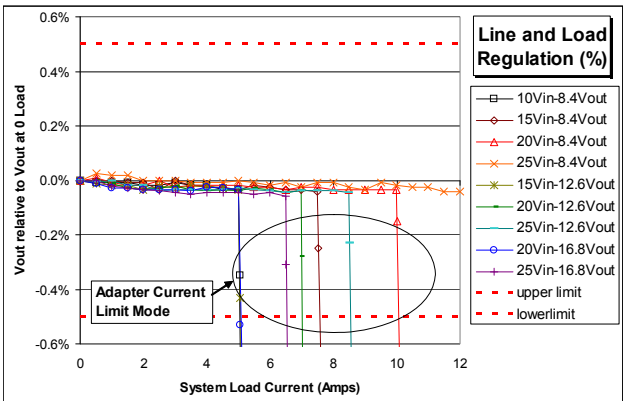


FIGURE 18. LINE AND LOAD REGULATION IN NVDC MODE AS A PERCENTAGE OF NO LOAD VOLTAGE

Functional Pin Descriptions

BOOT

Connect BOOT to a 0.1µF ceramic capacitor to PHASE pin and connect to the cathode of the bootstrap Schottky diode.

UGATE

UGATE is the high-side MOSFET gate drive output.

SGATE

SGATE is the AC adapter power source select output. The SGATE pin drives an external P-MOSFET used to switch to AC adapter as the system power source.

BGATE

Battery power source select output. This pin drives an external P-channel MOSFET used to switch the battery as the system power source in non Narrow VDC systems. When the voltage at CSON pin is higher than the AC adapter output voltage at DCIN, BGATE is driven to low and selects the battery as the power source. In Narrow VDC systems BGATE should be unconnected.

LGATE

LGATE is the low-side MOSFET gate drive output; swing between 0V and VDDP.

PHASE

The Phase connection pin connects to the high-side MOSFET source, output inductor, and low-side MOSFET drain.

CSOP/CSON

CSOP/CSON is the battery charging current sensing positive/negative input. The differential voltage across CSOP and CSON is used to sense the battery charging current, and is compared with the charging current limit threshold to regulate the charging current. The CSON pin is also used as the battery feedback voltage to perform voltage regulation.

CSIP/CSIN

CSIP/CSIN is the AC adapter current sensing positive/negative input. The differential voltage across CSIP and CSIN is used to sense the AC adapter current, and is compared with the AC adapter current limit to regulate the AC adapter current.

GND

GND is an analog ground.

DCIN

The DCIN pin is the input of the internal 5V LDO. Connect it to the AC adapter output. Connect a 0.1µF ceramic capacitor from DCIN to CSON.

ACSET

ACSET is an AC adapter detection input. Connect to a resistor divider from the AC adapter output.

ACPRN

Open-drain output signals AC adapter is present. ACPRN pulls low when ACSET is higher than 1.26V and pulled high when ACSET is lower than 1.26V.

DCSET

DCSET is a lower voltage adapter detection input (like aircraft power 15V). Allows the adapter to power the system where battery charging has been disabled.

DCPRN

Open-drain output signals DC adapter is present. DCPRN pulls low when DCSET is higher than 1.26V and pulled high when DCSET is lower than 1.26V.

EN

EN is the Charge Enable input. Connecting EN to high enables the charge control function; connecting EN to low disables charging functions. Use with a thermistor to detect a hot battery and suspend charging.

FB

The negative feedback of the voltage amplifier which sets the output voltage at CSON. An internal resistor divider from CSON adjusts the voltage feedback signal in the ratio of 6:1 for CELLS = GND, 8:1 for CELLS = VDD and 4:1 for CELLS = float.

PGND

PGND is the power ground. Connect PGND to the source of the low-side MOSFET.

VDD

VDD is an internal LDO output to supply IC analog circuit. Connect a 1µF ceramic capacitor to ground.

VDDP

VDDP is the supply voltage for the low-side MOSFET gate driver. Connect a 4.7Ω resistor to VDD and a 1µF ceramic capacitor to power ground.

ICOMP

ICOMP is a current loop error amplifier output.

VCOMP

VCOMP is a voltage loop amplifier output.

CELLS

This pin is used to select the battery voltage. CELLS = VDD for a 4S battery pack, CELLS = GND for a 3S battery pack, CELLS = Float for a 2S battery pack.

VADJ

VADJ adjusts battery regulation voltage. VADJ = VREF for 4.2V + 5% per cell; VADJ = Floating for 4.2V per cell; VADJ = GND for 4.2V - 5% per cell. Connect to a resistor divider to program the desired battery cell voltage between 4.2V - 5% and 4.2V + 5%.

CHLIM

CHLIM is the battery charge current limit set pin.CHLIM input voltage range is 0.1V to 3.6V. When CHLIM = 3.3V, the set point for CSOP - CSON is 165mV. The charger shuts down if CHLIM is forced below 88mV.

ACLIM

ACLIM is the adapter current limit set pin. ACLIM = VREF for 100mV, ACLIM = Floating for 75mV, and ACLIM = GND for 50mV. Connect a resistor divider to program the adapter current limit threshold between 50mV and 100mV.

VREF

VREF is a 2.39V reference output pin. It is internally compensated. Do not connect a decoupling capacitor.

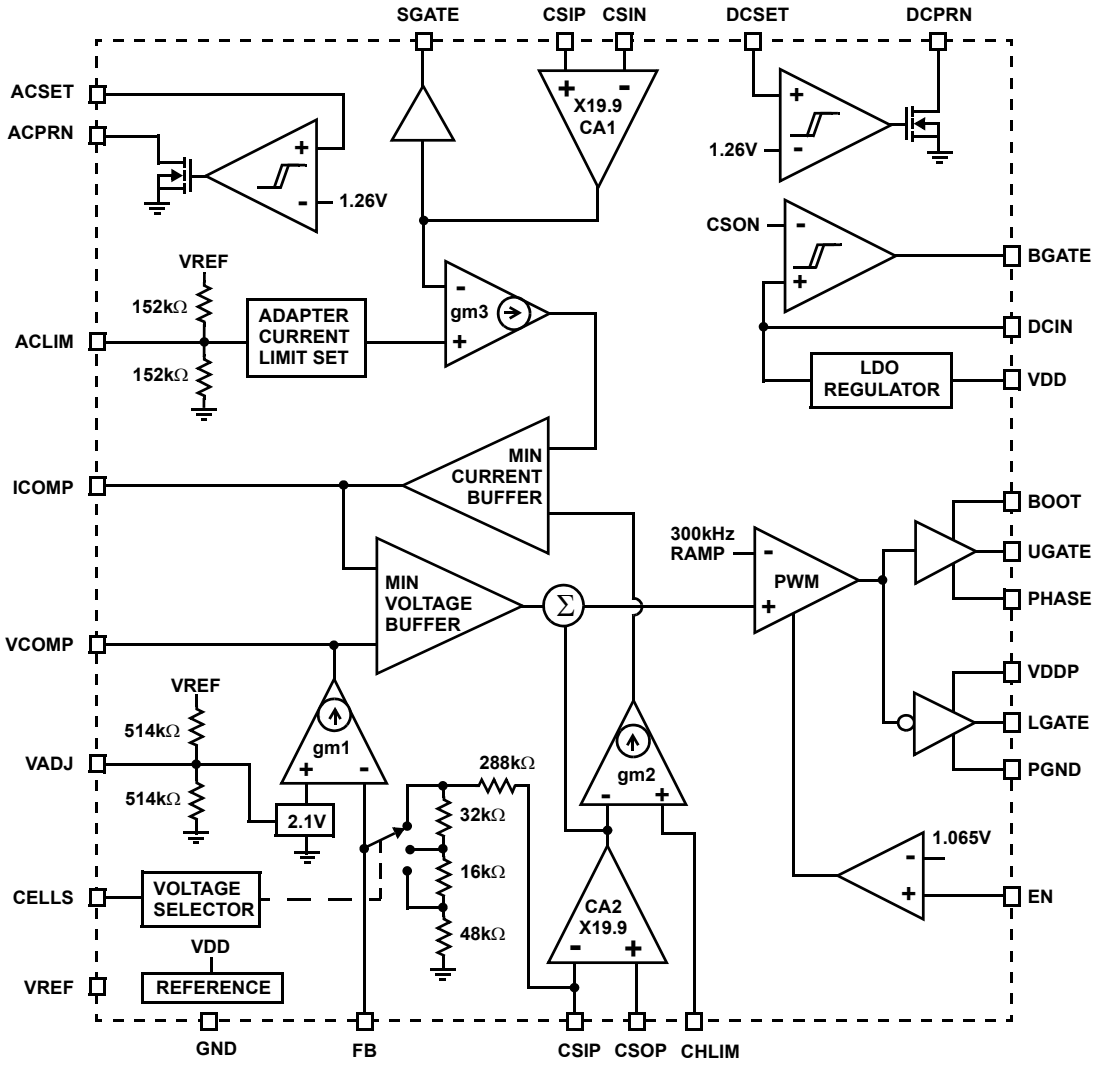


FIGURE 19. FUNCTIONAL BLOCK DIAGRAM

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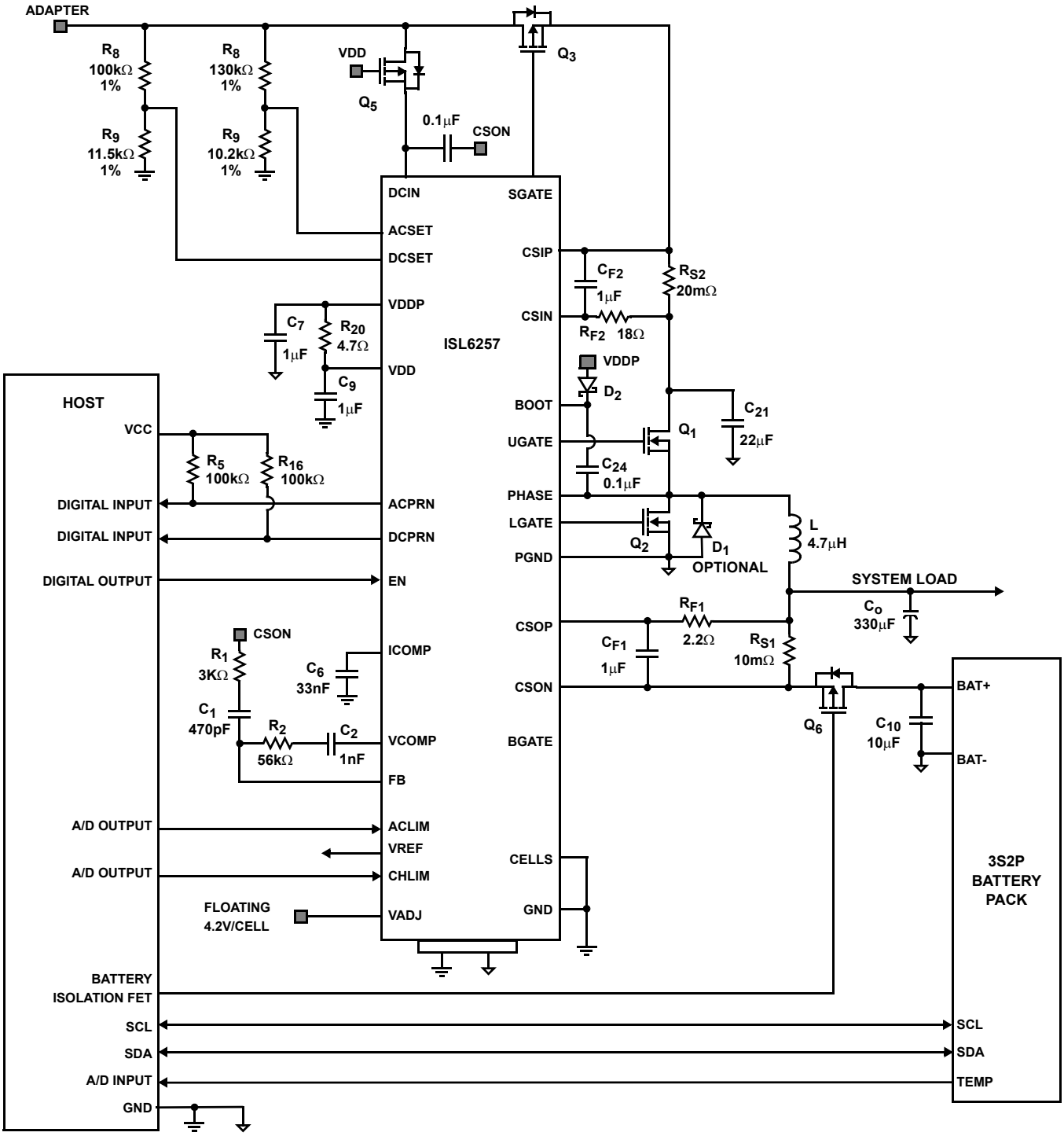


FIGURE 20. ISL6257 TYPICAL NVDC APPLICATION CIRCUIT WITH µP CONTROL

Theory of Operation

Introduction

The ISL6257 includes all of the functions necessary to charge 2 to 4 cell Li-Ion and Li-polymer batteries. A high efficiency synchronous buck converter is used to control the charging voltage and charging current up to 10A. The ISL6257 has input current limiting and analog inputs for setting the charge current and charge voltage; CHLIM inputs are used to control charge current. VADJ and CELLS inputs are used to control charge voltage.

The ISL6257 charges the battery with constant charge current (set by the CHLIM input) until the battery voltage rises to a programmed charge voltage (set by the VADJ and CELLS input) then the charger begins to operate in a constant voltage mode. The charger also drives an adapter isolation P-channel MOSFET on SGATE to efficiently switch in the adapter supply.

The EN input allows shutdown of the charger through a command from a micro-controller. It also uses EN to safely shutdown the charger when the battery is in extremely hot conditions. Figure 19 shows the IC functional block diagram.

The synchronous buck converter uses external N-channel MOSFETs to convert the input voltage to the required charging current and charging voltage. Figure 20 shows the ISL6257 typical application circuit which uses a micro-controller to adjust the charging current set by CHLIM input for aircraft power applications. The voltage at CHLIM and the value of R11 sets the charging current. The DC/DC converter generates the control signals to drive two external N-channel MOSFETs to regulate the voltage and current set by the ACLIM, CHLIM, VADJ and CELLS inputs.

The ISL6257 features a voltage regulation loop (VCOMP) and two current regulation loops (ICOMP). The VCOMP voltage regulation loop monitors CSON to ensure that its voltage never exceeds the battery charge voltage set by VADJ and CELLS. The ICOMP current regulation loops regulate the battery charging current delivered to the battery to ensure that it never exceeds the charging current limit set by CHLIM; and the ICOMP current regulation loops also regulate the input current drawn from the AC adapter to ensure that it never exceeds the input current limit set by ACLIM, and to prevent a system crash and AC adapter overload.

PWM Control

The ISL6257 employs a fixed frequency PWM voltage mode control architecture with a feed-forward function. The feed-forward function maintains a constant modulator gain of 11 to achieve fast line regulation as the buck input voltage changes. When the battery charge voltage approaches the input voltage, the DC/DC converter operates in dropout mode, where there is a timer to prevent the frequency from dropping into the audible frequency range. It can achieve duty cycle of up to 99.6%.

An adaptive gate drive scheme is used to control the dead time between two switches. The dead time control circuit monitors the LGATE output and prevents the upper side MOSFET from turning on until LGATE is fully off, preventing cross-conduction and shoot-through. In order for the dead time circuit to work properly, there must be a low resistance, low inductance path from the LGATE driver to MOSFET gate, and from the source of MOSFET to PGND. The external Schottky diode is between the VDDP pin and BOOT pin to keep the bootstrap capacitor charged.

Setting the Battery Regulation Voltage

The ISL6257 uses a high-accuracy trimmed band-gap voltage reference to regulate the battery charging voltage. The VADJ input adjusts the charger output voltage. The VADJ control voltage can vary from 0 to VREF, providing a 10% adjustment range (from 4.2V - 5% per cell to 4.2V + 5% per cell) on CSON regulation voltage. An overall voltage accuracy of better than 0.5% is achieved.

The per-cell battery termination voltage is a function of the battery chemistry. Consult the battery manufacturers to determine this voltage.

- Float VADJ to set the battery voltage V_{CSON} = 4.2V × number of the cells,
- Connect VADJ to VREF to set 4.41V × number of cells,
- Connect VADJ to ground to set 3.99V × number of the cells.

So, the maximum battery voltage of 17.6V can be achieved. Note that other battery charge voltages can be set by connecting a resistor divider from VREF to ground. The resistor divider should be sized to draw no more than 100µA from VREF or connect a low impedance voltage source like the D/A converter in the micro-controller. The programmed battery voltage per cell can be determined by Equation 1:

$$V_{CELL} = 0.175 \cdot V_{VADJ} + 3.99V \quad \text{(EQ. 1)}$$

An external resistor divider from VREF sets the voltage at VADJ according to Equation 2:

$$V_{VADJ} = VREF \times \frac{R_{bot_VADJ} \| 514k\Omega}{R_{top_VADJ} \| 514k\Omega + R_{bot_VADJ} \| 514k\Omega} \quad \text{(EQ. 2)}$$

To minimize accuracy loss due to interaction with VADJ's internal resistor divider, ensure the AC resistance looking back into the external resistor divider is less than 25k.

Connect CELLS as shown in Table 1 to charge 2, 3 or 4 Li+ cells. When charging other cell chemistries, use CELLS to select an output voltage range for the charger. The internal error amplifier gm1 maintains voltage regulation. The voltage error amplifier is compensated at VCOMP. The component values shown in Figure 20 provide suitable performance for most applications. Individual compensation of the voltage

regulation and current-regulation loops allows for optimal compensation.

TABLE 1. CELL NUMBER PROGRAMMING

CELLS	CELL NUMBER
VDD	4
GND	3
Float	2

Setting the Battery Charge Current Limit

The CHLIM input sets the maximum charging current. The current set by the current sense-resistor connects between CSOP and CSON. The full-scale differential voltage between CSOP and CSON is 165mV for CHLIM = 3.3V, so the maximum charging current is 4.125A for a 40mΩ sensing resistor. Other battery charge current-sense threshold values can be set by connecting a resistor divider from VREF or 3.3V to ground, or by connecting a low impedance voltage source like a D/A converter in the micro-controller. Unlike VADJ and ACLIM, CHLIM does not have an internal resistor divider network. The charge current limit threshold is given by Equation 3:

$$I_{CHG} = \left(\frac{165mV}{R_1}\right)\left(\frac{V_{CHLIM}}{3.3V}\right) \quad \text{(EQ. 3)}$$

To set the trickle charge current for the dumb charger, an A/D output controlled by the micro-controller is connected to CHLIM pin. The trickle charge current is determined by Equation 4:

$$I_{CHG} = \left(\frac{165mV}{R_1}\right)\left(\frac{V_{CHLIM,trickle}}{3.3V}\right) \quad \text{(EQ. 4)}$$

When the CHLIM voltage is below 88mV (typical), it will disable the battery charge. When choosing the current sensing resistor, note that the voltage drop across the sensing resistor causes further power dissipation, reducing efficiency. However, adjusting CHLIM voltage to reduce the voltage across the current sense resistor R11 will degrade accuracy due to the smaller signal to the input of the current sense amplifier. There is a trade-off between accuracy and power dissipation. A low pass filter is recommended to eliminate switching noise. Connect the resistor to the CSOP pin instead of the CSON pin, as the CSOP pin has lower bias current and less influence on current-sense accuracy and voltage regulation accuracy.

Setting the Input Current Limit

The total input current from an AC adapter, or other DC source, is a function of the system supply current and the battery-charging current. The input current regulator limits the input current by reducing the charging current, when the input current exceeds the input current limit set by ACLIM. System current normally fluctuates as portions of the system are powered up or down. Without input current regulation, the source must be able to supply the maximum system current and the maximum charger input current simultaneously. By using the input current limiter, the current capability of the AC adapter can be lowered, reducing system cost.

The ISL6257 limits the battery charge current when the input current-limit threshold is exceeded, ensuring the battery charger does not load down the AC adapter voltage. This constant input current regulation allows the adapter to fully power the system and prevent the AC adapter from overloading and crashing the system bus.

An internal amplifier gm3 compares the voltage between CSIP and CSIN to the input current limit threshold voltage set by ACLIM. Connect ACLIM to REF, Float and GND for the full-scale input current limit threshold voltage of 100mV, 75mV and 50mV, respectively, or use a resistor divider from VREF to ground to set the input current limit as Equation 5:

$$I_{INPUT} = \frac{1}{R_2}\cdot\left(\frac{0.05}{VREF}\cdot V_{ACLIM} + 0.05\right)$$

$$V_{ACLIM} = VREF\cdot\left(\frac{R_{bot,ACLIM} \parallel 152k\Omega}{R_{top,ACLIM} \parallel 152k\Omega + R_{bot,ACLIM} \parallel 152k\Omega}\right) \quad \text{(EQ. 5)}$$

When choosing the current sense resistor, note that the voltage drop across this resistor causes further power dissipation, reducing efficiency. The AC adapter current sense accuracy is very important. Use a 1% tolerance current-sense resistor. The highest accuracy of ±1.5% is achieved with 100mV current-sense threshold voltage for ACLIM = VREF, but it has the highest power dissipation. For example, it has 400mW power dissipation for rated 4A AC adapter and 1W sensing resistor may have to be used. ±2.5% and ±4.5% accuracy can be achieved with 75mV and 50mV current-sense threshold voltage for ACLIM = Floating and ACLIM = GND, respectively.

A low pass filter is suggested to eliminate the switching noise. Connect the resistor to CSIN pin instead of CSIP pin because CSIN pin has lower bias current and less influence on the current-sense accuracy.

AC Adapter Detection

Connect the AC adapter voltage through a resistor divider to ACSET to detect when AC power is available, as shown in Figure 20. ACPRN is an open-drain output and is high when ACSET is less than $V_{th,fall}$, and active low when ACSET is above $V_{th,rise}$. $V_{th,rise}$ and $V_{th,fall}$ are given by Equation 6 and Equation 7:

$$V_{th,rise} = \left(\frac{R_8}{R_9} + 1\right) \cdot V_{ACSET} \quad \text{(EQ. 6)}$$

$$V_{th,fall} = \left(\frac{R_8}{R_9} + 1\right) \cdot V_{ACSET} - I_{hys} \cdot R_8 \quad \text{(EQ. 7)}$$

where:

- I_{hys} is the ACSET input bias current hysteresis, and
- V_{ACSET} = 1.24V (min), 1.26V (typ) and 1.28V (max).

The hysteresis is $I_{hys}R_8$, where I_{hys} = 2.2µA (min), 3.4µA (typ) and 4.4µA (max).

DC Adapter Detection

Connect the DC input through a resistor divider to DCSET to detect when lower voltage (i.e. aircraft) DC power is available. DCPRN is an open-drain output and is high when DCSET is less than $V_{th,fall}$, and active low when DCSET is above $V_{th,rise}$. $V_{th,rise}$ and $V_{th,fall}$ are given by Equation 8 and Equation 9:

$$V_{th,rise} = \left(\frac{R_{24}}{R_{25}} + 1\right) \bullet V_{DCSET} \quad \text{(EQ. 8)}$$

$$V_{th,fall} = \left(\frac{R_{24}}{R_{25}} + 1\right) \bullet V_{DCSET} - I_{hys}R_{24} \quad \text{(EQ. 9)}$$

where:

- I_{hys} is the DCSET input bias current hysteresis, and
- V_{DCSET} = 1.24V (min), 1.26V (typ) and 1.28V (max).

The hysteresis is $I_{hys}R_{14}$, where I_{hys} = 2.2µA (min), 3.4µA (typ) and 4.4µA (max).

LDO Regulator

VDD provides a 5.0V supply voltage from the internal LDO regulator from DCIN and can deliver up to 30mA of current. The MOSFET drivers are powered by VDDP, which must be connected to VDDP as shown in Figure 20. VDDP connects to VDD through an external low pass filter. Bypass VDDP and VDD with a 1µF capacitor.

Shutdown

The ISL6257 features a low-power shutdown mode. Driving EN low shuts down the ISL6257. In shutdown, the DC/DC converter is disabled, and VCOMP and ICOMP are pulled to ground. The ACPRN and DCPRN outputs continue to function.

EN can be driven by a thermistor to allow automatic shutdown of the ISL6257 when the battery pack is hot. Often an NTC thermistor is included inside the battery pack to measure its temperature. When connected to the charger, the thermistor forms a voltage divider with a resistive pull-up to the VREF. The threshold voltage of EN is 1.0V with 60mV hysteresis. The thermistor can be selected to have a resistance vs temperature characteristic that abruptly decreases above a critical temperature. This arrangement automatically shuts down the ISL6257 when the battery pack is above a critical temperature.

Another method for inhibiting charging is to force CHLIM below 85mV (typ).

Supply Isolation

If the voltage across the adapter sense resistor R_2 is typically greater than 8mV, the P-channel MOSFET controlled by SGATE is turned on reducing the power dissipation. If the voltage across the adapter sense resistor R_2 is less than 3mV, SGATE turns off the P-channel MOSFET isolating the adapter from the system bus.

Battery Power Source Selection and Aircraft Power Application

The battery voltage is monitored by CSON. If the battery voltage measured on CSON is less than the adapter voltage measured on DCIN, then the P-channel MOSFET controlled by SGATE is allowed to turn on when the adapter current is high enough. If it is greater, then the P-channel MOSFET controlled by SGATE turns off.

When operating on aircraft power it is desirable to disable charging to minimize loading of the aircraft power systems. DCIN is usually lower when connected to aircraft power (15V) than it is when connected AC power (20V). The DCSET pin provides means of detecting this lower DC input voltage. If the DC input voltage is below the ACSET threshold and above the DCET threshold, ACPRN will be high and DCPRN will be low, and the host may turn off Q_5 (Figure 20) to stop charging the battery.

Short Circuit Protection

Since the battery charger will regulate the charge current to the limit set by CHLIM, it automatically has short circuit protection and is able to provide the charge current to wake up an extremely discharged battery.

Over Temperature Protection

If the die temperature exceeds +150°C, it stops charging. Once the die temperature drops below +125°C, charging will start up again.

Application Information

The following battery charger design refers to the typical application circuit in Figure 20, where typical battery configuration of 3S2P is used. This section describes how to select the external components including the inductor, input and output capacitors, switching MOSFETs, and current sensing resistors.

Inductor Selection

The inductor selection has trade-offs between cost, size and efficiency. For example, the lower the inductance, the smaller the size, but ripple current is higher. This also results in higher AC losses in the magnetic core and the windings, which decrease the system efficiency. On the other hand, the higher inductance results in lower ripple current and smaller output filter capacitors, but it has higher DCR (DC resistance of the inductor) loss, and has slower transient response. So, the practical inductor design is based on the inductor ripple current being ±15% to ±20% of the maximum operating DC current at maximum input voltage. Maximum ripple is at 50% duty cycle or $V_{BAT} = V_{IN,MAX}/2$. The required inductance can be calculated from Equation 10:

$$L = \frac{R_{IN,\,MAX}}{4 \cdot I_{SW} \cdot I_{RIPPLE}} \quad \text{(EQ. 10)}$$

Where $V_{IN,MAX}$ and f_{SW} are the maximum input voltage, and switching frequency, respectively.

The inductor ripple current ΔI is found from Equation 11:

$$I_{RIPPLE} = 0.3 \cdot I_{L,\,MAX} \quad \text{(EQ. 11)}$$

where the maximum peak-to-peak ripple current is 30% of the maximum charge current is used.

For $V_{IN,MAX}$ = 19V, V_{BAT} = 12.6V, $I_{L,MAX}$ = 10A, and f_s = 300kHz, the calculated inductance is 4.7µH. Ferrite cores are often the best choice since they are optimized at 300kHz to 600kHz operation with low core loss. The core must be large enough not to saturate at the peak inductor current I_{Peak} in Equation 12:

$$I_{PEAK} = I_{L,\,MAX} + \frac{1}{2} \cdot I_{RIPPLE} \quad \text{(EQ. 12)}$$

Output Capacitor Selection

The output capacitor in parallel with the battery is used to absorb the high frequency switching ripple current and supply very high di/dt load transients. In a Narrow VDC system the output capacitance is also the bypass capacitance on the input of the CORE regulator and may be several hundred µF. The following examples use 330µF with ESR = 6mΩ.

The RMS value of the output ripple current I_{rms} is given by Equation 13:

$$I_{RMS} = \frac{V_{IN,\,MAX}}{\sqrt{12} \cdot L \cdot F_{SW}} \cdot D \cdot (1 - D) \quad \text{(EQ. 13)}$$

where the duty cycle D is the ratio of the output voltage (battery voltage) over the input voltage for continuous conduction mode, which is typical operation for the battery charger. During the battery charge period, the output voltage varies from its initial battery voltage to the rated battery voltage. So, the duty cycle change can be in the range of between 0.5 and 0.88 for the minimum battery voltage of 10V (2.5V/Cell) and the maximum battery voltage of 16.8V. The maximum RMS value of the output ripple current occurs at the duty cycle of 0.5 and is expressed as Equation 14:

$$I_{RMS} = \frac{V_{IN,\,MAX}}{4 \cdot \sqrt{12} \cdot L \cdot F_{SW}} \quad \text{(EQ. 14)}$$

For $V_{IN,MAX}$ = 19V, L = 4.7µH, and f_s = 300kHz, the maximum RMS current is 0.98A. Ceramic capacitors are good choices to absorb this current and also has very small size. Organic polymer capacitors have high capacitance with small size and have a significant equivalent series resistance (ESR). Although ESR adds to ripple voltage, it also creates a high frequency zero that helps the closed loop operation of the buck regulator.

EMI considerations usually make it desirable to minimize ripple current in the battery leads. Beads may be added in series with the battery pack to increase the battery impedance at 300kHz switching frequency. Switching ripple current splits between the battery and the output capacitor depending on the ESR of the output capacitor and battery impedance. If the ESR of the output capacitor is 10mΩ and battery impedance is raised to 2Ω with a bead, then only 0.5% of the ripple current will flow in the battery.

MOSFET Selection

The notebook battery charger synchronous buck converter has the input voltage from the AC adapter output. The maximum AC adapter output voltage does not exceed 25V. Therefore, MOSFETs should be used that are rated for 30V VDS with low $r_{DS(ON)}$ at 5V VGS.

The high-side MOSFET must be able to dissipate the conduction losses plus the switching losses. For the battery charger application, the input voltage of the synchronous buck converter is equal to the AC adapter output voltage, which is relatively constant. The maximum efficiency is achieved by selecting a high-side MOSFET that has the conduction losses equal to the switching losses. Switching losses in the low-side FET are very small. The choice of low-side FET is a trade off between conduction losses ($r_{DS(ON)}$) and cost. A good rule of thumb for the $r_{DS(ON)}$ of the low-side FET is 2X the $r_{DS(ON)}$ of the high-side FET.

The ISL6257 LGATE gate driver can drive sufficient gate current to switch most MOSFETs efficiently. However, some FETs may exhibit cross conduction (or shoot through) due to current injected into the drain-to-source parasitic capacitor (C_{gd}) by the high dV/dt rising edge at phase node when the high-side MOSFET turns on. Although LGATE sink current (1.8A typical) is more than enough to switch the FET off quickly, voltage drops across parasitic impedances between LGATE and the MOSFET can allow the gate to rise during the fast rising edge of voltage on the drain. MOSFETs with low

threshold voltage (<1.5V) and low ratio of C_{gs}/C_{gd} (<5) and high gate resistance (>4Ω) may be turned on for a few ns by the high dV/dt (rising edge) on their drain. This can be avoided with higher threshold voltage and C_{gs}/C_{gd} ratio. Another way to avoid cross conduction is slowing the turn-on speed of the high-side MOSFET by connecting a resistor between the BOOT pin and the boot strap cap.

For the high-side MOSFET, the worst-case conduction losses occur at the minimum input voltage as shown in Equation 15:

$$P_{Q1,\,conduction} = \frac{V_{OUT}}{V_{IN}} \cdot {I_{BAT}}^2 \cdot r_{DS(ON)} \quad \text{(EQ. 15)}$$

The optimum efficiency occurs when the switching losses equal the conduction losses. However, it is difficult to calculate the switching losses in the high-side MOSFET since it must allow for difficult-to-quantify factors that influence the turn-on and turn-off times. These factors include the MOSFET internal gate resistance, gate charge, threshold voltage, stray inductance, pull-up and pull-down resistance of the gate driver. The following switching loss calculation (Equation 16) provides a rough estimate.

$$P_{Q1,\,Switching} = \quad \text{(EQ. 16)}$$
$$\frac{1}{2}V_{IN}I_{LV}f_{sw}\left(\frac{Q_{gd}}{I_{g,\,source}}\right) + \frac{1}{2}V_{IN}I_{LP}f_{sw}\left(\frac{Q_{gd}}{I_{g,\,sink}}\right) + Q_{rr}V_{IN}f_{sw}$$

where the following are the peak gate-drive source/sink current of Q_1, respectively:

- Q_{gd}: drain-to-gate charge,
- Q_{rr}: total reverse recovery charge of the body-diode in low-side MOSFET,
- I_{LV}: inductor valley current,
- I_{LP}: Inductor peak current,
- $I_{g,sink}$
- $I_{g,source}$

To achieve low switching losses, it requires low drain-to-gate charge Q_{gd}. Generally, the lower the drain-to-gate charge, the higher the on-resistance. Therefore, there is a trade-off between the on-resistance and drain-to-gate charge. Good MOSFET selection is based on the Figure of Merit (FOM), which is a product of the total gate charge and on-resistance. Usually, the smaller the value of FOM, the higher the efficiency for the same application.

For the low-side MOSFET, the worst-case power dissipation occurs at minimum battery voltage and maximum input voltage (Equation 17):

$$P_{Q2} = \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \cdot {I_{BAT}}^2 \cdot r_{DS(ON)} \quad \text{(EQ. 17)}$$

Choose a low-side MOSFET that has the lowest possible on-resistance with a moderate-sized package like the SO-8 and is reasonably priced. The switching losses are not an issue for the low-side MOSFET because it operates at zero-voltage-switching.

Choose a Schottky diode in parallel with low-side MOSFET Q_2 with a forward voltage drop low enough to prevent the low-side MOSFET Q_2 body-diode from turning on during the dead time. This also reduces the power loss in the high-side MOSFET associated with the reverse recovery of the low-side MOSFET Q_2 body diode.

As a general rule, select a diode with DC current rating equal to one-third of the load current. One option is to choose a combined MOSFET with the Schottky diode in a single package. The integrated packages may work better in practice because there is less stray inductance due to a short connection. This Schottky diode is optional and may be removed if efficiency loss can be tolerated. In addition, ensure that the required total gate drive current for the selected MOSFETs should be less than 24mA. So, the total gate charge for the high-side and low-side MOSFETs is limited by Equation 18:

$$Q_{GATE} \leq \frac{1_{GATE}}{f_{sw}} \quad \text{(EQ. 18)}$$

where I_{GATE} is the total gate drive current and should be less than 24mA. Substituting I_{GATE} = 24mA and f_s = 300kHz into Equation 18 yields that the total gate charge should be less than 80nC. Therefore, the ISL6257 easily drives the battery charge current up to 8A.

Snubber Design

ISL6257's buck regulator operates in discontinuous current mode (DCM) when the load current is less than half the peak-to-peak current in the inductor. After the low-side FET turns off, the phase voltage rings due to the high impedance with both FETs off. This can be seen in Figure 9. Adding a snubber (resistor in series with a capacitor) from the phase node to ground can greatly reduce the ringing. In some situations a snubber can improve output ripple and regulation.

The snubber capacitor should be approximately twice the parasitic capacitance on the phase node. This can be estimated by operating at very low load current (100mA) and measuring the ringing frequency.

CSNUB and RSNUB can be calculated from Equation 19:

$$C_{SNUB} = \frac{2}{(2\pi f_{ring})^2 \cdot L} \qquad R_{SNUB} = \frac{1}{2 \cdot C_{SNUB} \cdot f_{ring}} \tag{EQ. 19}$$

Input Capacitor Selection

The input capacitor absorbs the ripple current from the synchronous buck converter, which is given by Equation 20:

$$I_{RMS} = I_{BAT}\frac{\sqrt{V_{OUT} \cdot (V_{IN} - V_{OUT})}}{V_{IN}} \tag{EQ. 20}$$

This RMS ripple current must be smaller than the rated RMS current in the capacitor datasheet. Non-tantalum chemistries (ceramic, aluminum, or OSCON) are preferred due to their resistance to power-up surge currents when the AC adapter is plugged into the battery charger. For notebook battery charger applications, it is recommend that ceramic capacitors or polymer capacitors from Sanyo be used due to their small size and reasonable cost.

Table 2 shows the component lists for the typical application circuit in Figure 20.

TABLE 2. COMPONENT LIST

PARTS	PART NUMBERS AND MANUFACTURER
C_{21}, C_{10}	22µF/25V ceramic capacitor, TDK, C5750X7R1E226M
C_{12}, C_{24}	0.1µF/50V ceramic capacitor
C_3, C_7, C_9	1µF/10V ceramic capacitor, Taiyo Yuden LMK212BJ105MG
C_2	1nF ceramic capacitor
C_6	33nF ceramic capacitor
C_o	330µF, 6mΩ electrolytic capacitor (system load)
C_1	470pF ceramic capacitor
D_1	30V/3A Schottky diode, EC31QS03L (optional)
D_2	100mA/30V Schottky Diode, Central Semiconductor
L	4.7µH/10.2A/8.8mΩ, Toko, FDA1254-4R7M
Q_1	6mΩ/30V, HAT2168HFDS6912A, Fairchild
Q_2	2.5mΩ/30V HAT2165H
Q_3	-30V/30mΩ, Si4835BDY, Siliconix
Q_5	Signal P-channel MOSFET, NDS352AP
Q_6	-30V/30mΩ, Si4835BDY, Siliconix
R_1	3kΩ, ±1%, (0805)
R_2	56kΩ, ±1%, (0805)
R_{S1}	10mΩ, ±1%, LRC-LR2512-01-R010-F, IRC
R_{S2}	20mΩ, ±1%, LRC-LR2010-01-R020-F, IRC
R_{F2}	18Ω, ±5%, (0805)
R_{F1}	2.2Ω, ±5%, (0805)
R_5, R_7	100kΩ, ±5%, (0805)
R_8	130k, ±1%, (0805)
R_9	10.2kΩ, ±1%, (0805)
R_{20}	4.7Ω, ±5%, (0805)

TABLE 2. COMPONENT LIST (Continued)

PARTS	PART NUMBERS AND MANUFACTURER
R_{24}	100kΩ, ±1%, (0805)
R_{15}	11.5kΩ, ±1%, (0805)
R_{16}	100kΩ, ±1%, (0805)

Loop Compensation Design

ISL6257 has three closed loop control modes. One controls the output voltage when the battery is fully charged or absent. A second controls the current into the battery when charging and the third limits current drawn from the adapter. The charge current and input current control loops are compensated by a single capacitor on the ICOMP pin. The voltage control loop is compensated by a network shown in Figure 23. Descriptions of these control loops and guidelines for selecting compensation components will be given in the following sections. Which loop controls the output is determined by the minimum current buffer and the minimum voltage buffer shown in Figure 19. These three loops will be described separately.

Transconductance Amplifiers gm1, gm2 and gm3

ISL6257 uses several transconductance amplifiers (also known as gm amps). Most commercially available op amps are voltage controlled voltage sources with gain expressed as $A = V_{OUT}/V_{IN}$. gm amps are voltage controlled current sources with gain expressed as $gm = I_{OUT}/V_{IN}$. gm will appear in some of the equations for poles and zeros in the compensation.

PWM Gain F_m

The Pulse Width Modulator in the ISL6257 converts voltage at VCOMP (or ICOMP) to a duty cycle by comparing VCOMP to a triangle wave (duty = $VCOMP/V_{PP\ RAMP}$). The low-pass filter formed by L and C_O convert the duty cycle to a DC output voltage ($Vo = V_{DCIN}$*duty). In ISL6257, the triangle wave amplitude is proportional to V_{DCIN}. Making the ramp amplitude proportional to DCIN makes the gain from VCOMP to the PHASE output a constant 11 and is independent of DCIN.

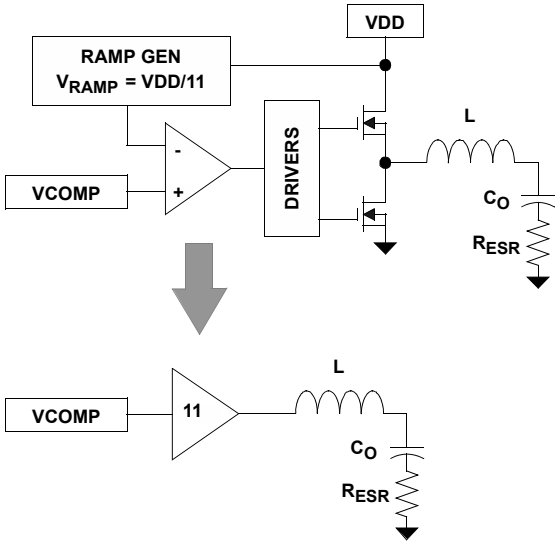


FIGURE 21. FOR SMALL SIGNAL AC ANALYSIS, THE PWM AND POWER STAGE CAN BE MODELED AS A SIMPLE GAIN OF 11.

Output LC Filter Transfer Functions

The gain from the phase node to the system output and battery depend entirely on external components. Transfer function $A_{LC}(s)$ is shown in Equation 21 and Equation 22:

$$A_{LC} = \frac{\left(1 - \frac{s}{\omega_{ESR}}\right)}{\left(\frac{s^2}{\omega_{DP}} + \frac{s}{(\omega_{DP} \cdot Q)} + 1\right)} \qquad \text{(EQ. 21)}$$

$$\omega_{ESR} = \frac{1}{(R_{ESR} \cdot C_o)} \qquad \omega_{DP} = \frac{1}{(\sqrt{L \cdot C_o})} \qquad Q = R_o \cdot \sqrt{\frac{L}{C_o}} \qquad \text{(EQ. 22)}$$

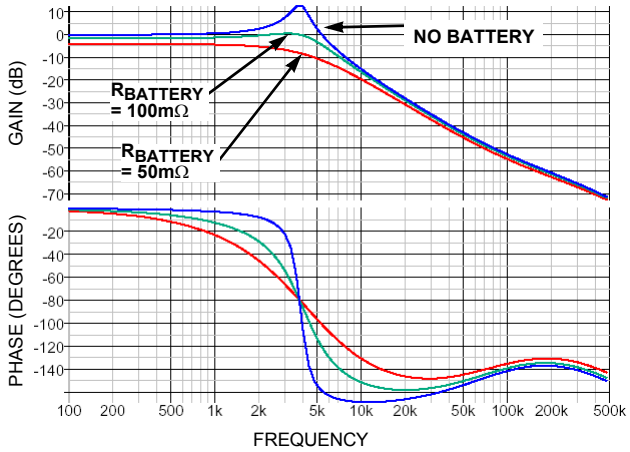


FIGURE 22. FREQUENCY RESPONSE OF THE LC OUTPUT FILTER

The load resistance R_O is a combination of MOSFET $r_{DS(ON)}$, inductor DCR and the internal resistance of the battery (normally between 50mΩ and 200mΩ) in parallel with the system. The system load may be modeled as a current sink in parallel with a resistance. For AC analysis of the voltage control loop this may be treated as a very high resistance or an open circuit. The worst case for voltage mode control is when the battery is absent. This results in the highest Q of the LC filter and the lowest phase margin.

Voltage Control Loop

The voltage error amplifier controls the output when the battery is not drawing current and the input current is below the limit. Under these conditions VCOMP controls the charger's output because the 2 current error amplifiers (gm2 and gm3) output their maximum current and charge the capacitor on ICOMP to its maximum voltage (limited to 1.2V above VCOMP). With high voltage on ICOMP, the minimum voltage buffer output equals the voltage on VCOMP. The voltage control loop is shown in Figure 23.

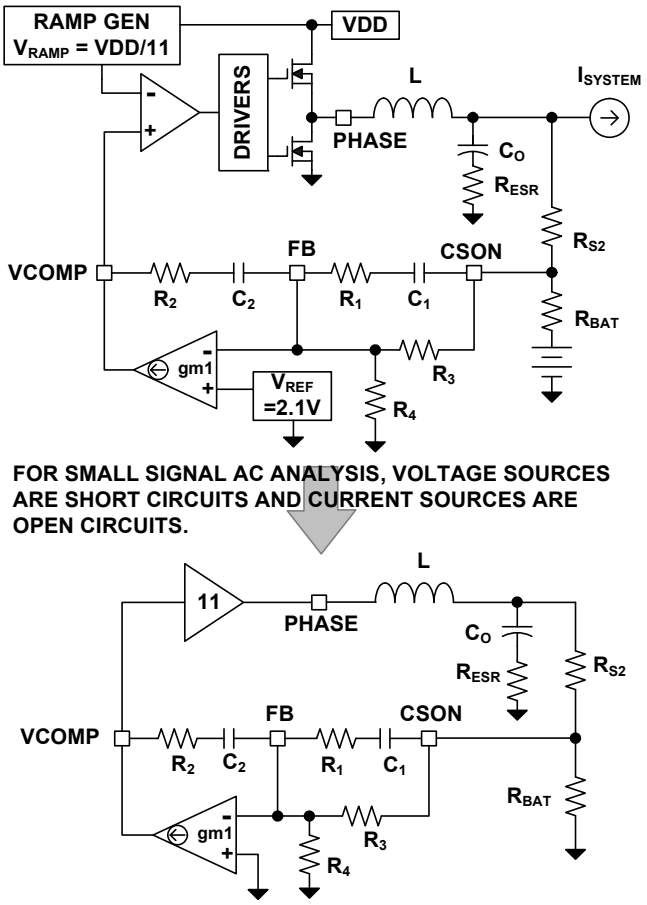


FIGURE 23. VOLTAGE LOOP COMPENSATOR

The compensation network consists of the voltage error amplifier gm1 and the compensation network R_1, C_1, R_2 and C_2. R_3 and R_4 are internal divider resisters that set the DC output voltage. For a 3 cell battery, R_3 = 320kΩ and R_4 = 64kΩ. The equations below relate the compensation network's poles, zeros and gain to the components in Figure 20. Figure 24 shows an asymptotic Bode plot of the DC/DC converter's gain vs. frequency. It is strongly recommended that F_{Z1} is approximately 1/4*F_{DP} and F_{Z2} is approximately 1/2*F_{DP}.

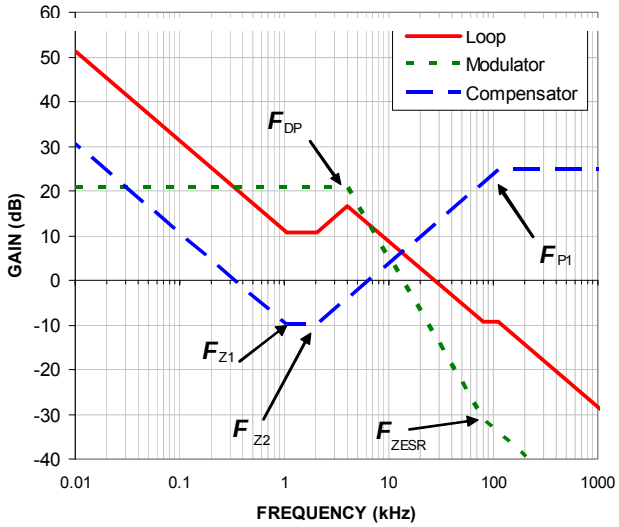


FIGURE 24. ASYMPTOTIC BODE PLOT OF THE VOLTAGE CONTROL LOOP GAIN

Compensation Break Frequency Equations

$$F_{Z1} = \frac{1}{(2\pi \cdot C_1 \cdot (R_1 + R_3))} \quad \text{(EQ. 23)}$$

$$F_{Z2} = \frac{1}{\left(2\pi \cdot C_2 \cdot \left\{R_2 - \frac{1}{gm1}\right\}\right)} \qquad \frac{1}{gm1} = 4.17k\Omega \quad \text{(EQ. 24)}$$

$$F_{DP} = \frac{1}{(2\pi\sqrt{L \cdot C_o})} \qquad F_{P1} = \frac{1}{(2\pi \cdot R_1 \cdot C_1)} \quad \text{(EQ. 25)}$$

$$F_{ESR} = \frac{1}{(2\pi \cdot C_o \cdot R_{ESR})} \quad \text{(EQ. 26)}$$

TABLE 3.

CELLS	R_3
2	288kΩ
3	320kΩ
4	336kΩ

Charge Current Control Loop

When the battery voltage is less than the fully charged voltage, the voltage error amplifier goes to it's maximum output (limited to 1.2V above ICOMP) and the ICOMP voltage controls the loop through the minimum voltage buffer. Figure 25 shows the charge current control loop.

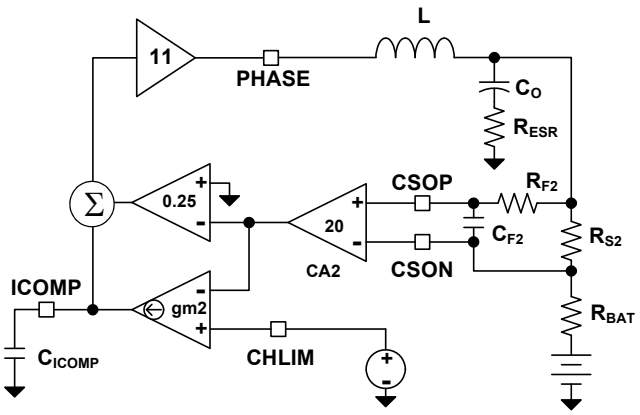


FIGURE 25. CHARGE CURRENT LIMIT LOOP

The compensation capacitor (C_{ICOMP}) gives the error amplifier (gm2) a pole at a very low frequency (<<1Hz) and a a zero at F_{Z1}. F_{Z1} is created by the 0.25*CA2 output added to ICOMP. The loop response has another zero due to the output capacitor's esr.

A filter should be added between R_{S2} and CSOP and CSON to reduce switching noise. The filter roll off frequency should be between the cross over frequency and the switching frequency (~100kHz). R_{F2} should be small (<10Ω) to minimize offsets due to leakage current into CSOP.

$$F_{DP} = \frac{1}{(2\pi\sqrt{L \cdot C_o})} \quad \text{(EQ. 27)}$$

$$F_{ZESR} = \frac{1}{(2\pi \cdot C_o \cdot R_{ESR})} \quad \text{(EQ. 28)}$$

$$F_{Z1} = \frac{4 \cdot gm2}{(2\pi \cdot C_{ICOMP})} \qquad gm2 = 50\mu A/V \quad \text{(EQ. 29)}$$

$$F_{FILTER} = \frac{1}{(2\pi \cdot C_{F2} \cdot R_{F2})} \quad \text{(EQ. 30)}$$

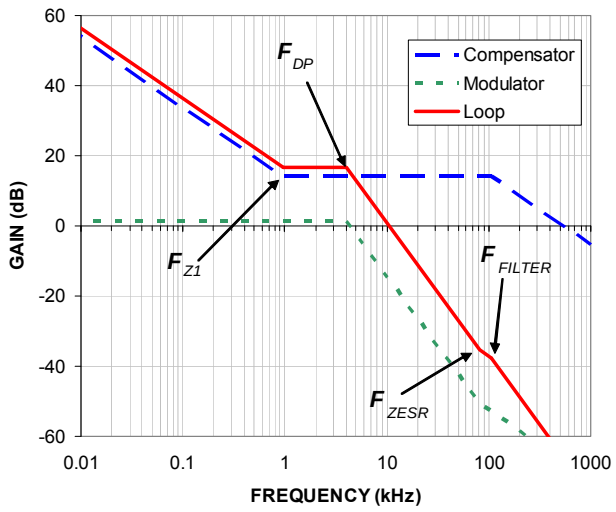


FIGURE 26. CHARGE CURRENT LOOP BODE PLOTS

C_{ICOMP} should be chosen using Equation 31 to set $F_{Z1} = F_{DP}/10$. The crossover frequency will be approximately 2.5 * F_{DP}. The phase margin will be between +10°C and +40°C depending on F_{ZESR}.

$$C_{ICOMP} = \frac{4 \cdot gm2}{2\pi \cdot F_{DP}/10} \quad \text{(EQ. 31)}$$

Adapter Current Limit Control Loop

If the combined battery charge current and system load current draws current that equals the adapter current limit set by the ACLIM pin, ISL6257 will reduce the current to the battery and/or reduce the output voltage to hold the adapter current at the limit. Figure 17 shows the effect on output voltage as the load current is swept up beyond the adapter current limit. Above the adapter current limit the minimum current buffer equals the output of gm3 and ICOMP controls the charger output. Figure 27 shows the resulting adapter current control system.

A filter should be added between R_{S1} and CSIP and CSIN to reduce switching noise. The filter roll off frequency should be between the cross over frequency and the switching frequency (~100kHz).

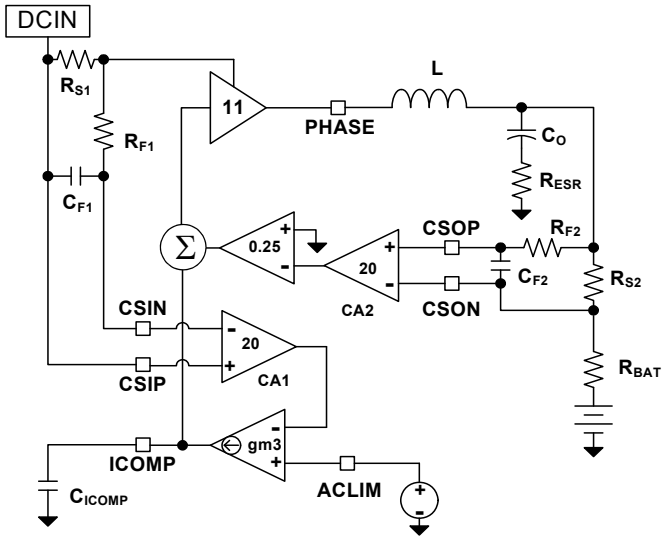


FIGURE 27. ADAPTER CURRENT LIMIT LOOP

The loop response equations, bode plots and the selection of C_{ICOMP} are the same as the charge current control loop with loop gain reduced by the duty cycle. In other words, if the duty cycle D = 50%, the loop gain will be 6dB lower than the loop gain in Figure 26. This gives lower crossover frequency and higher phase margin in this mode.

PCB Layout Considerations

Power and Signal Layers Placement on the PCB

As a general rule, power layers should be close together, either on the top or bottom of the board, with signal layers on the opposite side of the board. As an example, layer arrangement on a 4-layer board is shown below:

1. Top Layer: signal lines, or half board for signal lines and the other half board for power lines
2. Signal Ground
3. Power Layers: Power Ground
4. Bottom Layer: Power MOSFET, Inductors and other Power traces

Separate the power voltage and current flowing path from the control and logic level signal path. The controller IC will stay on the signal layer, which is isolated by the signal ground to the power signal traces.

Component Placement

The power MOSFET should be close to the IC so that the gate drive signal, the LGATE, UGATE, PHASE, and BOOT, traces can be short.

Place the components in such a way that the area under the IC has less noise traces with high dV/dt and di/dt, such as gate signals and phase node signals.

Signal Ground and Power Ground Connection

At minimum, a reasonably large area of copper, which will shield other noise couplings through the IC, should be used as signal ground beneath the IC. The best tie-point between the signal ground and the power ground is at the negative side of the output capacitor on each side, where there is little noise; a noisy trace beneath the IC is not recommended.

GND and VDD Pin

At least one high quality ceramic decoupling cap should be used to cross these two pins. The decoupling cap can be put close to the IC.

LGATE Pin

This is the gate drive signal for the bottom MOSFET of the buck converter. The signal going through this trace has both high dV/dt and high di/dt, and the peak charging and discharging current is very high. These two traces should be short, wide, and away from other traces. There should be no other traces in parallel with these traces on any layer.

PGND Pin

PGND pin should be laid out to the negative side of the relevant output cap with separate traces.The negative side of the output capacitor must be close to the source node of the bottom MOSFET. This trace is the return path of LGATE.

PHASE Pin

This trace should be short, and positioned away from other weak signal traces. This node has a very high dV/dt with a voltage swing from the input voltage to ground. No trace should be in parallel with it. This trace is also the return path for UGATE. Connect this pin to the high-side MOSFET source.

UGATE Pin

This pin has a square shape waveform with high dV/dt. It provides the gate drive current to charge and discharge the top MOSFET with high di/dt. This trace should be wide, short, and away from other traces similar to the LGATE.

BOOT Pin

This pin's di/dt is as high as the UGATE; therefore, this trace should be as short as possible.

CSIP, CSIN Pins

The input current sense resistor connects to the CSIP and CSIN pins through a low pass filter. The traces should be away and guarded/shielded from the high dV/dt and di/dt nodes like Phase, Boot.

CSOP, CSON Pins

The charging current sense resistor connects to the CSOP and the CSON pins through a low pass filter. The traces should be away and guarded/shielded from the high dV/dt and di/dt nodes like PHASE, BOOT. In general, the current sense resistor should be close to the IC.

EN Pin

This pin stays high at enable mode and low at idle mode and is relatively robust. Enable signals should refer to the signal ground.

DCIN Pin

This pin connects to AC adapter output voltage, and should be less noise sensitive.

Copper Size for the Phase Node

The capacitance of PHASE should be kept very low to minimize ringing. It would be best to limit the size of the PHASE node copper in strict accordance with the current and thermal management of the application.

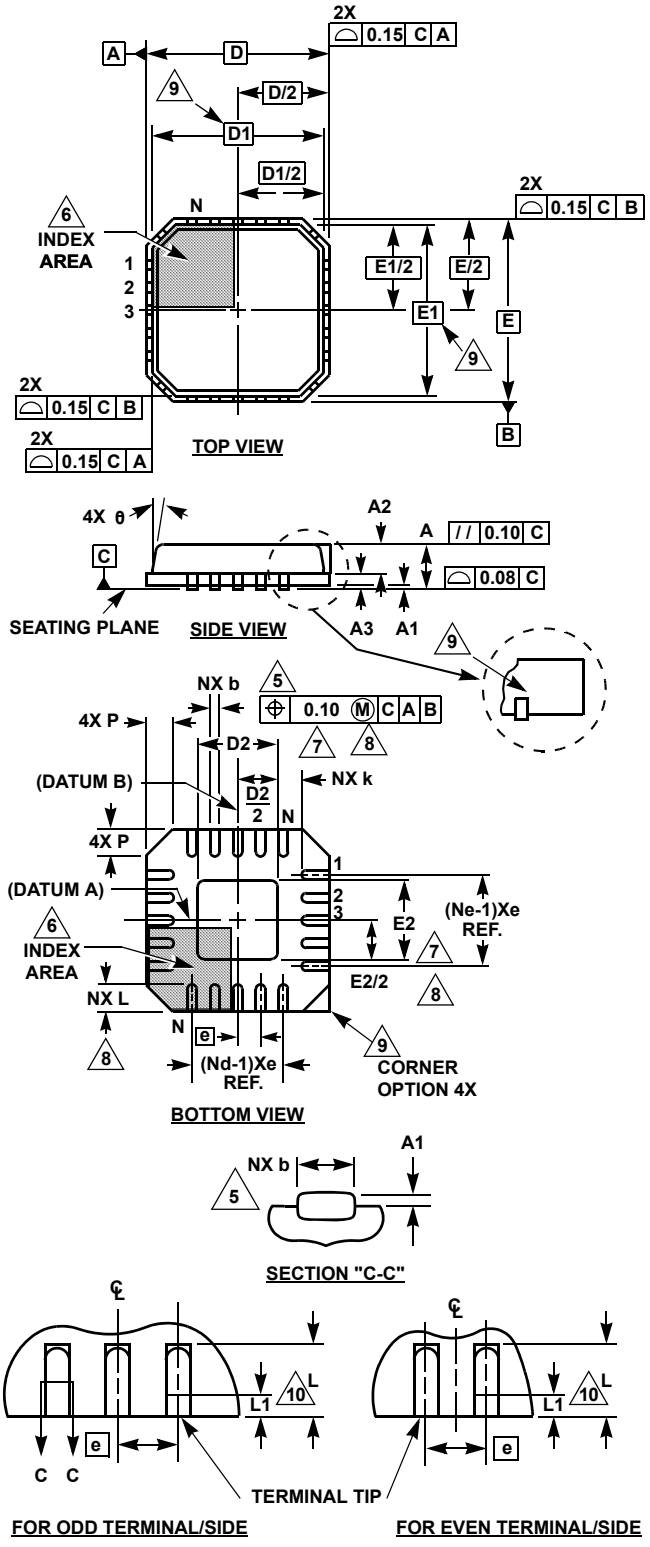
Identify the Power and Signal Ground

The input and output capacitors of the converters, the source terminal of the bottom switching MOSFET PGND should connect to the power ground. The other components should connect to signal ground. Signal and power ground are tied together at one point.

Clamping Capacitor for Switching MOSFET

It is recommended that ceramic caps be used closely connected to the drain of the high-side MOSFET, and the source of the low-side MOSFET. This capacitor reduces the noise and the power loss of the MOSFET.

Quad Flat No-Lead Plastic Package (QFN)
Micro Lead Frame Plastic Package (MLFP)



L28.5x5

28 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE (COMPLIANT TO JEDEC MO-220VHHD-1 ISSUE I)

SYMBOL	MILLIMETERS			NOTES
	MIN	NOMINAL	MAX	
A	0.80	0.90	1.00	-
A1	-	0.02	0.05	-
A2	-	0.65	1.00	9
A3		0.20 REF		9
b	0.18	0.25	0.30	5,8
D		5.00 BSC		-
D1		4.75 BSC		9
D2	2.95	3.10	3.25	7,8
E		5.00 BSC		-
E1		4.75 BSC		9
E2	2.95	3.10	3.25	7,8
e		0.50 BSC		-
k	0.20	-	-	-
L	0.50	0.60	0.75	8
N		28		2
Nd		7		3
Ne		7		3
P	-	-	0.60	9
θ	-	-	12	9

Rev. 1 11/04

NOTES:

1. Dimensioning and tolerancing conform to ASME Y14.5-1994.
2. N is the number of terminals.
3. Nd and Ne refer to the number of terminals on each D and E.
4. All dimensions are in millimeters. Angles are in degrees.
5. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
7. Dimensions D2 and E2 are for the exposed pads which provide improved electrical and thermal performance.
8. Nominal dimensions are provided to assist with PCB Land Pattern Design efforts, see Intersil Technical Brief TB389.
9. Features and dimensions A2, A3, D1, E1, P & θ are present when Anvil singulation method is used and not present for saw singulation.