
ISOLATED EVALUATION BOARD FOR THE Si3402B

1. Description

The Si3402B isolated evaluation board (Si3402BISO-EVB Rev 2) is a reference design for power supplies in Power over Ethernet (PoE) Powered Device (PD) applications. The Si3402B is described more completely in the data sheet and application notes. This document describes only the Si3402BISO-EVB evaluation board. An evaluation board demonstrating the non-isolated application is described in the Si3402B-EVB User's Guide.

2. Planning for Successful Designs

Silicon Labs strongly recommends the use of the schematic and layout databases provided with the evaluation boards as the starting point for your design. Use of external components other than those described and recommended in this document is generally discouraged. Refer to Table 2 on page 9 for more information on critical component specifications. Careful attention to the recommended layout guidelines is required to enable robust designs and full specification compliance. To help ensure design success, please submit your schematic and layout databases to www.silabs.com/support for review and feedback.

3. Si3402B Board Interface

Ethernet data and power are applied to the board through the RJ-45 connector (J1). The board itself has no Ethernet data transmission functionality, but, as a convenience, the Ethernet transformer secondary is brought out to the test points. Power may be applied in the following ways:

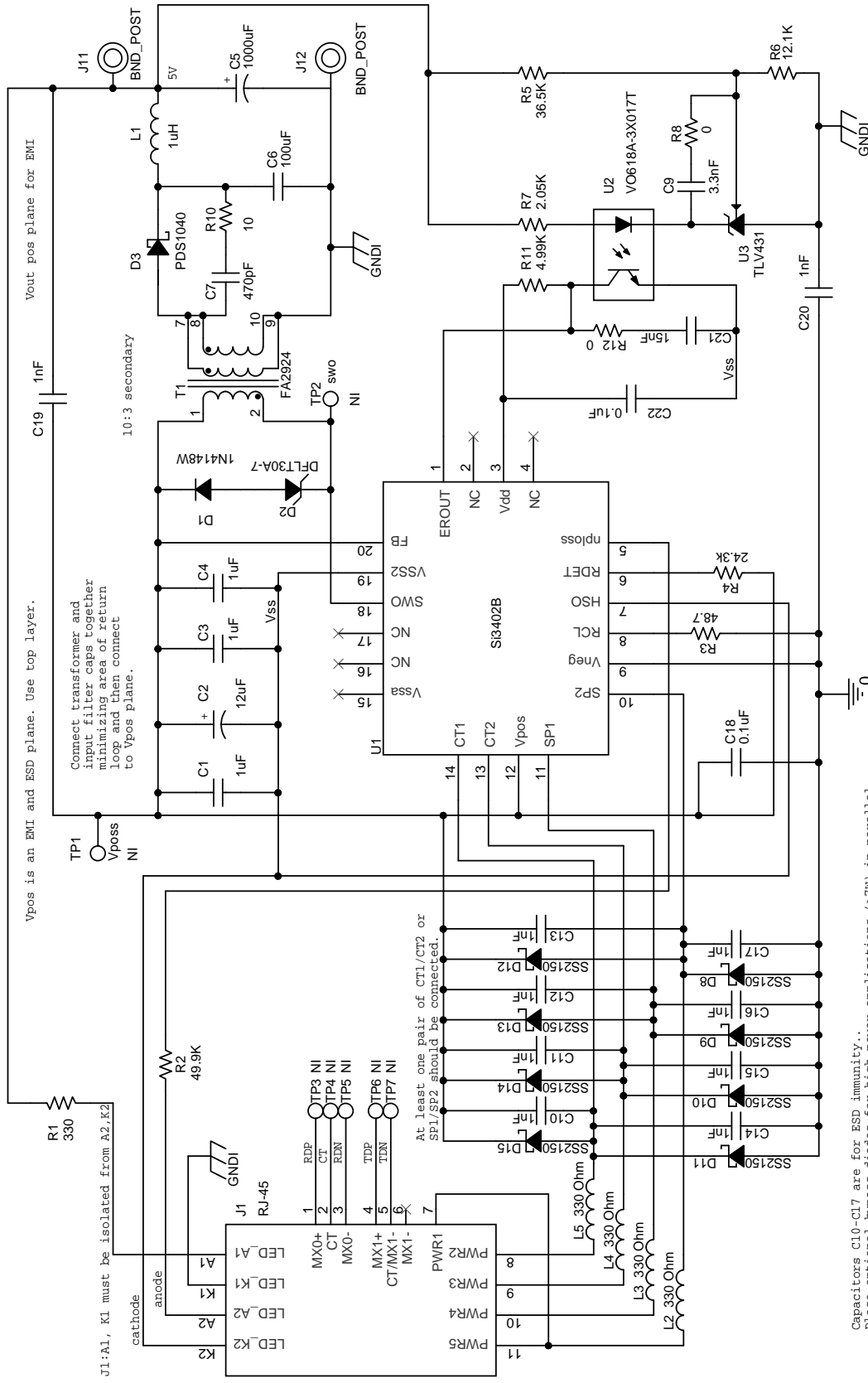
- Connecting a dc source to Pins 1, 2 and 3, 6 of the Ethernet cable (either polarity).
- Connecting a dc source to Pins 4, 5 and 7, 8 of the Ethernet cable (either polarity).
- Using an IEEE 802.3-2015-compliant, PoE-capable PSE, such as Trendnet TPE-1020WS.

The Si3402BISO-EVB board schematics and layout are shown in Figures 1 through 6.

The dc output is at connectors J11(+) and J12(-). Boards are generally shipped configured to produce +5 V output voltage but can be configured for +3.3 V or other output voltages as shown in Table 2 on page 9. The preconfigured Class 3 signature also can be modified according to Table 3 on page 10. The D8–D15 Schottky-type diode bridge bypass is recommended only for higher power levels (Class 3 operation). For lower power levels, such as Class 1 and Class 2, the diodes can be removed. When the Si3402B is used in external diode bridge configuration, it requires at least one pair of the CTx and SPx pins to be connected to the PoE voltage input terminals (to the input of the external bridge).

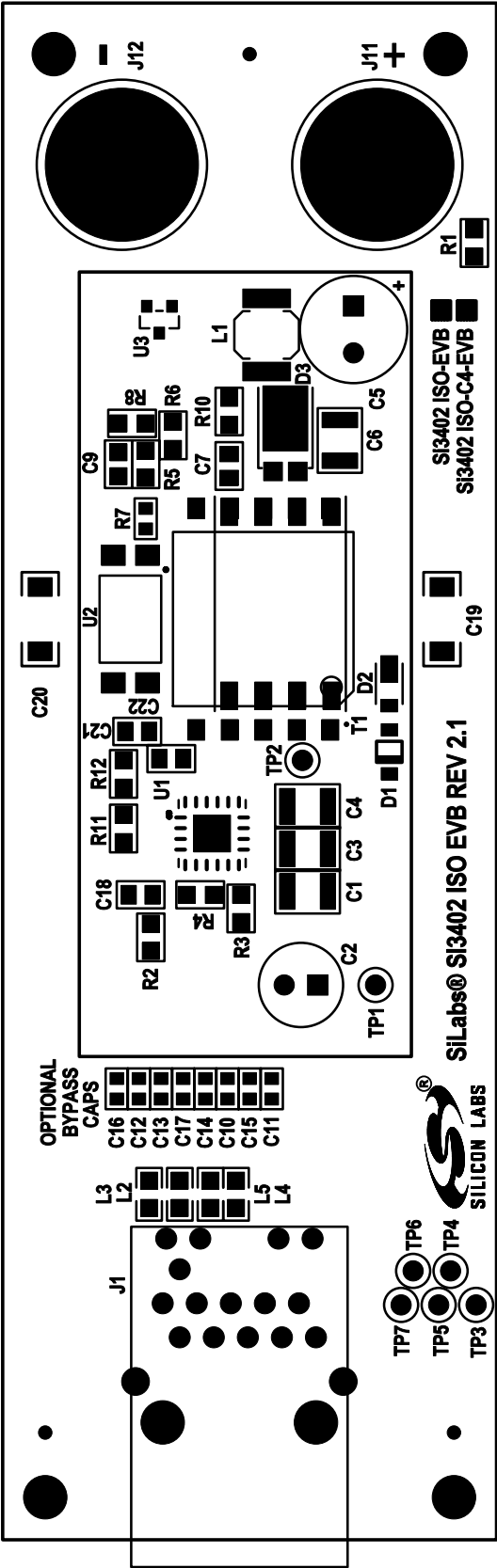
The feedback loop compensation has been optimized for 3.3, 5, 9, and 12 V output as well as with standard and low ESR capacitors in the output filter section (Table 2 on page 9). The use of low ESR capacitors is recommended for lower output ripple, improved load transient response and low temperature (below 0 °C) operation.

Si3402BISO-EVB



400 W Cesar Chavez St, Austin, TX
78701, United States

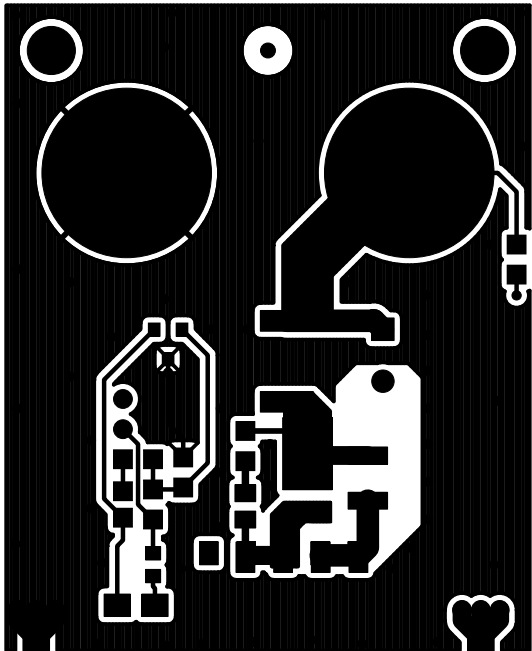
Figure 1. Si3402B Schematic—5 V, Class 3 PD



PRIMARY ASSEMBLY

PRIMARY SILKSCREEN

Figure 2. Si3402B Layout (Top Layer)



PRIMARY SIDE

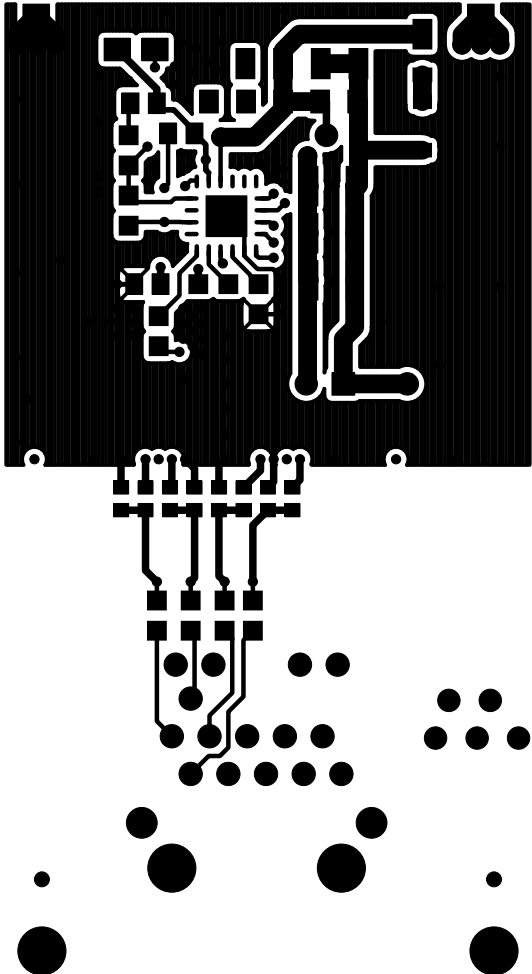
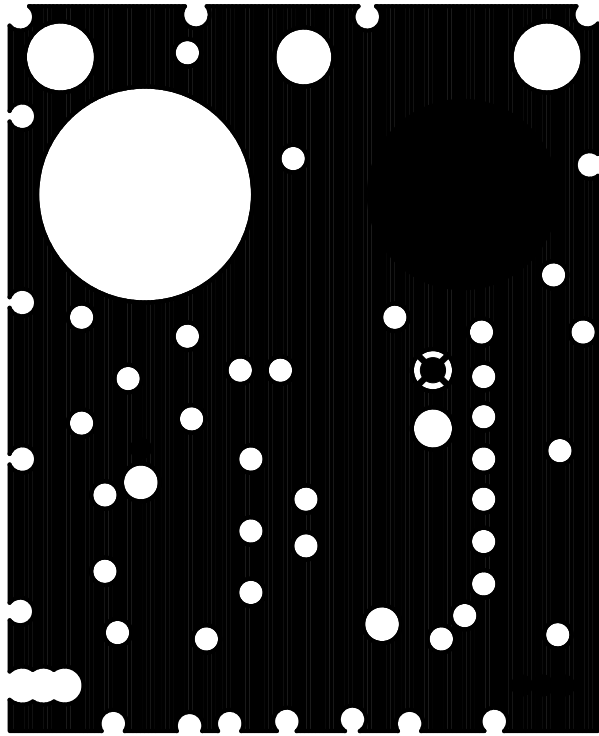


Figure 3. Primary Side (Layer 2)



INTERNAL 1

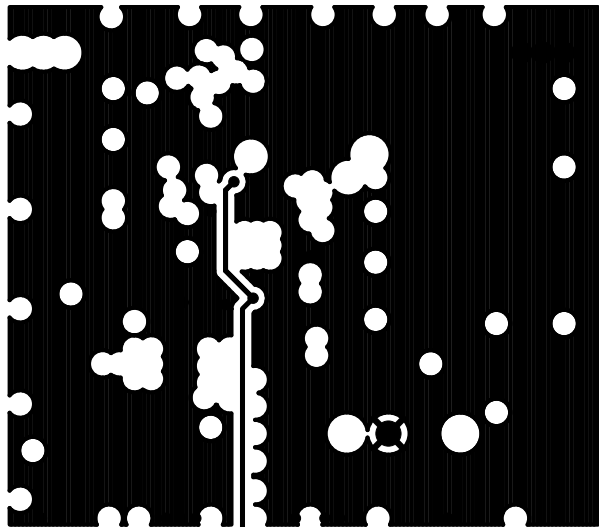
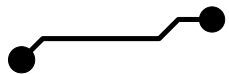
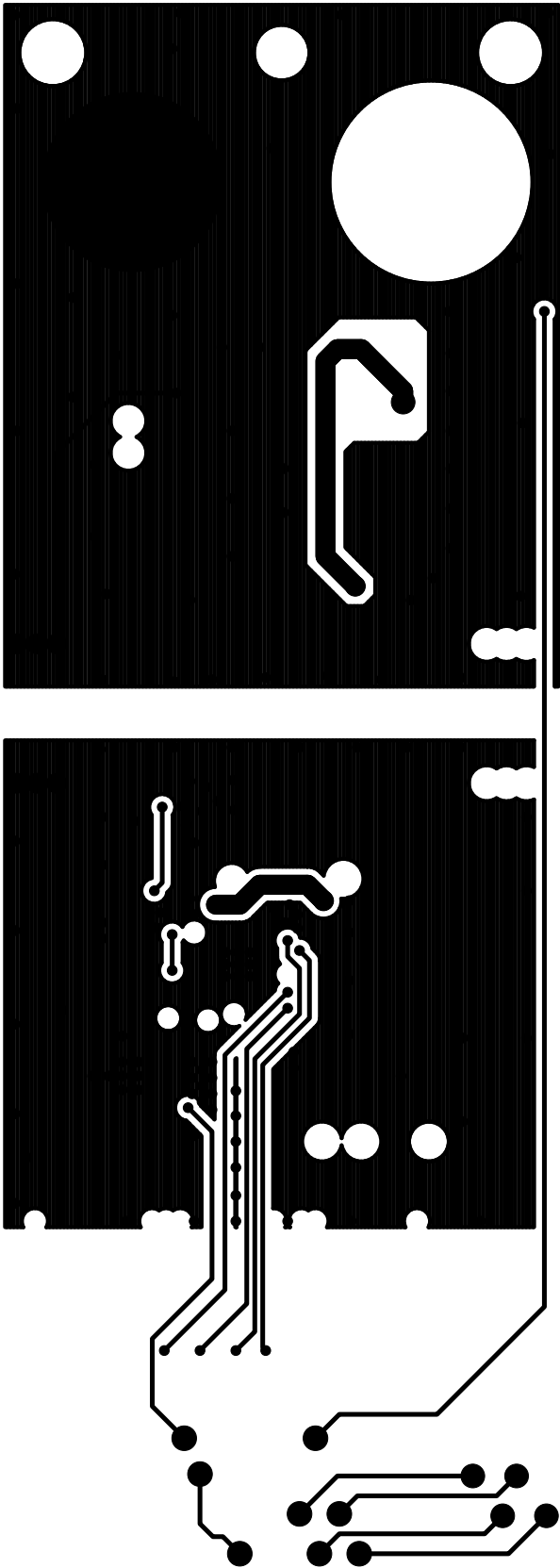


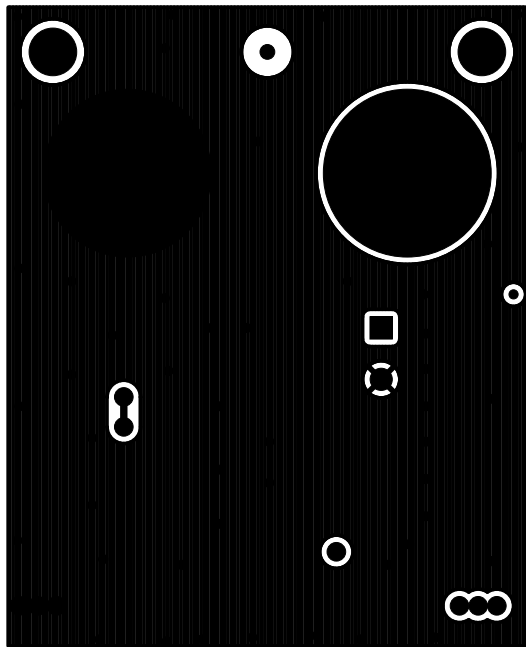
Figure 4. Internal 1 (Layer 3)





INTERNAL 2

Figure 5. Internal 2 (Layer 4)



SECONDARY SIDE

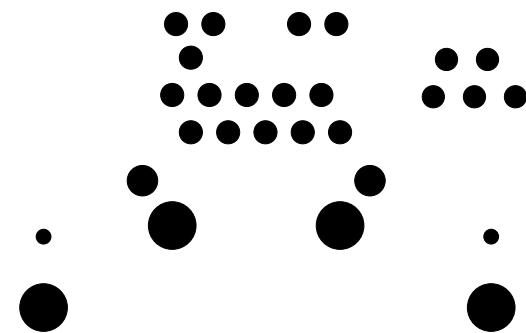
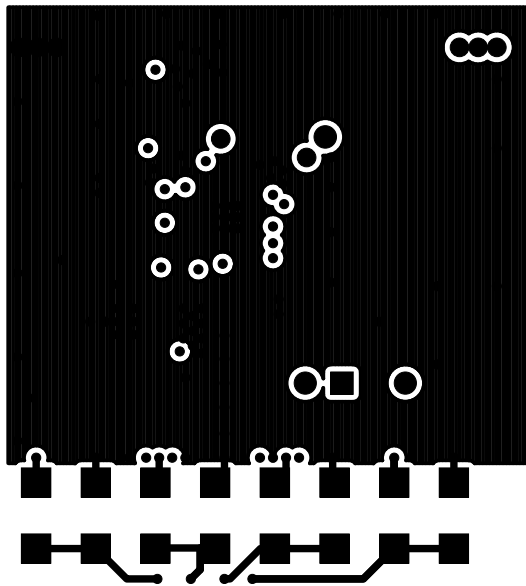


Figure 6. Secondary Side (Bottom Layer)

Si3402BISO-EVB

4. Bill of Materials

The following bill of materials is for a 5 V Class 3 design. For Class 1 and Class 2 designs, in addition to updating the classification resistor (R3), the external diode bridge (D8–D15) can be removed to reduce BOM costs. Tables 2 and 3 list changes to the bill of materials for other output voltages and classification levels. Refer to “AN956: Using the Si3402B PoE PD Controller in Isolated and Non-Isolated Designs” for more information.

Table 1. Si3402BISO-EVB Bill of Materials

| Qty | Value | Ref | Rating | Voltage | Tol | Type | PCB Footprint | Mfr Part Number | Mfr |
|---------------------------------|-----------------|--|---------|---------|-----------|------------|---------------------|------------------|----------------------|
| 3 | 1 μ F | C1, C3, C4 | | 100 V | \pm 10% | X7R | C1210 | C1210X7R101-105K | Venkel |
| 1 | 12 μ F | C2 | | 100 V | \pm 20% | Alum_Elec | C2.5X6.3MM-RAD | EEUFC2A120 | Panasonic |
| 1 | 1000 μ F | C5 | | 6.3 V | \pm 20% | Alum_Elec | C3.5X8MM-RAD | ECA0JM102 | Panasonic |
| 1 | 100 μ F | C6 | | 6.3 V | \pm 10% | X5R | C1210 | C1210X5R6R3-107K | Venkel |
| 1 | 470 pF | C7 | | 50 V | \pm 10% | X7R | C0805 | C0805X7R500-471K | Venkel |
| 1 | 3.3 nF | C9 | | 16 V | \pm 10% | X7R | C0805 | C0805X7R160-332K | Venkel |
| 8 | 1 nF | C10, C11, C12, C13, C14, C15, C16, C17 | | 100 V | \pm 10% | X7R | C0603 | C0603X7R101-102K | Venkel |
| 1 | 0.1 μ F | C18 | | 100 V | \pm 10% | X7R | C0805 | C0805X7R101-104K | Venkel |
| 2 | 1 nF | C19, C20 | | 3000 V | \pm 10% | X7R | C1808 | C1808X7R302-102K | Venkel |
| 1 | 15 nF | C21 | | 16 V | \pm 10% | X7R | C0805 | C0805X7R160-153K | Venkel |
| 1 | 0.1 μ F | C22 | | 16 V | \pm 10% | X7R | C0805 | C0805X7R160-104K | Venkel |
| 1 | 1N4148W | D1 | 2 A | 100 V | | Fast | SOD123 | 1N4148W | Diodes Inc |
| 1 | DFLT30A-7 | D2 | 4.65 A | 30 V | | Zener | POWERDI-123 | DFLT30A-7 | Diodes Inc. |
| 1 | PDS1040 | D3 | 10 A | 40 V | | Schottky | POWERDI-5 | PDS1040-13 | Diodes Inc. |
| 8 | SS2150 | D8, D9, D10, D11, D12, D13, D14, D15 | 2 A | 150 V | | Single | DO-214AC | SS2150-LTP | MCC |
| 1 | RJ-45 | J1 | | | | Receptacle | RJ45-SI-52004 | SI-52003-F | Bel |
| 2 | BND_POST | J11, J12 | 15 A | | | Banana | Banana-Jack | 101 | ABBATRON HH SMITH |
| 1 | 1 μ H | L1 | 2.9 A | | \pm 20% | Shielded | IND-6.6X4.45MM | DO1608C-102ML_ | Coilcraft |
| 4 | 330 Ω | L2, L3, L4, L5 | 1500 mA | | | SMT | L0805 | BLM21PG331SN1 | MuRata |
| 1 | 330 Ω | R1 | 1/10 W | | \pm 1% | ThickFilm | R0805 | CR0805-10W-3300F | Venkel |
| 1 | 49.9 k Ω | R2 | 1/10 W | | \pm 1% | ThickFilm | R0805 | CR0805-10W-4992F | Venkel |
| 1 | 48.7 Ω | R3 | 1/8 W | | \pm 1% | ThickFilm | R0805 | CRCW080548R7FKTA | Vishay |
| 1 | 24.3 k Ω | R4 | 1/8 W | | \pm 1% | ThickFilm | R0805 | CRCW080524K3FKEA | Vishay |
| 1 | 36.5 k Ω | R5 | 1/10 W | | \pm 1% | ThickFilm | R0805 | CR0805-10W-3652F | Venkel |
| 1 | 12.1 k Ω | R6 | 1/10 W | | \pm 1% | ThickFilm | R0805 | CR0805-10W-1212F | Venkel |
| 1 | 2.05 k Ω | R7 | 1/16 W | | \pm 1% | ThickFilm | R0603 | CR0603-16W-2051F | Venkel |
| 2 | 0 Ω | R8, R12 | 2 A | | | ThickFilm | R0805 | CR0805-10W-000 | Venkel |
| 1 | 10 Ω | R10 | 1/10 W | | \pm 1% | ThickFilm | R0805 | CR0805-10W-10R0F | Venkel |
| 1 | 4.99 k Ω | R11 | 1/10 W | | \pm 1% | ThickFilm | R0805 | CR0805-10W-4991F | Venkel |
| 1 | FA2924 | T1 | | | | | XFMR-FA2924 | FA2924-AL | Coilcraft |
| 1 | Si3402B | U1 | | 100 | | PD | QFN20N5X5P0.8 | Si3402B | Silicon Labs |
| 1 | VO618A-3X017T | U2 | | | | | SO4N10.16P2.54-AKEC | VO618A-3X017T | Vishay |
| 1 | TLV431 | U3 | | | | Shunt | TLV431-DBZ | TLV431BCDBZR | TI |
| Not Installed Components | | | | | | | | | |
| 7 | Black | TP1, TP2, TP3, TP4, TP5, TP6, TP7 | | | | Loop | Testpoint | 5001 | Keystone |

Table 2. Component Selection for other Output Voltages and Filter Types

| | | | | | | |
|---|---|------------------------|---|------------|--|---------------|
| 3.3 V Output | Transformer* EP10 FA2671 EP13FA2924AL | | Output Rectifier: PDS1040 Snubber: R10, C7 10 W, 470 pF | | Reference Any TLV431 | |
| | R5 R6 | C6 | C5 | Panasonic | R7, R8, R12 | C9,C21 |
| Standard ESR Output Filter | 24.3 k Ω 14.7 k Ω | 100 μ F X5R | 1000 μ F 6.3 V | ECA0JM102 | 500 Ω , 1.1 k Ω , 475 Ω | 10 nF, 33 nF, |
| Low ESR Output Filter | 24.3 k Ω 14.7 k Ω | 100 μ F X5R | 560 μ F 6.3 V | EEUFM0J561 | 324 Ω , 2 k Ω , 820 Ω | 10 nF, 100 nF |
| 5.0 V Output | Transformer* EP10 FA2671 EP13FA2924CL | | Output Rectifier PDS1040 Snubber: R10, C7 10 Ω , 470 pF | | Reference Any TLV431 | |
| | R5 R6 | C6 | C5 | Panasonic | R7, R8, R12 | C9, C21 |
| Standard ESR Output Filter | 36.5 k Ω 12.1 k Ω | 100 μ F X5R | 1000 μ F 6.3 V | ECA0JM102 | 2.05 k Ω , 0 Ω , 0 Ω | 3.3nF, 15 nF |
| Low ESR Output Filter | 36.5 k Ω 12.1 k Ω | 100 μ F X5R | 560 μ F 6.3 V | EEUFM0J561 | 2.05 k Ω , 0 Ω , 0 Ω | 3.3nF, 33 nF |
| 9.0 V Output | Transformer* EP10 FA2672 EP13FA2805CL | | Output Rectifier: PDS5100 Snubber: R10, C7 20 Ω , 68 pF | | Reference Higher voltage e.g., TLV431ASNT1G | |
| | R5 R6 | C6 | C5 | Panasonic | R1,R7, R8, R12 | C9,C21 |
| Standard ESR Output Filter | 66.5 k Ω 10.5 k Ω | 22 μ F X5R 16 V | 470 μ F 16 V | ECA1M471 | 1.3 k Ω , 3 k Ω , 0 Ω , 0 Ω | 10 nF, 15 nF |
| Low ESR Output Filter | 66.5 k Ω 10.5 k Ω | 22 μ F X5R 16 V | 330 μ F 16 V | EEUFM1C331 | 3 k Ω , 0 Ω , 0 Ω | 10 nF, 15 nF |
| 12.0 V Output | Transformer* EP10 FA2672 EP13FA2805CL | | Output rectifier: PDS5100 Snubber: R10, C7 20 Ω , 68 pF | | Reference Higher Voltage e.g., TLV431ASNT1G | |
| | R5 R6 | C6 | C5 | Panasonic | R1,R7, R8, R12 | C9,C21 |
| Standard ESR Output Filter | 88.7 k Ω 10.2 k Ω | 22 μ F X5R 16 V | 470 μ F 16 V | ECA1M471 | 1.3 k Ω , 3 k Ω , 0 Ω , 0 Ω | 10 nF, 15 nF |
| Low ESR Output Filter | 88.7 k Ω 10.2 k Ω | 22 μ F X5R 16 V | 330 μ F 16 V | EEUFM1C331 | 1.3 k Ω , 3 k Ω , 0 Ω , 0 Ω | 10 nF, 15 nF |
| *Note: Coilcraft part number. EP13 core is recommended for >10 W output power. | | | | | | |

Table 3. Component Selection for Different Classification Levels

| Class | R3 (1%) |
|--------------|----------------|
| 0 | Open |
| 1 | 140 |
| 2 | 75 |
| 3 | 45.3 |

APPENDIX—Si3402BISO DESIGN AND LAYOUT CHECKLIST

Introduction

Although all four EVB designs are preconfigured as Class 3 PDs with 5 V outputs, the schematics and layouts can easily be adapted to meet a wide variety of common output voltages and power levels.

The complete EVB design databases for the standard 5 V/Class 3 configuration are included in the EVB kit and can also be requested through Silicon Labs customer support at www.silabs.com/PoE under the “Documentation” link. Silicon Labs strongly recommends using these EVB schematics and layout files as a starting point to ensure robust performance and to help avoid common mistakes in the schematic capture and PCB layout processes.

Following are recommended design checklists that can assist in trouble-free development of robust PD designs:

Refer also to the Si3402B data sheet and AN956 when using the checklists below.

1. Design Planning Checklist:

- a. Silicon Labs strongly recommends using the EVB schematics and layout files as a starting point as you begin integrating the Si3402B into your system design process.
- b. Determine your load’s power requirements (i.e., V_{OUT} and I_{OUT} consumed by the PD, including the typical expected transient surge conditions). In general, to achieve the highest overall efficiency performance of the Si3402, choose the highest voltage used in your PD and then post regulate to the lower supply rails, if necessary.
- c. If your PD design consumes >7 W, make sure you bypass the Si3402’s on-chip diode bridges with external Schottky diode bridges or discrete Schottky diodes. Bypassing the Si3402’s on-chip diode bridges with external bridges or discrete diodes is required to help spread the heat generated in designs dissipating ≥ 7 W.
- d. Based on your required PD power level, select the appropriate class resistor value by referring to Table 3 of AN956. This sets the Rclass resistor (R3 in Figure 1 on page 2).
- e. The feedback loop stability has been checked over the entire load range for the specific component choices in Table 1. Low ESR filter capacitors will give better load transient response and lower output ripple so they are generally preferred. For the standard ESR capacitor, the ESR increase at very low temperatures may cause a loop stability issue. A typical evaluation board has been shown to exhibit instability under very heavy loads at -20 °C. Due to self-heating, this condition is not a great concern. However, using a low ESR filter capacitor solves this problem (but requires some recompensation of the feedback loop). Silicon Laboratories recommends against component substitution in the filtering and feedback path as this may result in unstable operation. Also, use care in situations that have additional capacitive loading as this will also affect loop stability.

2. General Design Checklist Items:

- a. ESD caps (C10–C17 in Figure 1) are strongly recommended for designs where system-level ESD (IEC6100-4-2) must provide >15 kV tolerance.
- b. If your design uses an AUX supply, make sure to include a $3\ \Omega$ surge limiting resistor in series with the AUX supply for hot insertion. Refer to AN956 when AUX supply is 48 V.
- c. Silicon Labs strongly recommends the inclusion of a minimum load (250 mW) to avoid switcher pulsing when no load is present, and to avoid false disconnection when less than 10 mA is drawn from the PSE. If your load is not at least 250 mW, add a resistor load to dissipate at least 250 mW.
- d. If using PLOSS function, make sure it’s properly terminated for connection in your PD subsystem. If PLOSS is not needed, leave this pin floating.

3. Layout Guidelines:

- a. Make sure the VNEG pin of the Si3402B is connected to the backside of the QFN package with an adequate thermal plane, as noted in the data sheet and AN956.
- b. Keep the trace length from connecting to SWO and retuning to Vss1 and Vss2 as short as possible. Make all of the power (high current) traces as short, direct, and thick as possible. It is a good practice on a standard PCB board to make the traces an absolute minimum of 15 mils (0.381 mm) per Ampere.
- c. Usually one standard via handles 200 mA of current. If the trace will need to conduct a significant amount of current from one plane to the other use multiple vias.
- d. Keep the circular area of the loop from the Switcher FET output to the inductor or transformer and returning from the input filter capacitors (C1–C4) to Vss2 as small a diameter as possible. Also, minimize the circular area of the loop from the output of the inductor or transformer to the Schottky diode and returning through the first stage output filter capacitor back to the inductor or transformer as small as possible. If possible, keep the direction of current flow in these two loops the same.
- e. Connect the sense points to the output terminals directly to avoid load regulation issues related to IR drops in the PCB traces. The sense points are the output side of R5 and Pin 3 of TLV431.
- f. Keep the feedback and loop stability components as far from the transformer/inductor and noisy power traces as possible.
- g. If the outputs have a ground plane or positive output plane, do not connect the high current carrying components and the filter capacitors through the plane. Connect them together and then connect to the plane at a single point.
- h. As a convenience in layout, please note that the IC is symmetrical with respect to CT1, CT2, SP1 and SP2. These leads can be interchanged. At least one pair of CT1/CT2 or SP1/SP2 should be connected.

To help ensure first pass success, please submit your schematics and layout files to www.silabs.com/support for review. Other technical questions may be submitted as well.

DOCUMENT CHANGE LIST

Revision 1.1 to Revision 1.2

- Initial release of Si3402BISO-EVB User's Guide, modified from Si3402-ISO-EVB User's Guide Revision 1.1.



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Silicon Laboratories Inc.
400 West Cesar Chavez
Austin, TX 78701
USA

<http://www.silabs.com>