Data Sheet
February 1998

microelectronics group

Lucent Technologies
Bell Labs Innovations

T7502 Dual PCM Codec with Filters

Features

- +5 V only
- Automatic powerdown mode
- Low-power, latch-up-free CMOS technology
- On-chip sample and hold, autozero, and precision voltage reference
- Differential architecture for high noise immunity and power supply rejection
- Automatic master clock frequency selection
- 2.048 MHz or 4.096 MHz fixed data rate
- Frame sync controlled channel swapping
- Differential analog I/O
- 300 Ω output drivers
- Operating temperature range: –40 °C to +85 °C
- A-law companding

Applications

- Speakerphone
- Telephone answering device (TAD)
- POTS for ISDN

Description

The T7502 device is a single-chip, two-channel A-law PCM codec with filters. This integrated circuit provides analog-to-digital and digital-to-analog conversion. It provides the transmit and receive filtering necessary to interface a voice telephone circuit to a time-division multiplexed (TDM) system. The device features a differential transmit amplifier, and the power receive amplifier is capable of driving 600 Ω differentially. PCM timing is defined by a single frame sync pulse. This device operates in a delayed timing mode (digital data is valid one clock cycle after frame sync goes high). The T7502 is packaged in a 20-pin SOJ.

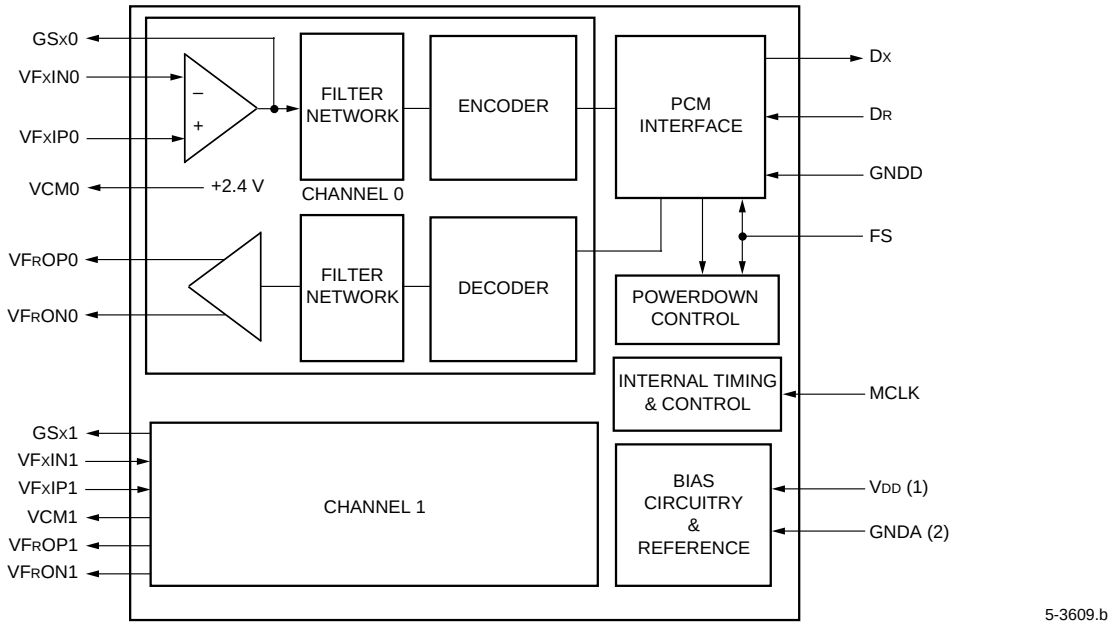


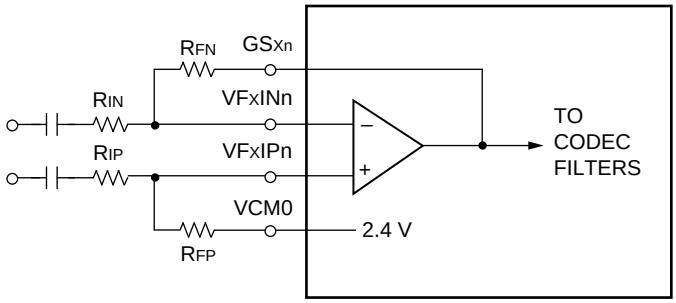
Figure 1. Block Diagram

Functional Description

The T7502 has one frame sync (FS) input that determines transmit and receive data timing for both channels. The width of the FS pulse determines the order of the two channels on the PCM buses. If FS is nominally one MCLK period wide (see Figure 5), the data for channel 0 is first. If FS is nominally two or more MCLK periods wide (Figure 6), the data for channel 1 is first. During a single 125 µs frame, the frame sync input is supplied a single pulse.

The frequency of the master clock must be either 2.048 MHz or 4.096 MHz. Internal circuitry determines the master clock frequency during the powerup reset interval.

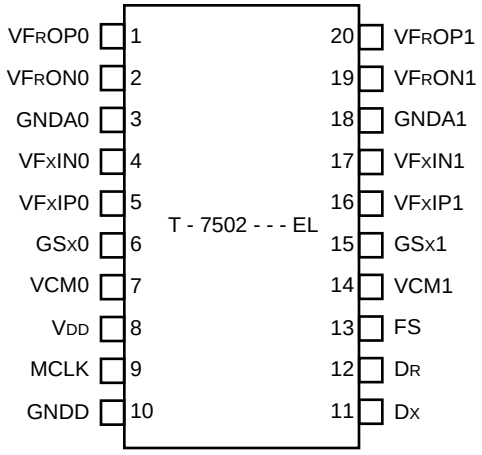
Powerdown is achieved by removing the FS pulse for at least 500 µs with MCLK active, after which MCLK may be removed. Both channels are powered down together. Powerdown is not guaranteed if MCLK is lost, unless the device is already in the powerdown mode.



5-3787

Figure 2. Typical Analog Input Section

Pin Information



5-3788.a

Figure 3. Pin Diagram

Pin Information (continued)

Table 1. Pin Descriptions

Symbol	Pin	Type	Name/Function
VFXIN1 VFXIN0	17 4	I	**Voice Frequency Transmitter Negative Input.** Analog inverting input to the uncommitted operational amplifier at the transmit filter input.
VFXIP1 VFXIP0	16 5	I	**Voice Frequency Transmitter Positive Input.** Analog noninverting input to the uncommitted operational amplifier at the transmit filter input.
GSX1 GSX0	15 6	O	**Gain Set for Transmitter.** Output of the transmit uncommitted operational amplifier. The pin is the input to the transmit differential filters.
VFROP1 VFROP0	20 1	O	**Voice Frequency Receiver Positive Output.** This pin can drive ≥300 Ω loads.
VFRON1 VFRON0	19 2	O	**Voice Frequency Receiver Negative Output.** This pin can drive ≥300 Ω loads.
VDD	8	—	**+5 V Power Supply**. This pin should be bypassed to analog ground with at least 0.1 µF of capacitance as close to the device as possible. VDD serves both analog and digital internal circuits.
GNDA1 GNDA0	18 3	—	**Analog Grounds**. Both ground pins must be connected on the circuit board. AGND serves both analog and digital internal circuits.
DR	12	I	**Receive PCM Data Input**. The data on this pin is shifted into the device on the falling edges of MCLK. Sixteen consecutive bits of data (8 bits for channel 0, and 8 bits for channel 1) are entered after the FS pulse has been detected.
DX	11	O	**Transmit PCM Data Output**. This pin remains in the high-impedance state except during active transmit time slots. Sixteen consecutive bits of data (8 bits for channel 0 and 8 bits for channel 1) are shifted out on the rising edge of MCLK. Data is shifted out on the rising edge of MCLK.
MCLK	9	I	**Master Clock Input**. The frequency must be 2.048 MHz or 4.096 MHz. This clock serves as the bit clock for all PCM data transfer. A 40% to 60% duty cycle is required.
GNDD	10	—	**Digital Ground**. Ground connection for the digital circuitry.
FS	13	I^{d}*	**Frame Sync**. This signal is an edge trigger and must be high for a minimum of one MCLK cycle. This signal must be derived from MCLK. If FS is low for 500 µs while MCLK remains active, then the device fully powers down. An internal pull-down device is included on FS.
VCM0 VCM1	7 14	O	**Voltage Common Mode**. 2.4 Vdc.

* I^{d} indicates a pull-down device is included on this lead.

Absolute Maximum Ratings

Stresses in excess of the absolute maximum ratings can cause permanent damage to the device. These are absolute stress ratings only. Functional operation of the device is not implied at these or any other conditions in excess of those given in the operational sections of this data sheet. Exposure to absolute maximum ratings for extended periods can adversely affect device reliability.

Parameter	Symbol	Min	Max	Unit
Storage Temperature Range	T_{stg}	–55	150	°C
Power Supply Voltage	V_{DD}	—	6.5	V
Voltage on Any Pin with Respect to Ground	—	–0.5	0.5 + V_{DD}	V
Maximum Power Dissipation (package limit)	P_D	—	600	mW

Handling Precautions

Although protection circuitry has been designed into this device, proper precautions should be taken to avoid exposure to electrostatic discharge (ESD) during handling and mounting. Lucent Technologies Microelectronics Group employs a human-body model (HBM) and a charged-device model (CDM) for ESD-susceptibility testing and protection design evaluation. ESD voltage thresholds are dependent on the circuit parameters used to define the model. No industry-wide standard has been adopted for CDM. However, a standard HBM (resistance = 1500 Ω, capacitance = 100 pF) is widely used and therefore can be used for comparison purposes. The HBM ESD threshold presented here was obtained by using these circuit parameters:

HBM ESD Threshold Voltage	
Device	**Rating**
T7502	>2000 V

Electrical Characteristics

Specifications apply for T_A = –40 °C to +85 °C, V_{DD} = 5 V ± 5%, MCLK = either 2.048 MHz or 4.096 MHz, and GND = 0 V, unless otherwise noted.

dc Characteristics

Table 2. Digital Interface

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Low Voltage	V_{IL}	All digital inputs	—	—	0.8	V
Input High Voltage	V_{IH}	All digital inputs	2.0	—	—	V
Output Low Voltage	V_{OL}	D_X, I_L = 3.2 mA	—	—	0.4	V
Output High Voltage	V_{OH}	D_X, I_L = –3.2 mA	2.4	—	—	V
		D_X, I_L = –320 µA	3.5	—	—	V
Input Current Pins Without Pull-down	I_I	Any digital input GND < V_{IN} < V_{DD}	–10	±0.01	10	µA
Input Current Pin with Pull-down	I_I	Any digital input GND < V_{IN} < V_{DD}	2	10	150	µA
Output Current in High-impedance State	I_{OZ}	D_X	–30	±0.02	30	µA
Input Capacitance	C_I	—	—	—	5	pF

Electrical Characteristics (continued)

dc Characteristics (continued)

Table 3. Power Dissipation

Power measurements are made at MCLK = 4.096 MHz, outputs unloaded.

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Powerdown Current	I_{DDO}	MCLK present and FS ≤ 0.4 V	—	0.1	1	mA
Powerup Current	I_{DDU}	MCLK, FS pulse present	—	18	25	mA

Transmission Characteristics

Table 4. Analog Interface

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Resistance, FSxI	R_{VFXI}	VFxI = 2.4 V	1.0	—	—	MΩ
Input Leakage Current, VFxI	I_{BVFXI}	VFxI = 2.4 V	–2.4	±0.01	2.4	µA
Input Capacitance, VFxIN, VFxIP	—	—		—	10	pF
Input Offset Voltage of Uncommitted Op Amp, VFxIN – VFxIP	—	—	–5	—	5	mV
Input Common-mode Voltage Range, VFxIN, VFxIP	—	—	1.2	—	V_{DD} – 1.75	V
Input Common-mode Rejection Ratio, VFxIN, VFxIP	—	—	—	60	—	dB
Gain Bandwidth Product (10 kHz) of Uncommitted Op Amp	—	—	—	3000	—	kHz
Equivalent Input Noise Between VFxIN and VFxIP at GSx	—	—	—	–30	—	dBrnC
Output Voltage Range, GSx	—	—	0.5	—	V_{DD} – 0.5	V
dc Open-loop Voltage Gain, GSx	A_{VOL}	—	90	—	—	dB
Differential Output dc Offset Voltage	—	—	–80	±10	80	mV
Load Capacitance, GSx	CL_{X1}	—	—	—	50	pF
Load Resistance, GSx	RL_{X1}	—	10	—	—	kΩ
VCM Output Voltage Referenced to GND	—	—	2.25	2.35	2.5	V
VCM Output Load Capacitance	—	—	0	—	50	pF
Load Resistance, V_{CM}	RL_{VCM}	—	10	—	—	kΩ
Load Resistance, VFRO	RL_{VFRO}	—	300	—	—	Ω
Load Capacitance, VFRO	CL_{VFRO}	—	—	—	100	pF
Output Resistance, VFRO	RO_{VFRO}	0 dBm0, 1020 Hz PCM code applied to D_R	—	0.3	3	Ω
Output Voltage, VFRO	VO_R	Alternating ± zero A-law PCM code applied to D_R	2.25	2.35	2.5	V
Output Leakage Current, VFRO, Powerdown	IO_{VFRO}	—	–30	±0.02	30	µA
Output Voltage Swing, VFRO	V_{SWR}	RL = 300 Ω	3.2	—	—	Vp-p

Transmission Characteristics (continued)

ac Transmission Characteristics

Unless otherwise noted, the analog input is a 0 dBm0, 1020 Hz sine wave; the input amplifier is set for unity gain. The digital input is a PCM bit stream equivalent to that obtained by passing a 0 dBm0, 1020 Hz sine wave through an ideal encoder. The output level is sin(x)/x-corrected.

Table 5. Absolute Gain

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Encoder Milliwatt Response (transmit gain tolerance)	EmW	Signal input of 0.775 Vrms A-law	–0.25	—	0.25	dBm0
Decoder Milliwatt Response (receive gain tolerance)	DmW	Measured single-ended relative to 0.775 Vrms A-law, PCM input of 0 dBm0 1020 Hz RL = 10 kΩ	–0.25	—	0.25	dBm0

Table 6. Gain Tracking

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Transmit Gain Tracking Error Sinusoidal Input	GT_X	+3 dBm0 to –37 dBm0 –37 dBm0 to –50 dBm0	–0.25 –0.50	— —	0.25 0.50	dB dB
Receive Gain Tracking Error Sinusoidal Input	GT_R	+3 dBm0 to –37 dBm0 –37 dBm0 to –50 dBm0	–0.25 –0.50	— —	0.25 0.50	dB dB

Table 7. Distortion

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Transmit Signal to Distortion	SD_X	A-law +3 dBm0 ≤ VF_XI ≤ –30 dBm0	35	—	—	dB
		A-law –30 dBm0 ≤ VF_XI ≤ –40 dBm0	29	—	—	dB
		A-law –40 dBm0 ≤ VFxI ≤ –45 dBm0	25	—	—	dB
Receive Signal to Distortion	SD_R	A-law +3 dBm0 ≤ VF_RO ≤ –30 dBm0	35	—	—	dB
		A-law –30 dBm0 ≤ VF_RO ≤ –40 dBm0	29	—	—	dB
		A-law –40 dBm0 ≤ VF_RO ≤ –45 dBm0	25	—	—	dB
Single Frequency Distortion, Transmit	SFD_X	200 Hz—3400 Hz, 0 dBm0 input, output any other single frequency ≤ 3400 Hz	—	—	–38	dBm0
Single Frequency Distortion, Receive	SFD_R	200 Hz—3400 Hz, 0 dBm0 input, output any other single frequency ≤ 3400 Hz	—	—	–40	dBm0
Intermodulation Distortion	IMD	Transmit or receive, two frequencies in the range (300 Hz—3400 Hz) at –6 dBm0	—	—	–42	dBm0

Transmission Characteristics (continued)

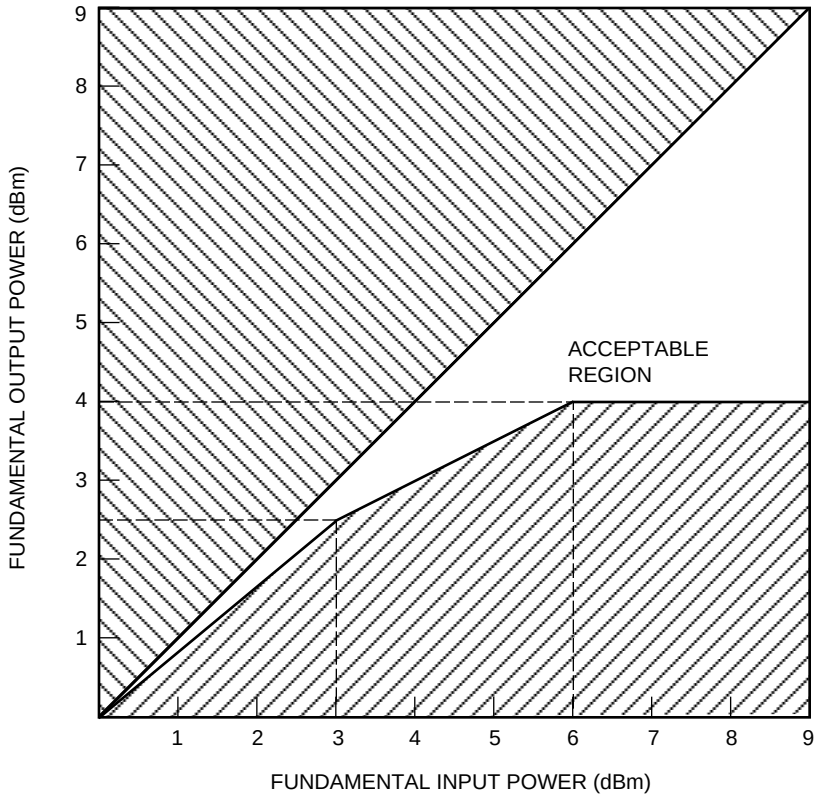
ac Transmission Characteristics (continued)

Table 8. Envelope Delay Distortion

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
TX Delay, Absolute	D_{XA}	f = 1600 Hz	—	—	230	µs
TX Delay, Relative to 1600 Hz	D_{XR}	f = 500 Hz—600 Hz f = 600 Hz—800 Hz f = 800 Hz—1000 Hz f = 1000 Hz—1600 Hz f = 1600 Hz—2600 Hz f = 2600 Hz—2800 Hz f = 2800 Hz—3000 Hz	— — — — — — —	— — — — — — —	220 145 75 40 75 105 155	µs µs µs µs µs µs µs
RX Delay, Absolute	D_{RA}	f = 1600 Hz	—	—	275	µs
RX Delay, Relative to 1600 Hz	D_{RR}	f = 500 Hz—1000 Hz f = 1000 Hz—1600 Hz f = 1600 Hz—2600 Hz f = 2600 Hz—2800 Hz f = 2800 Hz—3000 Hz	–40 –30 — — —	— — — — —	— — 90 125 175	µs µs µs µs µs
Round Trip Delay, Absolute	D_{RTA}	With or between channels f = 1600 Hz	—	—	470	µs

Overload Compression

Figure 4 shows the region of operation for encoder signal levels above the reference input power (0 dBm0).



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Figure 4. Overload Compression

Transmission Characteristics (continued)

ac Transmission Characteristics (continued)

Table 9. Noise

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Transmit Noise, A-Law	N_{Xp}	Input amplifier gain = 36 dB	—	–68.5	–68	dBm0p
Receive Noise, A-Law	N_{Rp}	PCM code is A-law positive one.	—	–82	–75	dBm0p
Noise, Single Frequency	N_{RS}	f = 0 kHz—100 kHz, VF_XIN = 0 Vrms, measurement at VF_RO, $D_R = D_X$	—	—	–53	dBm0
Power Supply Rejection Transmit	PSR_X	V_{DD} = 5.0 Vdc + 100 mVrms: f = 0 kHz—4 kHz f = 4 kHz—50 kHz	 36 30	 — —	 — —	 dB dB
Power Supply Rejection Receive	PSR_X	PCM code is positive one LSB. V_{DD} = 5.0 Vdc + 100 mVrms: f = 0 kHz—4 kHz f = 4 kHz—25 kHz f = 25 kHz—50 kHz	 36 40 30	 — — —	 — — —	 dB dB dB
Spurious Out-of-Band Signals at VF_RO Relative to Input	SOS	0 dBm0, 300 Hz—3400 Hz input PCM code applied: 4600 Hz—7600 Hz 7600 Hz—8400 Hz 8400 Hz—50 kHz	 — — —	 — — —	 –30 –40 –30	 dB dB dB

Table 10. Receive Gain Relative to Gain at 1.02 kHz

Frequency (Hz)	Min	Typ	Max	Unit
Below 3000	–0.150	±0.04	0.150	dB
3140	–0.570	±0.04	0.150	dB
3380	–0.735	–0.50	0.010	dB
3860	—	–10.70	–9.400	dB
4600 and above	—	—	–28	dB

Table 11. Transmit Gain Relative to Gain at 1.02 kHz

Frequency (Hz)	Min	Typ	Max	Unit
16.67	—	–50	–30	dB
40	—	–34	–26	dB
50	—	–36	–30	dB
60	—	–50	–30	dB
200	–1.800	–0.5	0	dB
300 to 3000	–0.150	±0.04	0.150	dB
3140	–0.570	±0.04	0.150	dB
3380	–0.735	–0.50	0.010	dB
3860	—	–10.70	–9.400	dB
4600 and above	—	—	–32	dB

Transmission Characteristics (continued)

ac Transmission Characteristics (continued)

Table 12. Interchannel Crosstalk (Between Channels) R_F = ≤400 kΩ*

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Transmit to Receive Crosstalk 0 dBm0 Transmit Levels	CT_{XX-RY}	f = 300 Hz—3400 Hz idle PCM code for channel under test; 0 dBm0 into any other single-channel VF_XIN	—	—	–75	dB
Receive to Transmit Crosstalk 0 dBm0 Receive Levels	CT_{RX-XY}	f = 300 Hz—3400 Hz VF_XIN = 0 Vrms for channel under test; 0 dBm0 code level on any other single-channel D_R	—	—	–75	dB
Transmit to Transmit Crosstalk 0 dBm0 Transmit Levels	CT_{XX-XY}	f = 300 Hz—3400 Hz 0 dBm0 applied to any single-channel VF_XIN except channel under test, which has VF_XIN = 0 Vrms	—	—	–75	dB
Receive to Receive Crosstalk 0 dBm0 Receive Levels	CT_{RX-RY}	f = 300 Hz—3400 Hz 0 dBm0 code level on any single-channel D_R except channel under test which has idle code applied	—	—	–75	dB

* For Table 12, crosstalk into the transmit channels (VF_XIN) can be significantly affected by parasitic capacitive feeds from GS_X and VF_RO outputs. PWB layouts should be arranged to keep these parasitics low. The resistor value of RF (from GS_X to VF_XIN) should also be kept as low as possible (while maintaining the load on GS_X above 10 kΩ per Table 4) to minimize crosstalk.

Table 13. Intrachannel Crosstalk (Within Channels) R_F = ≤400 kΩ*

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Transmit to Receive Crosstalk 0 dBm0 Transmit Levels	CT_{XX-RX}	f = 300 Hz—3400 Hz idle PCM code for channel under test; 0 dBm0 into VF_XIN	—	—	–65	dB
Receive to Transmit Crosstalk 0 dBm0 Receive Levels	CT_{RX-XX}	f = 300 Hz—3400 Hz VF_XIN = 0 Vrms for channel under test; 0 dBm0 code level on D_R	—	—	–65	dB

* For Table 13, crosstalk into the transmit channels (VF_XIN) can be significantly affected by parasitic capacitive feeds from GS_X and VF_RO outputs. PWB layouts should be arranged to keep these parasitics low. The resistor value of RF (from GS_X to VF_XIN) should also be kept as low as possible (while maintaining the load on GS_X above 10 kΩ per Table 4) to minimize crosstalk.

Timing Characteristics

Table 14. Clock Section (See Figures 5 and 6.)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
tMCHMCL1	Clock Pulse Width	—	97	—	—	ns
tCDC	Duty Cycle, MC	—	40	—	60	%
tMCH1MCH2 tMCL2MCL1	Clock Rise and Fall Time	—	0	—	15	ns

Table 15. Transmit Section (See Figures 5 and 6.)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
tMCHDV	Data Enabled on TS Entry	$0 < C_{LOAD} < 100$ pF	0	—	60	ns
tMCHDV1	Data Delay from MC	$0 < C_{LOAD} < 100$ pF	0	—	60	ns
tMCHDZ*	Data Float on TS Exit	$C_{LOAD} = 0$	10	—	100	ns
tFSHMCL	Frame-sync Hold Time	—	50	—	—	ns
tMCLFSH	Frame-sync High Setup	—	50	—	—	ns
tFSLMCL	Frame-sync Low Setup	—	50	—	—	ns

* Timing parameter tMCHDZ is referenced to a high-impedance state.

Table 16. Receive Section (See Figures 5 and 6.)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
tDVMCL	Receive Data Setup	—	30	—	—	ns
tMCLDV	Receive Data Hold	—	15	—	—	ns

Timing Characteristics (continued)

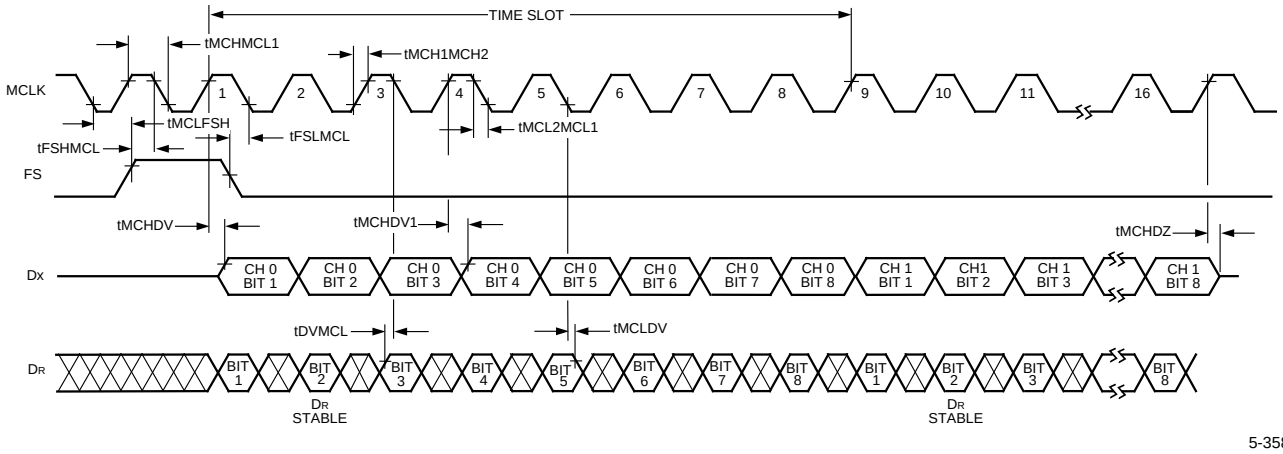


Figure 5. Short FS Transmit and Receive Timing (Channel 0 First)

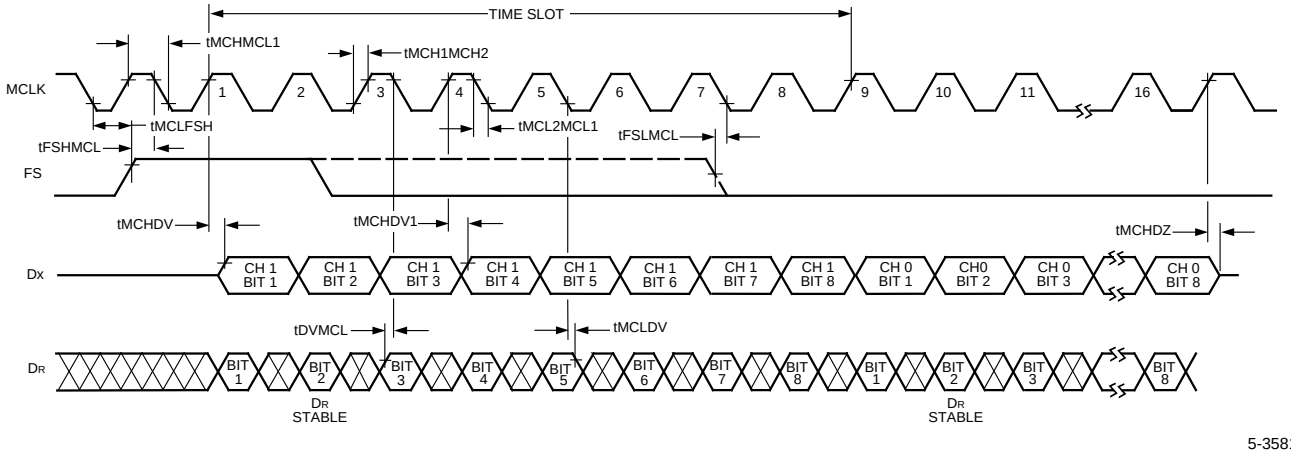


Figure 6. Long FS Transmit and Receive Timing (Channel 1 First)

Applications

Figure 7 shows one possible analog connection. Fully differential structures used for the inputs minimize the noise gain from the internal 2.4 V bias voltage to the output of the single-ended transmitter op amp. The forward path gain is G, and by using resistors on the positive side that are a factor of 1/(2G + 1) of those on the negative side, the microphone and transformer feeds are kept well balanced. Using this ratio, G can be as low as unity (0 dB) without exceeding the common-mode limit of the op amp.

Users have wide latitude when selecting between a balanced amplifier configuration or a single-ended configuration. Single-ended configurations usually need fewer external components (e.g., $R_{IP} = \infty$ and $R_{FP} = 0$ in Figure 2) but have two disadvantages: one, dc blocking from the source is typically required; two, internally generated noise at the common-mode pin VCM0 or VCM1 is amplified by G. For G > 10 (20 dB), this noise gain can become the factor that could limit performance. Single-ended configurations can be used even with microphones and transformers ($R_{IP} = 0$ in these cases), but parasitic issues become somewhat more complex; so single-ended configurations are only suggested for gains of four (12 dB) or less.

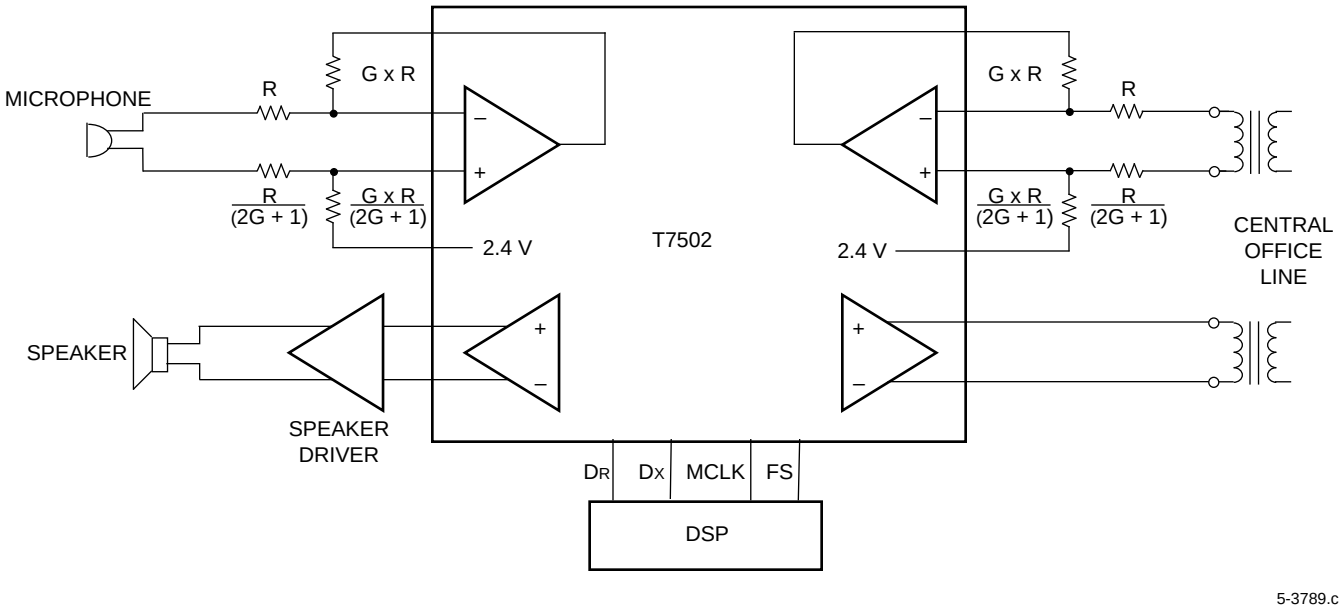
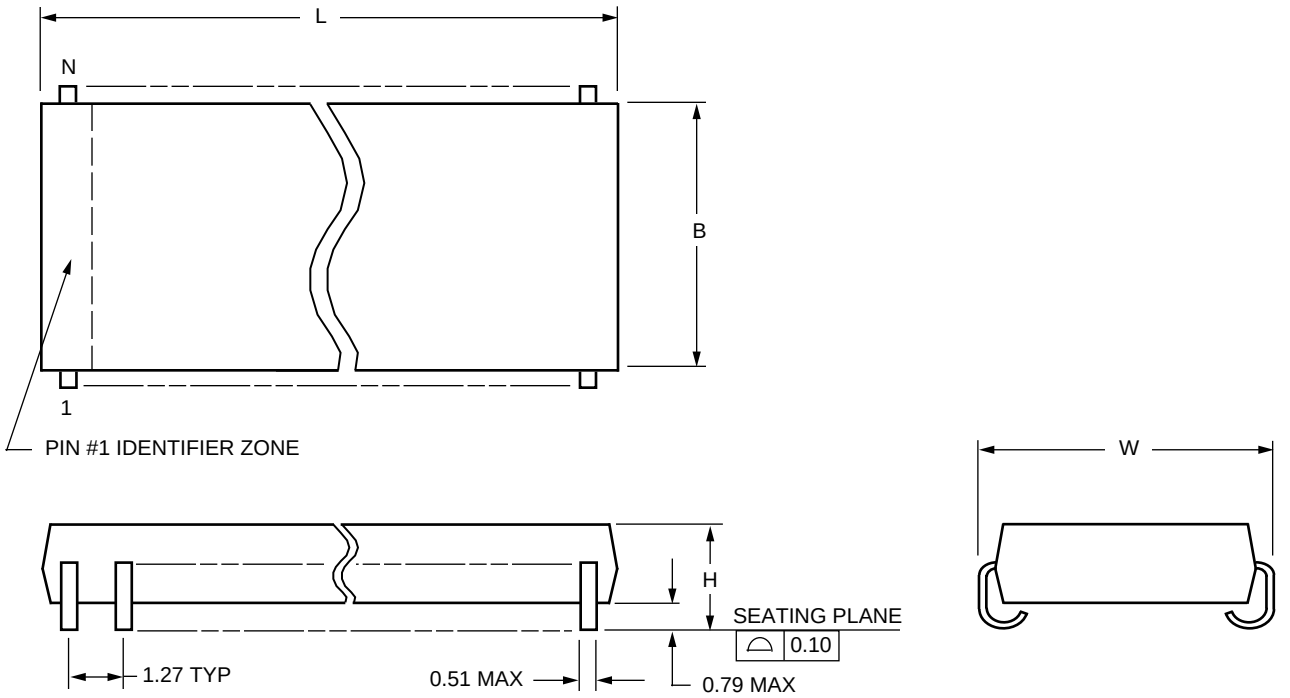


Figure 7. Typical T7502 Application

Outline Diagram

20-Pin SOJ

Controlling dimensions are in inches.



5-4413r4

Package Description	Package Dimensions				
	Number of Pins (N)	Maximum Length (L)	Maximum Width Without Leads (B)	Maximum Width Including Leads (W)	Maximum Height Above Board (H)
SOJ (Small Outline, J-Lead)	20	12.95	7.62	8.81	3.18

Ordering Information

Device Code	Package	Temperature	Comcode
T - 7502 - - - EL	20-Pin SOJ	–40 °C to +85 °C	107622888

Notes

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