Data Sheet April 1999 File Number 4079.1

15A, 60V, 0.065 Ohm, ESD Rated, Logic Level, N-Channel Power MOSFETs

These are N-Channel power MOSFETs manufactured using the MegaFET process. This process, which uses feature sizes approaching those of LSI circuits, gives optimum utilization of silicon, resulting in outstanding performance. They were designed for use in applications such as switching regulators, switching converters, motor drivers, and relay drivers. These transistors can be operated directly from integrated circuits.

Formerly developmental type TA49165.

Ordering Information

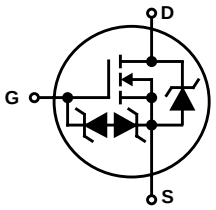
PART NUMBER	PACKAGE	BRAND
RFD15N06LE	TO-251AA	F15N6L
RFD15N06LESM	TO-252AA	F15N6L

NOTE: When ordering, use the entire part number. For ordering in tape and reel, add the suffix 9A to the part number, i.e. RFD15N06LESM9A.

Features

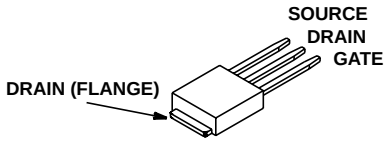
- 15A, 60V
- $r_{DS(ON)} = 0.065\Omega$
- 2kV ESD Protected
- Temperature Compensating PSPICE™ Model
- Peak Current vs Pulse Width Curve
- UIS Rating Curve
- $175^{o}C$ Operating Temperature
- Related Literature
  - TB334 “Guidelines for Soldering Surface Mount Components to PC Boards”

Symbol

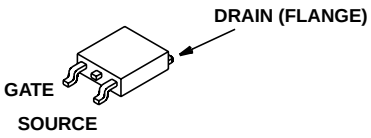


Packaging

JEDEC TO-251AA



JEDEC TO-252AA



CAUTION: These devices are sensitive to electrostatic discharge; follow proper ESD Handling Procedures.
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Absolute Maximum Ratings $T_C = 25^oC$, Unless Otherwise Specified

		RFD15N06LE, RFD15N06LESM	UNITS
Drain to Source Voltage (Note 1)	V_{DSS}	60	V
Drain to Gate Voltage (R_{GS} = 20kΩ) (Note 1)	V_{DGR}	60	V
Gate to Source Voltage	V_{GS}	±10	V
Continuous Drain Current	I_D	15	A
Pulsed Drain Current (Note 3)	I_{DM}	Refer to Peak Current Curve	
Pulsed Avalanche Rating	E_{AS}	Refer to UIS Curve	
Power Dissipation	P_D	72	W
Derate above 25^oC		0.48	$W/^oC$
Operating and Storage Temperature	T_J, T_{STG}	-55 to 175	^oC
Electrostatic Discharge Rating MIL-STD-883, Category B(2)	ESD	2	kV
Maximum Temperature for Soldering			
Leads at 0.063in (1.6mm) from Case for 10s	T_L	300	^oC
Package Body for 10s, See Techbrief 334	T_{pkg}	260	^oC

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. $T_J = 25^oC$ to 150^oC.

Electrical Specifications $T_C = 25^oC$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Drain to Source Breakdown Voltage	BV_{DSS}	I_D = 250μA, V_{GS} = 0V, Figure 13		60	-	-	V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{GS} = V_{DS}, I_D = 250μA, Figure 12		1	-	2	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 48V, V_{GS} = 0V	$T_C = 25^oC$	-	-	1	μA
			$T_C = 150^oC$	-	-	50	μA
Gate to Source Leakage Current	I_{GSS}	V_{GS} = ±10V		-	-	10	μA
Drain to Source On Resistance	$r_{DS(ON)}$	I_D = 15A, V_{GS} = 5V		-	-	0.065	Ω
Turn-On Time	t_{ON}	V_{DD} = 30V, I_D = 15A, R_L = 2.0Ω, V_{GS} = 5V, R_{GS} = 2.5Ω Figures 10, 18, 19		-	-	77	ns
Turn-On Delay Time	$t_{d(ON)}$			-	11	-	ns
Rise Time	t_r			-	40	-	ns
Turn-Off Delay Time	$t_{d(OFF)}$			-	30	-	ns
Fall Time	t_f			-	18	-	ns
Turn-Off Time	t_{OFF}			-	-	75	ns
Total Gate Charge	$Q_{g(TOT)}$	V_{GS} = 0V to 10V	V_{DD} = 48V, I_D = 15A, R_L = 3.20Ω Figures 20, 21	-	39	49	nC
Gate Charge at 5V	$Q_{g(5)}$	V_{GS} = 0V to 5V		-	21	26	nC
Threshold Gate Charge	$Q_{g(TH)}$	V_{GS} = 0V to 1V		-	0.95	1.20	nC
Input Capacitance	C_{ISS}	V_{DS} = 25V, V_{GS} = 0V, f = 1MHz Figure 14		-	855	-	pF
Output Capacitance	C_{OSS}			-	240	-	pF
Reverse Transfer Capacitance	C_{RSS}			-	75	-	pF
Thermal Resistance Junction to Case	$R_{\theta JC}$			-	-	2.08	$^oC/W$
Thermal Resistance Junction to Ambient	$R_{\theta JA}$	TO-251 and TO-252		-	-	100	$^oC/W$

Source to Drain Diode Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Source to Drain Diode Voltage	V_{SD}	I_{SD} = 15A	-	-	1.5	V
Diode Reverse Recovery Time	t_{rr}	I_{SD} = 15A, dI_{SD}/dt = 100A/μs	-	-	80	ns

NOTES:

2. Pulse Test: Pulse Width ≤ 300ms, Duty Cycle ≤ 2%.
3. Repetitive Rating: Pulse Width limited by max junction temperature. See Transient Thermal Impedance Curve (Figure 3) and Peak Current Capability Curve (Figure 5).

Typical Performance Curves Unless Otherwise Specified

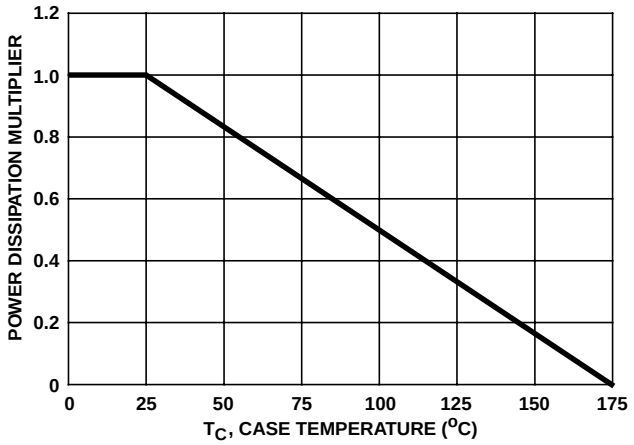


FIGURE 1. NORMALIZED POWER DISSIPATION vs CASE TEMPERATURE

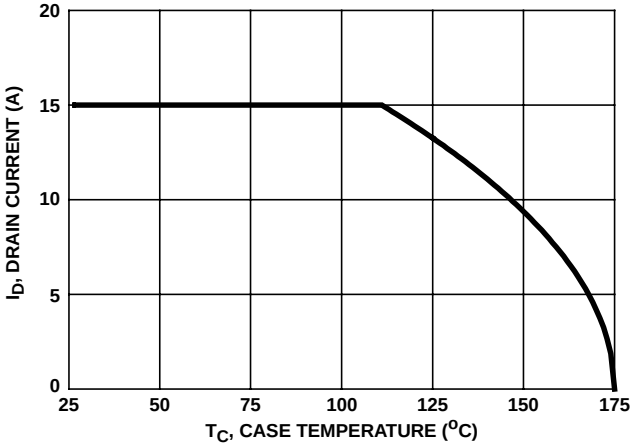


FIGURE 2. MAXIMUM CONTINUOUS DRAIN CURRENT vs CASE TEMPERATURE

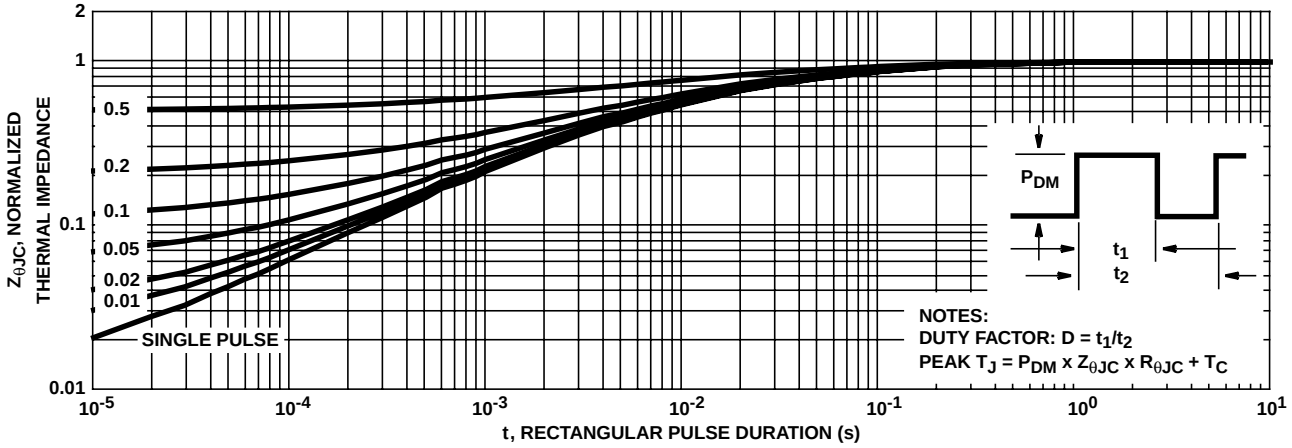


FIGURE 3. NORMALIZED MAXIMUM TRANSIENT THERMAL IMPEDANCE

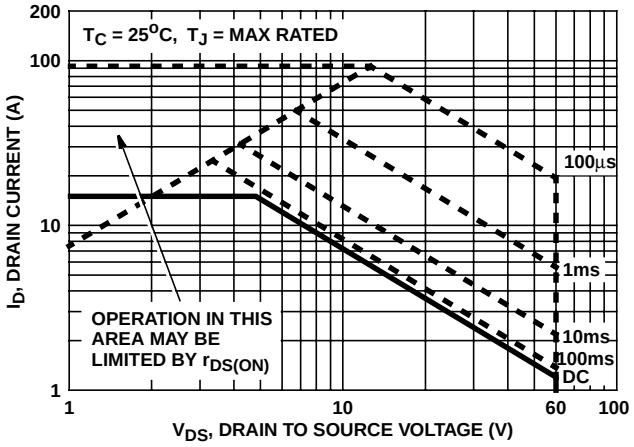


FIGURE 4. FORWARD BIAS SAFE OPERATING AREA

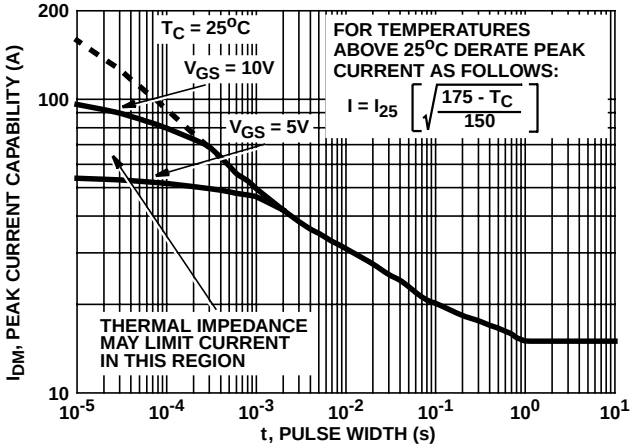
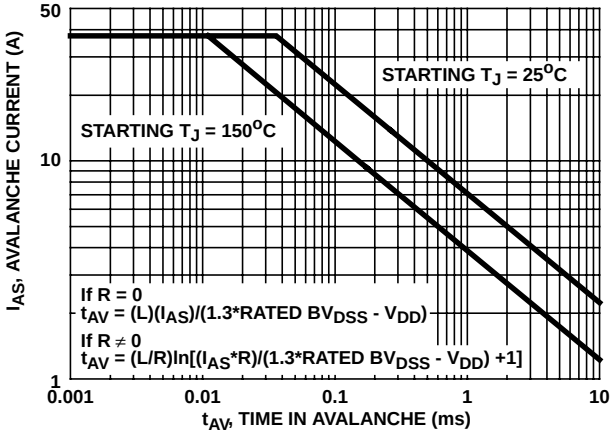


FIGURE 5. PEAK CURRENT CAPABILITY

Typical Performance Curves Unless Otherwise Specified **(Continued)**



NOTE: Refer to Intersil Application Notes AN9321 and AN9322.

FIGURE 6. UNCLAMPED INDUCTIVE SWITCHING

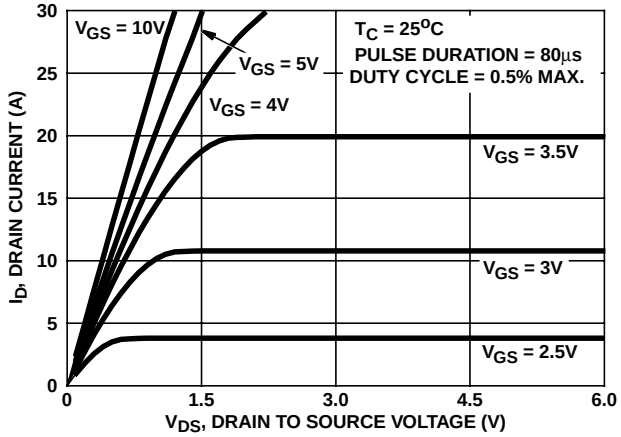


FIGURE 7. SATURATION CHARACTERISTICS

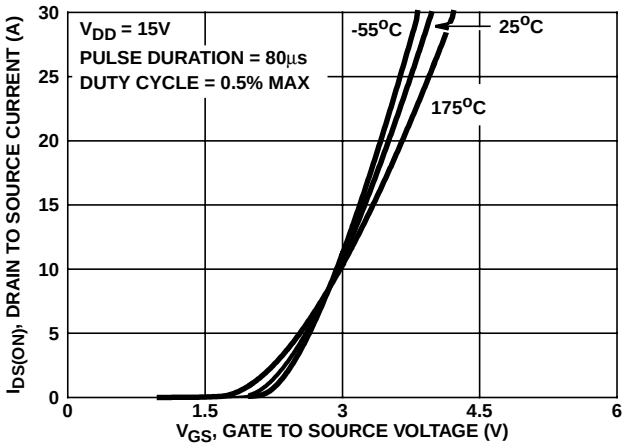


FIGURE 8. TRANSFER CHARACTERISTICS

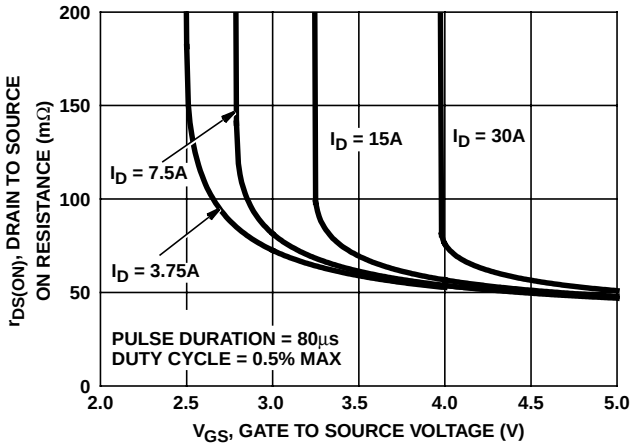


FIGURE 9. DRAIN TO SOURCE ON RESISTANCE vs GATE VOLTAGE AND DRAIN CURRENT

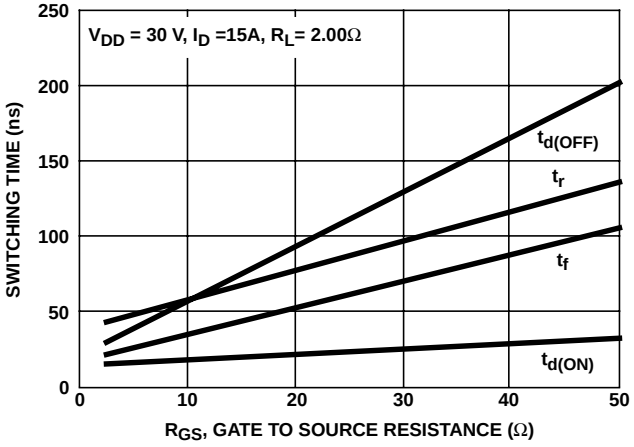


FIGURE 10. SWITCHING TIME vs GATE RESISTANCE

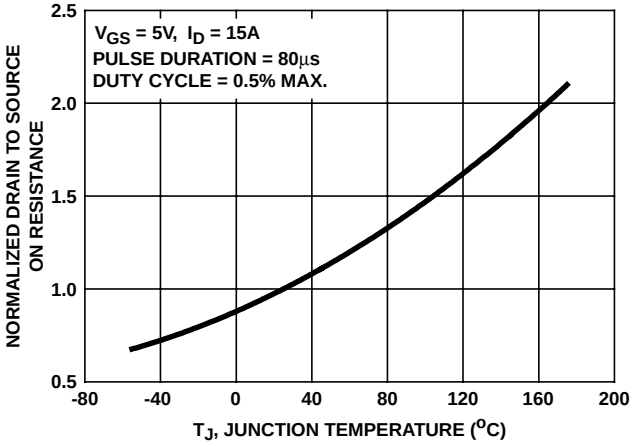


FIGURE 11. NORMALIZED DRAIN TO SOURCE ON RESISTANCE vs JUNCTION TEMPERATURE

Typical Performance Curves Unless Otherwise Specified **(Continued)**

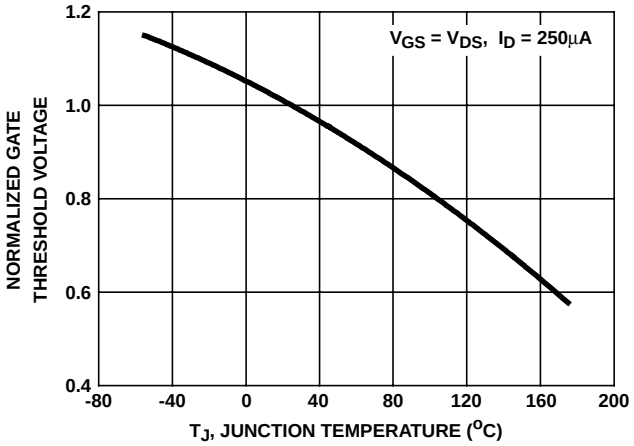


FIGURE 12. NORMALIZED GATE THRESHOLD VOLTAGE vs JUNCTION TEMPERATURE

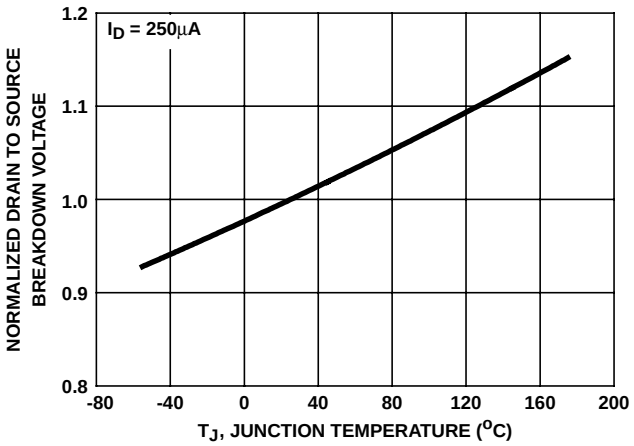


FIGURE 13. NORMALIZED DRAIN TO SOURCE BREAKDOWN VOLTAGE vs JUNCTION TEMPERATURE

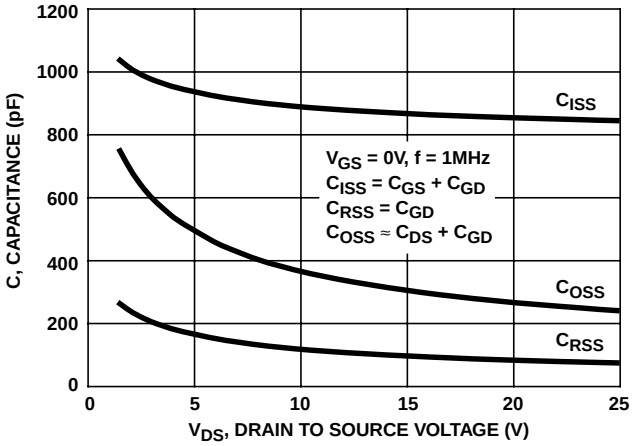
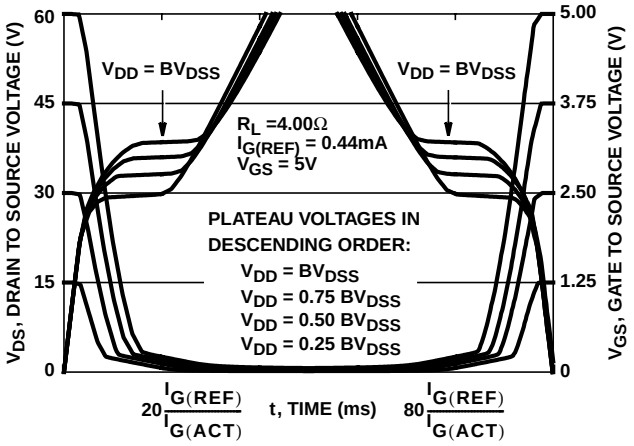


FIGURE 14. CAPACITANCE vs DRAIN TO SOURCE VOLTAGE



NOTE: Refer to Intersil Application Notes AN7254 and AN7260.

FIGURE 15. NORMALIZED SWITCHING WAVEFORMS FOR CONSTANT GATE CURRENT

Test Circuits and Waveforms

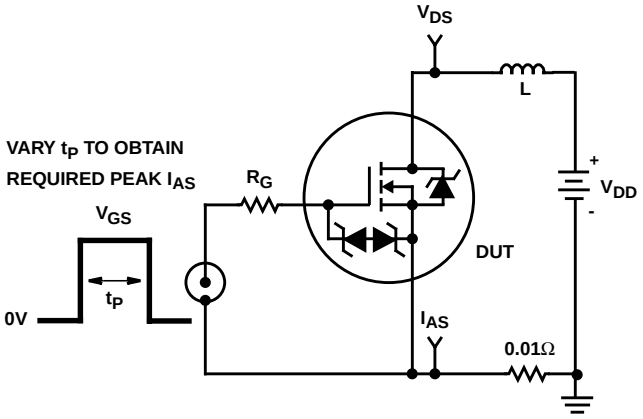


FIGURE 16. UNCLAMPED ENERGY TEST CIRCUIT

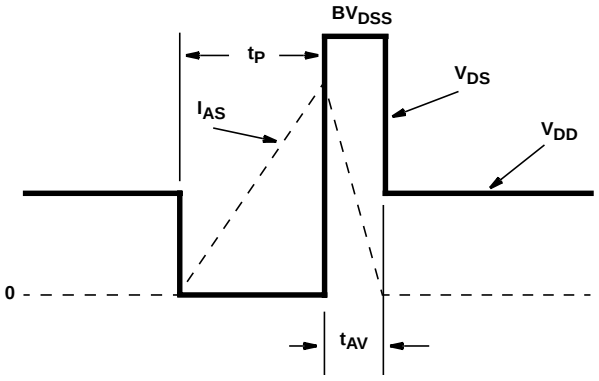


FIGURE 17. UNCLAMPED ENERGY WAVEFORMS

Test Circuits and Waveforms (Continued)

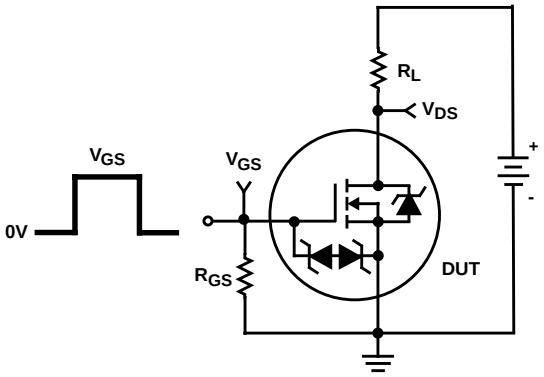


FIGURE 18. SWITCHING TIME TEST CIRCUIT

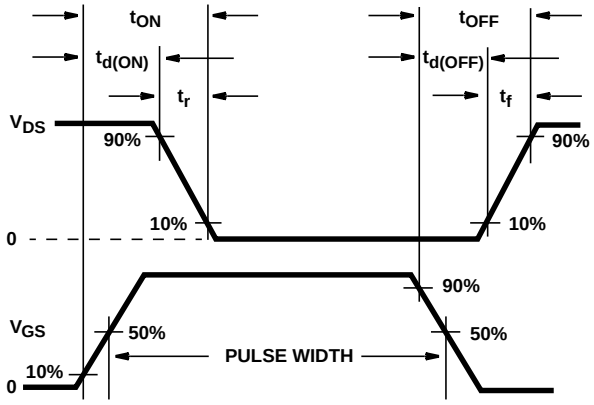


FIGURE 19. RESISTIVE SWITCHING WAVEFORMS

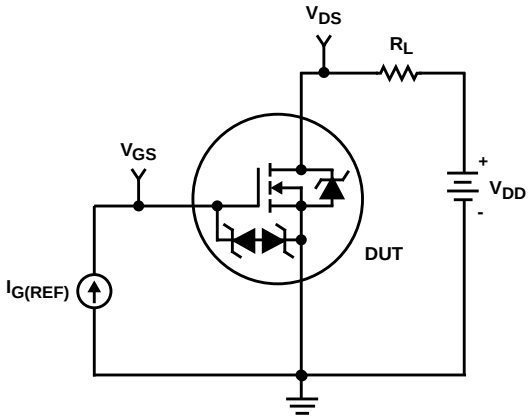


FIGURE 20. GATE CHARGE TEST CIRCUIT

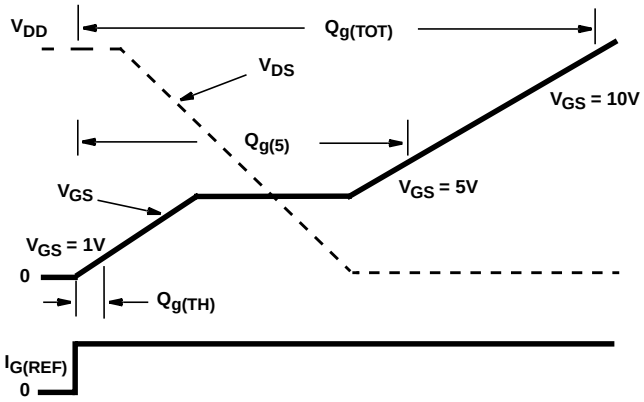


FIGURE 21. GATE CHARGE WAVEFORMS

PSPICE Electrical Model

SUBCKT RFD15N06LE 2 1 3 ; rev 5/13/95

```
CA  12  8 2.50e-9
CB  15  14 2.4e-9
CIN  6  8 7.70e-10

DBODY  7  5  DBODYMOD
DBREAK  5 11  DBREAKMOD
DESD1 91 9  DESD1MOD
DESD2 91 7 DESD2MOD
DPLCAP 10  5  DPLCAPMOD

EBREAK  11  7  17  18 65.18
EDS  14  8  5  8  1
EGS  13  8  6  8  1
ESG  6  10  6  8  1
EVTHRES 6 21 19 8  1
EVTEMP 20 6 18 22 1

IT  8  17  1

LDRAIN  2  5  1e-9
LGATE 1  9 2.77e-9
LSOURCE  3  7 2.98e-9

MMED 16  6  8  8  MMEDMOD
MSTRO 16  6  8  8  MSTROMOD
MWEAK 16  21  8  8  MWEAKMOD

RBREAK  17  18  RBREAKMOD  1
RDRAIN  50  16  RDRAINMOD 14.52e-3
RGATE 9 20 2.6
RLDRAIN  2  5  10
RLGATE 1 9 27.7
RLSOURCE 3 7 29.8
RSLC1  5  51  RSLCMOD 1e-6
RSLC2  5  50  1e3
RSOURCE  8  7  RSOURCEMOD 20.05e-3
RVTHRES 22 8 RVTHRESMOD 1
RVTEMP 18  19  RVTEMPMOD  1

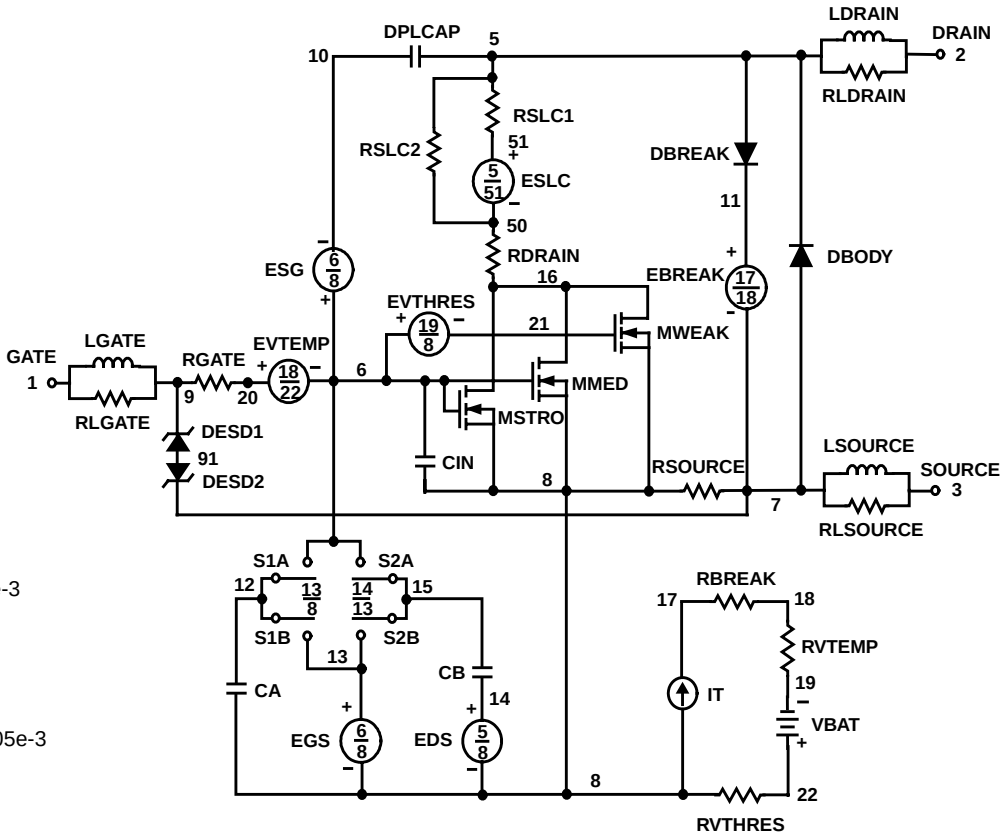
S1A  6  12  13  8  S1AMOD
S1B  13  12  13  8  S1BMOD
S2A  6  15  14  13  S2AMOD
S2B  13  15  14  13  S2BMOD

VBAT 22 19  DC  1

ESLC 51 50  VALUE = {(V(5,51)/ABS(V(5,51)))*(PWR(V(5,51)/(1e-6*72),5))}

.MODEL DBODYMOD D (IS = 6.5e-13  RS = 1.20e-2  TRS1 = 1.75e-3  TRS2 = 5.08e-6  CJO = 7.45e-10 TT = 4.61e-8 M = 0.46)
.MODEL DBREAKMOD D (RS = 1.28e-1  TRS1 = -2.15e-3  TRS2 = 1.05e-5)
.MODEL DESD1MOD D (BV = 12.7 TBV1 = 0 TBV2 = 0 RS = 35 TRS1 = 1.2e-6 TRS2 = 0)
.MODEL DESD2MOD D (BV = 12.7 TBV1 = 0 TBV2 = 0 RS = 0 TRS1 =0 TRS2 = 0)
.MODEL DPLCAPMOD D (CJO = 4.32e-10  IS = 1e-30  N = 10 M = 0.54)
.MODEL MMEDMOD NMOS (VTO = 1.60  KP = 1.75 IS = 1e-30  N = 10  TOX = 1  L = 1u  W = 1u RG = 2.60)
.MODEL MSTROMOD NMOS (VTO = 1.93  KP = 26.0 IS = 1e-30  N = 10  TOX = 1  L = 1u  W = 1u)
.MODEL MWEAKMOD NMOS (VTO = 1.39  KP = 0.09  IS = 1e-30  N = 10  TOX = 1  L = 1u  W = 1u RG = 26.0 RS = 0.1)
.MODEL RBREAKMOD RES (TC1 = 9.76e-4  TC2 = 5.11e-7)
.MODEL RDRAINMOD RES (TC1 = 1.30e-2  TC2 = 4.49e-5)
.MODEL RSLCMOD RES (TC1 =3.00e-3  TC2 = 6.00e-6)
.MODEL RSOURCEMOD RES (TC1 = 0  TC2 = 0)
.MODEL RVTHRESMOD RES (TC1 = -1.43e-3  TC2 = -6.72e-6)
.MODEL RVTEMPMOD RES (TC1 = -9.91e-4  TC2 = 1.02e-6)
.MODEL S1AMOD VSWITCH (RON = 1e-5  ROFF = 0.1  VON = -4.85  VOFF = -1.85)
.MODEL S1BMOD VSWITCH (RON = 1e-5  ROFF = 0.1  VON = -1.85  VOFF = -4.85)
.MODEL S2AMOD VSWITCH (RON = 1e-5  ROFF = 0.1  VON = -1.35  VOFF = 1.65)
.MODEL S2BMOD VSWITCH (RON = 1e-5  ROFF = 0.1  VON = 1.65  VOFF = -1.35

.ENDS
```



NOTE: For further discussion of the PSPICE model, consult **A New PSPICE Sub-Circuit for the Power MOSFET Featuring Global Temperature Options**; IEEE Power Electronics Specialist Conference Records, 1991.

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