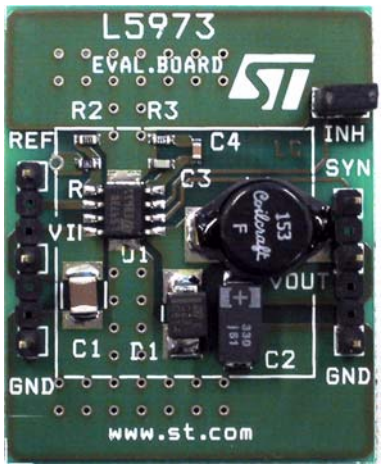
AN1518
Application note

Designing with the 2.5 A DC-DC converter L5973D

Introduction

The L5973D is a step-down monolithic power switching regulator capable of delivering up to 2.5 A at output voltages from 1.235 V to 35 V. The operating input voltage ranges from 4.4 V to 36 V. It has been designed using BCDV technology and the power switching element is implemented through a P-channel D-MOS transistor. It does not require a bootstrap capacitor, and the duty cycle can range up to 100%. An internal oscillator fixes the switching frequency at 250 kHz. This minimizes the LC output filter. A synchronization pin is available for cases where a higher frequency (up to 500 kHz) is required. Pulse-by-pulse and frequency foldback overcurrent protection offer effective short circuit protection. Other features are voltage feed-forward, protection against feedback disconnection, inhibit and thermal shutdown. The device is housed in an HSOP8 package with exposed pad that helps to reduce the thermal resistance junction-to-ambient (R_{Thj-a}) down to approximately 40 °C/W.

Figure 1. Evaluation board

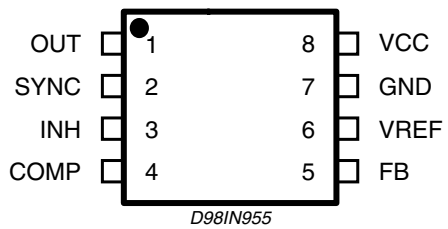


L5973D (HSOP8) board dimensions: 23x20 mm

Figure 2. Package

HSOP8 - Exposed Pad

Figure 3. Pin connection



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1 Pin functions

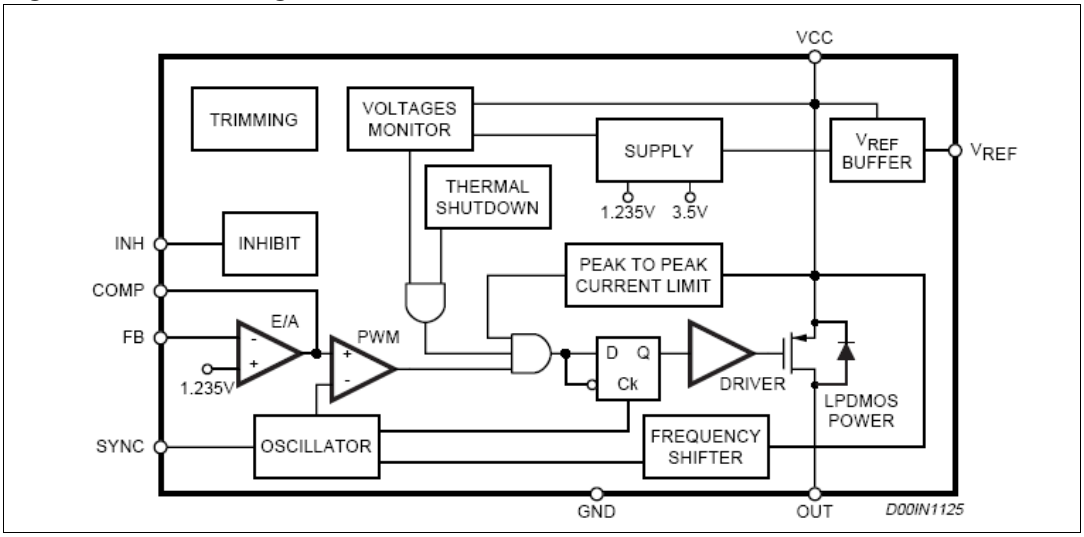
1.1 Pin description

Table 1. Pin functions

N.	Name	Description
1	OUT	Regulator output
2	SYNC	Master/slave synchronization. When open, a signal synchronous with the turn-OFF of the internal power is present. When connected to an external signal at a frequency higher than the internal one, the device is synchronized by the external signal. Connecting the SYNC pins of two devices, the one with the higher frequency works as master and the other one works as slave.
3	INH	A logical signal (active high) disables the device. With an IHN higher than 2.2 V the device is OFF and with an INH lower than 0.8 V, the device is ON. If INH is not used, the pin must be grounded. When it is open, an internal pull-up disables the device.
4	COMP	E/A output to be used for frequency compensation
5	FB	Step-down feedback input. Connecting the output voltage directly to this pin results in an output voltage of 1.235 V. An external resistor divider is required for higher output voltages (the typical value for the resistor connected between this pin and ground is 4.7 k).
6	V_{REF}	Reference voltage of 3.3 V. No filter capacitor is needed for stability
7	GND	Ground
8	V_{CC}	Unregulated DC input voltage

2 Block diagram

Figure 4. Block diagram



3 Functional description

The main internal blocks are shown in the device block diagram in *Figure 4*. They are:

- A voltage regulator supplying the internal circuitry. From this regulator, a 3.3 V reference voltage is externally available.
- A voltage monitor circuit which checks the input and the internal voltages.
- A fully integrated sawtooth oscillator with a frequency of 250 kHz ±15%, including also the voltage feed forward function and an input/output synchronization pin.
- Two embedded current limitation circuits which control the current that flows through the power switch. The pulse-by-pulse current limit forces the power switch OFF cycle by cycle if the current reaches an internal threshold, while the frequency shifter reduces the switching frequency in order to significantly reduce the duty cycle.
- A transconductance error amplifier.
- A pulse width modulator (PWM) comparator and the relative logic circuitry necessary to drive the internal power.
- A high side driver for the internal P-MOS switch.
- An inhibit block for stand-by operation.
- A circuit to implement the thermal protection function.

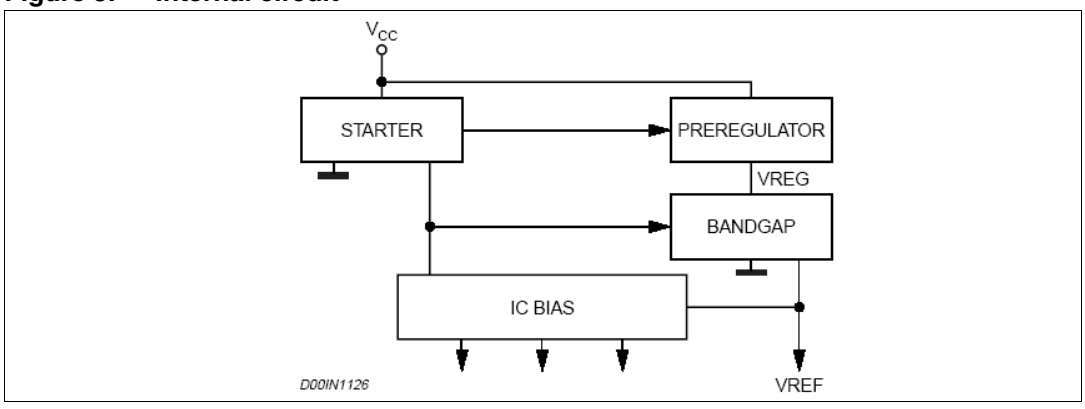
3.1 Power supply & voltage reference

The internal regulator circuit (shown in *Figure 5*) consists of a start-up circuit, an internal voltage Preregulator, the Bandgap voltage reference and the Bias block that provides current to all the blocks. The Starter supplies the start-up currents to the entire device when the input voltage goes high and the device is enabled (inhibit pin connected to ground). The Preregulator block supplies the Bandgap cell with a preregulated voltage V_{REG} that has a very low supply voltage noise sensitivity.

3.2 Voltages monitor

An internal block continuously senses the V_{cc}, V_{ref} and V_{bg}. If the voltages go higher than their thresholds, the regulator begins operating. There is also a hysteresis on the V_{CC} (UVLO).

Figure 5. Internal circuit



3.3 Oscillator & synchronizer

Figure 6 shows the block diagram of the oscillator circuit.

The Clock Generator provides the switching frequency of the device, which is internally fixed at 250 kHz. The Frequency Shifter block acts to reduce the switching frequency in case of strong overcurrent or short circuit. The clock signal is then used in the internal logic circuitry and is the input of the Ramp Generator and Synchronizer blocks.

The Ramp Generator circuit provides the sawtooth signal, used for PWM control and internal voltage feed-forward, while the synchronizer circuit generates the synchronization signal. The device also has a synchronization pin which can work both as Master and Slave.

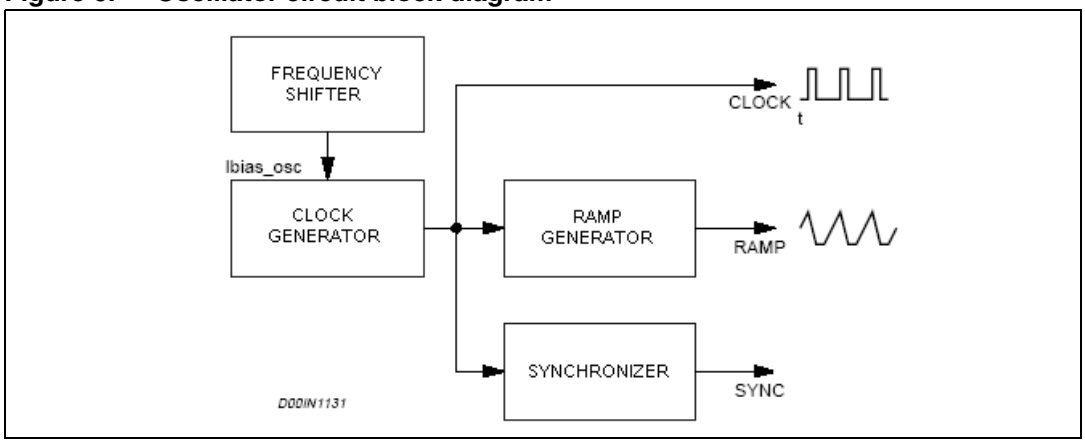
As Master, it serves to synchronize external devices to the internal switching frequency, and as Slave to synchronize itself using an external signal up to 500 kHz.

In particular, when connecting together two devices the one with the lower switching frequency works as a Slave and the other as Master.

To synchronize the device, the SYNC pin must pass from a low level to a level higher than the synchronization threshold with a duty cycle that can vary from approximately 10% to 90%, depending also on the signal frequency and amplitude.

The frequency of the synchronization signal must be, at a minimum, higher than the internal switching frequency of the device (250 kHz).

Figure 6. Oscillator circuit block diagram



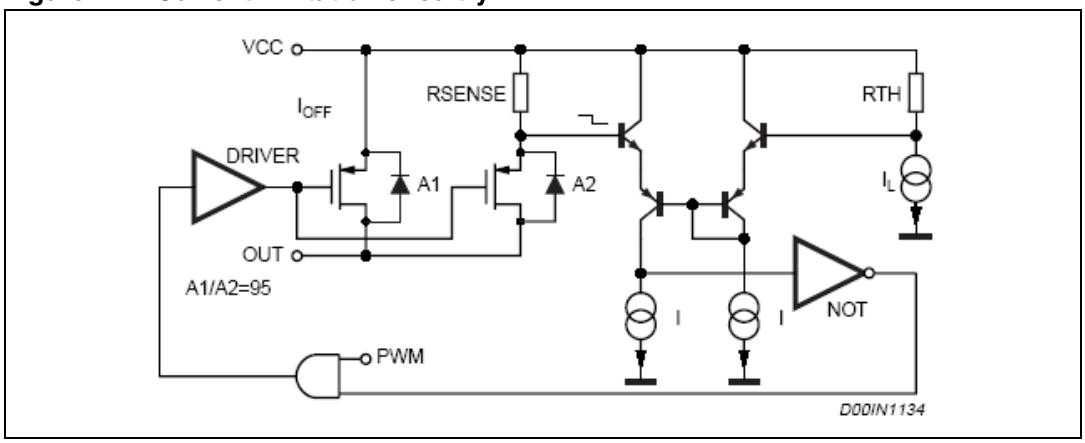
3.4 Current protection

The L5973D features two types of current limit protection: pulse-by-pulse and frequency foldback.

The schematic of the current limitation circuitry for the pulse-by-pulse protection is shown in *Figure 7*. The output power PDMOS transistor is split into two parallel PDMOS transistors. The smallest one includes a resistor in series, R_{SENSE}. The current is sensed through R_{SENSE} and if it reaches the threshold, the mirror becomes unbalanced and the PDMOS is switched off until the next falling edge of the internal clock pulse. Due to this reduction of the ON time, the output voltage decreases. Since the minimum switch ON time (necessary to avoid false a overcurrent signal) is too short to obtain a sufficiently low duty cycle at 250 kHz, the output current, in strong overcurrent or short circuit conditions, could increase

again. For this reason the switching frequency is also reduced, thus keeping the inductor current under its maximum threshold. The Frequency Shifter (*Figure 6*) functions based on the feedback voltage. As the feedback voltage decreases (due to the reduced duty cycle), the switching frequency decreases also.

Figure 7. Current limitation circuitry



3.5 Error amplifier

The voltage error amplifier is the core of the loop regulation. It is a transconductance operational amplifier whose non inverting input is connected to the internal voltage reference (1.235 V), while the inverting input (FB) is connected to the external divider or directly to the output voltage. The output (COMP) is connected to the external compensation network. The uncompensated error amplifier has the following characteristics:

Table 2. Uncompensated error amplifier characteristics

Description	Values
Transconductance	2300 µS
Low frequency gain	65dB
Minimum sink/source voltage	1500 µA/300 µA
Output voltage swing	0.4 V/3.65 V
Input bias current	2.5 µA

The error amplifier output is compared to the oscillator sawtooth to perform PWM control.

3.6 PWM comparator and power stage

This block compares the oscillator sawtooth and the error amplifier output signals to generate the PWM signal for the driving stage.

The power stage is a highly critical block, as it functions to guarantee a correct turn ON and turn OFF of the PDMOS. The turn ON of the power element, or more accurately, the rise time of the current at turn ON, is a very critical parameter. At a first approach, it appears that the faster the rise time, the lower the turn ON losses.

However, there is a limit introduced by the recovery time of the recirculation diode.

In fact, when the current of the power element is equal to the inductor current, the diode turns OFF and the drain of the power is able to go high. But during its recovery time, the diode can be considered a high value capacitor and this produces a very high peak current, responsible for numerous problems:

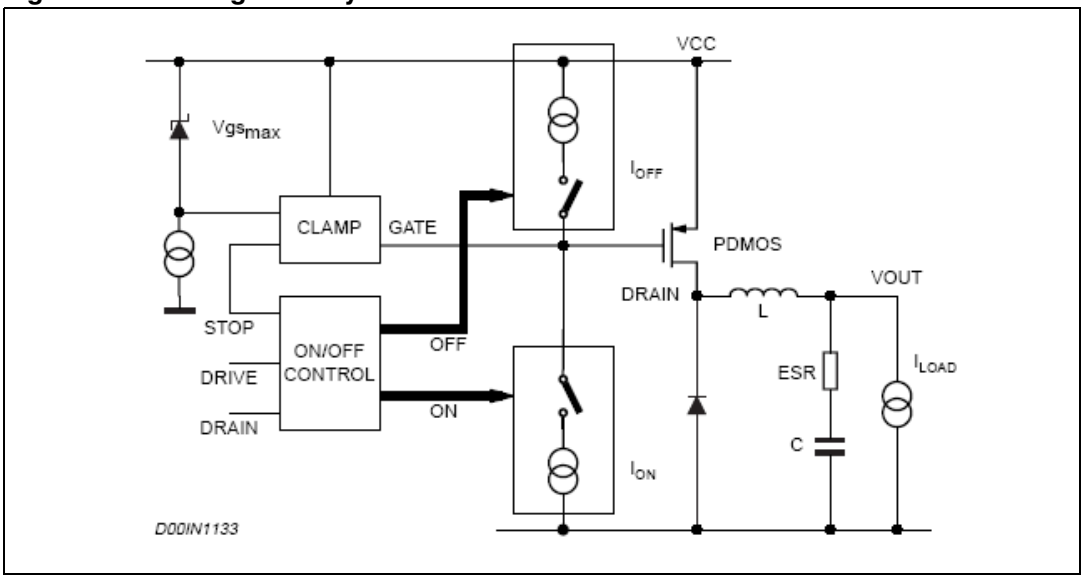
- Spikes on the device supply voltage that cause oscillations (and thus noise) due to the board parasitics.
- Turn ON overcurrent leads to a decrease in the efficiency and system reliability.
- Major EMI problems.
- Shorter freewheeling diode life.

The fall time of the current during turn OFF is also critical, as it produces voltage spikes (due to the parasitics elements of the board) that increase the voltage drop across the PDMOS.

In order to minimize these problems, a new driving circuit topology has been used and the block diagram is shown in *Figure 8* . The basic idea is to change the current levels used to turn the power switch ON and OFF, based on the PDMOS and the gate clamp status.

This circuitry allows the power switch to be turned OFF and ON quickly and addresses the freewheeling diode recovery time problem. The gate clamp is necessary to ensure that V_{GS} of the internal switch does not go higher than V_{GS}max. The ON/OFF Control block protects against any cross conduction between the supply line and ground.

Figure 8. Driving circuitry



3.7 Inhibit function

The inhibit feature is used to put the device in standby mode. With the INH pin higher than 2.2 V the device is disabled and the power consumption is reduced to less than 100 µA. With the INH pin lower than 0.8 V, the device is enabled. If the INH pin is left floating, an internal pull up ensures that the voltage at the pin reaches the inhibit threshold and the device is disabled. The pin is also V_{cc} compatible.

3.8 Thermal shutdown

The shutdown block generates a signal that turns OFF the power stage if the temperature of the chip goes higher than a fixed internal threshold (150 °C). The sensing element of the chip is very close to the PDMOS area, ensuring fast and accurate temperature detection. A hysteresis of approximately 20 °C keeps the device from turning ON and OFF continuously.

4 Additional features and protection

4.1 Feedback disconnection

If the feedback is disconnected, the duty cycle increases towards the maximum allowed value, bringing the output voltage close to the input supply. This condition could destroy the load.

To avoid this hazardous condition, the device is turned OFF if the feedback pin is left floating.

4.2 Output overvoltage protection

Overvoltage protection, or OVP, is achieved by using an internal comparator connected to the feedback, which turns OFF the power stage when the OVP threshold is reached. This threshold is typically 30% higher than the feedback voltage.

When a voltage divider is required to adjust the output voltage (*Figure 14*), the OVP intervention will be set at:

Equation 1

$$V_{OVP} = 1.3 \bullet \frac{R_1 + R_2}{R_2} \bullet V_{FB}$$

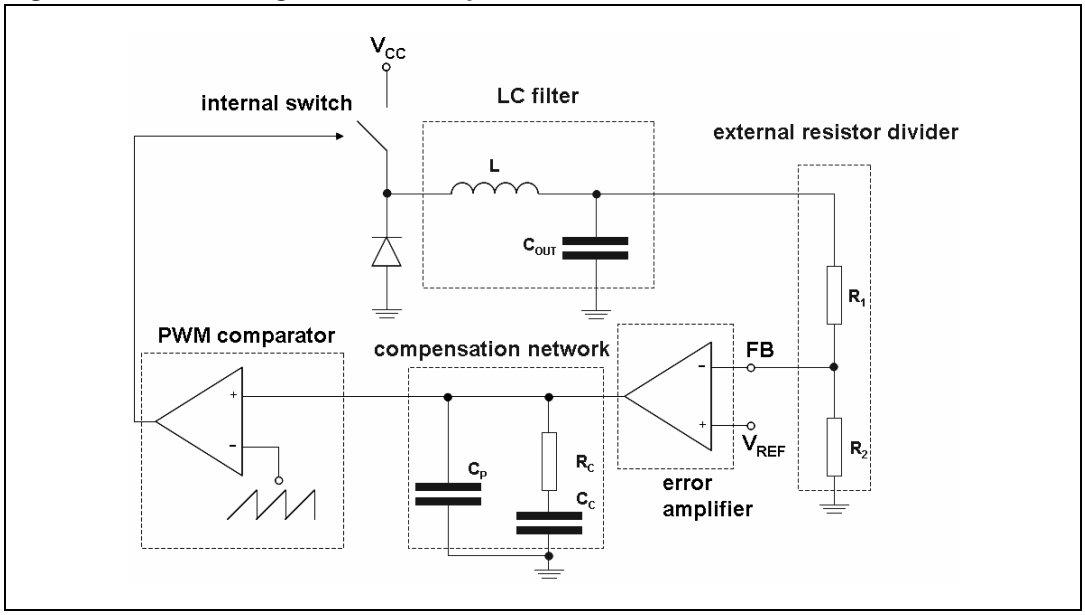
Where R_1 is the resistor connected between the output voltage and the feedback pin, and R_2 is between the feedback pin and ground.

4.3 Zero load

Due to the fact that the internal power is a PDMOS, no boostrap capacitor is required and so the device works properly even with no load at the output. In this case it works in burst mode, with a random burst repetition rate.

5 Closing the loop

Figure 9. Block diagram of the loop



6 Error amplifier and compensation network

The output L-C filter of a step-down converter contributes with 180 degrees phase shift in the control loop. For this reason a compensation network between the COMP pin and GROUND is added. The simplest compensation network together with the equivalent circuit of the error amplifier are shown in *Figure 10*. R_C and C_C introduce a pole and a zero in the open loop gain. CP does not significantly affect system stability but it is useful to reduce the noise of the COMP pin.

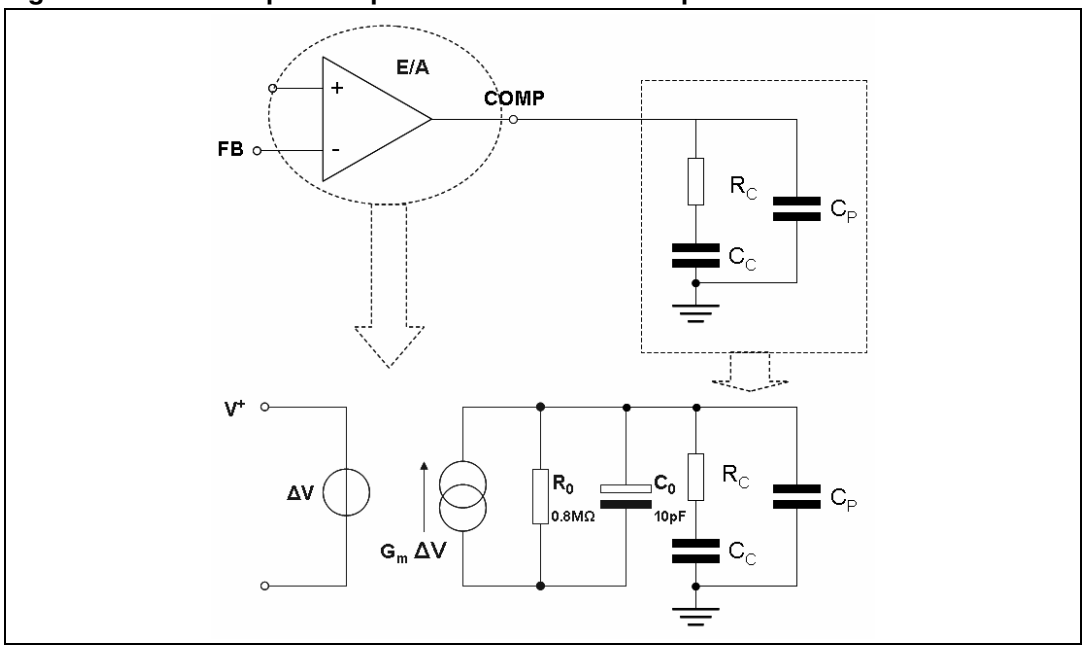
The transfer function of the error amplifier and its compensation network is:

Equation 2

$$A_0(s) = \frac{A_{V0} \bullet (1 + s \bullet R_c \bullet C_c)}{s^2 \bullet R_0 \bullet (C_0 + C_p) \bullet R_c \bullet C_c + s \bullet (R_0 \bullet C_c + R_0 \bullet (C_0 + C_p) + R_c \bullet C_c) + 1}$$

Where $A_{vo} = G_m \cdot R_o$

Figure 10. Error amplifier equivalent circuit and compensation network



The poles of this transfer function are (if $C_c >> C_0+C_P$):

Equation 3

$$F_{P1} = \frac{1}{2 \bullet \pi \bullet R_0 \bullet C_c}$$

Equation 4

$$F_{P2} = \frac{1}{2 \bullet \pi \bullet R_c \bullet (C_0 + C_p)}$$

whereas the zero is defined as:

Equation 5

$$F_{Z1} = \frac{1}{2 \bullet \pi \bullet R_c \bullet C_c}$$

F_{P1} is the low frequency which sets the bandwidth, while the zero F_{Z1} is usually put near to the frequency of the double pole of the L-C filter (see below). F_{P2} is usually at a very high frequency.

7 LC filter

The transfer function of the L-C filter is given by:

Equation 6

$$A_{LC}(s) = \frac{R_{LOAD} \bullet (1 + ESR \bullet C_{OUT} \bullet s)}{s^2 \bullet L \bullet C_{OUT} \bullet (ESR + R_{LOAD}) + s \bullet (ESR \bullet C_{OUT} \bullet R_{LOAD} + L) + R_{LOAD}}$$

where R_{LOAD} is defined as the ratio between V_{OUT} and I_{OUT}.

If R_{LOAD}>>ESR, the previous expression of A_{LC} can be simplified and becomes:

Equation 7

$$A_{LC}(s) = \frac{1 + ESR \bullet C_{OUT} \bullet s}{L \bullet C_{OUT} \bullet s^2 + ESR \bullet C_{OUT} \bullet s + 1}$$

The zero of this transfer function is given by:

Equation 8

$$F_O = \frac{1}{2 \bullet \pi \bullet ESR \bullet C_{OUT}}$$

F_0 is the zero introduced by the ESR of the output capacitor and it is very important to increase the phase margin of the loop.

The poles of the transfer function can be calculated through the following expression:

Equation 9

$$F_{PLC1,\ 2} = \frac{-ESR \bullet C_{OUT} \pm \sqrt{(ESR \bullet C_{OUT})^2 - 4 \bullet L \bullet C_{OUT}}}{2 \bullet L \bullet C_{OUT}}$$

In the denominator of A_{LC} the typical second order system equation can be recognized:

Equation 10

$$s^2 + 2 \bullet \delta \bullet \omega_h \bullet s + \omega^2_n$$

If the damping coefficient δ is very close to zero, the roots of the equation become a double root whose value is ω_h.

Similarly for A_{LC} the poles can usually be defined as a double pole whose value is:

Equation 11

$$F_{PLC} = \frac{1}{2 \bullet \pi \bullet \sqrt{L \bullet C_{OUT}}}$$

8 PWM comparator

The PWM gain is given by the following formula:

Equation 12

$$G_{PWM}(s) = \frac{V_{cc}}{(V_{OSCMAX} - V_{OSCMIN})}$$

where V_{OSCMAX} is the maximum value of a sawtooth waveform and V_{OSCMIN} is the minimum value. A voltage feed forward is implemented to ensure a constant GPWM. This is obtained by generating a sawtooth waveform directly proportional to the input voltage V_{CC}.

Equation 13

$$V_{OSCMAX} - V_{OSCMIN} = K \bullet V_{CC}$$

Where K is equal to 0.076. Therefore the PWM gain is also equal to:

Equation 14

$$G_{PWM}(s) = \frac{1}{K} = const$$

This means that even if the input voltage changes, the error amplifier does not change its value to keep the loop in regulation, thus ensuring a better line regulation and line transient response.

In summary, the Open Loop Gain can be expressed as:

Equation 15

$$G(s) = G_{PWM}(s) \bullet \frac{R_2}{R_1 + R_2} \bullet A_O(s) \bullet A_{LC}(s)$$

Example*:*

Considering R_C = 2.7 kΩ, C_C = 22 nF and C_P = 220 pF, the poles and zeroes of A_0 are:

F_{P1} = 9 Hz

F_{P2} = 256 kHz

F_{Z1} = 2.68 kHz

If L = 22 µH, C_{OUT} = 100 µF and ESR = 80 mΩ, the poles and zeroes of A_{LC} become:

F_{PLC} = 3.39 kHz

F_0 = 19.89 kHz

Finally R_1 = 5.6 kΩ and R_2 = 3.3 kΩ

The gain and phase bode diagrams are plotted respectively in *Figure 11* and *Figure 12*.

Figure 11. Module plot

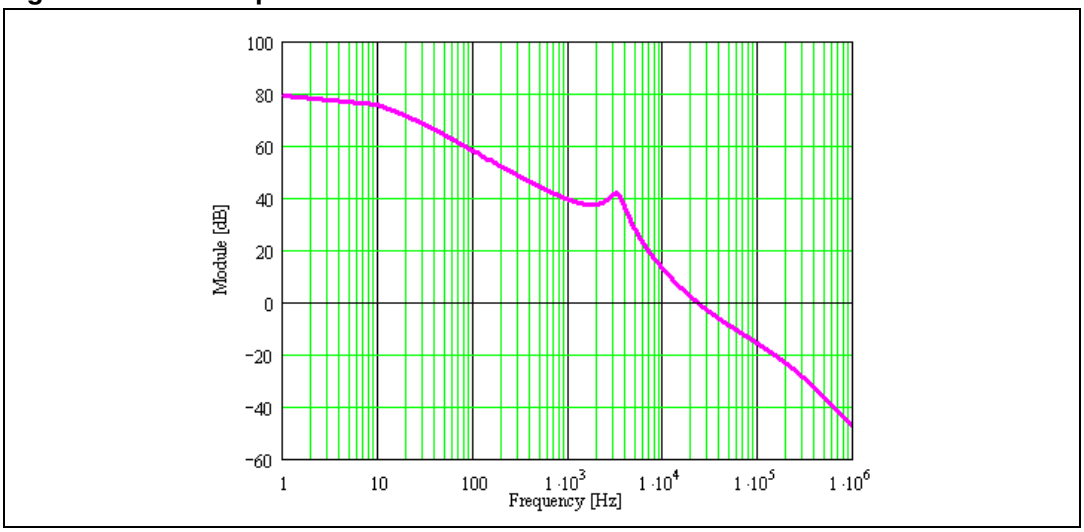
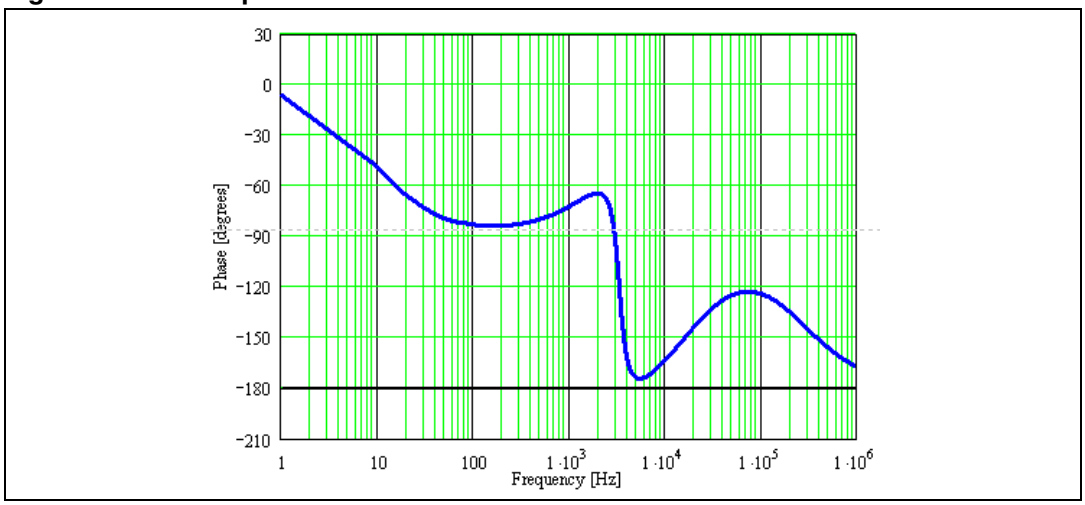


Figure 12. Phase plot



The cut-off frequency and the phase margin are:

Equation 16

$$F_C = 22.8KHz \quad \text{Phase margin} = 39.8°$$

9 Application information

9.1 Component selection

- Input capacitor

The input capacitor must be able to support the maximum input operating voltage and the maximum RMS input current.

Since step-down converters draw current from the input in pulses, the input current is squared and the height of each pulse is equal to the output current. The input capacitor has to absorb all this switching current, which can be up to the load current divided by two (worst case, with duty cycle of 50%). For this reason, the quality of these capacitors has to be very high to minimize the power dissipation generated by the internal ESR, thereby improving system reliability and efficiency. The critical parameter is usually the RMS current rating, which must be higher than the RMS input current. The maximum RMS input current (flowing through the input capacitor) is:

Equation 17

$$I_{RMS} = I_O \bullet \sqrt{D - \frac{2 \bullet D^2}{\eta} + \frac{D^2}{\eta}}$$

Where η is the expected system efficiency, D is the duty cycle and I_O is the output DC current. This function reaches its maximum value at D = 0.5 and the equivalent RMS current is equal to I_O divided by 2 (considering η= 1). The maximum and minimum duty cycles are:

Equation 18

$$D_{MAX} = \frac{V_{OUT} + V_F}{V_{INMIN} - V_{SW}}$$

and

Equation 19

$$D_{MIN} = \frac{V_{OUT} + V_F}{V_{INMAX} - V_{SW}}$$

Where V_F is the freewheeling diode forward voltage and V_{SW} the voltage drop across the internal PDMOS. Considering the range D_{MIN} to D_{MAX}, it is possible to determine the max IRMS going through the input capacitor. Capacitors that can be considered are:

Electrolytic capacitors:

These are widely used due to their low price and their availability in a wide range of RMS current ratings.

The only drawback is that, considering ripple current rating requirements, they are physically larger than other capacitors.

Ceramic capacitors:

If available for the required value and voltage rating, these capacitors usually have a higher RMS current rating for a given physical dimension (due to very low ESR).

The drawback is the considerably high cost.

Tantalum capacitors:

Very good, small tantalum capacitors with very low ESR are becoming more available. However, they can occasionally burn if subjected to very high current during charge.

Therefore, it is better to avoid this type of capacitor for the input filter of the device. They can, however, be subjected to high surge current when connected to the power supply.

Table 3. List of ceramic capacitors for the L597xD

Manufacturer	Series	Capacitor value (µ)	Rated voltage (V)
TDK	C3225	10	25
MURATA	GRM32	10	25
	GRM55	10	50

- Output capacitor

The output capacitor is very important to meet the output voltage ripple requirement.

Using a small inductor value is useful to reduce the size of the choke but it increases the current ripple. So, to reduce the output voltage ripple, a low ESR capacitor is required. Nevertheless, the ESR of the output capacitor introduces a zero in the open loop gain, which helps to increase the phase margin of the system. If the zero goes to a very high frequency, its effect is negligible. For this reason, ceramic capacitors and very low ESR capacitors in general should be avoided.

Tantalum and electrolytic capacitors are usually a good choice for this purpose. A list of some tantalum capacitor manufacturers is provided in *Table 4.: Output capacitor selection*.

Table 4. Output capacitor selection

Manufacturer	Series	Cap value (µF)	Rated voltage (V)	ESR (mΩ)
AVX	TPS	100 to 470	4 to 35	50 to 200
KEMET	T494/5	100 to 470	4 to 20	30 to 200
Sanyo POSCAP(1)	TPA/B/C	100 to 470	4 to 16	40 to 80
Sprague	595D	220 to 390	4 to 20	160 to 650

1. POSCAP capacitors have some characteristics which are very similar to tantalum.

- Inductor

The inductor value is very important as it fixes the ripple current flowing through the output capacitor. The ripple current is usually fixed at 20-40% of I_{omax}, which is 0.4 - 0.8 A with $I_O$max= 2 A. The approximate inductor value is obtained using the following formula:

Equation 20

$$L = \frac{(V_{IN} - V_{OUT})}{\Delta I} \bullet T_{ON}$$

where T_{ON} is the ON time of the internal switch, given by D · T. For example, with V_{OUT}=3.3 V, V_{IN}= 2 V and ΔI_O=0.6 A, the inductor value is about 17 µH. The peak current through the inductor is given by:

Equation 21

$$I_{PK} = I_O + \frac{\Delta I}{2}$$

and it can be observed that if the inductor value decreases, the peak current (which must be lower than the current limit of the device) increases. So, when the peak current is fixed, a higher inductor value allows a higher value for the output current. In the *Table 5.: Inductor selection*, some inductor manufacturers are listed.

Table 5. Inductor selection

Manufacturer	Series	Inductor value (µH)	Saturation current (A)
Coilcraft	DO3316	15 to 33	2.0 to 3.0
Coiltronics	UP1B	22 to 33	2.0 to 2.4
BI	HM76-3	15 to 33	2.5 to 3.3
Epcos	B82476	15 to 33	2 to 3
Wurth Elektronik	74456115	15 to 33	2.5 to 3

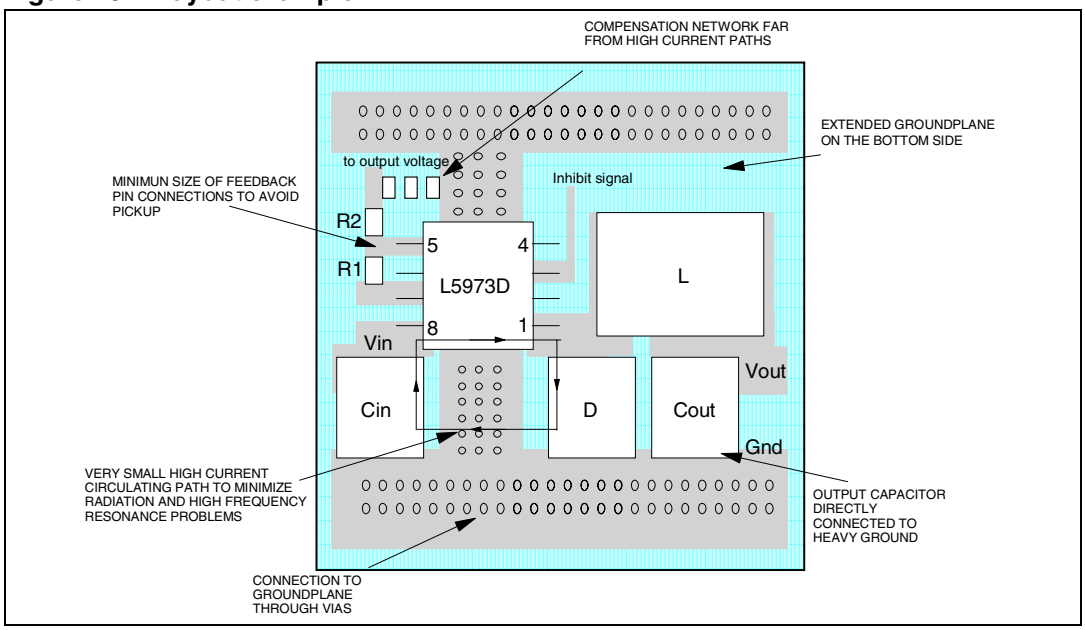
9.2 Layout considerations

The layout of switching DC-DC converters is very important to minimize noise and interference. Power-generating portions of the layout are the main cause of noise and so high switching current loop areas should be kept as small as possible and lead lengths as short as possible.

High impedance paths (in particular the feedback connections) are susceptible to interference, so they should be as far as possible from the high current paths. An layout example is provided in *Figure 13* below.

The input and output loops are minimized to avoid radiation and high frequency resonance problems. The feedback pin connections to the external divider are very close to the device to avoid pick-up noise. Another important issue is the groundplane of the board. Since the package has an exposed pad, it is very important to connect it to an extended groundplane in order to reduce the thermal resistance junction-to-ambient.

Figure 13. Layout example



9.3 Thermal considerations

The dissipated power of the device is tied to three different sources:

- Switching losses due to the not insignificant R_{DSON}, which are equal to:

Equation 22

$$P_{ON} = R_{DSON} \bullet (I_{OUT})^2 \bullet D$$

Where D is the duty cycle of the application. Note that the duty cycle is theoretically given by the ratio between V_{OUT} and V_{IN}, but in practice it is substantially higher than this value to compensate for the losses in the overall application. For this reason, the switching losses related to the R_{DSON} increase compared to an ideal case.

- Switching losses due to turning ON and OFF. These are derived using the following equation:

Equation 23

$$P_{SW} = V_{IN} \bullet I_{OUT} \bullet \frac{(T_{ON} + T_{OFF})}{2} \bullet F_{SW} = V_{IN} \bullet I_{OUT} \bullet T_{SW} \bullet F_{SW}$$

Where T_{ON} and T_{OFF} are the overlap times of the voltage across the power switch and the current flowing into it during the turn ON and turn OFF phases. T_{SW} is the equivalent switching time.

- Quiescent current losses.

Equation 24

$$P_Q = V_{IN} \bullet I_Q$$

Where I_Q is the quiescent current.

Example:

- V_{IN} = 5 V
- V_{OUT} = 3.3 V
- I_{OUT} = 2 A

R_{DSON} has a typical value of 0.25 @ 25 °C and increases up to a maximum value of 0.5. @ 150 °C. We can consider a value of 0.4 Ω

T_{SW} is approximately 70 ns.

I_Q has a typical value of 2.5 mA @ V_{IN} = 12 V.

The overall losses are:

Equation 25

$$P_{TOT} = R_{DSON} \bullet (I_{OUT})^2 \bullet D + V_{IN} \bullet I_{OUT} \bullet T_{SW} \bullet F_{SW} + V_{IN} \bullet I_Q =$$
$$= 0.4 \bullet 2^2 \bullet 0.7 + 5 \bullet 2 \bullet 70 \bullet 10^{-9} \bullet 250 \bullet 10^{-3} + 5 \bullet 2.5 \bullet 10^{-3} \cong 1,\ 3W$$

The junction temperature of device will be:

Equation 26

$$T_J = T_A + Rth_{J-A} \bullet P_{TOT}$$

Where T_A is the ambient temperature and Rth_{J-A} is the thermal resistance junction-to-ambient. Considering that the device is mounted on board with a good groundplane, that it has a thermal resistance junction-to-ambient (Rth_{J-A}) of about 42 °C/W, and an ambient temperature of about 70 °C:

Equation 27

$$T_J = 70 + 1.3 \bullet 42 \cong 125° C$$

9.4 Short-circuit protection

In overcurrent protection mode, when the peak current reaches the current limit, the device reduces the T_{ON} down to its minimum value (approximately 250 nsec) and the switching frequency to approximately one third of its nominal value (see *Section 3.4: Current protection*). In these conditions, the duty cycle is strongly reduced and, in most applications, this is enough to limit the current to ILIM. In any event, in case of heavy short-circuit at the output (V_O=0 V) and depending on the application conditions (V_{cc} value and parasitic effect of external components) the current peak could reach values higher than ILIM. This can be understood considering the inductor current ripple during the ON and OFF phases:

- ON phase

Equation 28

$$\Delta I_L = \frac{(V_{IN} - V_{out} - DCR_L \bullet I)}{L} = T_{ON}$$

- OFF phase

Equation 29

$$\Delta I_L = \frac{(V_D - V_{out} - DCR_L \bullet I)}{L} = T_{OFF}$$

where V_D is the voltage drop across the diode and DCR_L is the series resistance of the inductor.

In short-circuit conditions, V_{OUT} is negligible. So during T_{OFF}, the voltage applied to the inductor is very small and it could occur that the current ripple in this phase does not compensate for the current ripple during T_{ON}.

The maximum current peak can be easily measured through the inductor with V_O = 0 V (short-circuit) and V_{CC}=V_{INMAX}. In cases where application must sustain the short-circuit condition for an extended period, the external components (mainly the inductor and diode) must be selected based on this value.

Figure 14. Short-circuit current V_{IN} = 25 V

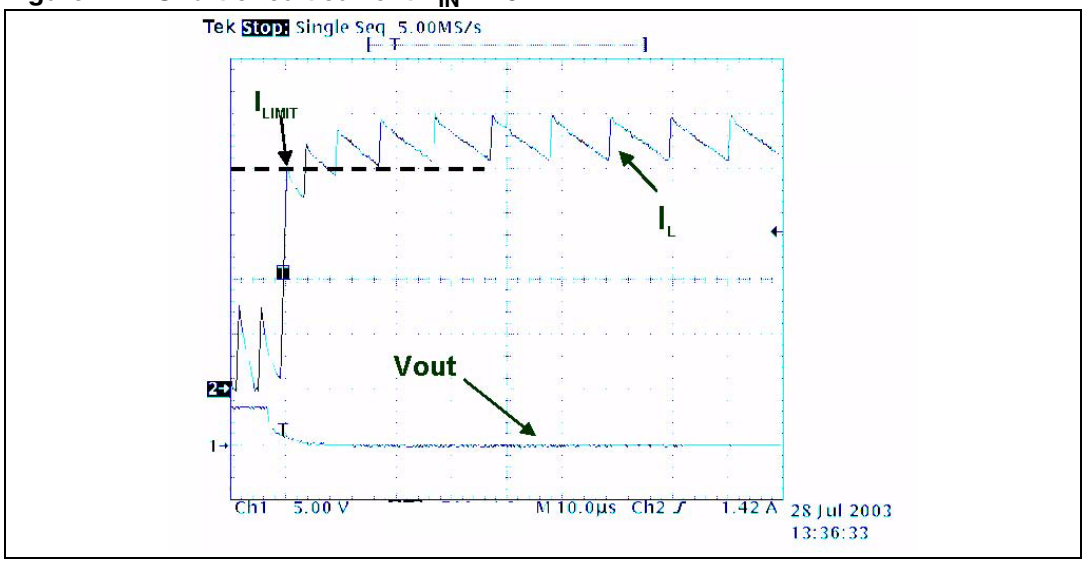
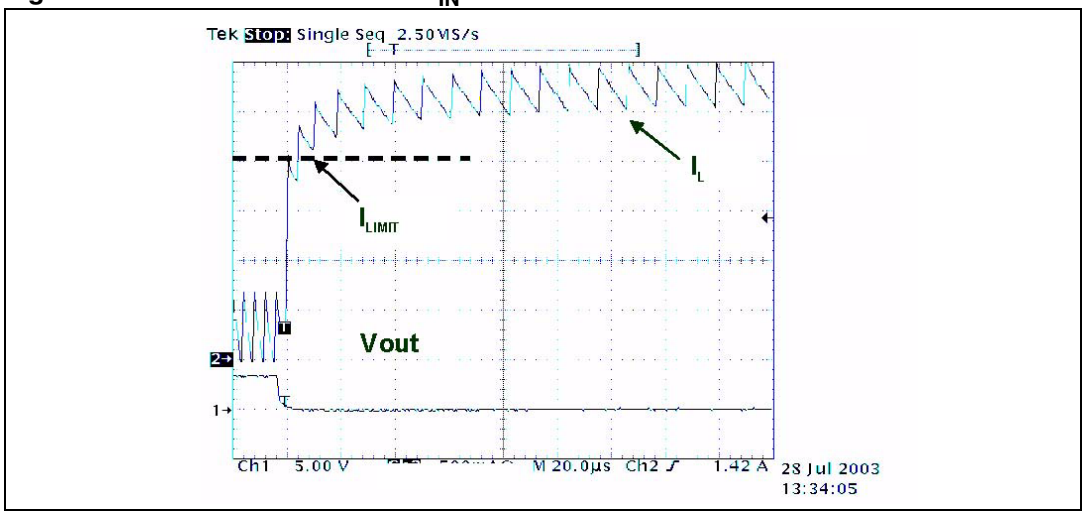


Figure 15. Short-circuit current V_{IN} = 30 V



In *Figure 14* and *Figure 15*, for example, it can be observed that when the input voltage increases for a given component list, the current peak increases also. The current limit is immediately triggered but the current peak increases until the current ripple during T_{OFF} is equal to the current ripple during T_{ON}.

9.5 Application circuit

Figure 16 shows the evaluation board application circuit, where the input supply voltage, V_{CC}, can range from 4.4 V to 25 V due to the voltage rating of the input capacitor, and the output voltage is adjustable from 1.235 V to V_{CC}.

Figure 16. Evaluation board application circuit

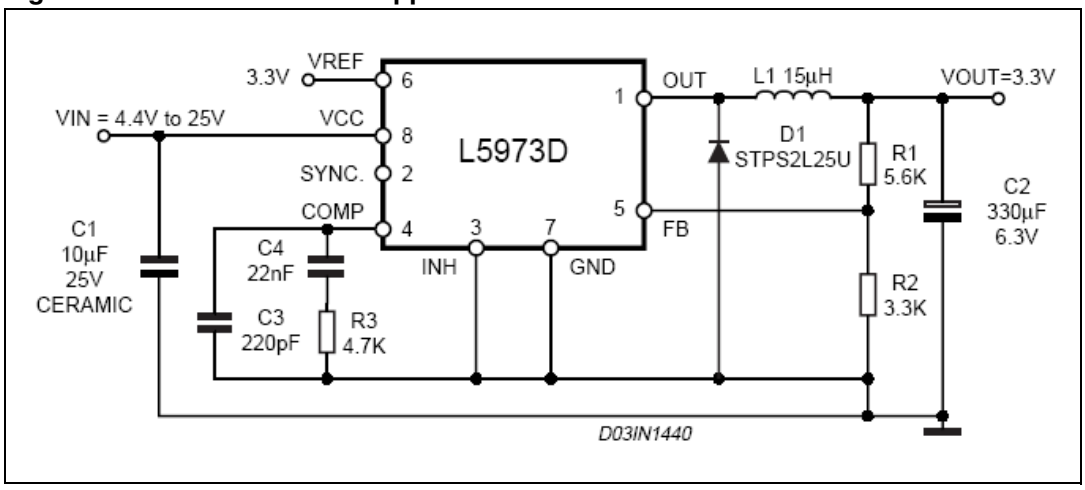


Table 6. Component list

Reference	Part number	Description	Manufacturer
C1	GRM32DR61E106KA12L	10 µF, 25 V	Murata
C2	POSCAP 6TPB330M	330 µF, 6.3 V	Sanyo

Table 6. Component list (continued)

Reference	Part number	Description	Manufacturer
C3	C1206C221J5GAC	220 pF, 5%, 50 V	KEMET
C4	C1206C223K5RAC	22 nF, 10%, 50 V	KEMET
R1		5.6 kΩ, 1%, 0.1 W 0603	Neohm
R2		3.3 kΩ, 1%, 0.1 W 0603	Neohm
R3		4.7 kΩ, 1%, 0.1 W 0603	Neohm
D1	STPS2L25U	2 A, 25 V	STMicroelectronics
L1	DO3316P-153	15 µH, 3 A	Coilcraft

Figure 17. PCB layout (component side)

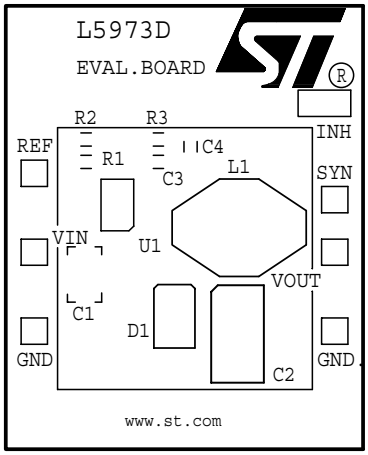


Figure 18. PCB layout (bottom side)

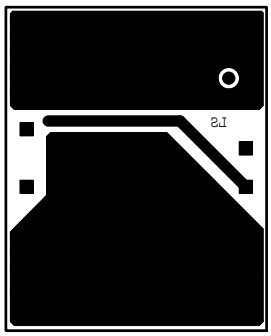
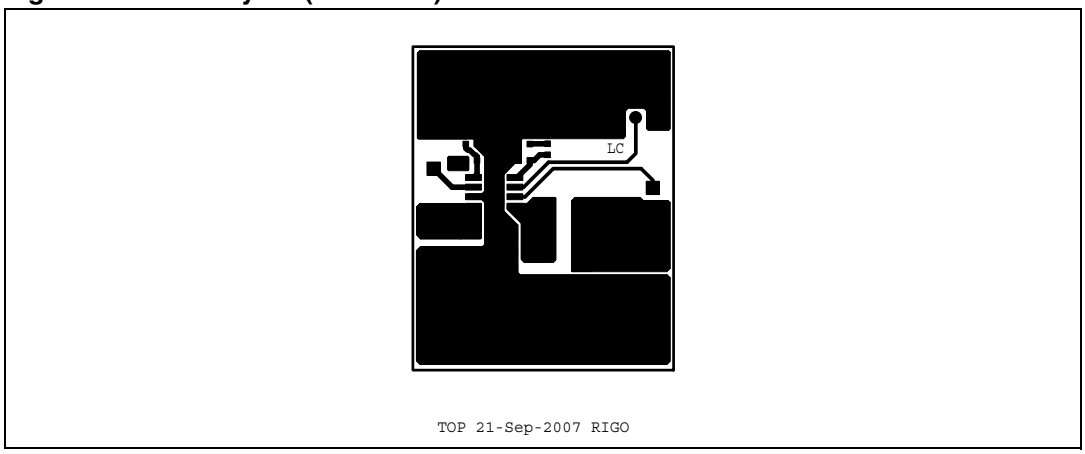


Figure 19. PCB layout (front side)



Below, some graphs are provided which show the T_j versus output current in different input and output voltage conditions, as well as some efficiency measurements.

Figure 20. Junction temperature vs. output current (V_{CC} = 5 V)

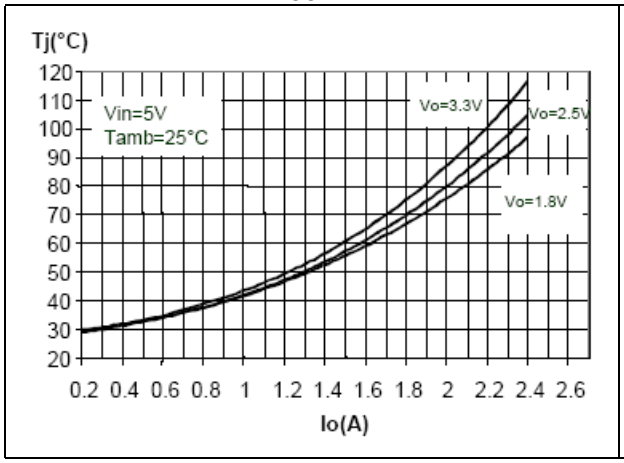


Figure 21. Efficiency vs. output current (V_{CC}= 5 V)

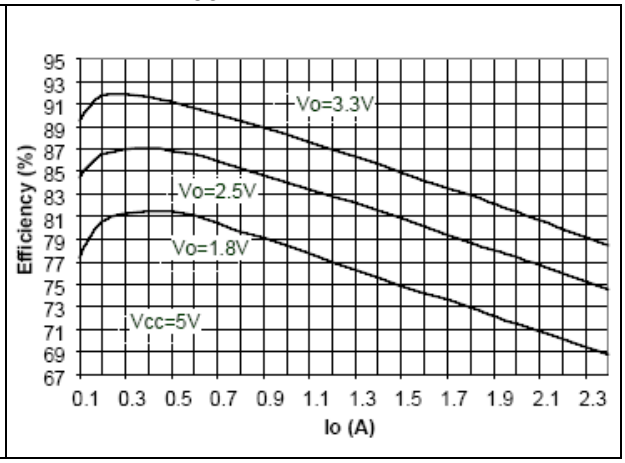


Figure 22. Junction temperature vs. output current (V_{CC} = 12 V)

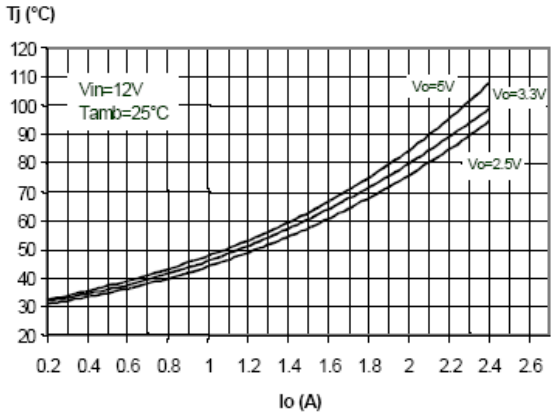
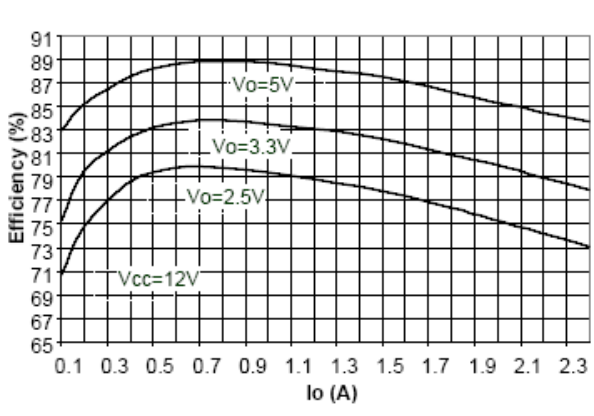


Figure 23. Efficiency vs. output current (V_{CC}=12 V)



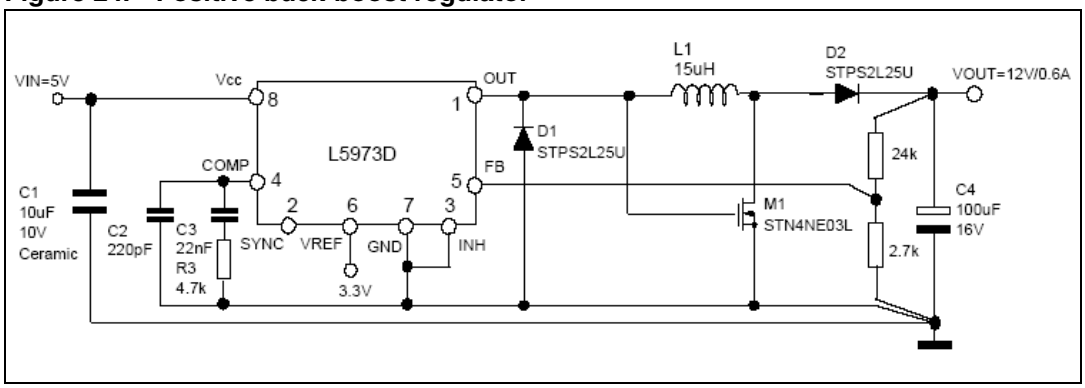
10 Application ideas

10.1 Positive buck-boost regulator

The device can be used to implement a step-up/down converter with a positive output voltage. The figure below shows the schematic circuit of this topology for a 12 V output voltage.

The input voltage can range from 5 V and 35 V. The output voltage is given by $V_O=V_{IN} \cdot D/(1-D)$, where D is the duty cycle. The maximum output current is given by $I_{OUT}=1\times (1-D)$. The current capability is reduced by the term (1-D) and so, for example, with a duty cycle of 0.5, and considering on average current through the switch of 2 A, the maximum output current deliverable to the load is 1 A. This is due to the fact that the current flowing through the internal power switch is delivered to the output only during the OFF phase.

Figure 24. Positive buck-boost regulator

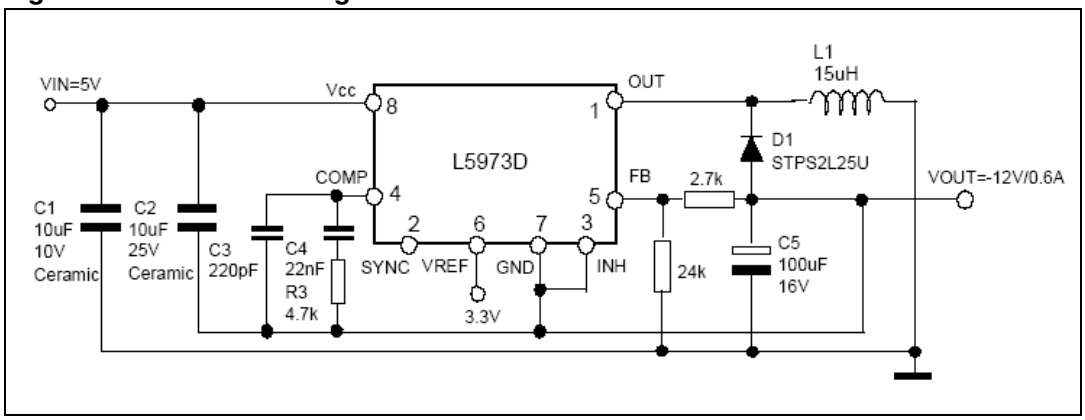


10.2 Buck-boost regulator

In *Figure 25*, the schematic circuit for a standard buck-boost topology is shown. The output voltage is given by $V_O=-V_{IN} \cdot D/(1-D)$.

The maximum output current is equal to $I_{OUT}=1 \cdot (1-D)$, for the same reason as that of the up/down converter. An important thing to take into account is that the ground pin of the device is connected to the negative output voltage. Therefore, the device is subjected to a voltage equal to V_{IN}-V_O, which must be lower than 36 V (the maximum operating input voltage).

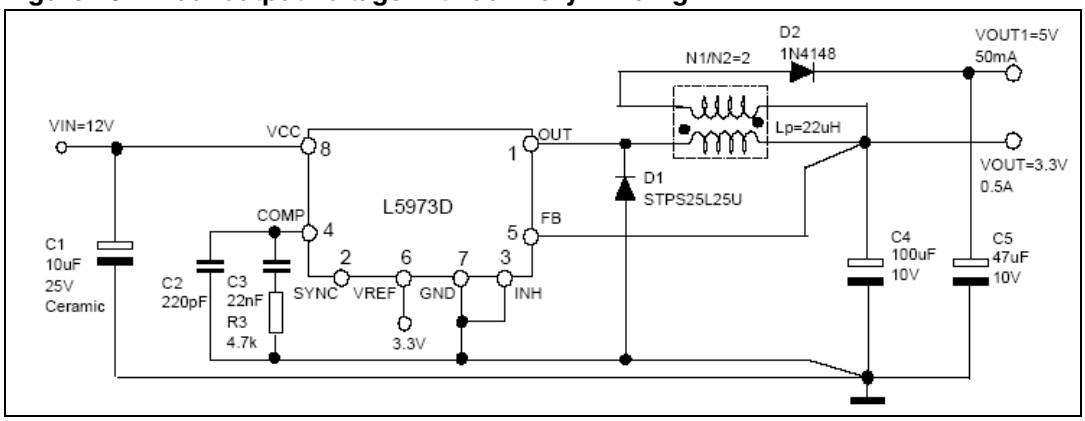
Figure 25. Buck-boost regulator



10.3 Dual output voltage with auxiliary winding

When two output voltages are required, it is possible to create a dual output voltage converter by using a coupled inductor. During the ON phase, the current is delivered to V_{OUT} while D2 is reverse-biased. During the OFF phase, the current is delivered, through the auxiliary winding, to the output voltage V_{OUT1}. This is possible only if the magnetic core has stored sufficient energy. So, to be certain that the application is working properly, the load related to the second output V_{OUT1} should be much lower than the load related to V_{OUT}.

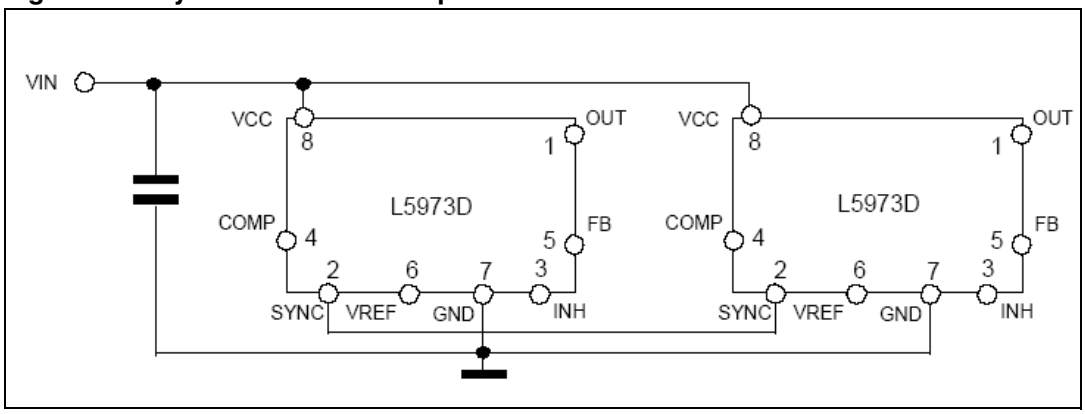
Figure 26. Dual output voltage with auxiliary winding



10.4 Synchronization example

Two or more devices (up to 6) can be synchronized simply by connecting the synchronization pins. In this case, the device with a slightly higher switching frequency value will work as a master and the ones with slightly lower switching frequency values will work as slaves. The device can also be synchronized from an external source. In this case the logic signal must have a frequency higher than the internal switching frequency of the device (250 kHz).

Figure 27. Synchronization example



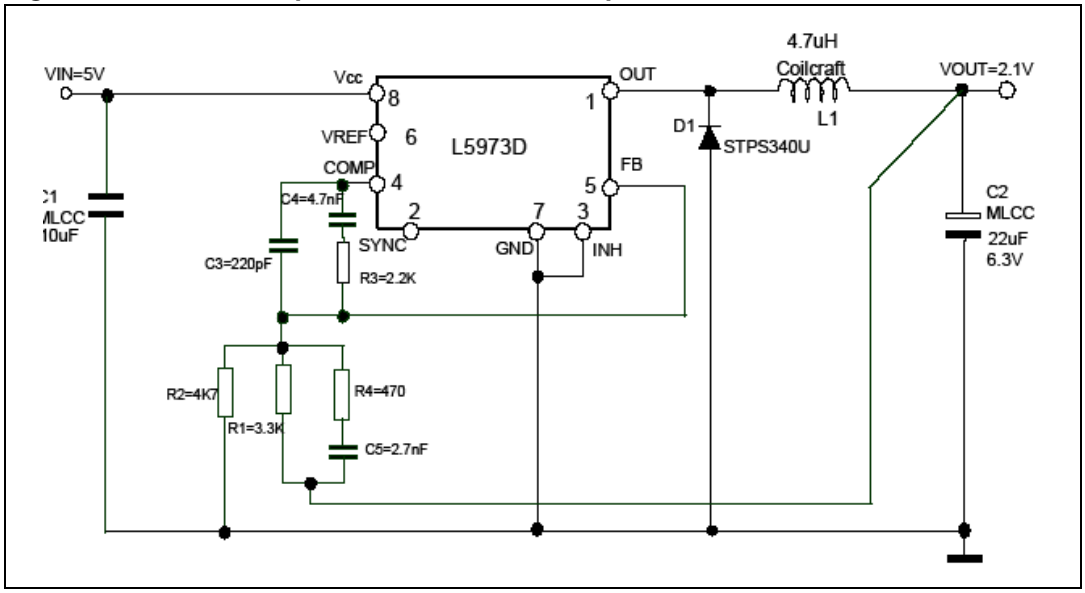
10.5 Compensation network with MLCC (multiple layer ceramic capacitor) at the output

MLCCs with values in the range of 10 µF-22 µF and rated voltages in the range of 10 V-25 V are available today at relatively low cost from many manufacturers.

These capacitors have very low ESR values (a few mΩ) and thus are occasionally used for the output filter in order to reduce the voltage ripple and the overall size of the application.

However, a very low ESR value affects the compensation of the loop (see *Section 5*) and in order to keep the system stable, a more complicated compensation network may be required. The figure below shows an example of a compensation network stabilizing the system with ceramic capacitors at the output (the optimum component value depends on the application).

Figure 28. MLCC compensation network example

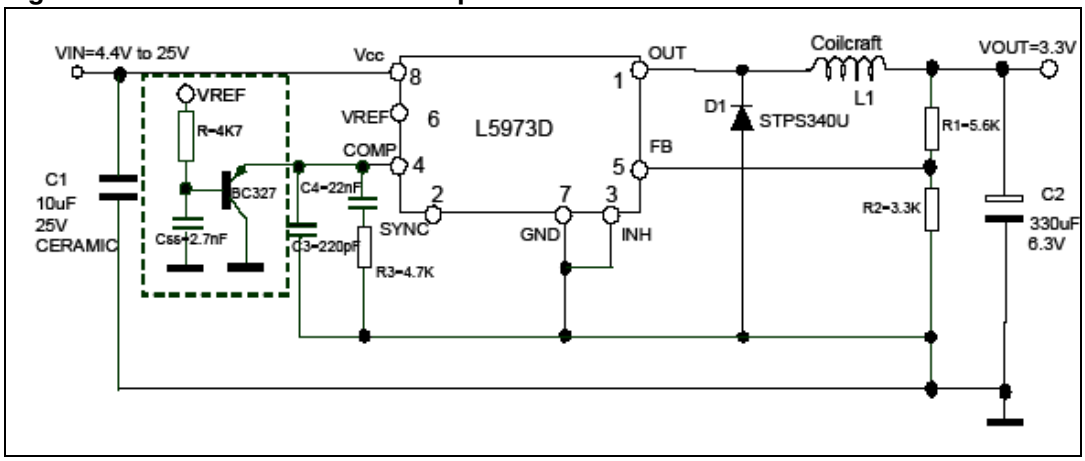


10.6 External SOFT_START network

At start-up the device can quickly increase the current up to the current limit in order to charge the output capacitor. If soft ramp-up of the output voltage is required, an external soft-start network can be implemented as shown in *Figure 29*. The capacitor C is charged up to an external reference through R and the B_{JT} clamps the COMP pin.

This clamps the duty cycle, limiting the slew rate of the output voltage.

Figure 29. Soft start network example



11 Revision history

Table 7. Document revision history

Date	Revision	Changes
07-Sep-2003	1	First release
05-Oct-2006	2	– New template – *Table 3* added
22-May-2007	3	– *Section 5: Closing the loop* modified
31-Jan-2008	4	– Minor text changes – Document title modified

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