KH103

Fast Settling, High Current Wideband Op Amp

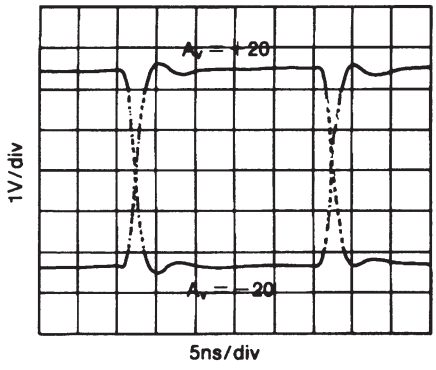
Features

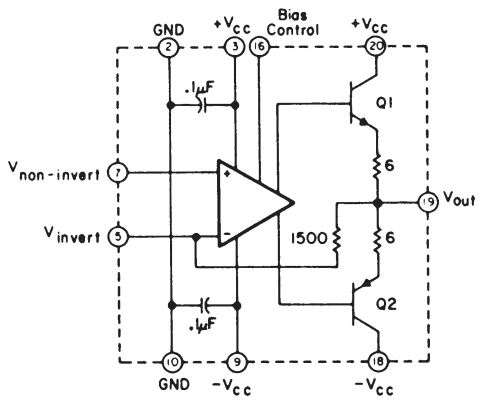
- 80MHz full-power bandwidth ($20V_{pp}$, 100Ω)
- 200mA output current
- 0.4% settling in 10ns
- 6000V/μs slew rate
- 4ns rise and fall times (20V)
- Direct replacement for CLC103

Applications

- Coaxial line driving
- DAC current to voltage amplifier
- Flash A to D driving
- Baseband and video communications
- Radar and IF processors

Small Signal Pulse Response





Typical Performance

parameter	gain setting						units
	+4	+20	+40	−4	−20	−40	
−3dB bandwidth	230	150	130	155	145	125	MHz
rise time (20V)	4	4	4	4	4	4	ns
slew rate	6	6	6	6	6	6	V/ns
settling time (0.4%)	10	10	12	10	10	12	ns

General Description

The KH103 is a high-power, wideband op amp designed for the most demanding high-speed applications. The wide bandwidth, fast settling, linear phase, and very low harmonic distortion provide the designer with the signal fidelity needed in applications such as driving flash A to Ds. The 80MHz full-power bandwidth and 200mA output current of the KH103 eliminate the need for power buffers in most applications; the KH103 is an excellent choice for driving large high-speed signals into coaxial lines.

In the design of the KH103 special care was taken in order to guarantee that the output settle quickly to within 0.4% of the final value for use with ultra fast flash A to D converters. This is one of the most demanding of all op amp requirements since settling time is affected by the op amps bandwidth, passband gain flatness, and harmonic distortion. This high degree of performance ensures excellent performance in many other demanding applications as well.

The dynamic performance of the KH103 is based on a current feedback topology that provides performance far beyond that available from conventional op amp designs. Unlike conventional op amps where optimum gain-bandwidth product occurs at a high gain, minimum settling time at a gain of -1, and maximum slew rate at a gain of +1, the KH103 provides consistent predictable performance across its entire gain range. For example, the table below shows how the -3dB bandwidth remain nearly constant over a wide range of gains. And since the amplifier is inherently stable, no external compensation is required. The result is shorter design time and the ability to accommodate design changes (in gain, for example) without loss of performance or redesign of compensation circuits.

The KH103 is constructed using thin film resistor/ bipolar transistor technology, and is available in the following versions:

KH103AI	-25°C to +85°C	24-pin Ceramic DIP
KH103AK	-55°C to +125°C	24-pin Ceramic DIP, features burn-in and hermetic testing
KH103AM	-55°C to +125°C	24-pin Ceramic DIP, environmentally screened and electronically tested to MIL-STD-883

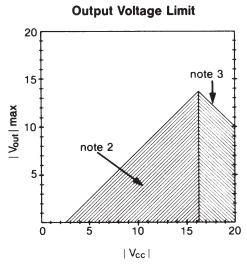
KH103 Electrical Characteristics (A_V = +20V, V_{CC} = ±15V, R_L = 100Ω; unless noted)

PARAMETERS	CONDITIONS	TYP	MAX & MIN RATINGS[1]			UNITS	SYMBOL
Ambient Temperature	KM103AK/AM	+25°C	−55°C	+25°C	+125°C		
Ambient Temperature	KM103AI	+25°C	−25°C	+25°C	+85°C		
FREQUENCY DOMAIN RESPONSE							
† −3dB bandwidth	V_{out} <4V_{pp}	150	>125	>135	>120	MHz	SSBW
gain flatness	V_{out} <4V_{pp}						
† peaking	0.1 to 50MHz	0.1	<0.6	<0.3	<0.3	dB	GFPL
† peaking	>50MHz	0.2	<1.5	<0.6	<0.6	dB	GFPH
† rolloff	at 100MHz	—	<0.4	<0.6	<0.8	dB	GFR
group delay	to 75MHz	3.0	—	—	—	ns	GD
linear phase deviation	to 75MHz	1	<3	<2	<4	°	LPD
reverse isolation – non-inverting	to 150MHz	55	>45	>45	>45	dB	RINI
TIME DOMAIN RESPONSE							
rise and fall time	5V step	2.3	<2.8	<2.6	<2.9	ns	TRS
	20V step	4	<5	<5	<5	ns	TRL
settling time to 0.4%	10V step	10	<25	<20	<25	ns	TSP
overshoot	5V step	5	<15	<10	<10	%	OS
slew rate (overdriven input)		6	>5	>5	>5	V/ns	SR
overload recovery							
<50ns pulse, 200% overdrive		30	—	—	—	ns	OR
DISTORTION AND NOISE RESPONSE							
†2nd harmonic distortion	$2V_{pp}$, 20MHz	−48	<−40	<−40	<−40	dBc	HD2
†3rd harmonic distortion	$2V_{pp}$, 20MHz	−48	<−40	<−40	<−40	dBc	HD3
equivalent input noise							
noise floor	>100kHz	−158	<−152	<−152	<−152	dBm(1Hz)	SNF
integrated noise	1kHz to 100MHz	28	<56	<56	<56	μV	INV
noise floor	>5MHz	−158	<−152	<−152	<−152	dBm(1Hz)	SNF
integrated noise	5MHz to 100MHz	28	<56	<56	<56	μV	INV
STATIC, DC PERFORMANCE							
*input offset voltage		10	<30	<25	<30	mV	VIO
average temperature coefficient		35	<120	<120	<120	μV/°C	DVIO
*input bias current	non-inverting	10	<40	<30	<40	μA	IBN
average temperature coefficient		20	<125	<125	<125	nA/°C	DIBN
*input bias current	inverting	20	<110	<60	<110	μA	IBI
average temperature coefficient		250	<500	<500	<500	nA/°C	DIBI
*power supply rejection ratio		54	>45	>45	>45	dB	PSRR
common mode rejection ratio		38	>30	>30	>30	dB	CMRR
*supply current	no load	30	<36	<34	<36	mA	ICC
MISCELLANEOUS PERFORMANCE							
non-inverting input	resistance	250	>100	>100	>100	kΩ	RIN
	capacitance	2.4	<3	<3	<3	pF	CIN
output impedance	at DC	—	<0.1	<0.1	<0.1	Ω	RO
	at 100MHz	2, 45	—	—	—	Ω, nH	ZO
output voltage range	no load	—	>±11	>±11	>±11	V	VO

Min/max ratings are based on product characterization and simulation. Individual parameters are tested as noted. Outgoing quality levels are determined from tested parameters.

Absolute Maximum Ratings

V_{CC} (reversed supplies will destroy part)		±20V
junction temperature (see thermal model)		+175°C
thermal resistance		see thermal model
storage temperature		-65°C to +150°C
lead temperature (soldering 10s)		+300°C
output current		±200mA
operating temperature:	AI	-25°C to +85°C
	AK, AM	-55C to +125°C

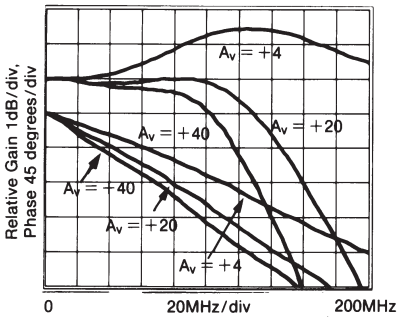


Notes

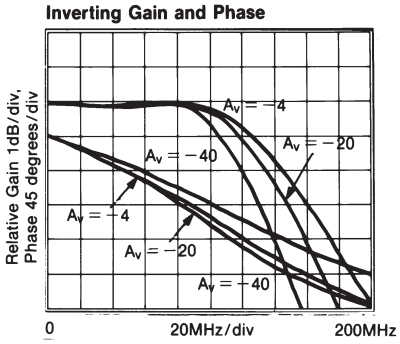
1) * AI, AK, AM 100% tested at +25°C
   † AK, AM 100% tested at at +25°C and sample tested at -55°C and +125°C
   † AI sample tested at +25°C
2) This rating protects against damage to the input stage caused by saturation of either the input or output stages. Under transient conditions not exceeding 1μs (duty cycle not exceeding 10% maximum input voltage may be as large as twice the maximum V_{cm} should never exceed ±5V. (V_{cm} is the voltage at the non-inverting input, pin 7).
3) This rating protects against exceeding transistor collector-emitter breakdown ratings. Recommended V_{CC} is ±15V.

KH103 Performance Characteristics (A_V = +20°C, V_{CC} = ±15V, R_L = 100Ω; unless noted)

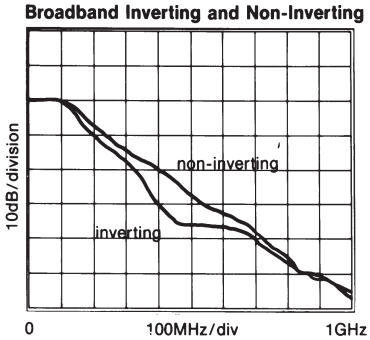
Non-Inverting Gain and Phase



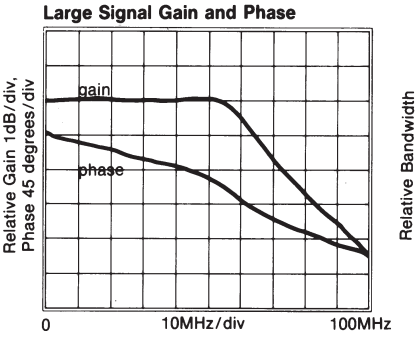
Inverting Gain and Phase



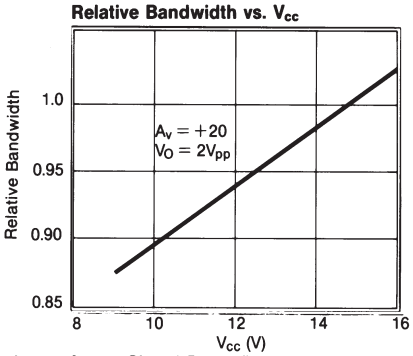
Broadband Inverting and Non-Inverting Gain



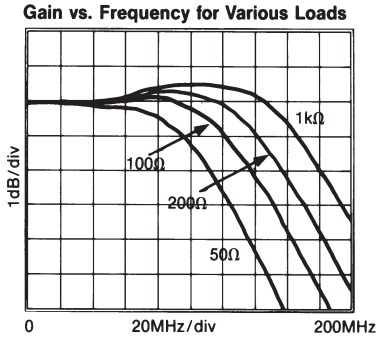
Large Signal Gain and Phase



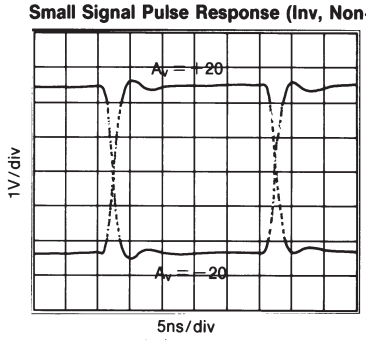
Relative Bandwidth vs. V_{cc}



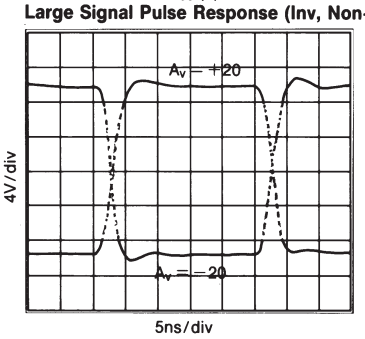
Gain vs. Frequency for Various Loads



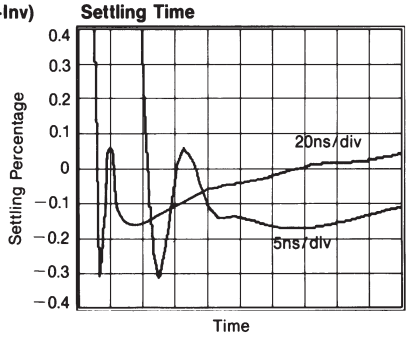
Small Signal Pulse Response (Inv, Non-Inv)



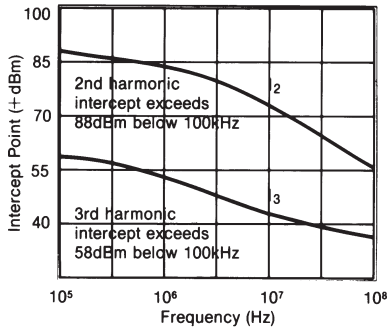
Large Signal Pulse Response (Inv, Non-Inv)



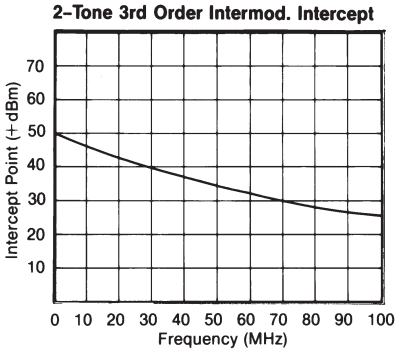
Settling Time



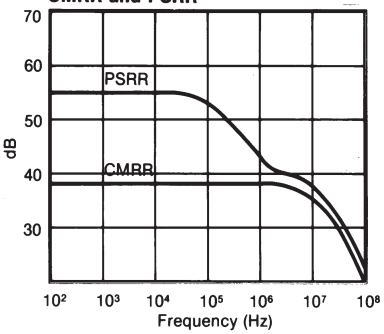
2nd and 3rd Harmonic Distortion Intercept



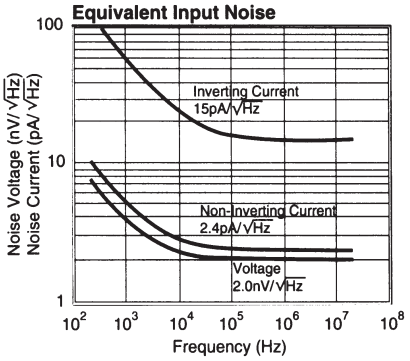
2-Tone 3rd Order Intermod. Intercept

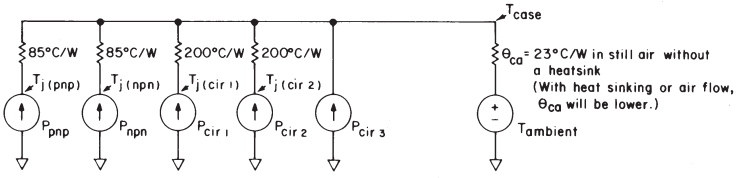


CMRR and PSRR



Equivalent Input Noise





P_{cir1} = 10mA [(+V_{cc})−V_{out}]
P_{cir2} = 10mA [V_{out} −(−V_{cc})]
P_{cir3} = I_C [(+V_{cc}) −(−V_{cc})] where I_C = 10mA at ±15V
P_{XXX} = I_{col} [(±V_{cc})−V_{out} −I_{col} (R_{col} +6)] where I_{col} = V_{out}/R_{load} or 9mA, whichever is greater. (Include R_f in R_{load}.)

(For positive V_{out} and V_{cc}, P_{XXX} is the power in the npn device. For negative V_{out} and V_{cc}, this power is in the pnp device.)
R_{col} is an external resistor (22 ohms recommended) between the xxx collector and ±V_{cc}.
$T_{j\,(pnp)}$ = (P_{pnp}) 85°C/W + (P_{total}) θ_{ca} + $T_{ambient}$, similar for $T_{j\,(npn)}$.
$T_{j\,(cir1)}$ = (P_{cir1}) 200°C/W + (P_{total}) θ_{ca} + $T_{ambient}$, similar for $T_{j\,(cir2)}$.

KH103 Operation

The KH103 is based on a unique design which uses current feedback instead of the usual voltage feedback. This design provides dynamic performance far beyond that previously available, yet it is used basically the same as the familiar voltage-feedback op amp (see the gain equations above).

Layout Considerations

To obtain optimum performance from any circuit operating at high frequencies, good PC layout is essential. Fortunately, the stable, well-behaved response of the KH103 makes operation at high frequencies less sensitive to layout than is the case with other wideband op amps, even though the KH103 has a much wider bandwidth.

In general, a good layout is one which minimizes the unwanted coupling of a signal between nodes in a circuit. A continuous ground plane from the signal input to output on the circuit side of the board is helpful. Traces should be kept short to minimize inductance. If long traces are needed, use microstrip transmission lines which are terminated in their characteristic impedance. At some high-impedance nodes, or in sensitive areas such as near pin 5 of the KH103, stray capacitance should be kept small by keeping nodes small and removing ground plans directly around the node.

The $\pm V_{CC}$ connections to the KH103 are internally bypassed to ground with 0.1μF capacitors to provide good high-frequency decoupling. It is recommended that 1μF or larger tantalum capacitors be provided for low-frequency decoupling. The 0.01μF capacitors shown at pins 18 and 20 in figures 1 and 2 should be kept within 0.1" of those pins. A wide strip of ground plane should be provided for a signal return path between the load-resistors ground and these capacitors.

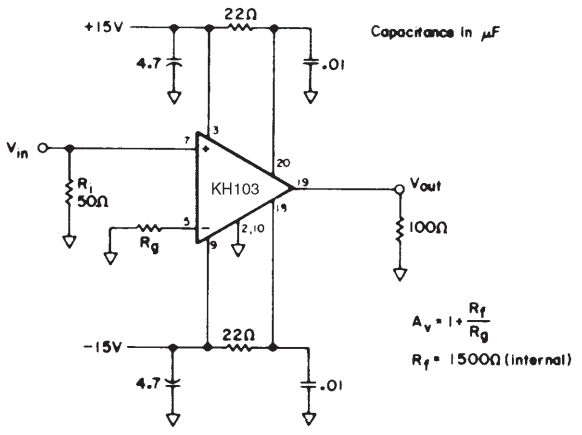


Figure 1: Recommended Non-Inverting Gain Circuit

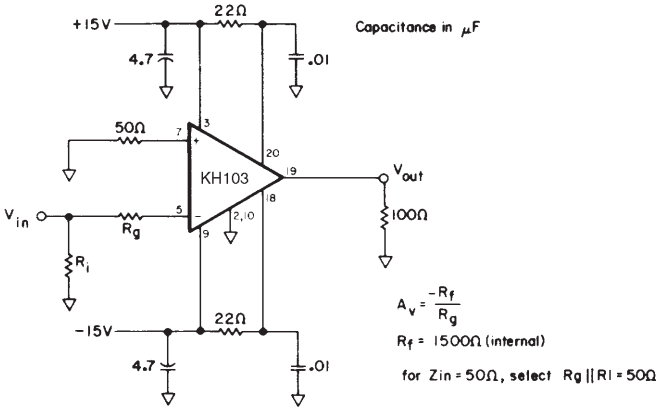


Figure 2: Recommended Inverting Gain Circuit

Since the layout of the PC board forms such an important part of the circuit, much time can be saved if prototype amplifier boards are tested early in the design stage.

Settling Time, Offset, and Drift

After an output transition has occurred. the output settles very rapidly to the final value and no change occurs for several microseconds. Thereafter, thermal gradients inside the KH103 will cause the output to begin to drift. When this cannot be tolerated, or when the initial offset voltage and drift is unacceptable, use of a composite amplifier is advised.

A composite amplifier can also be referred to as a feed-forward amplifier. Most feed-forward techniques such as those used In the vast majority of wideband op amps involve the use of a wideband AC-coupled channel in parallel with a low-bandwidth, high-gain DC-coupled amplifier. For the composite amplifier suggested for use with the KH103, the KH103 replaces the wideband AC-coupled amplifier and a low-cost monolithic op amp is used to supply high open-loop gain at low frequencies. Since the KH103 is strictly DC coupled throughout, crossover distortion of less than 0.01dB and 1° results.

For composite operation in the non-inverting mode, the circuit in Figure 1 should be modified by the addition of the circuit shown in Figure 3. For Inverting operation, modify the circuit in Figure 2 by the addition of the circuit in Figure 4. Keep all resistors which connect to the KH103 within 0.2" of the KH103 pins. The other side of these resistors should likewise be as close to U1 as possible. For good overall results, U1 should be similar to the LF356; this gives 5mV/°C input offset drift and the crossover frequency occurs at about 2MHz. Since U1 has a feedback network composed of R_a + R_b and a 15kΩ resistor, which is in parallel with R_g and the internal 1.5kΩ feedback resistor of the KH103, R_b must be adjusted to match the feedback ratios of the two networks. This in done by driving the composite amplifier

with a 70kHz square wave large enough to produce a transition from +5V to -5V at the KH103 output and adjusting R_b until the output of U1 is at a minimum. R_a should be about $9.5R_g$ for bad results; thus, R_b should be adjusted around the value of $0.5R_g$.

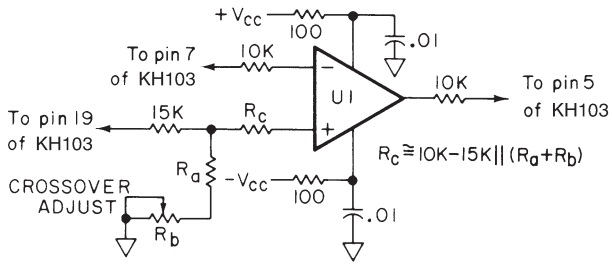


Figure 3: Non-Inverting Gain Composite Amplifier to be Used with Figure 1 Circuit

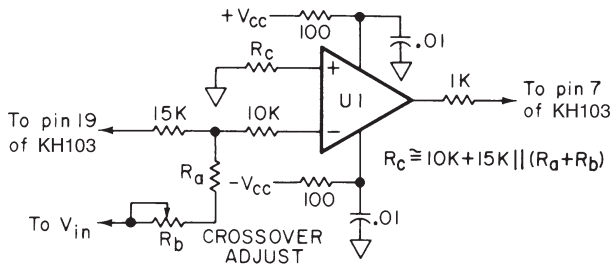


Figure 4: Inverting Gain Composite Amplifier to be Used with Figure 2 Circuit

Bias Control

In normal operation, the bias control pin (pin 16) is left unconnected. However, if control over the bias of the amplifier is desired, the bias control pin may be driven with a TTL signal; a TTL high level will turn the amplifier off.

Distortion and Noise

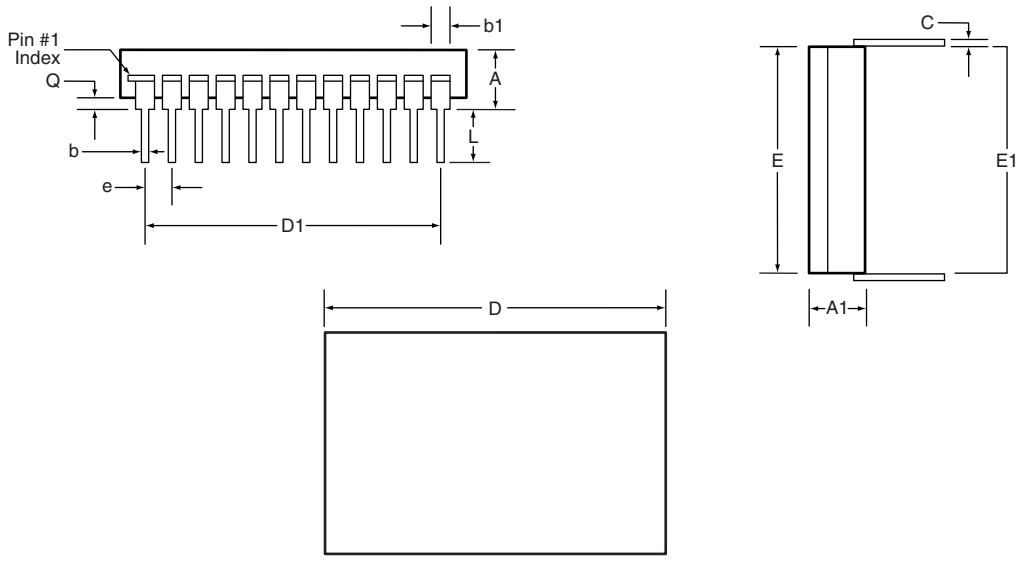
The graphs of intercept point versus frequency on the page 3 make it easy to predict the distortion at any frequency, given the output voltage of the KH103. First convert the output voltage V_o to $V_{rms} = (V_{pp}/2\sqrt{2})$ and then to $P = (10\log_{10}(20V_{rms}^2))$ to get the output power in dBm. At the frequency of interest, its 2nd harmonic will be $S_2 = (I_2 - P)$ dB below the level of P. Its third harmonic will be $S_3 = 2(I_3 - P)$ dB below the level of P, as will the two-tone third order intermodulation products. These approximations are useful for P < -1dB compression levels.

Approximate noise figure can determined for the KH103 using the Equivalent Input Noise graph on page 3. The following equation can be used to determine noise figure (F) in dB.

$$F = 10\log\left[1 + \frac{v_n^2 + \frac{i_n^2 R_F^2}{A_v^2}}{4kTR_s\Delta f}\right]$$

where v_n is the rms noise voltage and i_n is the rms noise current. Beyond the breakpoint of the curves (i.e. where they are flat) broadband noise figure equals spot noise, so Δf should equal one (1) and v_n and i_n should be read directly off the graph. Below the breakpoint, the noise must be integrated and Δf set to the appropriate bandwidth.

KH103 Package Dimensions



Symbol	Inches		Milimeters	
	Minimun	Maximum	Minimum	Maximum
A-Metal Lid	0.180	0.240	4.57	6.10
A-Ceramic Lid	0.195	0.255	4.95	6.48
A1-Metal Lid	0.145	0.175	3.68	4.45
A1-Ceramic Lid	0.160	0.190	4.06	4.83
b	0.014	0.026	0.36	0.66
b1	0.050 BSC		1.27 BSC	
c	0.008	0.018	0.20	0.46
D	1.275	1.310	33.39	33.27
D1	1.095	1.105	27.81	28.07
E	0.785	0.815	19.94	20.70
E1	0.790	0.810	20.07	20.57
e	0.100 BSC		2.54 BSC	
L	0.165 BSC		4.19 BSC	
Q	0.015	0.075	0.38	1.91

NOTES:

NOTES:

Seal: seam weld (AM, AK), epoxy (AI)
Lead finish: gold finish
Package composition:
Package: ceramic
Lid: kovar/nickel (AM, AK), ceramic (AI)
Leadframe: alloy 42
Die attach: epoxy

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