CY2XL11

100 MHz LVDS Clock Generator

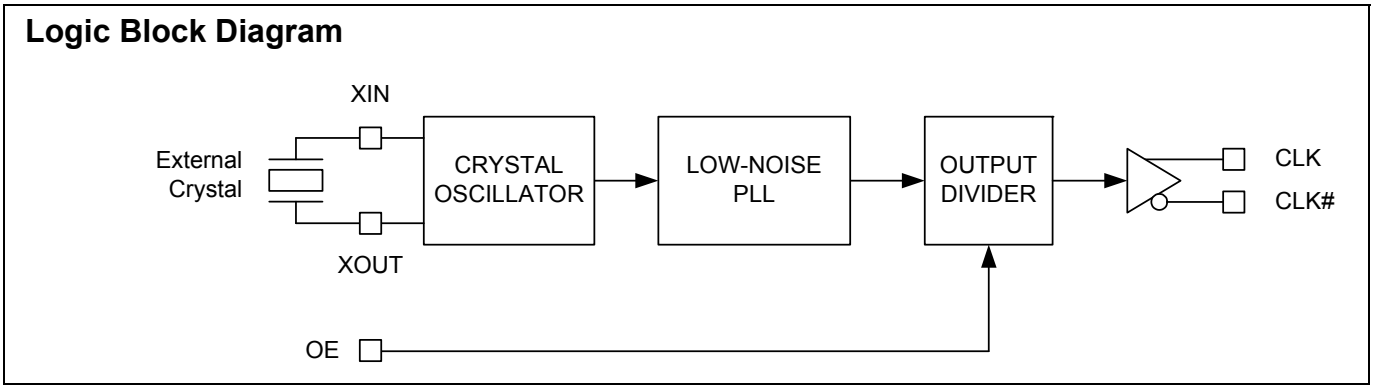
Features

- One LVDS Output Pair
- Output Frequency: 100 MHz
- External Crystal Frequency: 25 MHz
- Low RMS Phase Jitter at 100 MHz, using 25 MHz Crystal (637 kHz to 10 MHz): 0.53 ps (Typical)
- Pb-free 8-Pin TSSOP Package
- Supply Voltage: 3.3V or 2.5V
- Commercial Temperature Range

Functional Description

The CY2XL11 is a PLL (Phase Locked Loop) based high performance clock generator with a crystal oscillator interface and one LVDS output pair. It is optimized to generate PCI Express, FC, and other high performance clock frequencies. It also produces an output frequency that is four times the crystal frequency. It uses Cypress's low noise VCO technology to achieve less than 1 ps typical RMS phase jitter, that meets high performance systems' jitter requirements.

Logic Block Diagram



Pinouts

Figure 1. Pin Diagram - 8-Pin TSSOP



Table 1. Pin Definition - 8-Pin TSSOP

Pin Number	Pin Name	I/O Type	Description
1, 8	VDD	Power	3.3V or 2.5V power supply. All supply current flows through pin 1
2	VSS	Power	Ground
3, 4	XOUT, XIN	XTAL output and input	Parallel resonant crystal interface
5	OE	CMOS input	Output Enable. When HIGH, the output is enabled. When LOW, the output is high impedance
6,7	CLK#, CLK	LVDS output	Differential clock output

Frequency Table

Input Crystal Frequency (MHz)	PLL Multiplier Value	Output Frequency (MHz)
25	4	100

Absolute Maximum Conditions

Parameter	Description	Condition	Min	Max	Unit
V_{DD}	Supply Voltage		–0.5	4.4	V
V_{IN}[1]	Input Voltage, DC	Relative to V_{SS}	–0.5	V_{DD} + 0.5	V
T_S	Temperature, Storage	Non operating	–65	150	°C
T_J	Temperature, Junction			135	°C
ESD_{HBM}	ESD Protection (Human Body Model)	JEDEC STD 22-A114-B	2000		V
UL–94	Flammability Rating	At 1/8 in.	V–0		
Θ_{JA}[2]	Thermal Resistance, Junction to Ambient	0 m/s airflow	100		°C/W
		1 m/s airflow	91		
		2.5 m/s airflow	87		

Operating Conditions

Parameter	Description	Min	Max	Unit
V_{DD}	3.3V Supply Voltage	3.135	3.465	V
	2.5V Supply Voltage	2.375	2.625	V
T_A	Ambient Temperature	–5	70	°C
T_{PU}	Power up time for all V_{DD} to reach minimum specified voltage (ensure power ramps is monotonic)	0.05	500	ms

DC Electrical Characteristics

Parameter	Description	Test Conditions	Min	Typ	Max	Unit
I_{DD}[4]	Power Supply Current with output terminated	V_{DD} = 3.465V, OE = V_{DD}, output terminated	–	–	120	mA
		V_{DD} = 2.625V, OE = V_{DD}, output terminated	–	–	115	mA
V_{OD}[6]	LVDS Differential Output Voltage	V_{DD} = 3.3V or 2.5V, R_{TERM} = 100Ω between CLK and CLK#	250	–	450	mV
ΔV_{OD}[6]	Change in V_{OD} between Complementary Output States	V_{DD} = 3.3V or 2.5V, R_{TERM} = 100Ω between CLK and CLK#	–	–	50	mV
V_{OS}[7]	LVDS Offset Output Voltage	V_{DD} = 3.3V or 2.5V, R_{TERM} = 100Ω between CLK and CLK#	1.125	–	1.375	V
ΔV_{OS}	Change in V_{OS} between Complementary Output States	V_{DD} = 3.3V or 2.5V, R_{TERM} = 100Ω between CLK and CLK#	–	–	50	mV
I_{OZ}	Output Leakage Current	Three-state output, PD#/OE = V_{SS}	–35	–	35	µA

Notes
1. The voltage on any input or IO pin cannot exceed the power pin during power up.
2. Simulated using Apache Sentinel TI software. The board is derived from the JEDEC multilayer standard. It measures 76 x 114 x 1.6 mm and has 4-layers of copper (2/1/1/2 oz.). The internal layers are 100% copper planes, while the top and bottom layers have 50% metalization. No vias are included in the model.
3. Outputs are terminated with 100Ω between CLK and CLK#. Refer to Figure 8 on page 5.
4. I_{DD} includes ~4 mA of current that is dissipated externally in the output termination resistor.
5. Not 100% tested, guaranteed by design and characterization.
6. Refer to Figure 2 on page 4.
7. Refer to Figure 3 on page 4.

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DC Electrical Characteristics (continued)

Parameter	Description	Test Conditions	Min	Typ	Max	Unit
V_{IH}	Input High Voltage, OE pin		0.7*V_{DD}	–	–	V
V_{IL}	Input Low Voltage, OE pin		–	–	0.3*V_{DD}	V
I_{IH}	Input High Current, OE pin	OE = V_{DD}	–	–	115	µA
I_{IL}	Input Low Current, OE pin	OE = V_{SS}	–50	–	–	µA
C_{IN}	Input Capacitance, OE pin			15		pF
C_{INX}	Pin Capacitance, XIN & XOUT			4.5		pF

AC Electrical Characteristics[3]

Parameter	Description		Min	Typ	Max	Unit
F_{OUT}	Output Frequency		–	100	–	MHz
T_R, T_F[8]	Output Rise or Fall time	20% to 80% of full output swing	–	500	–	ps
$T_{Jitter(\phi)}$[11]	RMS Phase Jitter (Random)	F_{UT} =100 MHz, (637 kHz–10 MHz)	–	0.53	–	ps
T_{DC}[9]	Duty Cycle	Measured at zero crossing point	45	–	55	%
T_{OHZ}[10]	Output Disable Time	Time from falling edge on OE to stopped outputs (Asynchronous)	–	–	100	ns
T_{OE}[10]	Output Enable Time	Time from rising edge on OE to outputs at a valid frequency (Asynchronous)	–	–	100	ns
T_{LOCK}	Startup Time	Time for CLK to reach valid frequency measured from the time V_{DD} = V_{DD}(min.)	–	–	10	ms

Crystal Characteristics

Parameter	Description	Min	Max	Unit
	Mode of Oscillation	Fundamental		
F	Frequency	25	25	MHz
ESR	Equivalent Series Resistance	–	50	Ω
C_S	Shunt Capacitance	–	7	pF

Notes
8. Refer to Figure 4 on page 4.
9. Refer to Figure 5 on page 4.
10. Refer to Figure 6 on page 4.
11. Refer to Figure 7 on page 5.

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Switching Waveforms

Figure 2. Output Voltage Swing

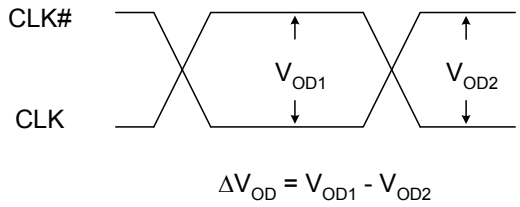


Figure 3. Output Offset Voltage

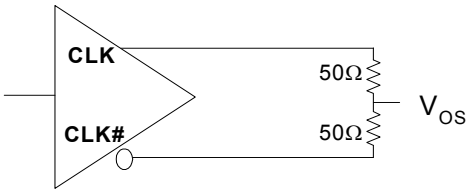


Figure 4. Output Rise or Fall Time

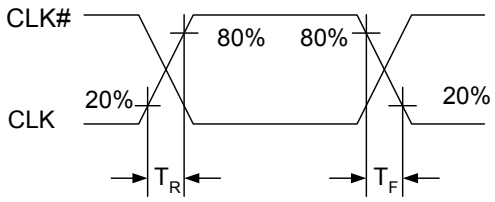


Figure 5. Duty Cycle Timing

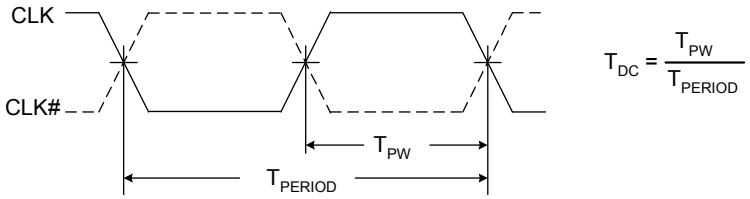
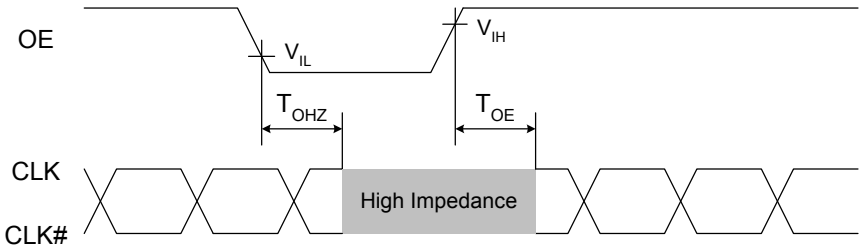
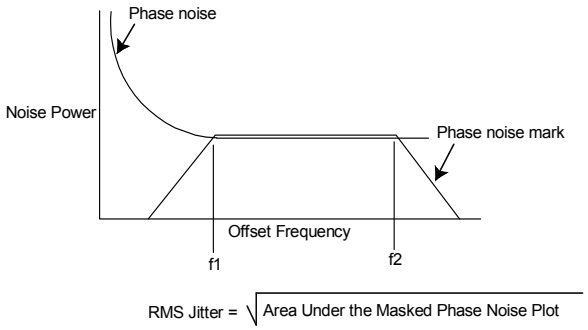


Figure 6. Output Enable and Disable Timing



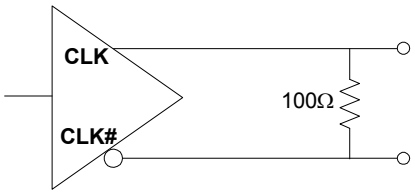
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Figure 7. RMS Phase Jitter



Termination Circuits

Figure 8. LVDS Termination



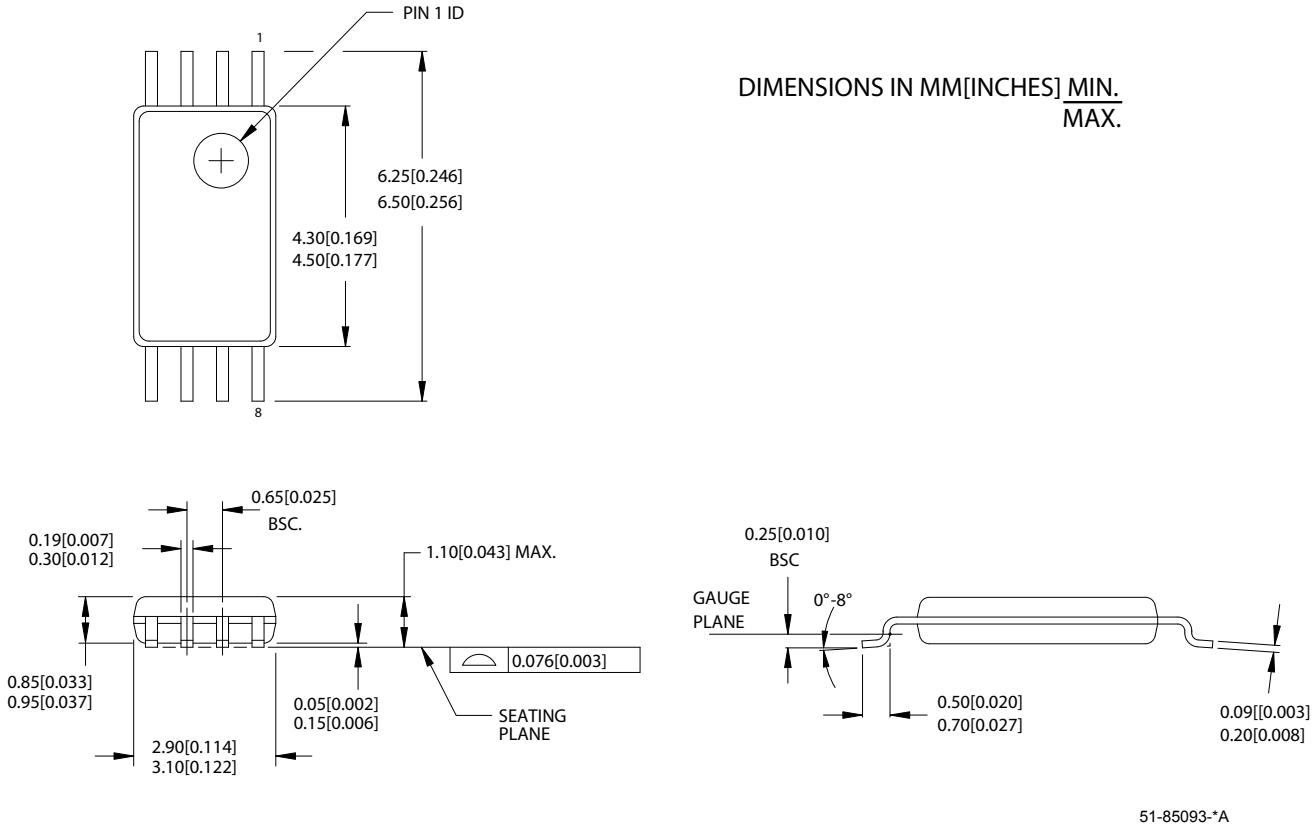
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Ordering Information

Part Number	Package Description	Product Flow
CY2XL11ZXC	8-pin TSSOP	Commercial, –5°C to 70°C
CY2XL11ZXCT	8-pin TSSOP - Tape and Reel	Commercial, –5°C to 70°C

Package Drawing and Dimensions

Figure 9. 8-Pin Thin Shrunk Small Outline Package (4.40 MM Body) Z8



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Document History Page

Document Title: CY2XL11 100 MHz LVDS Clock Generator Document Number: 001- 42886				
REV.	**ECN NO.**	**Submission Date**	**Orig. of Change**	**Description of Change**
**	2117527	See ECN	WWZ/KVM /AESA	New data sheet
*A	2669117	03/05/2009	KVM/ AESA	Changed crystal and output frequency Removed MSL spec Changed IIL value from -20 uA to -50 uA Changed IIH value from 20 uA to 115 uA Changed phase jitter value from 1 to 0.53 ps Changed junction temp from 125°C to 135°C Changed IDD from 150 mA to 120 mA Rise / fall time changed to 350 ps to 500ps Changed Data Sheet Status to Final
*B	2700242	04/30/2009	KVM/ PYRS	Typo correction Reformatted AC and DC tables Added IDD spec for 2.5V Added CINX and TLOCK specs Changed CIN from 7pF to 15pF
*C	2718433	06/12/2009	WWZ/HMT	No change. Submit to ECN for product launch.

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