DATA SHEET

GPCL A1/B1 Series

Low Power Sound Controller Series

Sep 15, 2015

Version 1.0

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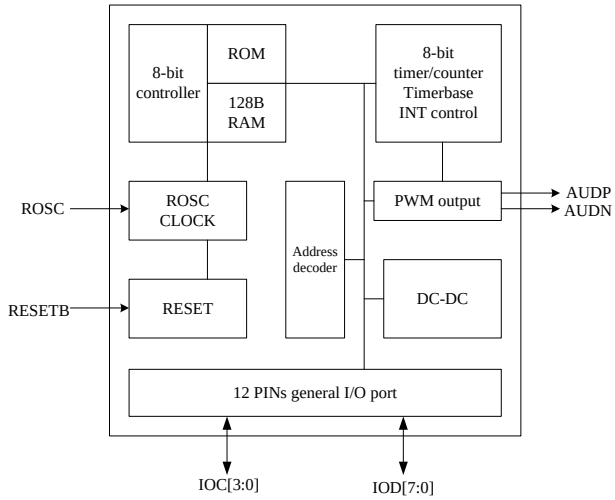
LOW POWER SOUND CONTROLLER SERIES

1. GENERAL DESCRIPTION

The GPCL A1/B1 series, a speech/wavetable synthesizer, features an 8-bit CMOS microprocessor, 128-byte working SRAM and working ROM (The different body equips different ROM size.). Other primary features include two 8-bit Timer/Counters, which can cascade to one 16-bit timer/counter, 12 Software Selectable I/Os and a pair of PWM output. It is designed for wide input voltage (1.0V ~ 1.7V; 1.3V~3.6V), and the circuit works at a stable and programmable pumped voltage (3.3V ~ 3.9V; 3.3V ~ 4.5V). Plus, a Clock Stop mode is built in for power savings. The unique power saving mode saves the RAM contents, but it freezes the oscillator to stop executing other functions. The maximum CPU frequency can run up to 6MHz and the instruction cycle is two clock cycles (min.) ~ six clock cycles (max.).

2. BLOCK DIAGRAM



3. FEATURES

- 8-bit microprocessor
- Working ROM (for size details, please refer to GPCL A1/B1 FAMILY LIST)
- 128-byte working SRAM
- Software-based audio processing
- Wide input voltage :
  1.0V~1.7V (one-battery , GPCLXXXA1)
  1.3V~3.6V (two-battery , GPCLXXXB1)
- Pumped voltage (DC-DC) for core power:
  3.3V~3.9V;Step:0.3V(one-battery , GPCLXXXA1)
  3.3V~4.5V;Step:0.3V(two-battery , GPCLXXXB1)
  *The output pumped voltage is greater than or equal to input voltage
- Operating clock: 6.0MHz
- Supports ROSC only
- Standby mode (Clock Stop mode) for power savings.
  Max. 5.0μA @1.5V (one-battery , GPCLXXXA1)
  Max. 10.0μA @ 3.0V (two-battery , GPCLXXXB1)
- 12 general I/Os
- Low Voltage Reset (LVR) function
- Two 8-bit timer/counters or combined to one 16-bit timer/counter
- Six INT sources
- Key wakeup function
- Watchdog function
- A pair of PWM outputs
- IR function

4. APPLICATION FIELD

- Intelligent education toys
  Ex. Pattern to voice (animal, car, color, etc.)
  Spelling (English or Chinese)
  Math
- Advanced toy controller
- General speech synthesizer

5. GPCL A1/B1 FAMILY LIST

Body	GPCL170A1	GPCL128A1	GPCL112A1	GPCL096A1	GPCL040A1	GPCL030A1	GPCL020A1	GPCL010A1
Voice Duration	170 Sec.	128 Sec.	112 Sec.	96 Sec.	40 Sec.	30 Sec.	20 Sec.	10 Sec.
Working Voltage	1.0V~1.7V (one-battery)	1.0V~1.7V (one-battery)	1.0V~1.7V (one-battery)	1.0V~1.7V (one-battery)	1.0V~1.7V (one-battery)	1.0V~1.7V (one-battery)	1.0V~1.7V (one-battery)	1.0V~1.7V (one-battery)
RAM Size	128B	128B	128B	128B	128B	128B	128B	128B
ROM Size	512KB	384KB	352KB	288KB	128KB	96KB	64KB	32KB

Body	GPCL170B1	GPCL128B1	GPCL112B1	GPCL096B1	GPCL040B1	GPCL030B1	GPCL020B1	GPCL010B1
Voice Duration	170 Sec.	128 Sec.	112 Sec.	96 Sec.	40 Sec.	30 Sec.	20 Sec.	10 Sec.
Working Voltage	1.3V~3.6V (two-battery)	1.3V~3.6V (two-battery)	1.3V~3.6V (two-battery)	1.3V~3.6V (two-battery)	1.3V~3.6V (two-battery)	1.3V~3.6V (two-battery)	1.3V~3.6V (two-battery)	1.3V~3.6V (two-battery)
RAM Size	128B	128B	128B	128B	128B	128B	128B	128B
ROM Size	512KB	384KB	352KB	288KB	128KB	96KB	64KB	32KB

6. SIGNAL DESCRIPTIONS

Mnemonic	Type	Description
RESETB	I	Reset pin, low active to reset whole system
IOD0	I/O	Bit-controlled programmable I/O pins
IOD1	I/O	In input mode, Port D can be either pure or pull-low state
IOD2	I/O	In output mode, Port D can be buffer
IOD3	I/O	Pins in Port D are the key wakeup I/O pins
IOD4	I/O	IOD6 : external interrupt
IOD5	I/O	IOD7: IR transmitter
IOD6	I/O	
IOD7	I/O	
IOC0	I/O	Nibble-controlled programmable I/O pins
IOC1	I/O	In input mode, Port C can be either pure or pull-low state. In output mode, Port C can be a buffer.
IOC2	I/O	
IOC3	I/O	
TEST	I	TEST pin, NC
ROSC	I	ROSC Resistor input (Resistor must be connected to VDD)
VDD	P	Digital Power Pad
VSS	P	Digital Ground
VIN	P	DC-DC: Power PAD
Lpump	I	DC-DC: Inductance input (Inductance must be connected to VIN)
VSSIN	P	DC-DC: Ground PAD
VDDO	P	DC-DC: Pumped voltage output
AUDP	O	Audio output
AVDD	P	PWM Power Pad
AVSS	P	PWM Ground Pad
AUDN	O	Audio output

7. FUNCTIONAL DESCRIPTIONS

7.1. CPU

The microprocessor in GPCL A1/B1 series is a high performance 8-bit processor equipped Accumulator, Program Counter, X and Y Register, Stack pointer and Processor Status Register (the same as the 6502 instruction structure). The maximum CPU speed of 6.0MHz is capable of bringing you clear speech and music as well as achieving the best performance.

7.2. RAM Area

The total RAM size is 128-byte (including Stack) starting from address $0080 through $00FF or mapping to $0180 through $01FF.

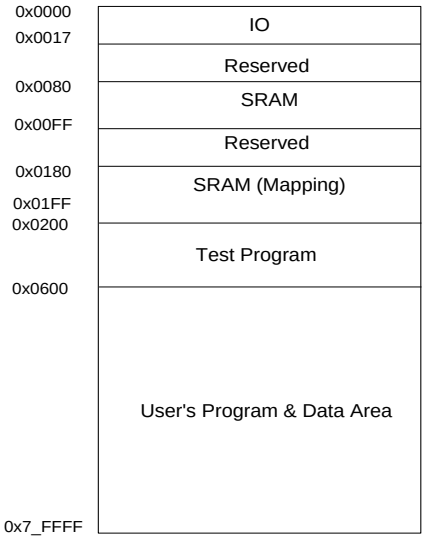
7.3. ROM Area

More details about GPCL A1/B1 series ROM size is listed in the following table. The ROM can be defined as the program area, audio data area or both. To access ROM, users shall program the BANK SELECT Register, choose bank, and access address to fetch data.

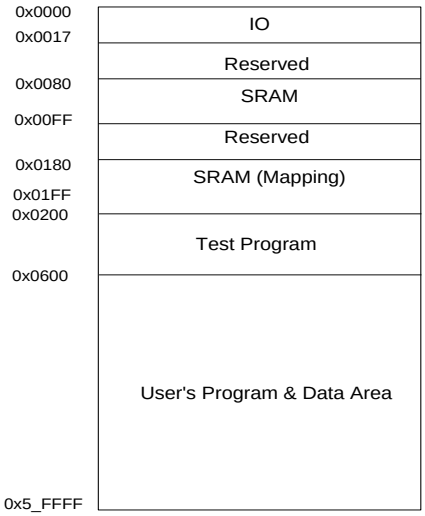
Body	ROM size	ROM Address
GPCL170A1 GPCL170B1	512KB	0x00600~0x7FFFF
GPCL128A1 GPCL128B1	384KB	0x00600~0x5FFFF
GPCL112A1 GPCL112B1	352KB	0x00600~0x57FFF
GPCL096A1 GPCL096B1	288KB	0x00600~0x47FFF
GPCL040A1 GPCL040B1	128KB	0x00600~0x1FFFF
GPCL030A1 GPCL030B1	96KB	0x00600~0x17FFF
GPCL020A1 GPCL020B1	64KB	0x00600~0x0FFFF
GPCL010A1 GPCL010B1	32KB	0x00600~0x07FFF

7.4. Map of Memory and I/Os

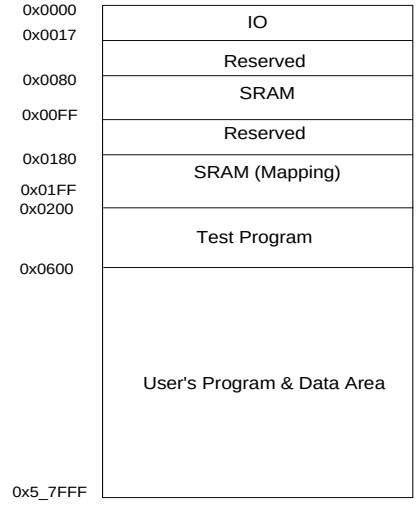
a. GPCL170A1, GPCL170B1



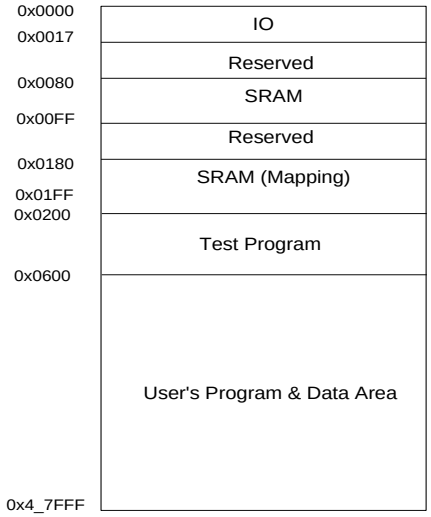
b. GPCL128A1 , GPCL128B1



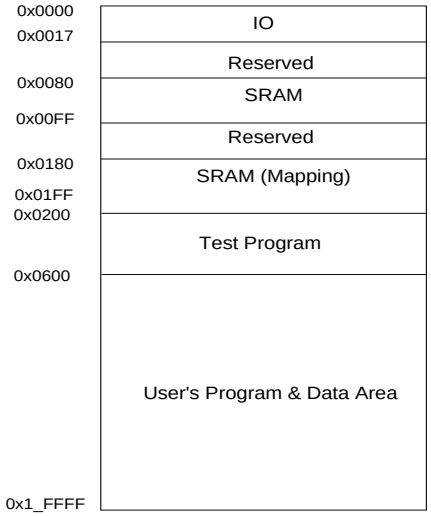
c. GPCL112A1 , GPCL112B1



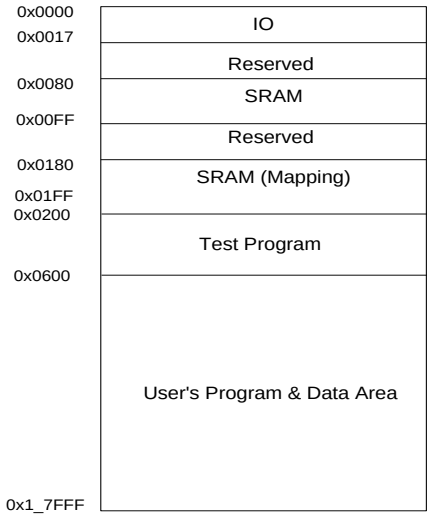
d. GPCL096A1 , GPCL096B1



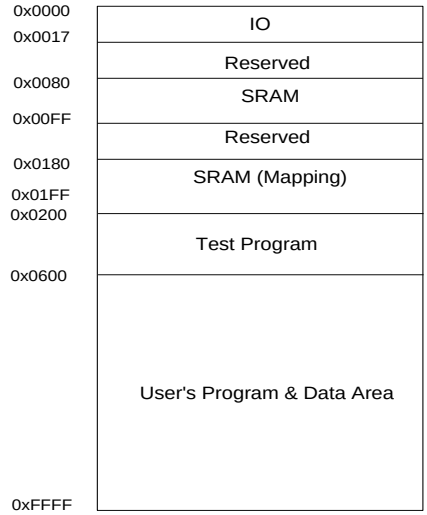
e. GPCL040A1 , GPCL040B1



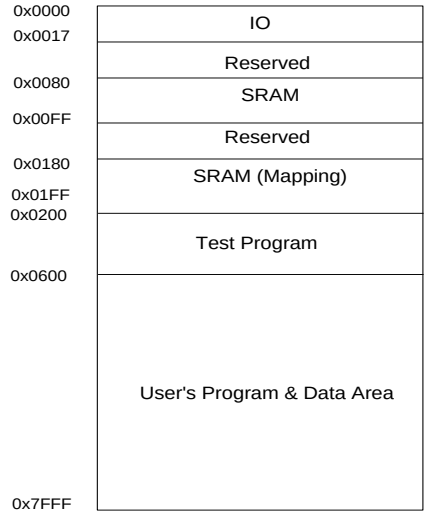
f. GPCL030A1 , GPCL030B1



g. GPCL020A1, GPCL020B1



h. GPCL010A1 , GPCL010B1

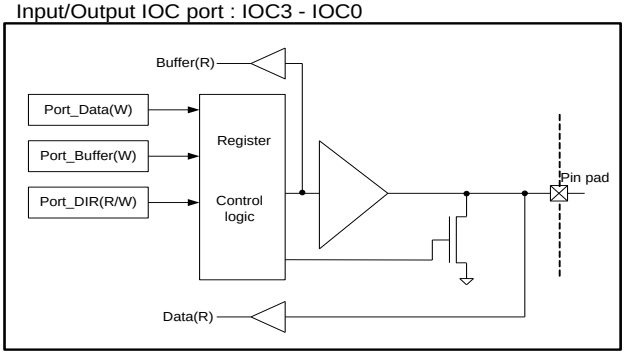


7.5. I/O Port

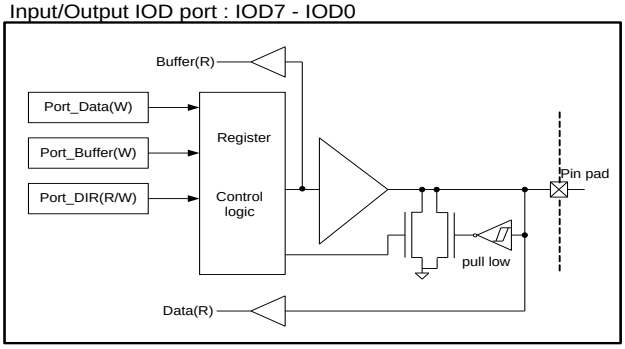
There are 12 IOs (IOC3-0 and IOD7-0) in the GPCL A1/B1 series; IOC3-0 is a nibble-controlled IO, but IOD7-0 is a bit-controlled IO. They can be programmed as input (pure input or pull-low) or output buffer. A pull-low input IOD7-0 keeps a less impedance to get better noise immunity. While pressing the key (IOD7-0 to VDD), a larger impedance is retained to save DC power. IOD6 can be programmed as an external interrupt source. IOD7 can be programmed as an IR transmitter.

7.6. IO Port Configuration

Input/Output IOC port : IOC3 - IOC0



Input/Output IOD port : IOD7 - IOD0



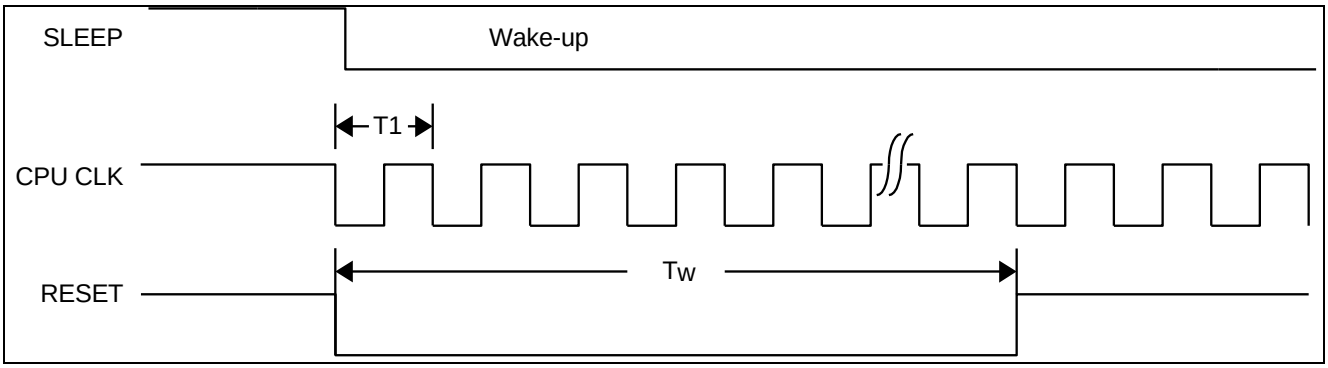
7.7. DC-DC

GPCL A1/B1 series can work wide input voltage (1.0V~1.7V; 1.3V~3.6V). Inside the chip, it is implemented a high efficient DC-DC circuit. The DC-DC circuit pumps input voltage to programmed voltage that supplies chip as working voltage.

7.8. Power Saving Mode

The GPCL A1/B1 series includes a power saving mode (Standby mode) for those applications that require very low standby current.

To enter standby mode, the Wake-up Register must be enabled and then stop the CPU clock by writing the STOP CLOCK Register to enter standby mode. In such mode, RAM and I/Os will retain at the previous states until awakened. Port IOD7-0 is the only wake-up source in the GPCL A1/B1 series. After GPCL A1/B1 series wakes up, the internal CPU will stay at RESET state for a period (Tw) and then continue to execute program. Wakeup Reset will neither affect RAM, nor I/Os.



$T1 = 1 / (F_{CPU})$

7.9. Timer/Counter

The GPCL A1/B1 series has two 8-bit timer/counters, TMA and TMB respectively. TMA can be specified as a timer, but TMB can be used as a timer or a counter. In the timer mode, TMA and TMB are re-loaded up-counters. When timer rolls over from $FF to $00, the carry (overflow) signal will make the user's preset value to be loaded into timer automatically and count up again. At the same time, the carry signal will generate an INT signal if the corresponding bit is enabled in the INT ENABLE Register. Suppose TMB is specified as a counter, it can be reset by loading #00 into the counter. After the counter has been activated, the value in the counter can also be read at the same time. The read instruction will neither affect the value of the counter nor reset it.

Clock source of Timer/Counter can be selected as follows:

Timer/Counter		Clock Source
TMA	8-BIT TIMER	CPU CLOCK (T) or T/8, T/64, TMB overflow
TMB	8-BIT TIMER	T, T/65536, EXTCLK, 0, 1

7.10. Speech and Melody

In speech synthesis, the GPCL A1/B1 series can use NMI for accurate sampling frequency. The user can store the speech data in ROM and play it back with realistic sound quality. Several algorithms are recommended for high fidelity and sound compression: PCM, ADPCM, SACM-A3400 and SACM-A3400 Pro.

8. ELECTRICAL SPECIFICATIONS

8.1. Absolute Maximum Ratings

Characteristics	Symbol	Ratings
DC Supply Voltage	V_+	< 7.0V
Input Voltage Range	V_{IN}	-0.5V to V_+ + 0.5V
Operating Temperature	T_A	0℃ to +60℃
Storage Temperature	T_{STO}	-50℃ to +150℃

Note: Stresses beyond those given in the Absolute Maximum Rating table may cause permanent damage to the device.

8.2. AC Characteristics (T_A = 25℃)

Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
OSC Frequency	F_{OSC}	-	-	6.0	MHz	VIN= 1.0V - 1.7V (one-battery , GPCLXXXA1) VIN= 1.3V - 3.6V (two-battery , GPCLXXXB1)

8.3. Power Characteristics (One-battery, GPCLXXXA1, TA = 25℃)

Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
Input Voltage (Min.) *	VIN	1.0	-	-	V	I(VDD)=40mA@VDD=3.3V, L=22uH/0.5W
Input Voltage (Max.)	VIN	-	-	1.7	V	-
Operating Voltage**	VDD	3.3	-	3.9	V	-
Standby Current	I_{STBY}	-	-	5.0	μA	VIN = 1.5V

*As I(VDD) is larger than the value of test condition; VDD can be observed voltage drop.

**VDD is the pumped voltage. It is larger than or equal to input voltage. It is possible to be lower with heavy loading under operating.

8.4. Power Characteristics (Two-battery, GPCLXXXB1, TA = 25℃)

Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
Input Voltage (Min.) *	VIN	1.3	-	-	V	I(VDD)=40mA@VDD=3.3V, L=22uH/0.5W
Input Voltage (Max.)	VIN	-	-	3.6	V	-
Operating Voltage**	VDD	3.3	-	4.5	V	-
Standby Current	I_{STBY}	-	-	10.0	μA	VIN = 3.0V

*As I(VDD) is larger than the value of test condition; VDD can be observed voltage drop.

**VDD is the pumped voltage. It is larger than or equal to input voltage. It is possible to be lower with heavy loading under operating.

8.5. DC Characteristics (One-battery, GPCLXXXA1, VDD=3.9V, T_A = 25℃)

Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
Operating Current	I_{OP}	-	14	-	mA	F_{osc} = 6.0MHz @ VDD=3.9V(no load) VIN=1.5V
Audio Output Current	I_{AUD}	-	180	-	mA	VDD = 3.9V, 8 Ohms load
Input High Level	V_{IH}	0.7 VDD	-	-	V	VDD = 3.9V
Input Low Level	V_{IL}	-	-	0.3 VDD	V	VDD = 3.9V
Output Source Current	I_{OH}	-	10	-	mA	VDD = 3.9V, V_{OH} = 2.73V

Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
Output Sink Current	I_{OL}	-	27	-	mA	VDD = 3.9V, V_{OL} = 1.17V
Input Resistor (IOC)	R_{IN}	-	125	-	KΩ	VDD = 3.9V, V_{IN} = VDD
Input Resistor (IOD)	R_{IN}	-	185	-	KΩ	VDD = 3.9V, V_{IN} = VDD

8.6. DC Characteristics (One-battery, GPCLXXXA1, VDD=3.3V, T_A = 25℃)

Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
Operating Current	I_{OP}	-	9.2	-	mA	F_{osc} = 6.0MHz @ VDD=3.3V(no load) VIN=1.5V
Audio Output Current	I_{AUD}	-	145	-	mA	VDD = 3.3V, 8 Ohms load
Input High Level	V_{IH}	0.7 VDD	-	-	V	VDD = 3.3V
Input Low Level	V_{IL}	-	-	0.3 VDD	V	VDD = 3.3V
Output Source Current	I_{OH}	-	8	-	mA	VDD = 3.3V, V_{OH} = 2.31V
Output Sink Current	I_{OL}	-	20	-	mA	VDD = 3.3V, V_{OL} = 0.99V
Input Resistor (IOC)	R_{IN}	-	140	-	KΩ	VDD = 3.3V, V_{IN} = VDD
Input Resistor (IOD)	R_{IN}	-	235	-	KΩ	VDD = 3.3V, V_{IN} = VDD

8.7. DC Characteristics (Two-battery, GPCLXXXB1, VDD=4.5V, T_A = 25℃)

Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
Operating Current	I_{OP}	-	9	-	mA	F_{osc} = 6.0MHz @ VDD=4.5V(no load) VIN=3.0V
Audio Output Current	I_{AUD}	-	215	-	mA	VDD = 4.5V, 8 Ohms load
Input High Level	V_{IH}	0.7 VDD	-	-	V	VDD = 4.5V
Input Low Level	V_{IL}	-	-	0.3 VDD	V	VDD = 4.5V
Output Source Current	I_{OH}	-	14	-	mA	VDD = 4.5V, V_{OH} = 3.15V
Output Sink Current	I_{OL}	-	35	-	mA	VDD = 4.5V, V_{OL} = 1.35V
Input Resistor (IOC)	R_{IN}	-	120	-	KΩ	VDD = 4.5V, V_{IN} = VDD
Input Resistor (IOD)	R_{IN}	-	155	-	KΩ	VDD = 4.5V, V_{IN} = VDD

8.8. DC Characteristics (Two-battery, GPCLXXXB1, VDD=3.3V, TA = 25℃)

Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
Operating Current I(VIN)	I_{OP}	-	4	-	mA	F_{osc} = 6.0MHz @ VDD=3.3V(no load) VIN=3.0V
Audio Output Current	I_{AUD}	-	145	-	mA	VDD = 3.3V, 8 Ohms load
Input High Level	V_{IH}	0.7 VDD	-	-	V	VDD = 3.3V
Input Low Level	V_{IL}	-	-	0.3 VDD	V	VDD = 3.3V
Output Source Current	I_{OH}	-	8	-	mA	VDD = 3.3V, V_{OH} = 2.31V
Output Sink Current	I_{OL}	-	20	-	mA	VDD = 3.3V, V_{OL} = 0.99V
Input Resistor (IOC)	R_{IN}	-	140	-	KΩ	VDD = 3.3V, V_{IO} = VDD
Input Resistor (IOD)	R_{IN}	-	235	-	KΩ	VDD = 3.3V, V_{IO} = VDD

8.9. Pump Efficiency (One-battery, GPCLXXXA1, T_A = 25℃)

Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
Pump Efficiency (L=22uH/0.5W, DCR =1 ohm)	Eff.	-	77	-	%	I(VDD)=30mA;VIN=1.5V; VDD=3.3V
		-	70	-	%	I(VDD)=60mA;VIN=1.5V; VDD=3.3V
		-	81	-	%	I(VDD)=30mA;VIN=1.5V; VDD=3.9V
		-	72	-	%	I(VDD)=60mA;VIN=1.5V; VDD=3.9V

*Use Color Code Inductor

8.10. Pump Efficiency (Two-battery, GPCLXXXB1, T_A = 25℃)

Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
Pump Efficiency (L=22uH/0.5W, DCR =1 ohm)	Eff.	-	88	-	%	I(VDD)=50mA;VIN=3.0V; VDD=3.9V
		-	85	-	%	I(VDD)=100mA;VIN=3.0V; VDD=3.9V
		-	87	-	%	I(VDD)=50mA;VIN=3.0V; VDD=4.5V
		-	85	-	%	I(VDD)=100mA;VIN=3.0V; VDD=4.5V

*Use Color Code Inductor

8.11. VIN v.s. Max. Supplied Current (I(VDD)) (One-battery, GPCLXXXA1, TA = 25℃)

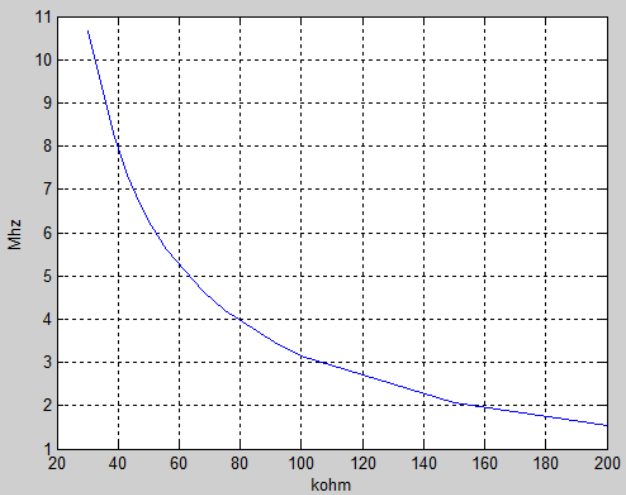
VIN (V)	I(VDD) (mA)	Condition
1.0	40	VDD=3.3V ; L=22uH/0.5W , DCR = 1 ohm(Color Code Inductor)
	20	VDD=3.9V ; L=22uH/0.5W , DCR = 1 ohm (Color Code Inductor)
1.2	60	VDD=3.3V ; L=22uH/0.5W, DCR = 1 ohm (Color Code Inductor)
	40	VDD=3.9V ; L=22uH/0.5W , DCR = 1 ohm (Color Code Inductor)
1.5	90	VDD=3.3V ; L=22uH/0.5W , DCR = 1 ohm (Color Code Inductor)
	80	VDD=3.9V ; L=22uH/0.5W , DCR = 1 ohm (Color Code Inductor)

8.12. VIN v.s. Max. Supplied Current (I(VDD)) (Two-battery, GPCLXXXB1, TA = 25℃)

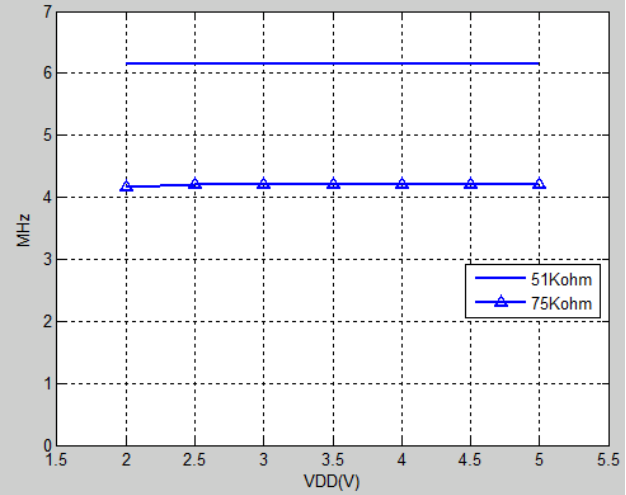
VIN (V)	I(VDD) (mA)	Condition
1.5	40	VDD=3.9V ; L=22uH/0.5W , DCR = 1 ohm (Color Code Inductor)
	20	VDD=4.5V ; L=22uH/0.5W , DCR = 1 ohm (Color Code Inductor)
1.8	90	VDD=3.9V ; L=22uH/0.5W , DCR = 1 ohm (Color Code Inductor)
	70	VDD=4.5V ; L=22uH/0.5W , DCR = 1 ohm (Color Code Inductor)
2.4	170	VDD=3.9V ; L=22uH/0.5W , DCR = 1 ohm (Color Code Inductor)
	150	VDD=4.5V ; L=22uH/0.5W , DCR = 1 ohm (Color Code Inductor)
3.0	200	VDD=3.9V ; L=22uH/0.5W , DCR = 1 ohm (Color Code Inductor)
	200	VDD=4.5V ; L=22uH/0.5W , DCR = 1 ohm (Color Code Inductor)

8.13. The Relationship between the ROSC and the FCPU

8.13.1. VDD = 3.3V, T_A = 25℃

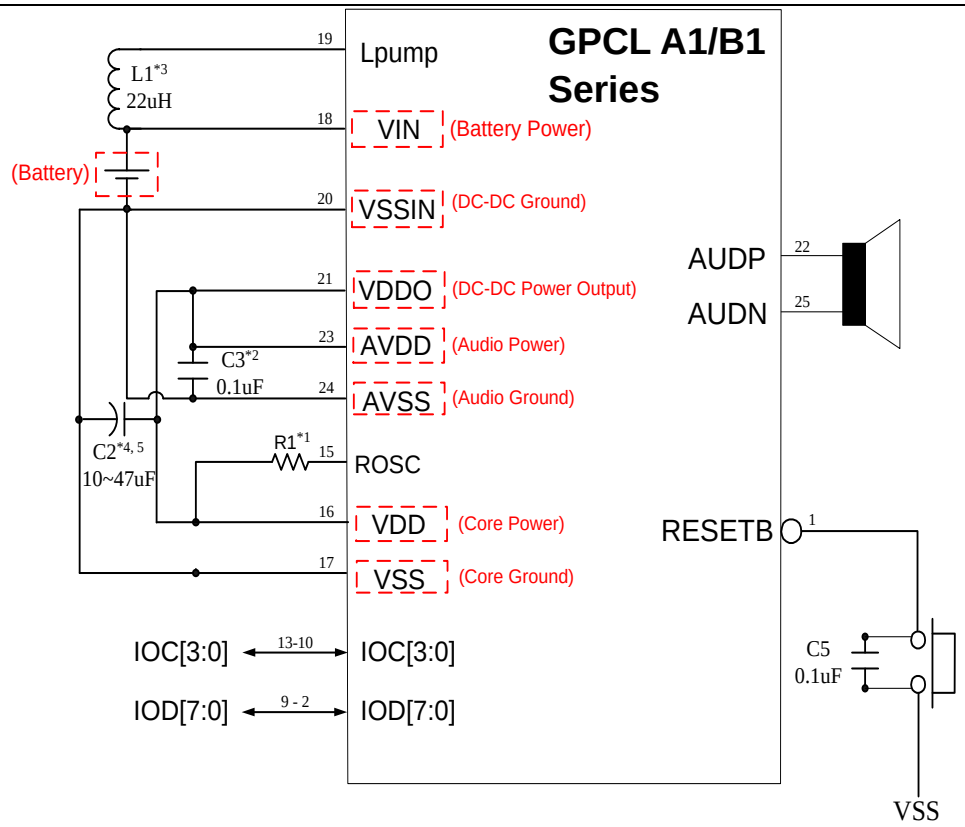


8.13.2. Frequency vs. VDD



9. APPLICATION CIRCUITS

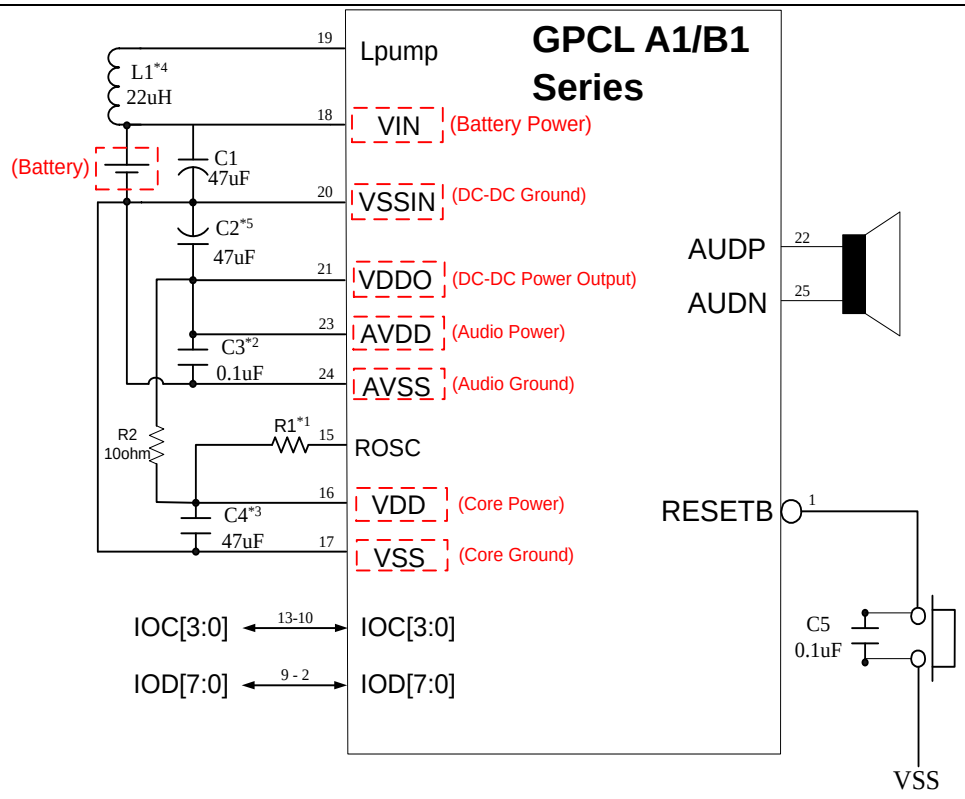
9.1. Light Loading And Circuit without Noise



PCB Layout Guidelines :

1. R1 should be as close as possible to ROSC pin.
2. C3 should be as close as possible to AVDD/AVSS, and C3 can be removed if there is good power line layout on PCB that no harm to sound quality.
3. L1 should be as close as possible to VIN/Lpump. **Please use inductor with lower resistance to gain higher efficiency. 22uH/0.5W@IDC(max)>250mA ,DCR<1.5ohm is the suggested inductance spec. .**
4. The value of C2 depends on the loading. 10uF~47uF is the suggested value range. One end of C2 should be placed between VSS and VSSIN. The other end of C2 should be placed between VDDO and VDD. C2 should be as close as possible to VDDO/VDD .
5. **Please use capacitor (C2) with low resistance to reduce noise , ESR<2 ohm in 0~70C is suggested.**

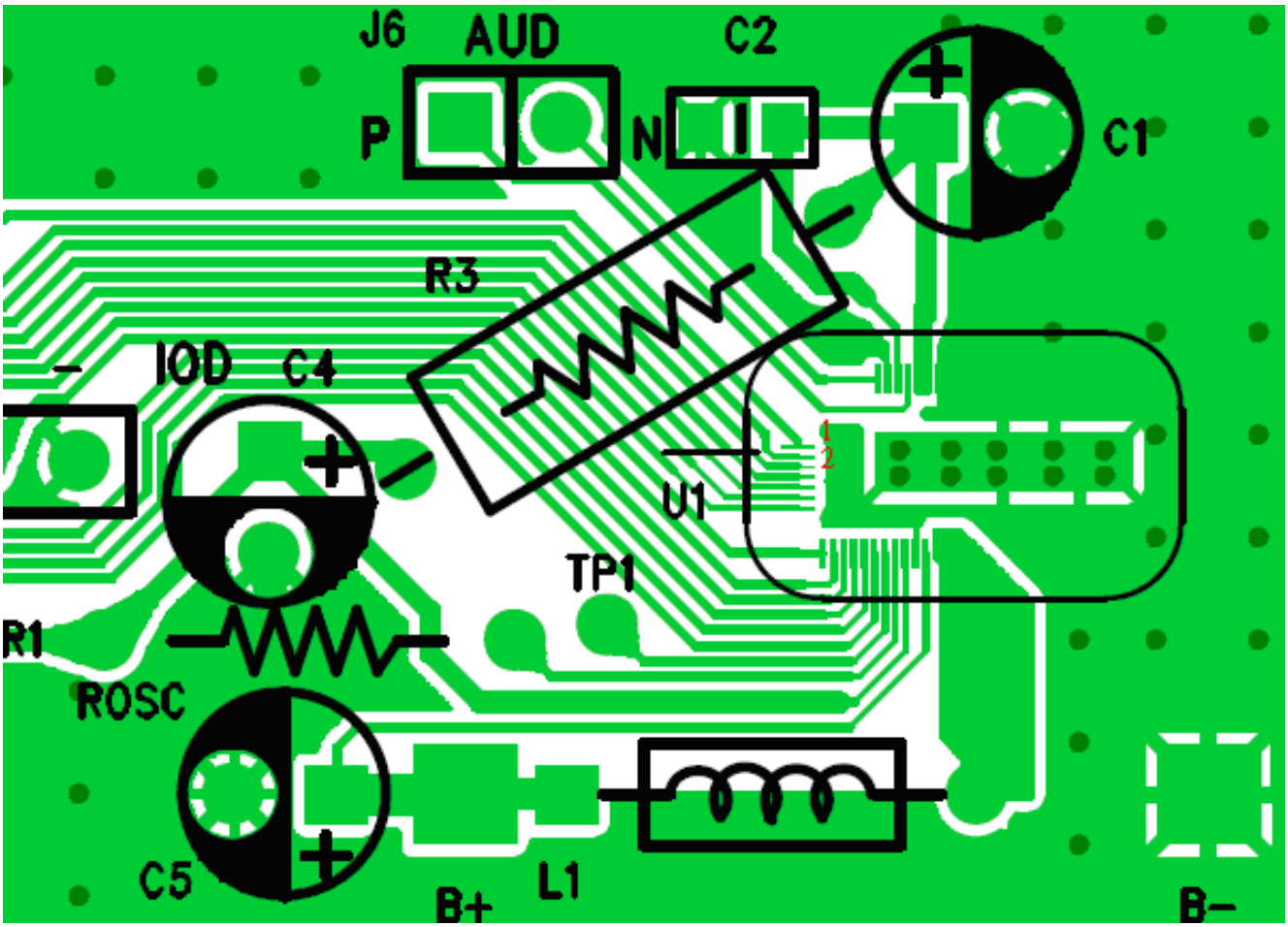
9.2. Heavy Loading or Circuit with Noise



PCB Layout Guidelines :

1. R1 should be as close as possible to ROSC pin.
2. C3 should be as close as possible to AVDD/AVSS, and C3 can be removed if there is good power line layout on PCB that no harm to sound quality.
3. C4 should be as close as possible to VDD/VSS, and C4 can be smaller if there is good power line layout on PCB that the power stable enough.
4. L1 should be as close as possible to VIN/Lpump**. Please use inductor with lower resistance to gain higher efficiency. 22uH/0.5W@IDC(max)>250mA ,DCR<1.5ohm is the suggested inductance spec.**
5. **Please use capacitor (C2) with low resistance to reduce noise , ESR<2 ohm in 0~70C is suggested.**

10. LAYOUT GUIDELINE



PCB layout guidelines:

1. The chip should be placed to where it makes VSSIN as close as possible to PCB pin out.
2. Make the width of VSSIN, VDDO and Lpump's PCB pin out as wide as possible.
3. The substrate under chip requires holes to dissipate heat and please connect substrate with VSS.
4. The route through chip, battery, and inductor should be as short as possible; its wire diameter should be as thick as possible.
5. Connect the VSS and battery's negative to a whole GND.
6. Place all chip's components as close as possible to IC, especially the 47uF capacitor to VDDO. ESR<2 ohm in 0~70C is suggested.
7. Please use inductance with lower resistance to gain higher efficiency. 22uH/0.5W@IDC(max)>250mA ,DCR<1.5ohm is the suggested inductance specification.

11. PACKAGE/PAD LOCATIONS

11.1. Ordering Information

Product Number	Package Type
GPCL170A1 - NnnV – C GPCL170B1 - NnnV - C	Chip form
GPCL128A1 - NnnV – C GPCL128B1 - NnnV – C	Chip form
GPCL112A1 - NnnV – C GPCL112B1 - NnnV – C	Chip form
GPCL096A1- NnnV – C GPCL096B1- NnnV - C	Chip form
GPCL040A1 - NnnV – C GPCL040B1 - NnnV – C	Chip form
GPCL030A1 - NnnV – C GPCL030B1 - NnnV – C	Chip form
GPCL020A1 - NnnV – C GPCL020B1 - NnnV – C	Chip form
GPCL010A1 - NnnV – C GPCL010B1 - NnnV – C	Chip form

Note1: Code number is assigned for customer.

Note2: Code number (N = A - Z or 0 - 9, nn = 00 - 99); version (V = A - Z).

12. DISCLAIMER

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13. REVISION HISTORY

Date	Revision #	Description	Page
Sep 15, 2015	1.0	Add ELECTRICAL SPECIFICATIONS section.	19
Aug 11, 2015	0.1	Original	16