HARRIS Semiconductor

RFM6N45, RFP6N45, RFP6N50

6A, 450V and 500V, 1.250 Ohm, N-Channel Power MOSFETs

September 1998

Features

- **6A, 450V and 500V**
- **$r_{DS(ON)}$ = 1.250Ω**
- **SOA is Power Dissipation Limited**
- **Nanosecond Switching Speeds**
- **Linear Transfer Characteristics**
- **High Input Impedence**
- **Majority Carrier Device**
- **Related Literature**
  - **TB334 "Guidelines for Soldering Surface Mount Components to PC Boards"**

Ordering Information

PART NUMBER	PACKAGE	BRAND
RFM6N45	TO-204AA	RFM6N45
RFP6N45	TO-204AA	RFP6N45
RFP6N50	TO-220AB	RFP6N50

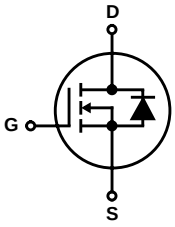
NOTE: When ordering, include the entire part number.

Description

These are N-Channel enhancement mode silicon gate power field effect transistors specifically designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high power bipolar switching transistors requiring high speed and low gate drive power. These types can be operated directly from integrated circuits.

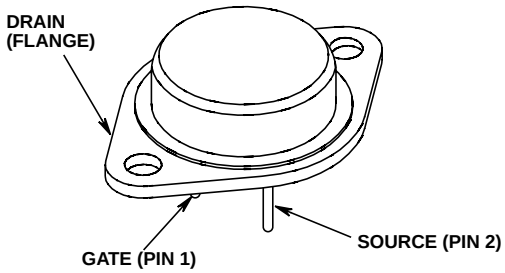
Formerly developmental type TA17425.

Symbol

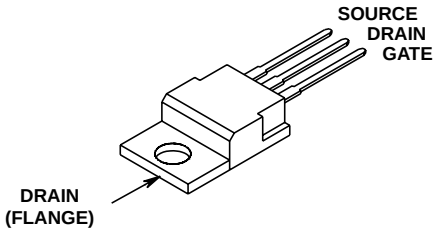


Packaging

JEDEC TO-204AA



JEDEC TO-220AB



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper ESD Handling Procedures.

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File Number **1494.2**

Absolute Maximum Ratings $T_C = 25^oC$, Unless Otherwise Specified

		RFM6N45	RFP6N45	RFP6N50	UNITS
Drain to Source Voltage (Note 1)	V_{DS}	450	450	500	V
Drain to Gate Voltage (RGS = 20kW) (Note 1)	V_{DGR}	450	450	500	V
Continuous Drain Current	I_D	6	6	6	A
Pulsed Drain Current (Note 3)	I_{DM}	15	15	15	A
Gate to Source Voltage	V_{GS}	±20	±20	±20	V
Maximum Power Dissipation	P_D	100	75	75	W
Linear Derating Factor		0.8	0.6	0.6	$W/^oC$
Operating and Storage Temperature	T_J, T_{STG}	-55 to 150	-55 to 150	-55 to 150	^oC
Maximum Temperature for Soldering					
Leads at 0.063in (1.6mm) from Case for 10s	T_L	300	300	300	^oC
Package Body for 10s, See Techbrief 334 (for TO-220)	T_{pkg}	260	260	260	^oC

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. $T_J = 25^oC$ to 125^oC.

Electrical Specifications $T_C = 25^oC$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Drain to Source Breakdown Voltage RFM6N45, RFP6N45	BV_{DSS}	I_D = 250µA, V_{GS} = 0V	450	-	-	V
RFP6N50			500	-	-	V
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}$, I_D = 250µA (Figure 8)	2	-	4	V
Zero-Gate Voltage Drain Current	I_{DSS}	V_{DS} = Rated BV_{DSS}, V_{GS} = 0V	-	-	1	µA
		V_{DS} = 0.8 x Rated BV_{DSS}, V_{GS} = 0V, $T_C = 125^oC$	-	-	25	µA
Gate to Source Leakage Current	I_{GSS}	V_{GS} = ±20V, V_{DS} = 0V	-	-	±100	nA
Drain to Source On Resistance(Note 2)	$r_{DS(ON)}$	I_D = 6A, V_{GS} = 10V, (Figures 6, 7)	-	-	1.250	Ω
Drain to Source On-Voltage (Note 2)	$V_{DS(ON)}$	I_D = 6A, V_{GS} = 10V	-	-	7.50	V
Turn-On Delay Time	$t_{d(ON)}$	I_D = 3A, V_{DD} = 250V, R_G = 50Ω, V_{GS} = 10V, R_L = 81Ω (Figures 10, 11, 12)	-	15	45	ns
Rise Time	t_r		-	40	80	ns
Turn-Off Delay Time	$t_{d(OFF)}$		-	190	300	ns
Fall Time	t_f		-	60	100	ns
Input Capacitance	C_{ISS}	V_{GS} = 0V, V_{DS} = 25V f = 1MHz, (Figure 9)	-	-	1500	pF
Output Capacitance	C_{OSS}		-	-	250	pF
Reverse Transfer Capacitance	C_{RSS}		-	-	200	pF
Thermal Resistance Junction to Case	$R_{\theta JC}$	RFM6N45	-	-	1.25	$^oC/W$
		RFP6N45, RFP6N50			1.67	$^oC/W$

Source to Drain Diode Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Source to Drain Diode Voltage (Note 2)	V_{SD}	I_{SD} = 3A	-	-	1.4	V
Diode Reverse Recovery Time	t_{rr}	I_{SD} = 4A, dI_{SD}/dt = 100A/µs	-	800	-	ns

NOTES:

2. Pulsed test: Pulse width ≤ 300µs duty cycle ≤ 2%
3. Repetitive rating: pulse width limited by maximum junction temperature.

Typical Performance Curves

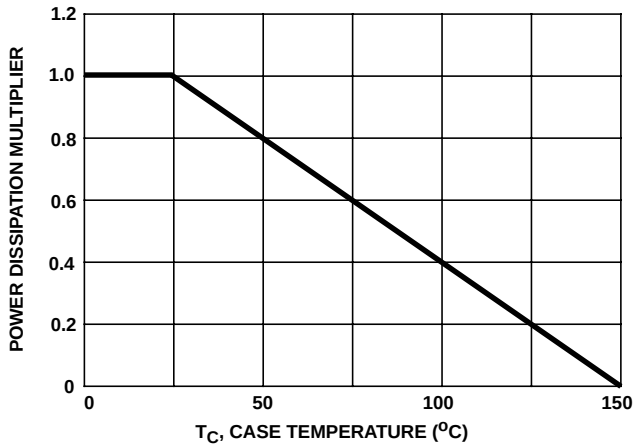


FIGURE 1. NORMALIZED POWER DISSIPATION vs CASE TEMPERATURE

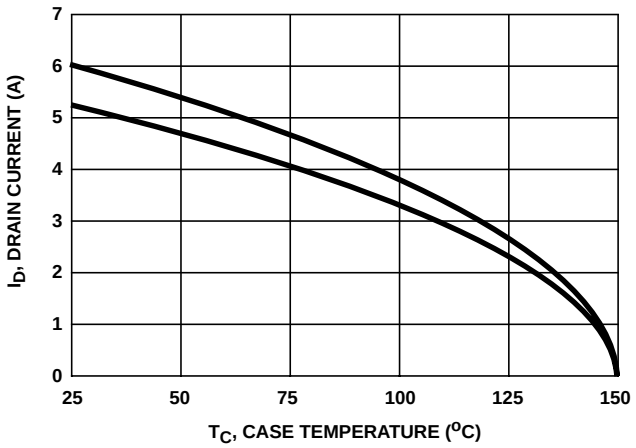


FIGURE 2. MAXIMUM CONTINUOUS DRAIN CURRENT vs CASE TEMPERATURE

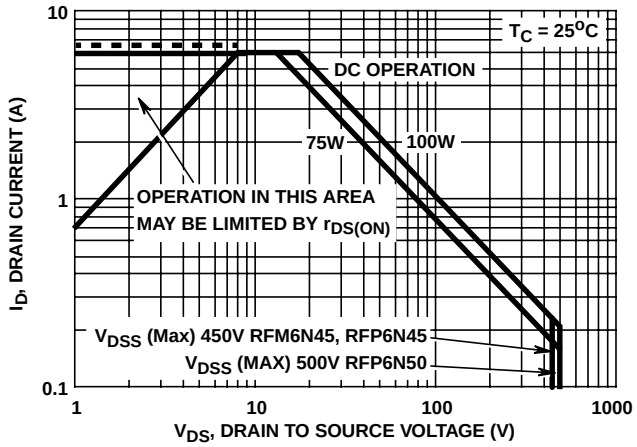


FIGURE 3. FORWARD BIAS SAFE OPERATING AREA

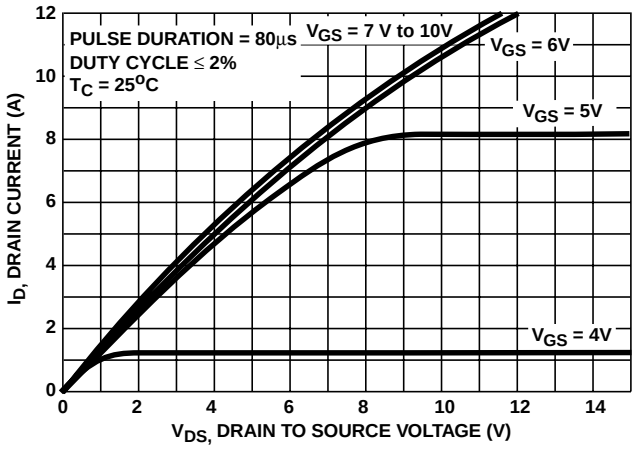


FIGURE 4. SATURATION CHARACTERISTICS

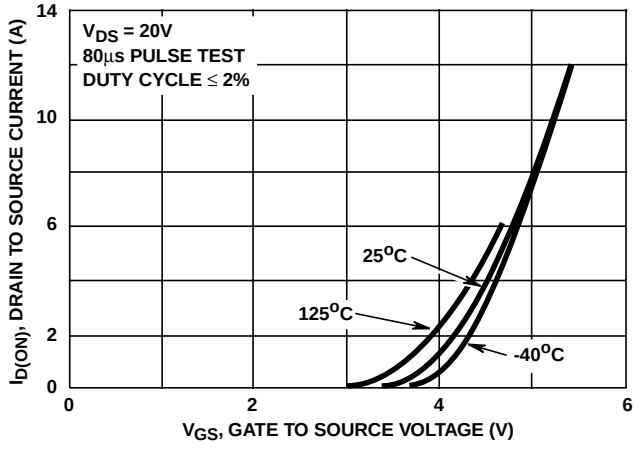


FIGURE 5. TRANSFER CHARACTERISTICS

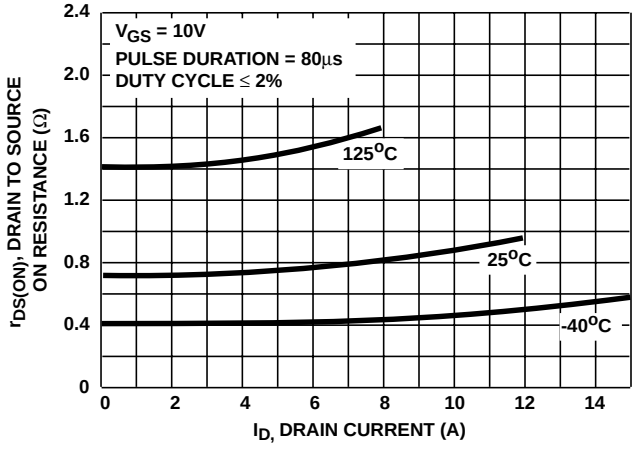


FIGURE 6. DRAIN TO SOURCE ON RESISTANCE vs DRAIN CURRENT

Typical Performance Curves (Continued)

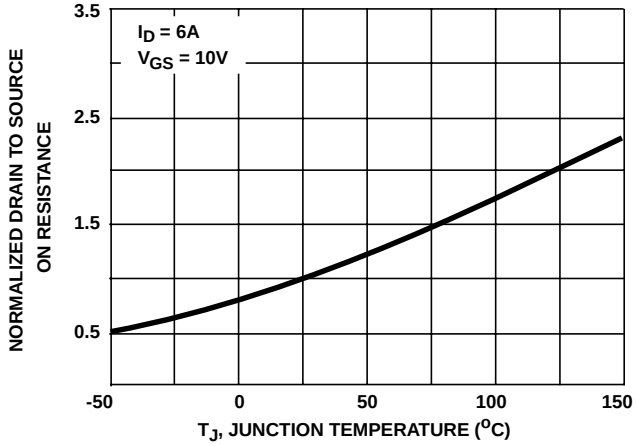


FIGURE 7. NORMALIZED DRAIN TO SOURCE ON RESISTANCE vs JUNCTION TEMPERATURE

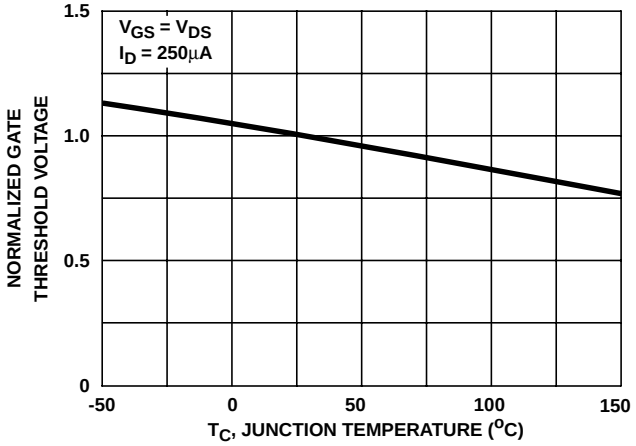


FIGURE 8. NORMALIZED GATE THRESHOLD VOLTAGE vs JUNCTION TEMPERATURE

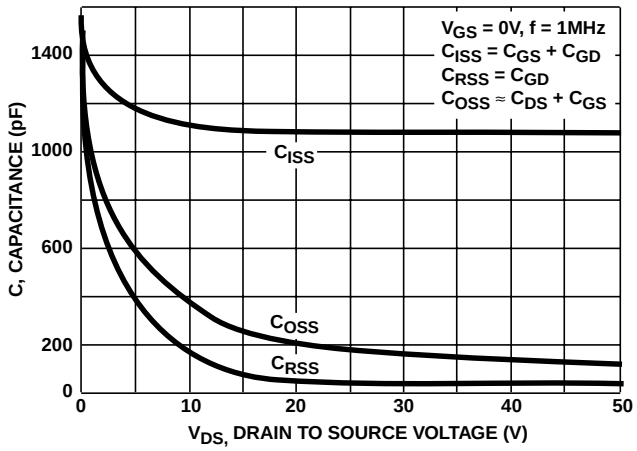
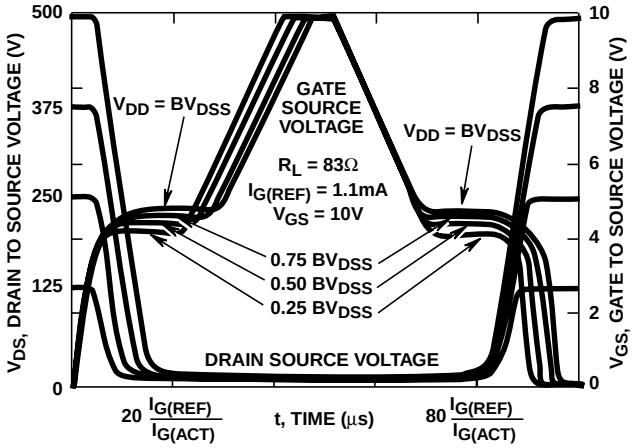


FIGURE 9. CAPACITANCE vs DRAIN TO SOURCE VOLTAGE



NOTE: Refer to Harris Applications Notes AN7254 and AN7260

FIGURE 10. NORMALIZED SWITCHING WAVEFORMS FOR CONSTANT GATE CURRENT

Test Circuits and Waveforms

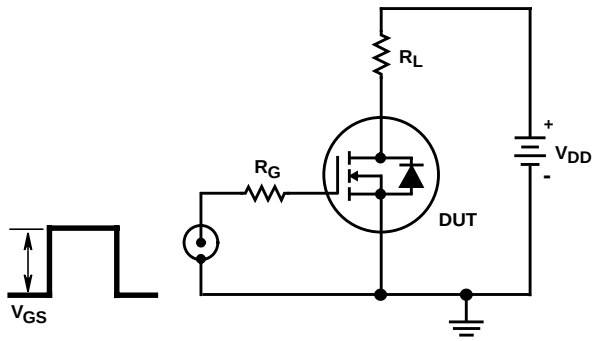


FIGURE 11. SWITCHING TIME TEST CIRCUIT

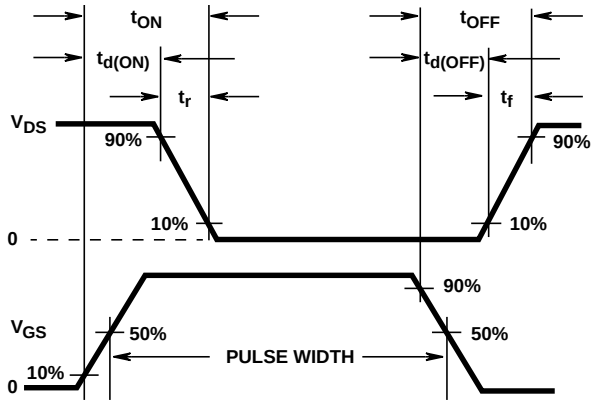


FIGURE 12. RESISTIVE SWITCHING WAVEFORMS