74ABT16821A

20-bit bus-interface D-type flip-flop; positive-edge trigger; 3-state

Rev. 03 — 16 March 2010 Product data sheet

1. General description

The 74ABT16821A high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The 74ABT16821A has two 10-bit, edge-triggered registers, with each register coupled to a 3-state output buffer. The two sections of each register are controlled independently by the clock (nCP) and output enable ($n\overline{OE}$) control gates.

Each register is fully edge triggered. The state of each D input, one set-up time before the LOW-to-HIGH clock transition, is transferred to the corresponding flip-flops Q output.

The 3-state output buffers are designed to drive heavily loaded 3-state buses, MOS memories, or MOS microprocessors.

The active-LOW output enable ($n\overline{OE}$) controls all ten 3-state buffers independent of the register operation. When $n\overline{OE}$ is LOW, the data in the register appears at the outputs. When $n\overline{OE}$ is HIGH, the outputs are in high-impedance OFF-state, which means they will neither drive nor load the bus.

2. Features and benefits

- 20-bit positive-edge triggered register
- Multiple V_{CC} and GND pins minimize switching noise
- Live insertion and extraction permitted
- Output capability: +64 mA and −32 mA
- Power-up 3-state
- Power-up reset
- Latch-up protection exceeds 500 mA per JESD78B class II level A
- ESD protection:
  - HBM JESD22-A114F exceeds 2000 V
  - MM JESD22-A115-A exceeds 200 V

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74ABT16821ADL	−40 °C to +85 °C	SSOP56	plastic shrink small outline package; 56 leads; body width 7.5 mm	SOT371-1
74ABT16821ADGG	−40 °C to +85 °C	TSSOP56	plastic thin shrink small outline package; 56 leads; body width 6.1 mm	SOT364-1

4. Functional diagram

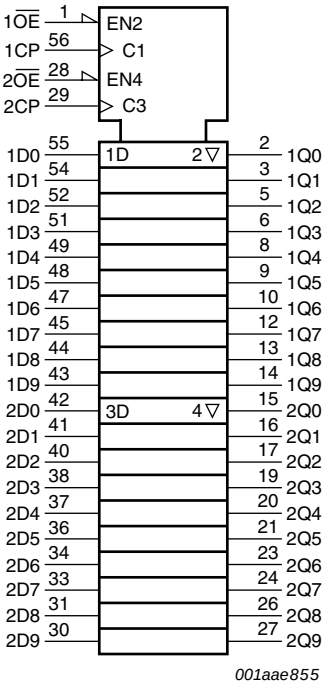


Fig 1. IEC logic symbol

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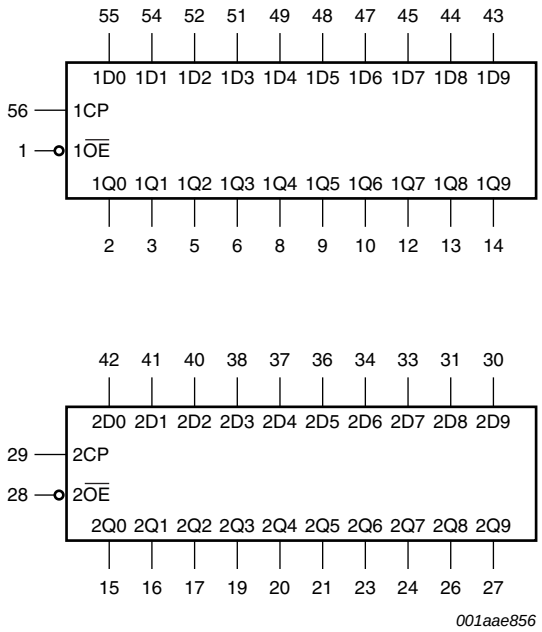


Fig 2. Logic symbol

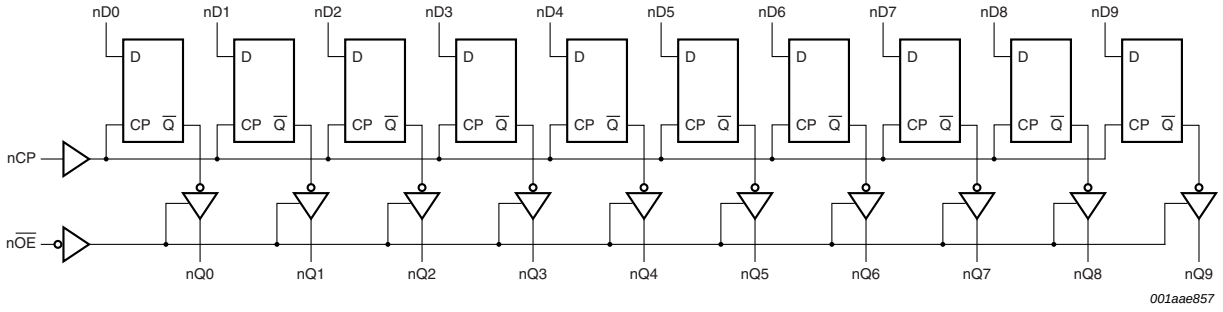


Fig 3. Logic diagram

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5. Pinning information

5.1 Pinning

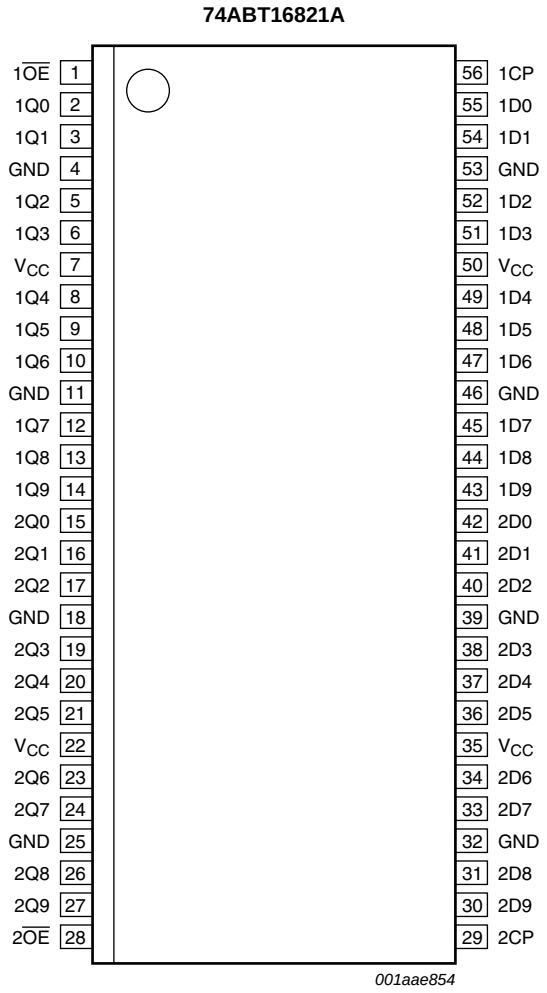


Fig 4. Pin configuration

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5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
1$\overline{OE}$, 2$\overline{OE}$	1, 28	output enable input (active LOW)
1Q0 to 1Q9	2, 3, 5, 6, 8, 9, 10, 12, 13, 14	data output
GND	4, 11, 18, 25, 32, 39, 46, 53	ground (0 V)
V_{CC}	7, 22, 35, 50	supply voltage
2Q0 to 2Q9	15, 16, 17, 19, 20, 21, 23, 24, 26, 27	data output
2CP, 1CP	29, 56	clock pulse input (active rising edge)
2D0 to 2D9	42, 41, 40, 38, 37, 36, 34, 33, 31, 30	data input
1D0 to1D9	55, 54, 52, 51, 49, 48, 47, 45, 44, 43	data input

6. Functional description

Table 3. Function table[1]

Input			Output	Internal register	Operating mode
n$\overline{OE}$	nCP	nDx	nQ0 to nQ9		
L	↑	l	L	L	load + read register
L	↑	h	H	H	load + read register
L	H or L	X	NC	NC	hold
H	L or H	X	Z	NC	disable output
H	↑	Dn	Z	Dn	disable output

[1] H = HIGH voltage level;
h = HIGH voltage level one set-up time prior to the LOW-to-HIGH clock transition;
L = LOW voltage level;
l = LOW voltage level one set-up time prior to the LOW-to-HIGH clock transition;
↑ = LOW-to-HIGH clock transition;
NC = no change;
X = don't care;
Z = high-impedance OFF-state.

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7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CC}	supply voltage			−0.5	+7.0	V
V_I	input voltage		[1]	−1.2	+7.0	V
V_O	output voltage	output in OFF-state or HIGH-state	[1]	−0.5	+5.5	V
I_{IK}	input clamping current	$V_I < 0$ V		−18	-	mA
I_{OK}	output clamping current	$V_O < 0$ V		−50	-	mA
I_O	output current	output in LOW-state		-	128	mA
		output in HIGH-state		−64	-	mA
T_j	junction temperature		[2]	-	150	°C
T_{stg}	storage temperature			−65	+150	°C

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150 °C.

8. Recommended operating conditions

Table 5. Operating conditions

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage		4.5	-	5.5	V
V_I	input voltage		0	-	V_{CC}	V
V_{IH}	HIGH-level input voltage		2.0	-	-	V
V_{IL}	LOW-level Input voltage		-	-	0.8	V
I_{OH}	HIGH-level output current		−32	-	-	mA
I_{OL}	LOW-level output current		-	-	64	mA
$\Delta t/\Delta V$	input transition rise and fall rate		0	-	10	ns/V
T_{amb}	ambient temperature	in free air	−40	-	+85	°C

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9. Static characteristics

Table 6. Static characteristics

Symbol	Parameter	Conditions		25 °C			–40 °C to +85 °C		Unit
				Min	Typ	Max	Min	Max	
V_{IK}	input clamping voltage	V_{CC} = 4.5 V; I_{IK} = –18 mA		–1.2	–0.9	-	–1.2	-	V
V_{OH}	HIGH-level output voltage	V_I = V_{IL} or V_{IH}							
		V_{CC} = 4.5 V; I_{OH} = –3 mA		2.5	2.9	-	2.5	-	V
		V_{CC} = 5.0 V; I_{OH} = –3 mA		3.0	3.4	-	3.0	-	V
		V_{CC} = 4.5 V; I_{OH} = –32 mA		2.0	2.4	-	2.0	-	V
V_{OL}	LOW-level output voltage	V_{CC} = 4.5 V; I_{OL} = 64 mA; V_I = V_{IL} or V_{IH}		-	0.36	0.55	-	0.55	V
$V_{OL(pu)}$	power-up LOW-level output voltage	V_{CC} = 5.5 V; I_O = 1 mA; V_I = GND or V_{CC}	[1]	-	0.13	0.55	-	0.55	V
I_I	input leakage current	V_{CC} = 5.5 V; V_I = V_{CC} or GND		-	±0.01	±1.0	-	±1.0	µA
I_{OFF}	power-off leakage current	V_{CC} = 0 V; V_I or V_O ≤ 4.5 V		-	±5.0	±100	-	±100	µA
$I_{O(pu/pd)}$	power-up/power-down output current	V_{CC} = 2.1 V; V_O = 0.5 V; V_I = GND or V_{CC}; $\overline{nOE}$ don't care	[2]	-	±5.0	±50	-	±50	µA
I_{OZ}	OFF-state output current	V_{CC} = 5.5 V; V_I = V_{IL} or V_{IH}							
		output HIGH-state at V_O = 2.7 V		-	1.0	10	-	10	µA
		output LOW-state at V_O = 0.5 V		-	–1.0	–10	-	–10	µA
I_{LO}	output leakage current	HIGH-state; V_O = 5.5 V; V_{CC} = 5.5 V; V_I = GND or V_{CC}		-	5.0	50	-	50	µA
I_O	output current	V_{CC} = 5.5 V; V_O = 2.5 V	[3]	–180	–90	–50	–180	–50	mA
I_{CC}	supply current	V_{CC} = 5.5 V; V_I = GND or V_{CC}							
		outputs HIGH-state		-	0.5	1.0	-	1.0	mA
		outputs LOW-state		-	10	19	-	19	mA
		outputs 3-state		-	0.5	1.0	-	1.0	mA
ΔI_{CC}	additional supply current	per input pin; V_{CC} = 5.5 V; one input at 3.4 V and other inputs at V_{CC} or GND	[4]	-	0.25	1.5	-	1.5	mA
C_I	input capacitance	V_I = 0 V or V_{CC}		-	3	-	-	-	
C_O	output capacitance	outputs disabled; V_O = 0 V or V_{CC}		-	7	-	-	-	

[1] For valid test results, data must not be loaded into the flip-flops (or latches) after applying the power.

[2] This parameter is valid for any V_{CC} between 0 V and 2.1 V, with a transition time of up to 10 ms. From V_{CC} = 2.1 V to V_{CC} = 5 V ± 10 % a transition time of up to 100 µs is permitted.

[3] Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

[4] This is the increase in supply current for each input at 3.4 V.

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10. Dynamic characteristics

Table 7. Dynamic characteristics

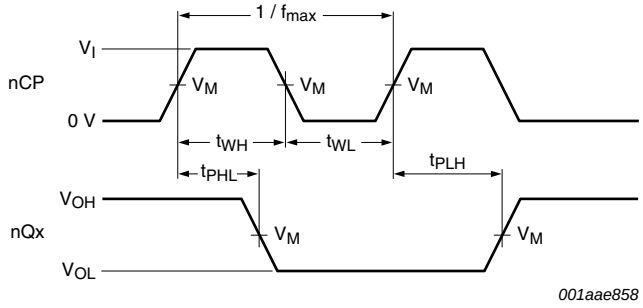
GND = 0 V; for test circuit, see Figure 8.

Symbol	Parameter	Conditions	25 °C; V_{CC} = 5.0 V			–40 °C to +85 °C; V_{CC} = 5.0 V ± 0.5 V		Unit
			Min	Typ	Max	Min	Max	
f_{max}	maximum frequency	see Figure 5	160	250	-	160	-	MHz
t_{PLH}	LOW to HIGH propagation delay	nCP to nQx, see Figure 5	1.3	2.4	3.3	1.3	3.7	ns
t_{PHL}	HIGH to LOW propagation delay	nCP to nQx, see Figure 5	1.1	2.0	2.6	1.1	3.0	ns
t_{PZH}	OFF-state to HIGH propagation delay	$n\overline{OE}$ to nQx; see Figure 6	1.4	2.5	3.3	1.4	4.1	ns
t_{PZL}	OFF-state to LOW propagation delay	$n\overline{OE}$ to nQx; see Figure 6	1.2	2.3	3.0	1.2	3.7	ns
t_{PHZ}	HIGH to OFF-state propagation delay	$n\overline{OE}$ to nQx; see Figure 6	1.6	3.2	4.1	1.6	4.8	ns
t_{PLZ}	LOW to OFF-state propagation delay	$n\overline{OE}$ to nQx; see Figure 6	1.3	2.3	3.1	1.3	3.3	ns
$t_{su(H)}$	set-up time HIGH	nDx to nCP; see Figure 7	1.8	1.2	-	1.8	-	ns
$t_{su(L)}$	set-up time LOW	nDx to nCP; see Figure 7	+1.8	–0.9	-	+1.8	-	ns
$t_{h(H)}$	hold time HIGH	nDx to nCP; see Figure 7	1.0	0.8	-	1.0	-	ns
$t_{h(L)}$	hold time LOW	nDx to nCP; see Figure 7	+1.0	–1.0	-	+1.0	-	ns
t_{WH}	pulse width HIGH	nCP; see Figure 5	2.5	0.8	-	2.5	-	ns
t_{WL}	pulse width LOW	nCP; see Figure 5	2.5	1.0	-	2.5	-	ns

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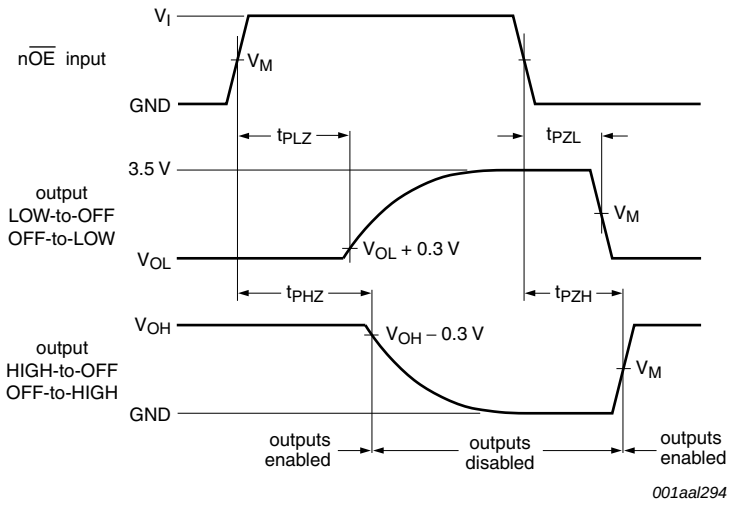
11. Waveforms



V_M = 1.5 V

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig 5. Propagation delay, clock input to output, clock pulse width, and maximum clock frequency



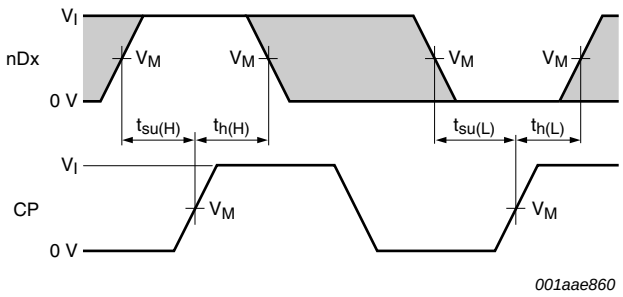
V_M = 1.5 V

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig 6. 3-state output enable time to HIGH-level and output disable time from HIGH- level

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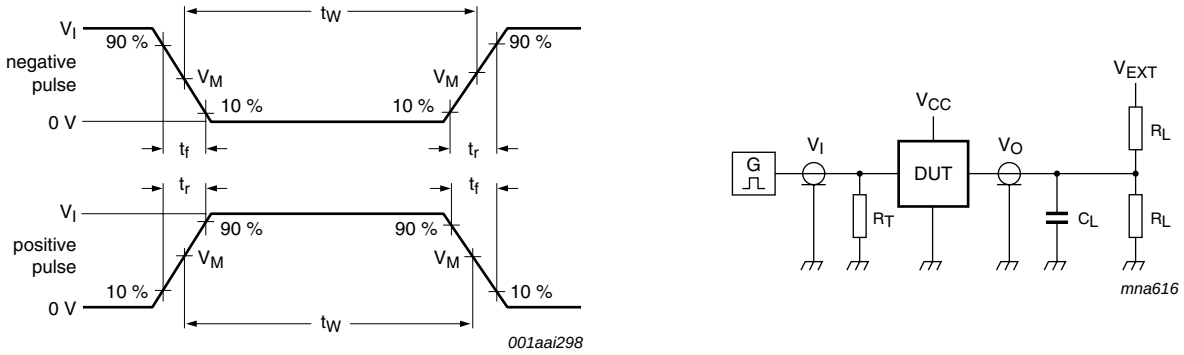
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The shaded areas indicate when the input is permitted to change for predictable output performance.

V_M = 1.5 V

Fig 7. Set-up and hold times data input (nDx) to clock (CP)



a. Input pulse definition

b. Test circuit

Test data is given in Table 8.

Definitions test circuit:

R_L = Load resistance.

C_L = Load capacitance including jig and probe capacitance.

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

V_{EXT} = External voltage for measuring switching times.

Fig 8. Load circuitry for switching times

Table 8. Test data

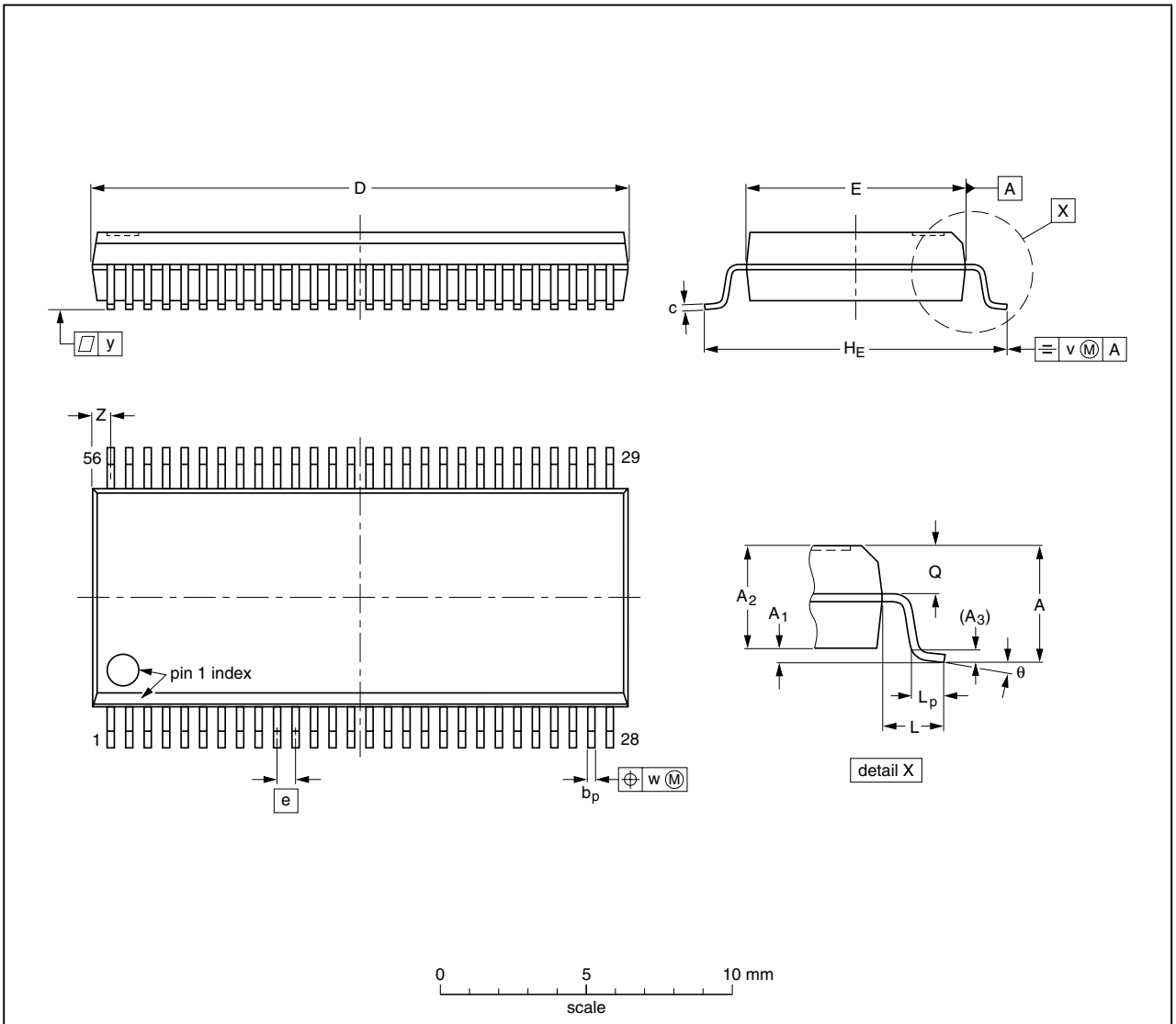
Input				Load		V_{EXT}		
V_I	f_I	t_W	t_r, t_f	C_L	R_L	t_{PHL}, t_{PLH}	t_{PZH}, t_{PHZ}	t_{PZL}, t_{PLZ}
3.0 V	1 MHz	500 ns	≤ 2.5 ns	50 pF	500 Ω	open	open	7.0 V

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12. Package outline

SSOP56: plastic shrink small outline package; 56 leads; body width 7.5 mm **SOT371-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2.8	0.4 0.2	2.35 2.20	0.25	0.3 0.2	0.22 0.13	18.55 18.30	7.6 7.4	0.635	10.4 10.1	1.4	1.0 0.6	1.2 1.0	0.25	0.18	0.1	0.85 0.40	8° 0°

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

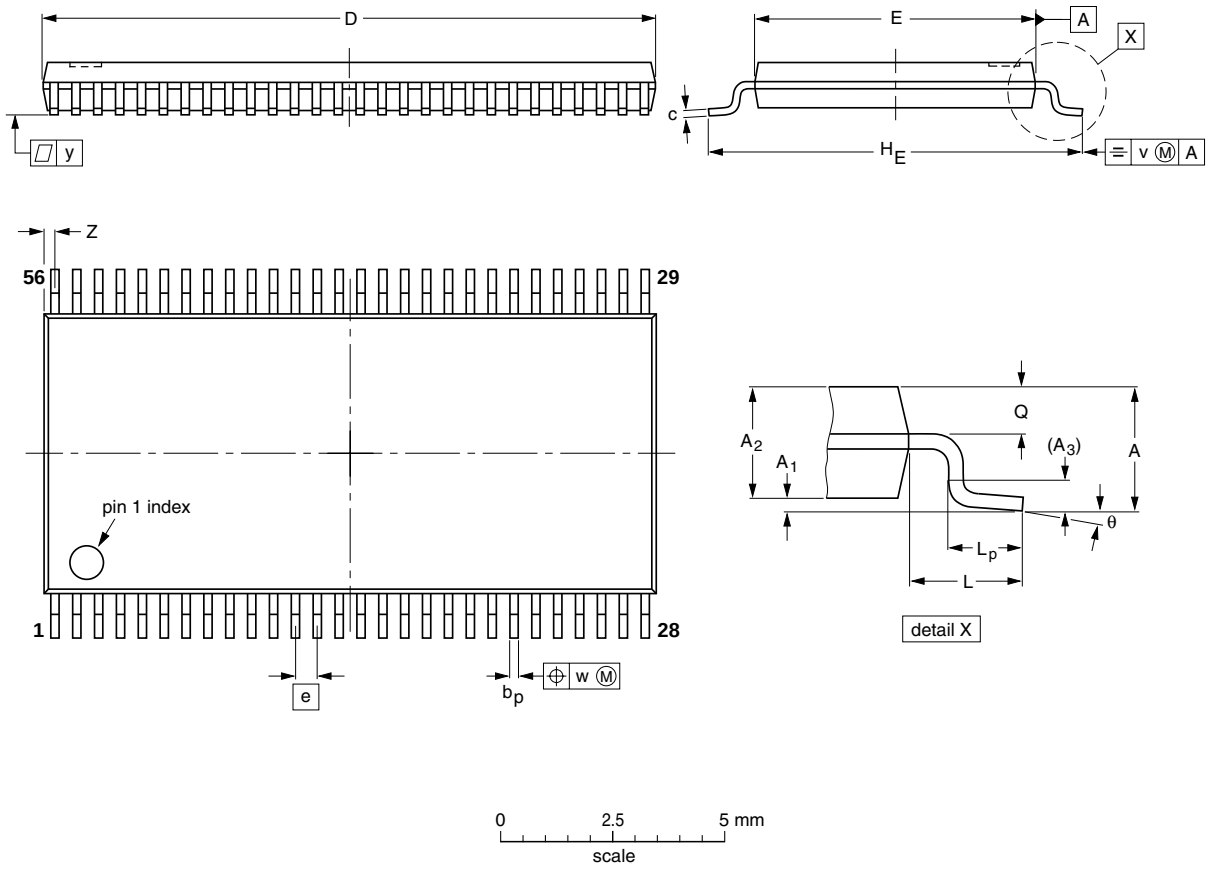
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT371-1		MO-118				~~99-12-27~~ 03-02-18

Fig 9. Package outline SOT371-1 (SSOP56)

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TSSOP56: plastic thin shrink small outline package; 56 leads; body width 6.1 mm **SOT364-1**



DIMENSIONS (mm are the original dimensions).

UNIT	A max.	A_1	A_2	A_3	b_p	c	D(1)	E(2)	e	H_E	L	L_p	Q	v	w	y	Z	θ
mm	1.2	0.15 0.05	1.05 0.85	0.25	0.28 0.17	0.2 0.1	14.1 13.9	6.2 6.0	0.5	8.3 7.9	1	0.8 0.4	0.50 0.35	0.25	0.08	0.1	0.5 0.1	8° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT364-1		MO-153				~~99-12-27~~ 03-02-19

Fig 10. Package outline SOT364-1 (TSSOP56)

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13. Abbreviations

Table 9. Abbreviations

Acronym	Description
BiCMOS	Bipolar Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model

14. Revision history

Table 10. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74ABT16821A_3	20100316	Product data sheet	-	74ABT_H16821A_2
Modifications:	• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. • Legal texts have been adapted to the new company name where appropriate. • Type number 74ABTH16821ADGG removed from Section 3 “Ordering information”.			
74ABT_H16821A_2	20021213	Product specification	-	74ABT_H16821A
74ABT_H16821A	19980227	Product specification	-	-

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15. Legal information

15.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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17. Contents

1 General description 1
2 Features and benefits 1
3 Ordering information 2
4 Functional diagram 2
5 Pinning information 4
5.1 Pinning 4
5.2 Pin description 5
6 Functional description 5
7 Limiting values 6
8 Recommended operating conditions 6
9 Static characteristics 7
10 Dynamic characteristics 8
11 Waveforms 9
12 Package outline 11
13 Abbreviations 13
14 Revision history 13
15 Legal information 14
15.1 Data sheet status 14
15.2 Definitions 14
15.3 Disclaimers 14
15.4 Trademarks 14
16 Contact information 15
17 Contents 16

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Date of release: 16 March 2010
Document identifier: 74ABT16821A_3