Product Overview

Address Spaces

Addressing Modes

Control Registers

Interrupt Structure

Instruction Set

1 PRODUCT OVERVIEW

SAM8 PRODUCT FAMILY

Samsung's new SAM8 family of 8-bit single-chip CMOS microcontrollers offers a fast and efficient CPU, a wide range of integrated peripherals, and various mask-programmable ROM sizes.

A dual address/data bus architecture and a large number of bit- or nibble-configurable I/O ports provide a flexible programming environment for applications with varied memory and I/O requirements.

Timer/counters with selectable operating modes are included to support real-time operations. Many SAM8 microcontrollers have an external interface that provides access to external memory and other peripheral devices.

The sophisticated interrupt structure recognizes up to eight interrupt levels. Each level can have one or more interrupt sources and vectors. Fast interrupt processing (within a minimum six CPU clocks) can be assigned to specific interrupt levels.

S3C8444 MICROCONTROLLER

The S3C8444 single-chip microcontroller is fabricated using a highly advanced CMOS process. Its design is based on the powerful SAM8 CPU core. Stop and Idle power-down modes were implemented to reduce power consumption. The size of the internal register file is logically expanded, increasing the addressable on-chip register space to 1040 bytes. A flexible yet sophisticated external interface is used to access up to 64-Kbytes of program and data memory. The S3C8444 is a versatile microcontroller that is ideal for use in a wide range of general-purpose applications such as CD-ROM/DVD-ROM drives.

Using the SAM8 modular design approach, the following peripherals were integrated with the SAM8 CPU core:

— Six configurable 8-bit general I/O ports
— One 8-bit n-channel, open-drain output port
— One 8-bit input port for A/D converter input or digital input
— Full-duplex serial data port with one synchronous and three asynchronous (UART) operating modes
— Two 8-bit timers with interval timer or PWM mode
— Two 16-bit timer/counters with four programmable operating modes
— Two programmable 8-bit PWM modules with corresponding output pins
— One 8-bit capture module with CAP input pin
— A/D converter with 8 selectable input pins

The S3C8444 is a versatile microcontroller that is ideal for use in a wide range of general-purpose ROM-less applications such as CD-ROM/DVD-ROM drivers.

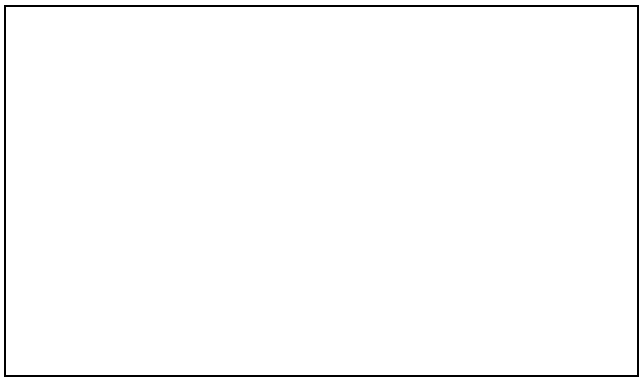


Figure 1–1. S3C8444 Microcontroller

FEATURES

CPU

- SAM8 CPU core

Memory

- 1040-byte of internal register file
- 4-kbyte internal program memory area

External Interface

- 64-Kbyte external data memory area
- 64-Kbyte external program memory (ROMless)
- 60-Kbyte external program memory (normal)

Instruction Set

- 78 instructions
- IDLE and STOP instructions

Instruction Execution Time

- 240 ns at 25 MHz f_{OSC} (minimum)

Interrupts

- 20 interrupt sources and 19 interrupt vectors
- Seven interrupt levels
- Fast interrupt processing (level0 and 3-7 only)

Timer/Counters

- Two 8-bit timers with interval timer or PWM mode (timers A and B)
- Two 16-bit timer/counters with four programmable operating modes (timers C and D)

General I/O

- Six 8-bit general I/O ports (ports 0,1,2,3,4, and 5)
- One 8-bit n-channel, open-drain output port (port 6)
- One 8-bit input port (for ADC input or port 7 digital input)

Serial Port

- Full-duplex serial data port (UART)
- Four programmable operating modes

PWM and Capture

- Two output channels (PWM0, PWM1)
- 8-bit resolution with 2-bit prescaler
- 97.66-kHz frequency (25-MHz CPU clock)
- Capture module with CAP input pin

Analog-to-Digital Converter

- Eight analog input pins
- 8-bit conversion resolution
- 7.68-µs conversion speed (25-MHz CPU clock)

Operating Temperature Range

- – 20°C to + 85°C

Operating Voltage Range

- 4.5 V to 5.5 V

Package Type

- 80-pin QFP, 80–pin TQFP

BLOCK DIAGRAM

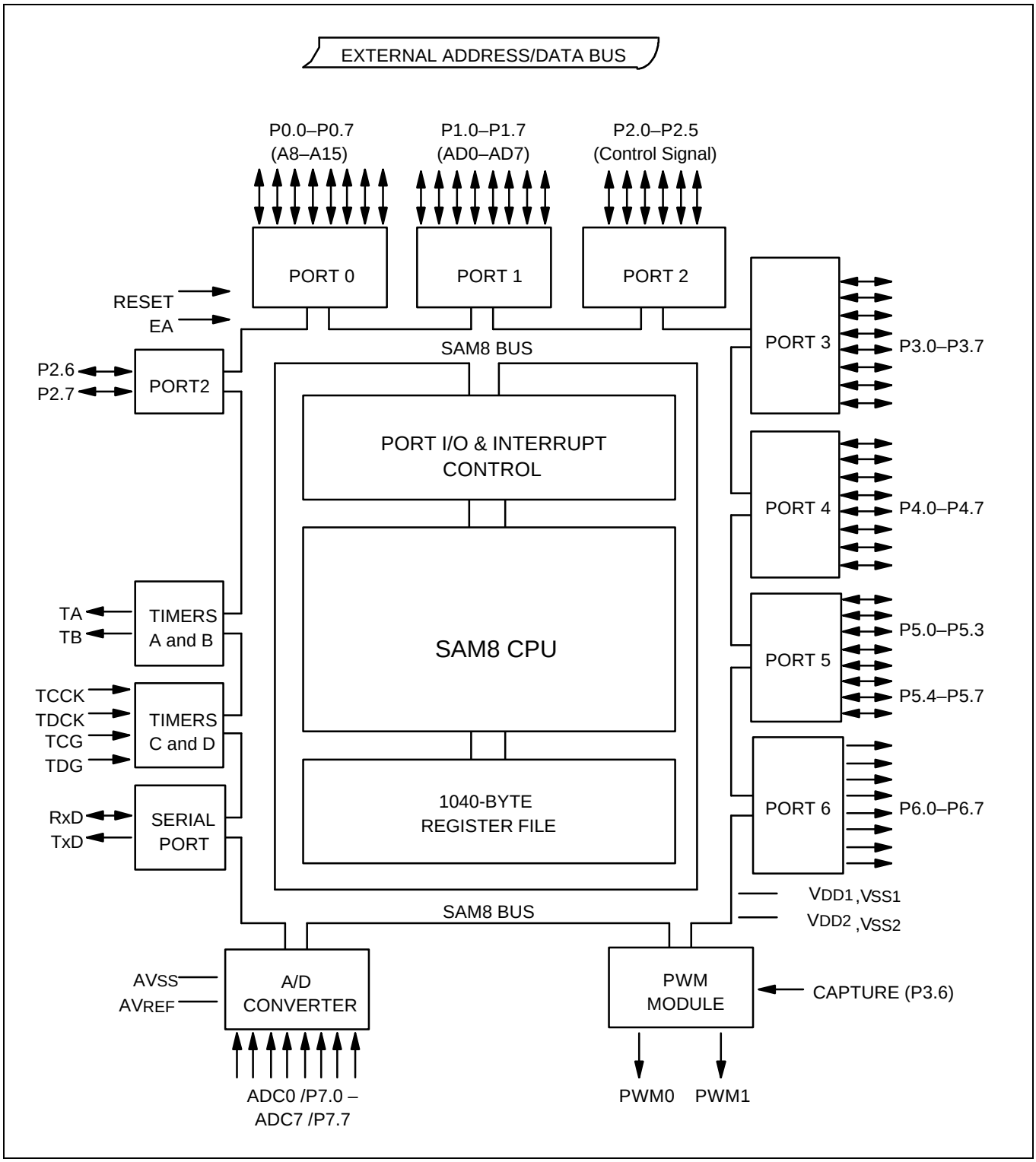


Figure 1–2. S3C8444 Block Diagram

PIN ASSIGNMENTS

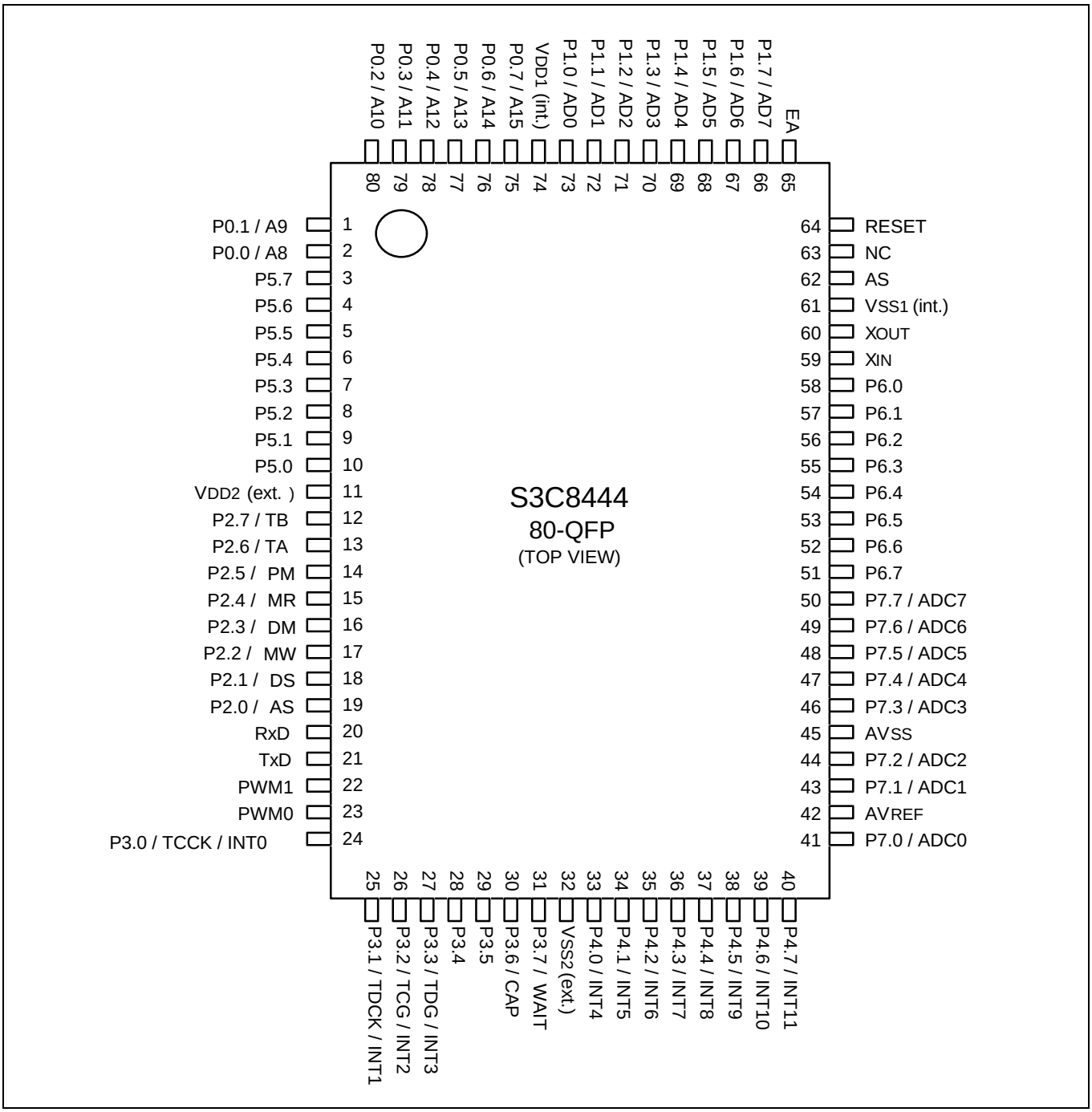


Figure 1–3. S3C8444 Pin Assignments

PIN ASSIGNMENTS (Continued)

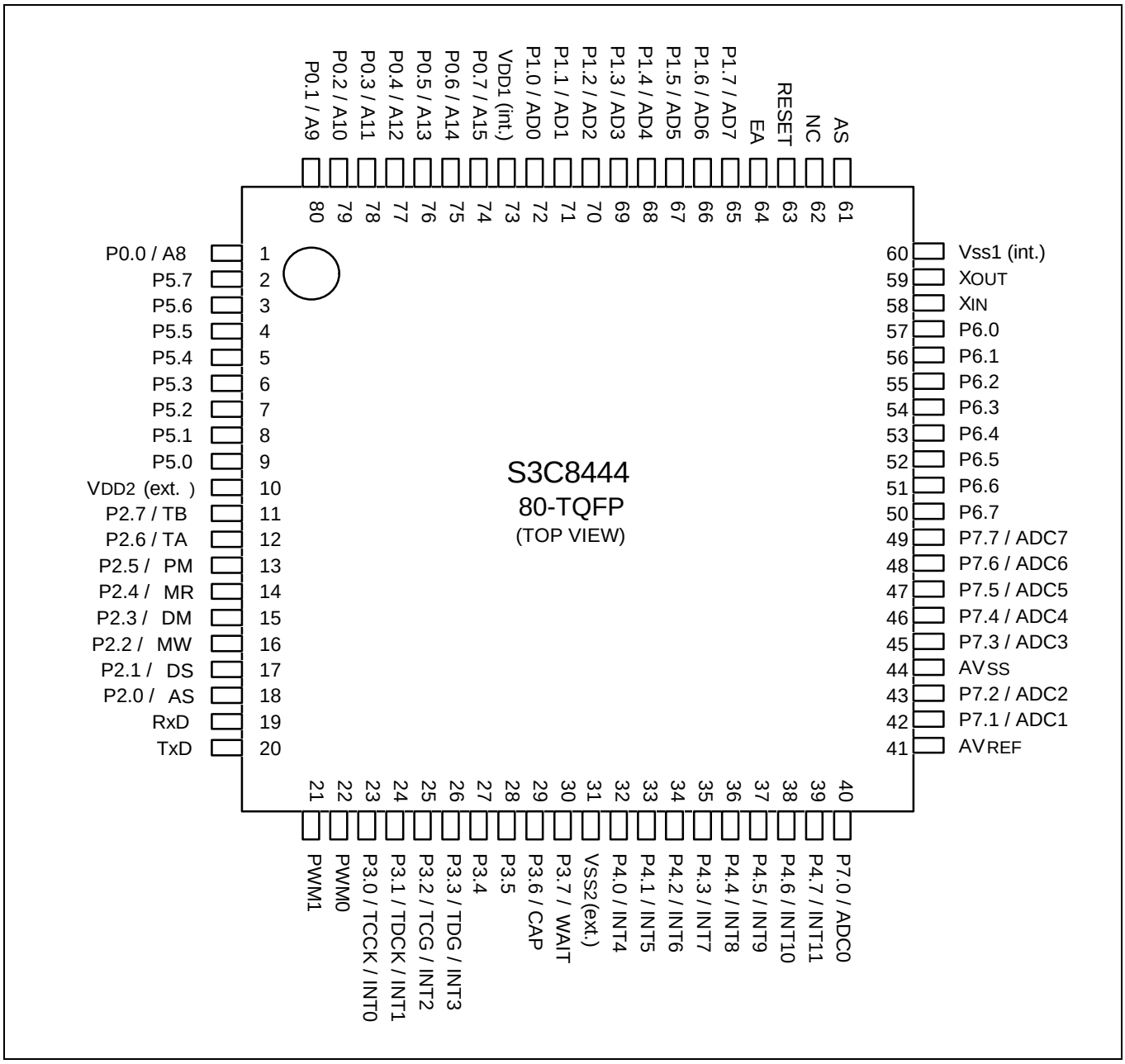


Figure 1–4. S3C8444 Pin Assignments

PIN DESCRIPTIONS

Table 1–1. S3C8444 Pin Descriptions

Pin Name	Pin Type	Pin Description	Circuit Type	QFP Pin Number	Share Pins
P0.0 - P0.7	I/O	Nibble programmable port; input or output mode selected by software; Schmitt trigger input or push-pull, open-drain output with software assignable pull-ups; alternately configurable as external interface address lines A8 - A15.	3	2, 1, 80-75	A8 - A15
P1.0 - P1.7	I/O	Same general characteristics as port 0; alternately configurable as external interface address/data lines AD0 - AD7.	3	73-66	AD0 - AD7
P2.0 - P2.7	I/O	General I/O port with Schmitt trigger input or push-pull output. bit programmable; P2.0 / Address Strobe (AS) P2.1 / Data Strobe (DS) P2.2 / Memory Write (MW) P2.3 / Data Memory select (DM) P2.4 / Memory Read (MR) P2.5 / Program Memory select (PM) P2.6 / timer A output (TA) P2.7 / timer B output (TB)	5	19 - 12	AS, DS, MW, DM, MR, PM, TA, TB
P3.0 - P3.7	I/O	General I/O port with bit programmable pins. Schmitt trigger input or push-pull output with software assignable pull-ups. Input or output mode is selectable by software. P3.0 - P3.3 are alternately used as inputs for external interrupts INT0-INT3, respectively (with noise filters and interrupt control): P3.0 / timer C clock input (TCCK) / INT0 P3.1 / timer D clock input (TDCK) / INT1 P3.2 / timer C gate input (TCG) / INT2 P3.3 / timer D gate input (TDG) / INT3 P3.6 / Capture data input (CAP) P3.7 / WAIT for slow memory interface	4	24-31	(See pin description)
P4.0 - P4.7	I/O	General I/O port with bit programmable pins. Schmitt trigger input or push-pull, open-drain output with software assignable pull-ups. Input or output mode is selectable by software. P4.0-P4.7 can alternately be used as inputs for external interrupts INT4-INT11, respectively (with noise filters and interrupt control)	4	33-40	INT4 - INT11

Table 1–1. S3C8444 Pin Descriptions (Continued)

Pin Name	Pin Type	Pin Description	Circuit Type	QFP Pin Number	Share Pins
P5.0–P5.7	I/O	General I/O port with nibble programmable pins. Schmitt trigger input or push-pull, open-drain output mode. Mode and pull-ups are assigned by software.	3	10–3	—
P6.0–P6.7	O	N-channel, open-drain output port; the pin circuits can withstand loads up to 9 volts.	8	58–51	—
ADC0–ADC7	I	Analog input pins for A/D converter module. Alternatively used as general-purpose digital input port 7.	2	41, 43–44, 46–50	P7.0–P7.7
AV_{REF}, AV_{SS}	—	A/D converter reference voltage and ground	—	42, 45	—
RxD	I/O	Serial data RxD pin for receive input and transmit output (mode 0)	6	20	—
TxD	O	Serial data TxD pin for transmit output and shift clock input (mode 0)	7	21	—
PWM0, PWM1	O	Pulse width modulation output pins	7	23, 22	—
TA, TB	O	Output pins for timer A and timer B	5	13, 12	P2.6, P2.7
INT0–INT11	I	External interrupt input pins	4	24–27, 33–40	P3.0–P3.3, P4.0–P4.7
TCCK, TDCK	I	External clock input for timer C and timer D	4	24, 25	P3.0, P3.1
TCG, TDG	I	Gate input pins for timer C and timer D	4	26, 27	P3.2, P3.3
CAP	I	Capture data input for PWM module	4	30	P3.6
WAIT	I	Input pin for the slow memory timing signal from the external interface	4	31	P3.7
RESET	I	System reset pin (pull-up resistor: 220 kΩ)	1	64	—
EA	I	External access (EA) pin with two modes: 5 V input: normal ROM-less operation with external interface (0 V is not allowed) 9 V–10 V input: for factory test mode	—	65	—
V_{DD1}, V_{SS1}	—	Power input pins for CPU operation (internal)	—	74, 61	—
V_{DD2}, V_{SS2}	—	Power input pins for port output (external)	—	11, 32	—
X_{IN}, X_{OUT}	—	Main oscillator pins	—	59, 60	—
AS	O	Address strobe	7	62	—
NC	—	No connection pins (connect to V_{SS})	—	62, 63	—

NOTE VDD1 must be connected to VDD2 in users application circuit, VSS1 & VSS2 also.

PIN CIRCUITS

Table 1–2. Pin Circuit Assignments for the S3C8444

Circuit Number	Circuit Type	S3C8444 Assignments
1	Input	RESET pin
2	Input	A/D converter input pins, ADC0–ADC7
3	I/O	Port 0, 1, and 5
4	I/O	Ports 3 and 4, TCCK, TDCK, TCG, TDG, CAP, WAIT, INT0–INT11
5	I/O	Port 2 (AS, DS, MW, DM, MR, PM, TA,TB)
6	I/O	Serial port RxD pin
7	Output	Serial port TxD pin, PWM0, PWM1 and AS
8	Output	Port 6 (n-channel, open-drain output with high current capability)

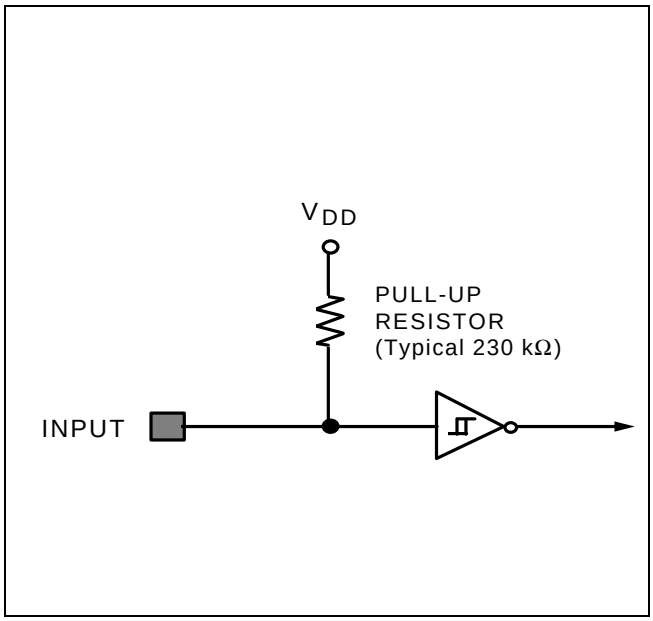


Figure 1–5. Pin Circuit Type 1 (RESET)

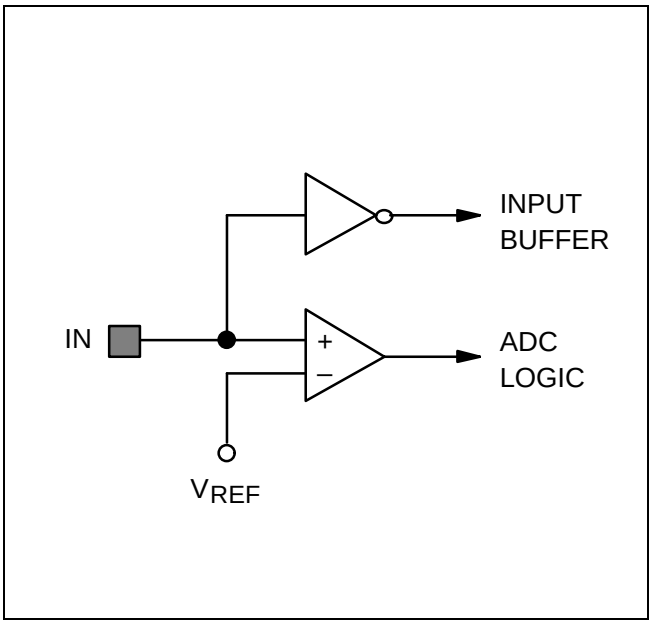


Figure 1–6. Pin Circuit Type 2 (ADC0–ADC7)

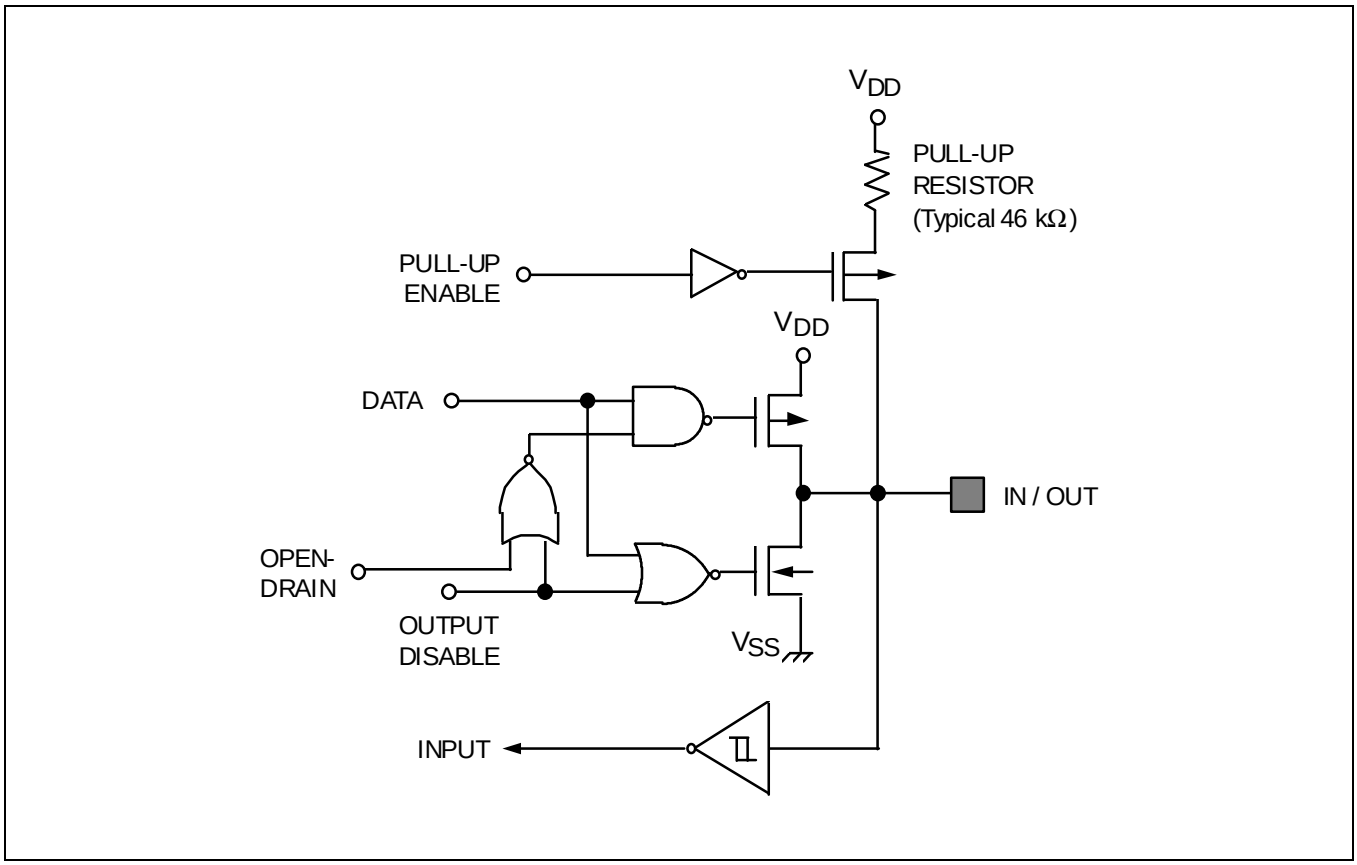


Figure 1–7. Pin Circuit Type 3 (Ports 0,1, and 5)

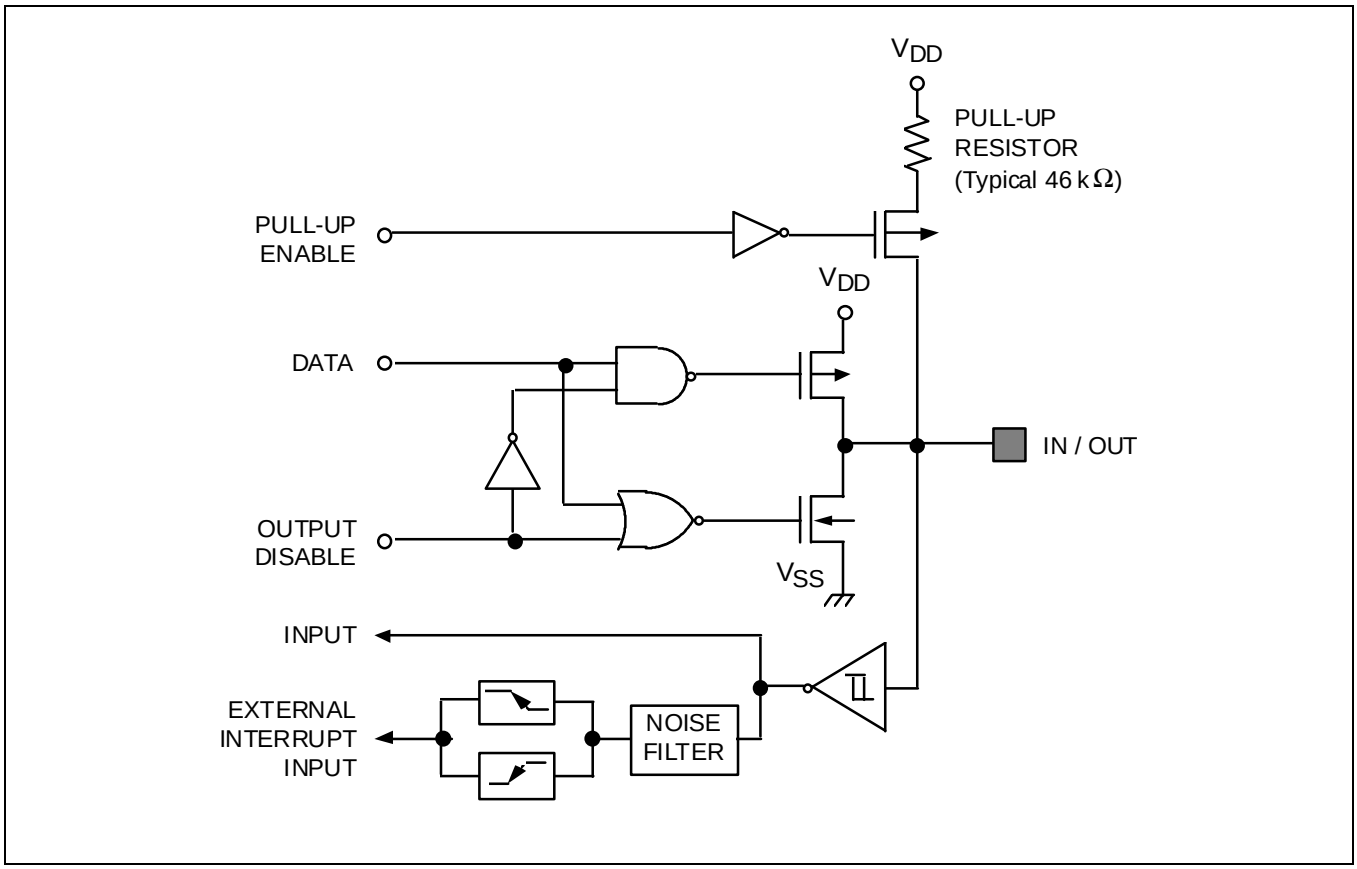


Figure 1–8. Pin Circuit Type 4
(Ports 3 and 4, TCCK, TDCK, TCG, TDG, CAP, WAIT, INT0–INT11)

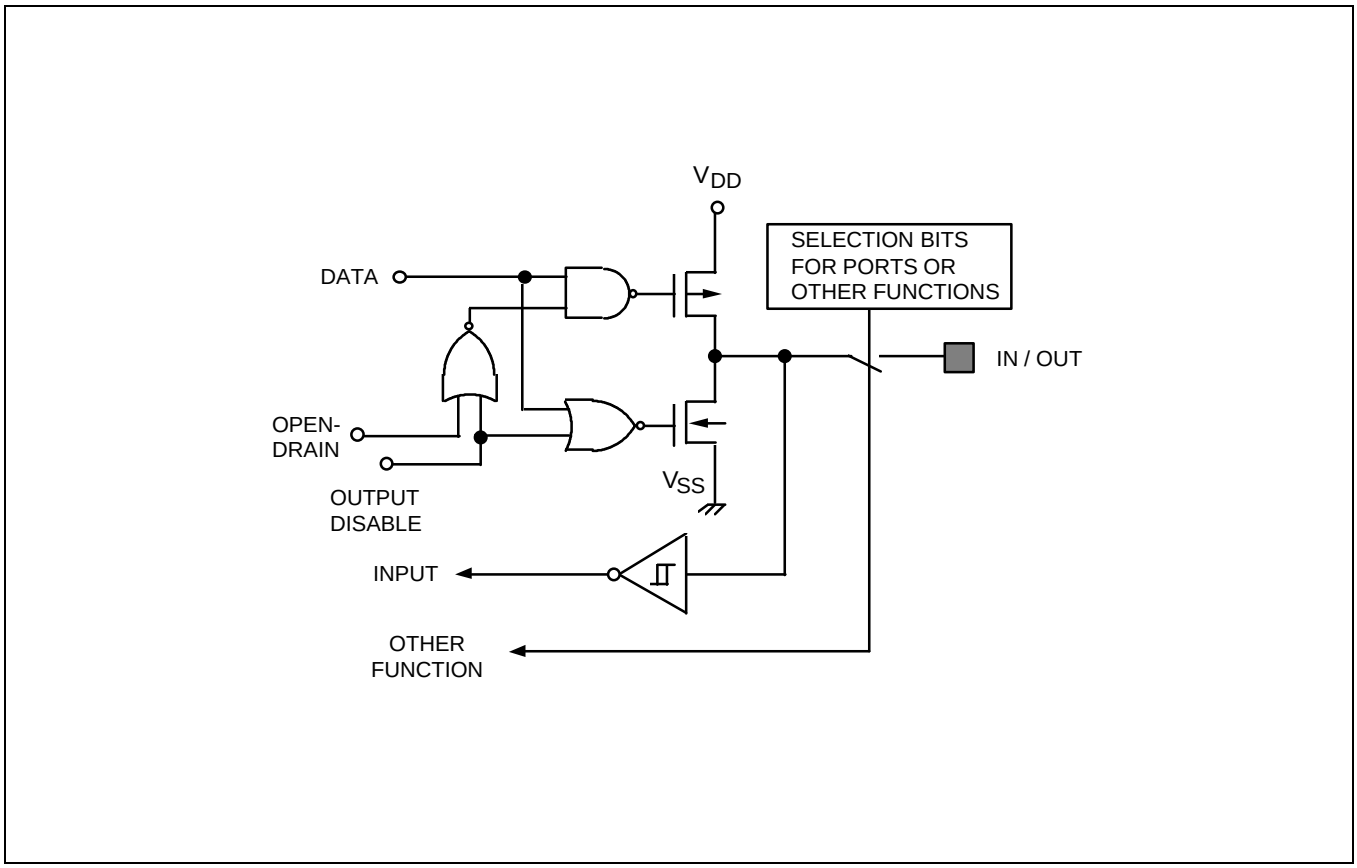


Figure 1–9. Pin Circuit Type 5 (Port 2, AS, DS, MW, DM, MR, PM, TA and TB)

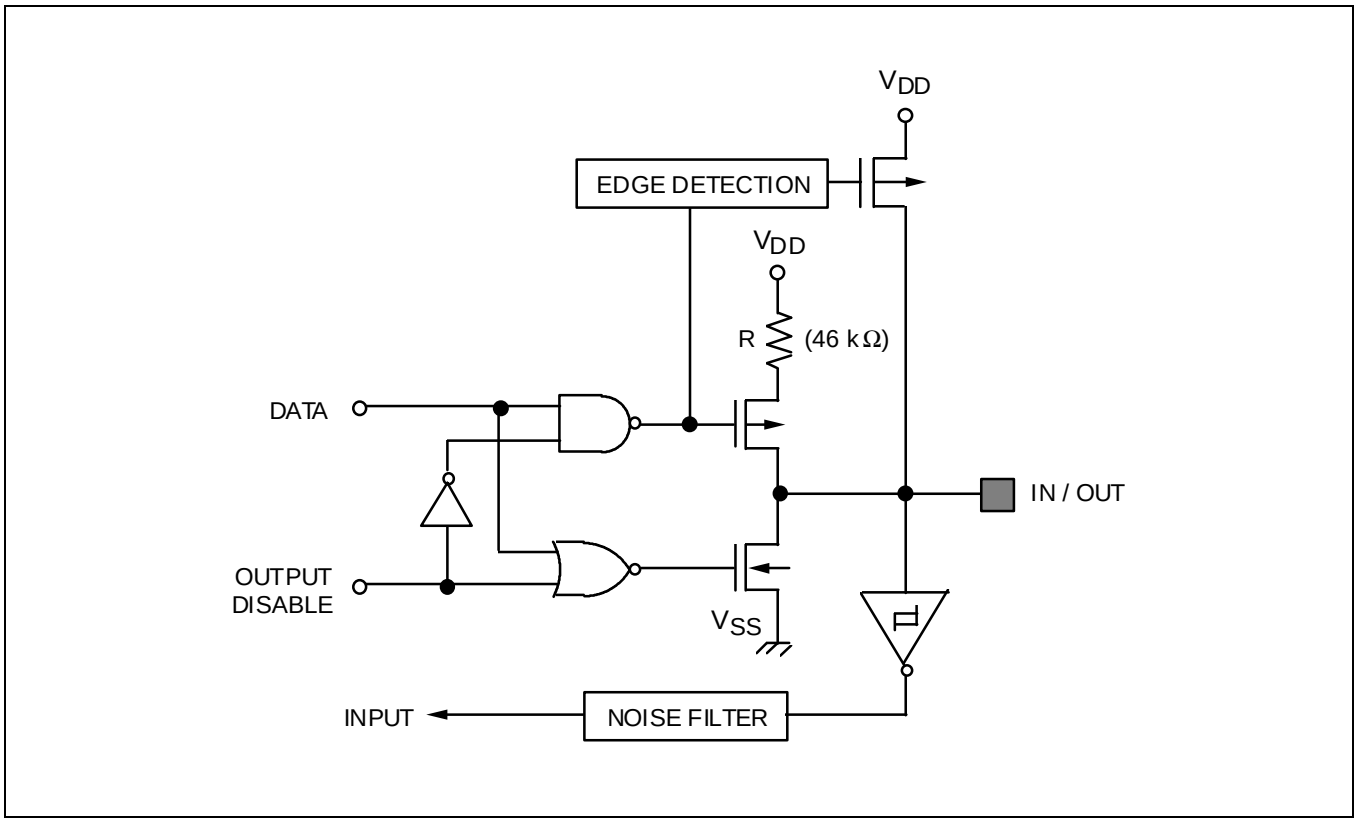


Figure 1–10. Pin Circuit Type 6 (Serial RxD Pin)

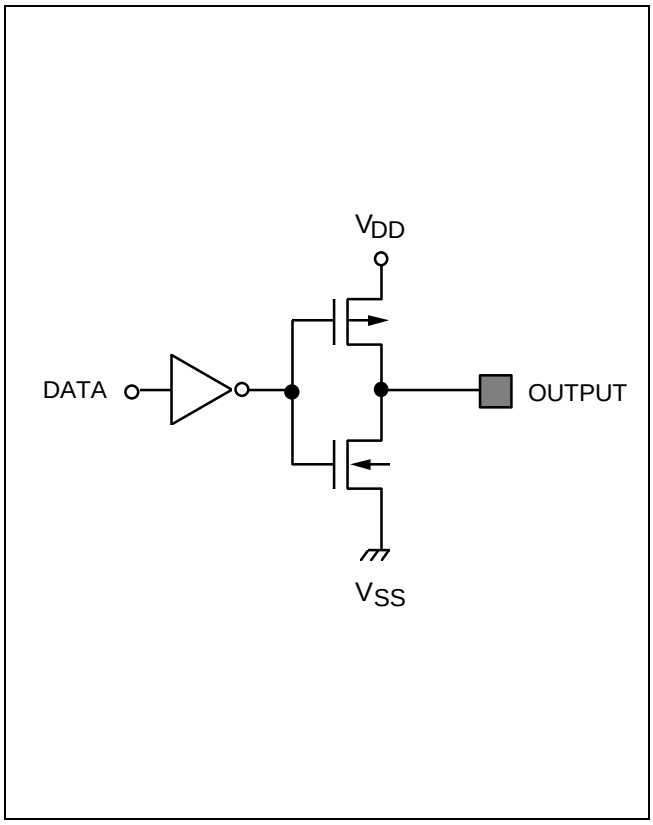
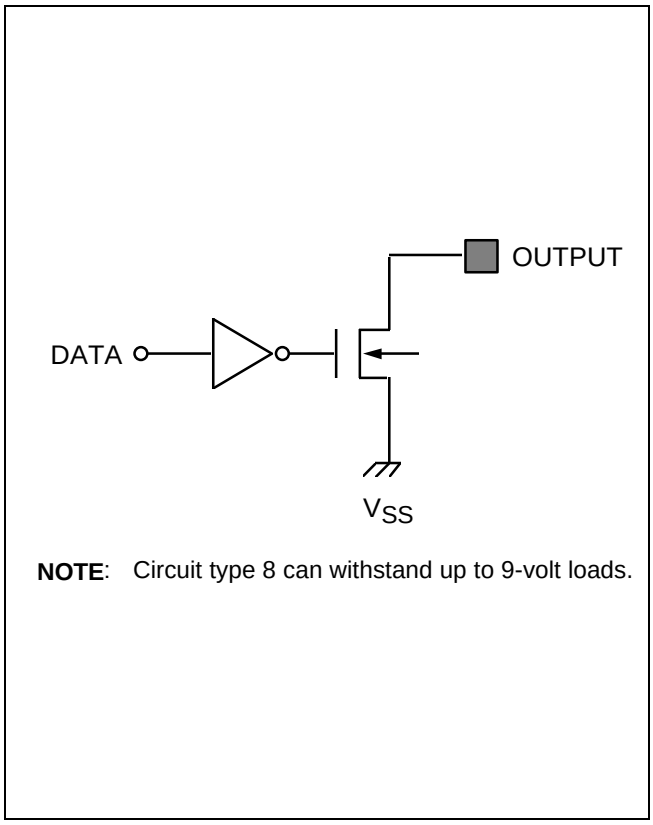


Figure 1–11. Pin Circuit Type 7 (AS, serial TxD Pin, PWM0, PWM1)



NOTE: Circuit type 8 can withstand up to 9-volt loads.

Figure 1–12. Pin Circuit Type 8 (Port 6)

16 ELECTRICAL DATA

In this section, S3C8444 electrical characteristics are presented in tables and graphs. The information is arranged in the following order:

— Absolute maximum ratings
— DC electrical characteristics
— AC electrical characteristics
— Input timing for external interrupts (ports 3 and 4)
— Input timing for RESET
— I/O capacitance
— Data retention supply voltage in Stop mode
— Stop mode release timing initiated by RESET
— A./D Converter Electrical Characteristics
— Serial port timing characteristics in mode 0 (10 MHz)
— Serial clock waveform
— Serial port timing in mode 0 (shift register mode)
— External memory timing characteristics (10 MHz)
— External memory read and write timing
— Recommended A/D converter circuit for highest absolute accuracy
— Main oscillator frequency (f_{OSC1})
— Main oscillator clock stabilization time (t_{ST1})
— Clock timing measurement at X_{IN}
— Suboscillator clock stabilization time (t_{ST2})
— Characteristic curves

Table 16–1. Absolute Maximum Ratings

(T_A = 25°C)

Parameter	Symbol	Conditions	Rating	Unit
Supply voltage	V_{DD}		– 0.3 to +7.0	V
Input voltage	V_{I1}	Port 6 only (open-drain)	– 0.3 to +10	V
	V_{I2}	All ports except port 6	– 0.3 to V_{DD} + 0.3	
Output voltage	V_O		– 0.3 to V_{DD} + 0.3	V
Output current high	I_{OH}	One I/O pin active	– 18	mA
		All I/O pins active	– 60	
Output current low	I_{OL}	One I/O pin active	30	mA
		Total pin current for ports 0, 2, 3, 4, 6	100	
		Total pin current for ports 1 and 5	200	
Operating temperature	T_A		– 20 to + 85	°C
Storage temperature	T_{STG}		– 65 to + 150	°C

Table 16–2. D.C. Electrical Characteristics

(T_A = – 20°C to + 85°C, V_{DD} = 4.5 V to 5.5 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input high voltage	V_{IH1}	All input pins except V_{IH2}	0.8 V_{DD}	–	V_{DD}	V
	V_{IH2}	X_{IN}	V_{DD} – 0.5			
Input low voltage	V_{IL1}	All input pins except V_{IL2}	–	–	0.2 V_{DD}	V
	V_{IL2}	X_{IN}			0.4	
Output high voltage	V_{OH1}	V_{DD} = 4.5 V to 5.5 V I_{OH} = – 1 mA Port 1 only	V_{DD} – 1.0	–	–	V
	V_{OH2}	V_{DD} = 4.5 V to 5.5V I_{OH} = – 200 µA All output pins except port 1	V_{DD} – 1.0			

Table 16–2. D.C. Electrical Characteristics (Continued)

(T_A = – 20°C to + 85°C, V_{DD} = 4.5 V to 5.5 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Output low voltage	V_{OL1}	V_{DD} = 4.5 V to 5.5 V I_{OL} = 2 mA All output pins except port 5	–	–	0.4	V
	V_{OL2}	V_{DD} = 4.5 V to 5.5 V I_{OL} = 1.5 mA Port 5				
Input high leakage current	I_{LIH1}	V_{IN} = V_{DD} All input pins except X_{IN}	–	–	3	µA
	I_{LIH2}	V_{IN} = V_{DD} X_{IN}			20	
Input low leakage current	I_{LIL1}	V_{IN} = 0 V All input pins except X_{IN}, and RESET	–	–	– 3	µA
	I_{LIL2}	V_{IN} = 0 V X_{IN}			– 20	
Output high leakage current	I_{LOH1}	V_{OUT} = V_{DD} All output pins except for port 6	–	–	5	µA
	I_{LOH2}	Port 6 (open-drain) V_{OUT} = 9 V			20	
Output low leakage current	I_{LOL}	V_{OUT} = 0 V	–	–	– 5	µA
Pull-up resistor	R_{L1}	V_{IN} = 0 V; V_{DD} = 5 V ± 10% Ports 0, 1, 4, 5, and RxD	30	46	80	kΩ
	R_{L2}	V_{IN} = 0 V; V_{DD} = 5 V ± 10% RESET only	120	230	320	
Supply current (1)	I_{DD1}	V_{DD} = 5 V ± 10% 25 MHz crystal oscillator	–	35	50	mA
		V_{DD} = 5 V ± 10% 10 MHz crystal oscillator		30		
	I_{DD2}	Idle mode: V_{DD} = 5 V ± 10% 25 MHz crystal oscillator		11	25	
		Idle mode: V_{DD} = 5 V ± 10% 10 MHz crystal oscillator		5		
	I_{DD3}	Stop mode; V_{DD} = 5 V ± 10%		3	20	µA

NOTE: Supply current does not include current drawn through internal pull-up resistors or external output current loads.

Table 16–3. A.C. Electrical Characteristics

(T_A = – 20°C to + 85°C, V_{DD} = 4.5 V to 6.0V)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Interrupt input high, low width	t_{INTH}, t_{INTL}	P3.0–P3.3, P4.0–P4.7	3	–	–	t_{CPU}
RESET input low width	t_{RSL}	Input	22	–	–	t_{CPU}

NOTES:
1. The unit t_{CPU} means one CPU clock period.
2. The oscillator frequency is the same as CPU clock frequency.

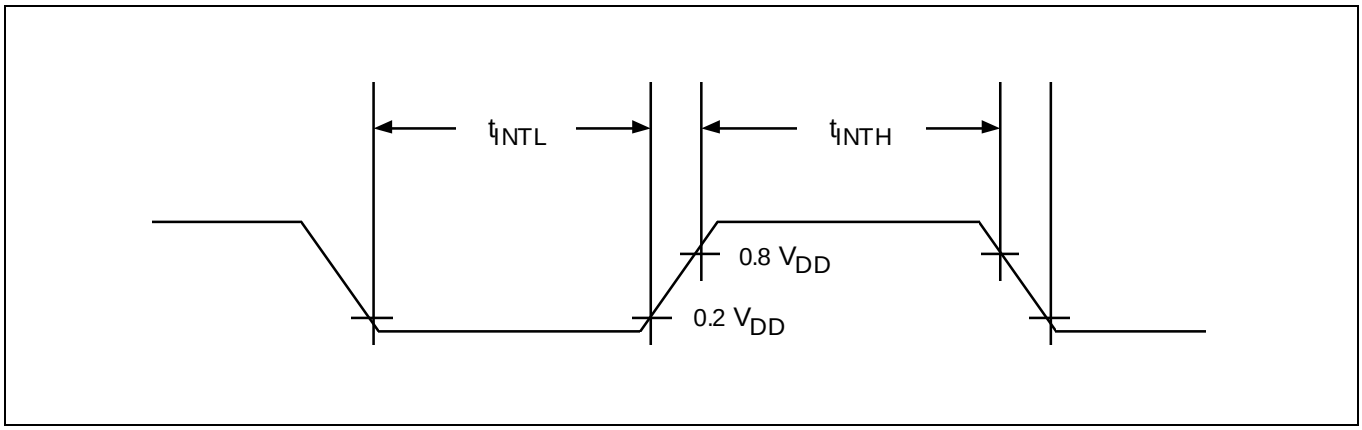


Figure 16–1. Input Timing for External Interrupts (Ports 3 and 4)

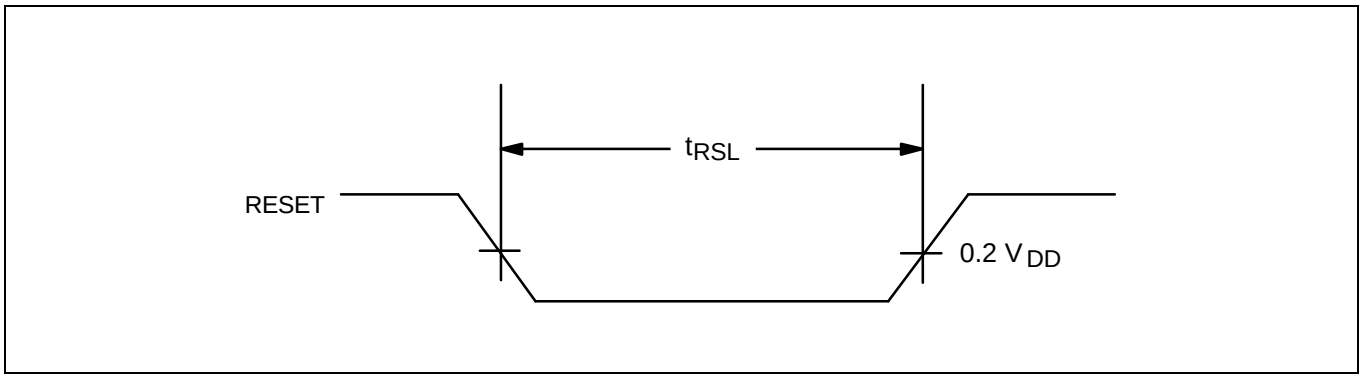


Figure 16–2. Input Timing for RESET

Table 16–4. Input/Output Capacitance

(T_A = – 20°C to + 85°C, V_{DD} = 0 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input capacitance	C_{IN}	f = 1 MHz; unmeasured pins are returned to V_{SS}	–	–	10	pF
Output capacitance	C_{OUT}					
I/O capacitance	C_{IO}					

Table 16–5. Data Retention Supply Voltage in Stop Mode

(T_A = – 20°C to + 85°C)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Data retention supply voltage	V_{DDDR}		2	–	6	V
Data retention supply current	I_{DDDR}	V_{DDDR} = 2 V	–	–	5	µA

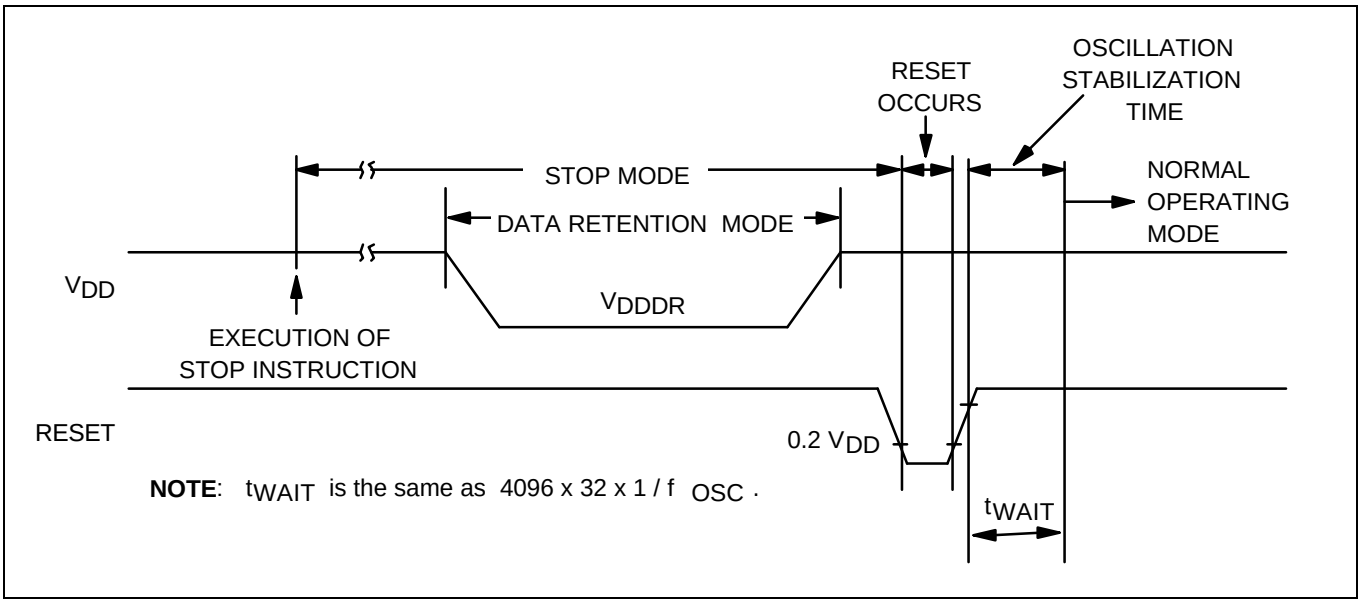


Figure 16–3. Stop Mode Release Timing Initiated by RESET

Table 16–6. A/D Converter Electrical Characteristics

(T_A = – 20°C to + 85°C, V_{DD} = 4.5 V to 6.0 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Resolution			8	8	8	bit
Absolute accuracy (1)		V_{DD} = 5.12 V CPU clock = 18 MHz AV_{REF} = 5.12 V AV_{SS} = 0 V	–	–	| 3 |	LSB
Conversion time (2)	t_{CON}		$t_{CPU} \times 192$ (3)	–	–	µs
Analog reference voltage	AV_{REF}		2.56	–	V_{DD}	V
Analog ground	AV_{SS}		V_{SS}	–	–	V
Analog input voltage	V_{IAN}		AV_{SS}	–	AV_{REF}	V
Analog input impedance	R_{AN}		2	–	–	M½

NOTES:
1. Excluding quantization error, absolute accuracy equals ± 1/2 LSB.
2. 'Conversion time' is the time required from the moment a conversion operation starts until it ends.
3. t_{CPU} is the CPU clock period.

Table 16–7. Serial Port Timing Characteristics in Mode 0 (10 MHz)

(T_A = – 20°C to + 85°C, V_{DD} = 4.5 V to 6.0V, V_{SS} = 0 V)

Parameter	Symbol	Min	Typ	Max	Unit
Serial port clock cycle time	t_{SCK}	500	$t_{CPU} \times 6$	700	ns
Output data setup to clock rising edge	t_{S1}	300	$t_{CPU} \times 5$	–	
Clock rising edge to input data valid	t_{S2}	–	–	300	
Output data hold after clock rising edge	t_{H1}	50	t_{CPU}	–	
Input data hold after clock rising edge	t_{H2}	0	–	–	
Serial port clock high, low width	t_{HIGH}, t_{LOW}	200	$t_{CPU} \times 3$	400	

NOTES:
1. All times are in ns and assume a 10 MHz input frequency.
2. The unit t_{CPU} means one CPU clock period.
3. The oscillator frequency is identical to the CPU clock frequency.

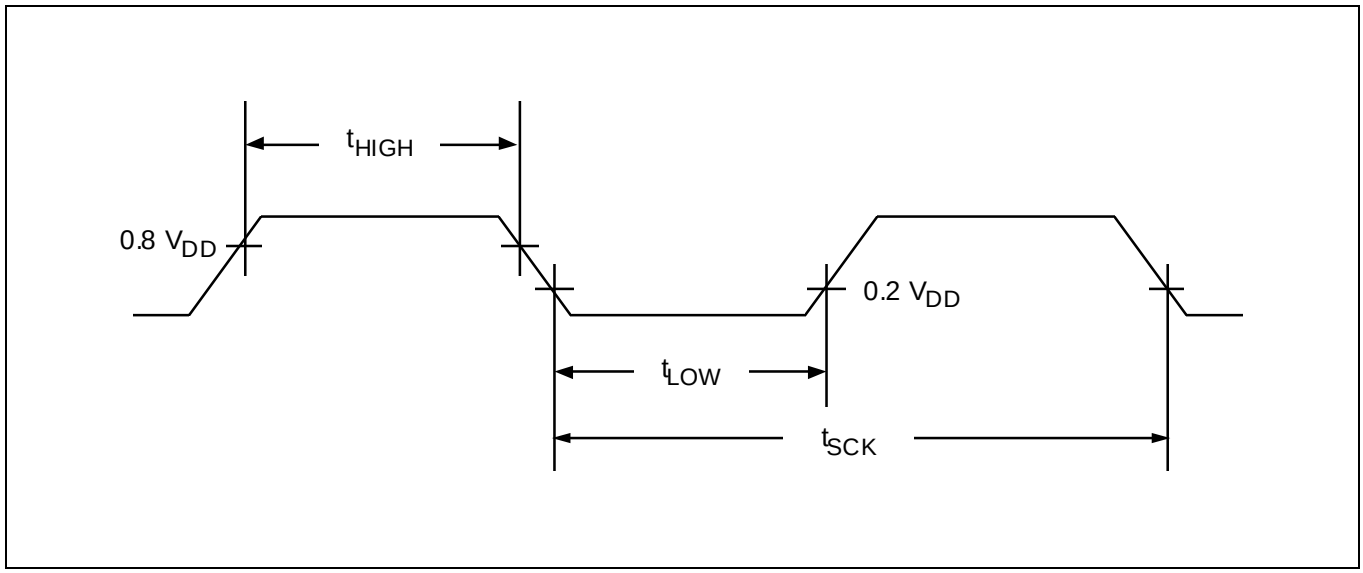
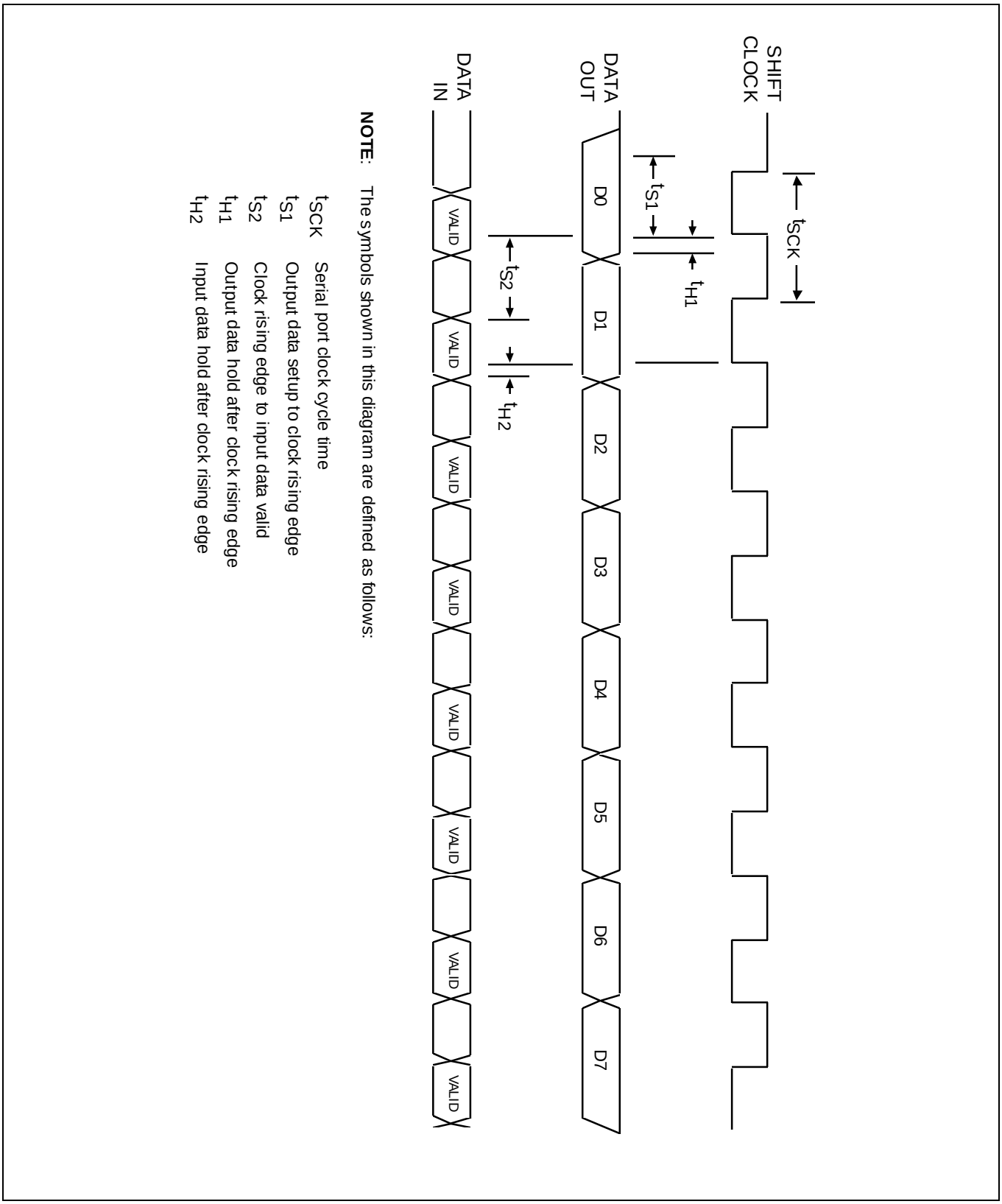


Figure 16–4. Serial Clock Waveform



NOTE: The symbols shown in this diagram are defined as follows:

t_{SCK}	Serial port clock cycle time
t_{S1}	Output data setup to clock rising edge
t_{S2}	Clock rising edge to input data valid
t_{H1}	Output data hold after clock rising edge
t_{H2}	Input data hold after clock rising edge

Figure 16–5. Serial Port Timing in Mode 0 (Shift Register Mode)

Table 16–8. External Memory Timing Characteristics (10 MHz)

(T_A = – 20°C to + 85°C, V_{DD} = 4.5 V to 6.0 V)

Number	Symbol	Parameter	Normal Timing		Extended Timing	
			Min	Max	Min	Max
1	t_{dA} (AS)	Address valid to AS ↑ delay	10	–	50	–
2	t_{dAS} (A)	AS ↑ to address float delay	35	–	85	–
3	t_{dAS} (DR)	AS ↑ to read data required valid	–	140	–	335
4	t_{wAS}	AS low width	35	–	85	–
5	t_{dA} (DS)	Address float to DS ↓	0	–	0	–
6a	t_{wDS} (read)	DS (read) low width	125	–	275	–
6b	t_{wDS} (write)	DS (write) low width	65	–	165	–
7	t_{dDS} (DR)	DS ↓ to read data required valid	–	80	–	255
8	t_{hDS} (DR)	Read data to DS ↑ hold time	0	–	0	–
9	t_{dDS} (A)	DS ↑ to address active delay	20	–	70	–
10	t_{dDS} (AS)	DS ↑ to AS ↓ delay	30	–	80	–
11	t_{dDO} (DS)	Write data valid to DS (write) ↓ delay	10	–	50	–
12	t_{dAS} (W)	AS ↑ to wait delay	–	90	–	335
13	t_{hDS} (W)	DS ↑ to wait hold time	0	–	0	–
14	t_{dRW} (AS)	R/W valid to AS ↑ delay	20	–	70	–
15	t_{dDS} (DW)	DS ↑ to write data not valid delay	20	–	70	–

NOTES:
1. All times are in ns and assume a 10 MHz input frequency.
2. Wait states add 100 ns to the time of numbers 3, 6a, 6b, and 7.
3. Auto-wait states add 100 ns to the time of number 12.

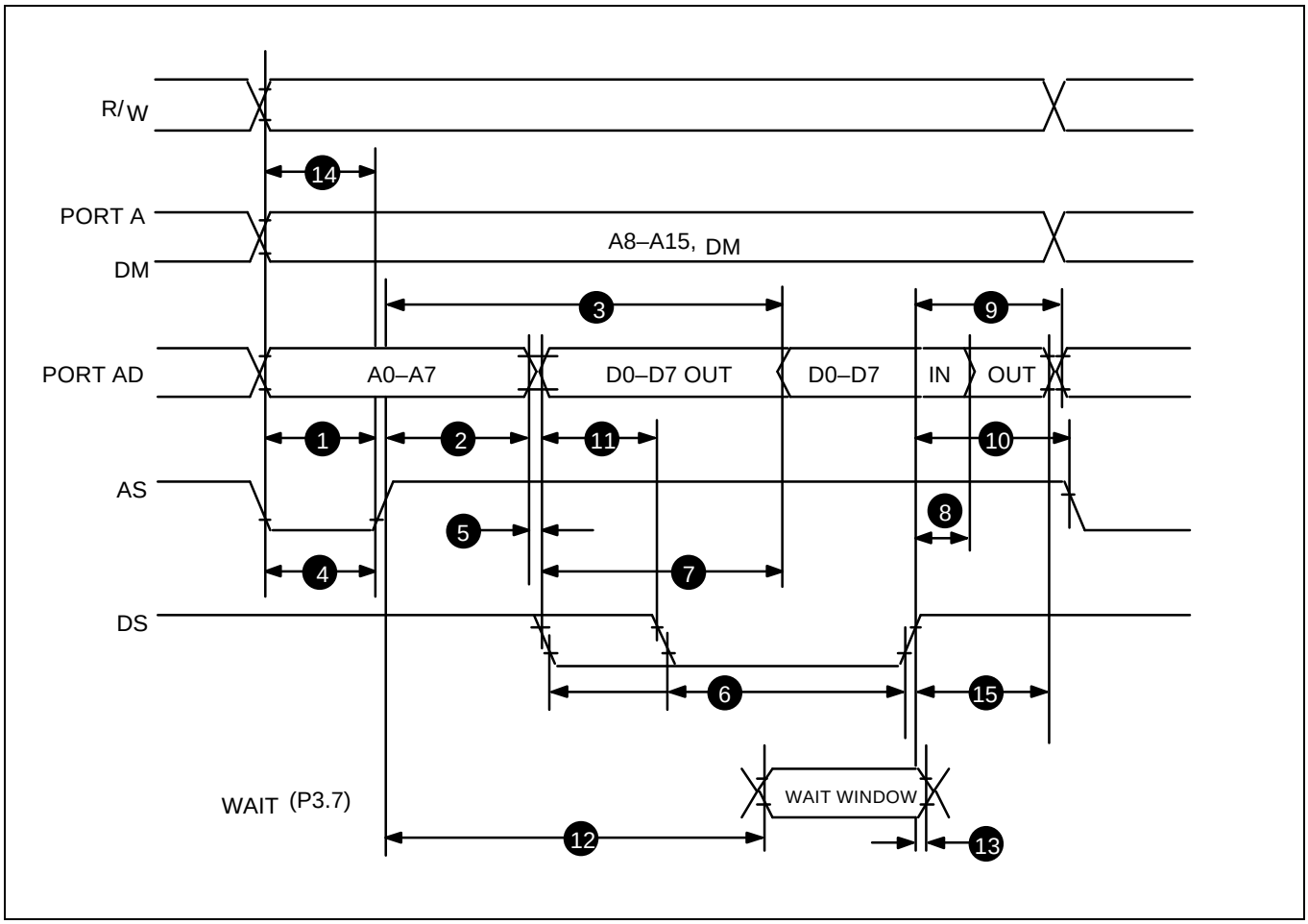
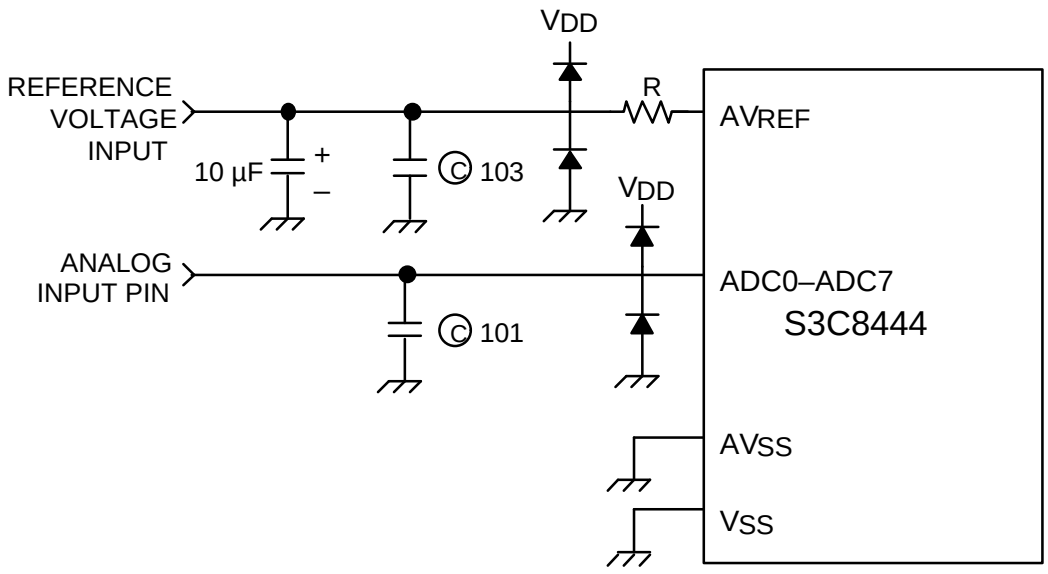


Figure 16–6. External Memory Read and Write Timing

(See Table 15–7 for a description of each timing point.)



NOTE The symbol 'R' signifies an offset resistor with a value of from 50 to 100 Ohms. If this resistor is omitted, the absolute accuracy will be maximum of 4 LSBs.

Figure 16–7. Recommended A/D Converter Circuit for Highest Absolute Accuracy

Table 16–9. Main Oscillator Frequency (f_{OSC1})

(T_A = – 20°C + 85°C, V_{DD} = 4.5 V to 6.0 V)

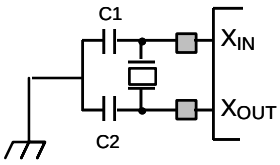
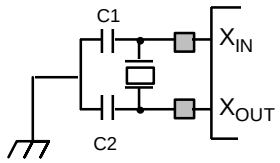
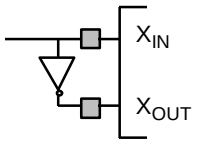
Oscillator	Clock Circuit	Test Condition	Min	Typ	Max	Unit
Crystal		CPU clock oscillation frequency	1	–	18	MHz
Ceramic		CPU clock oscillation frequency	1	–	18	MHz
External clock		X_{IN} input frequency	1	–	18	MHz

Table 16–10. Recommended Oscillator Constants

(T_A = – 20°C + 85°C, V_{DD} = 4.5 V to 6.0 V)

Manufacturer	Product Name	Load Cap (pF)		Oscillator Voltage Range (V)		Remarks
		C1	C2	MIN	MAX	
TDK	CCR20.0MS6	5	5	4.5	5.5	SMD Type
	CCR24.0M6	5	5	4.5	5.5	SMD Type
	CCR25.0M6	–	5	4.5	5.5	SMD Type

NOTE: On-chip C: 30pF ±20% built in.

Table 16–11. Main Oscillator Clock Stabilization Time (t_{ST1})

(T_A = – 20°C + 85°C, V_{DD} = 4.5 V to 6.0 V)

Oscillator	Test Condition	Min	Typ	Max	Unit
Crystal	V_{DD} = 4.5 V to 6.0 V	–	–	20	ms
Ceramic	Stabilization occurs when V_{DD} is equal to the minimum oscillator voltage range.	–	–	10	ms
External clock	X_{IN} input high and low level width (t_{XH}, t_{XL})	25	–	500	ns

NOTE: Oscillation stabilization time (t_{ST1}) is the time required for the CPU clock to return to its normal oscillation frequency after a power-on occurs, or when Stop mode is ended by a RESET signal. The RESET should therefore be held at low level until the t_{ST1} time has elapsed (see Figure 15–3).

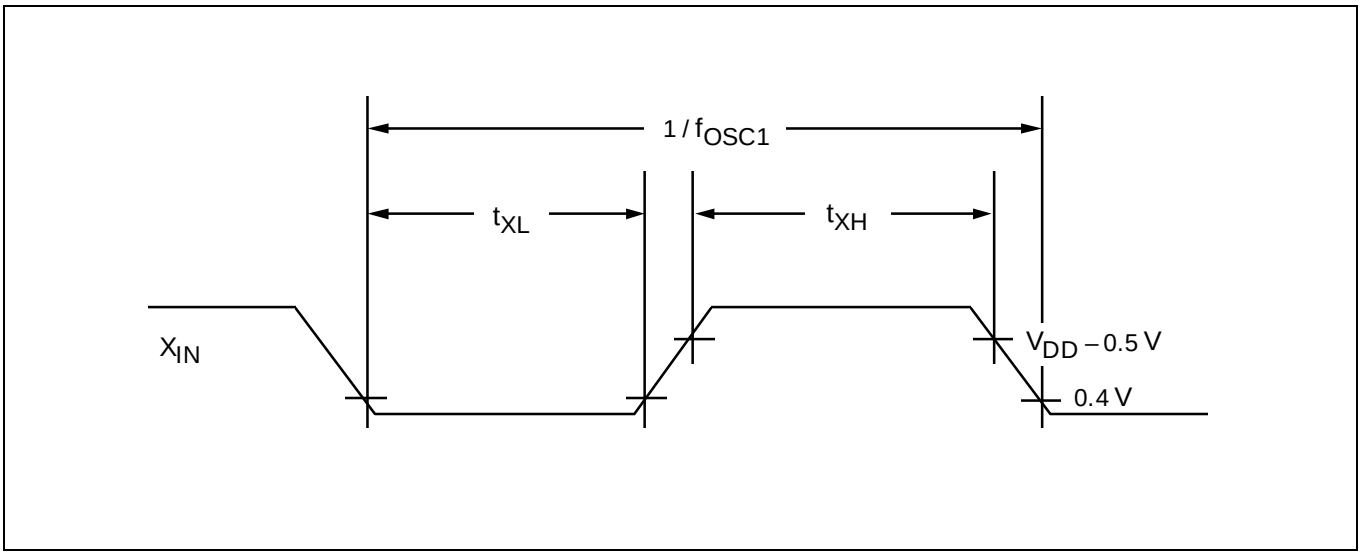


Figure 16–8. Clock Timing Measurement at X_{IN}

CHARACTERISTIC CURVES

NOTE

The characteristic values shown in the following graphs are based on actual test measurements. They do not, however, represent guaranteed operating values.

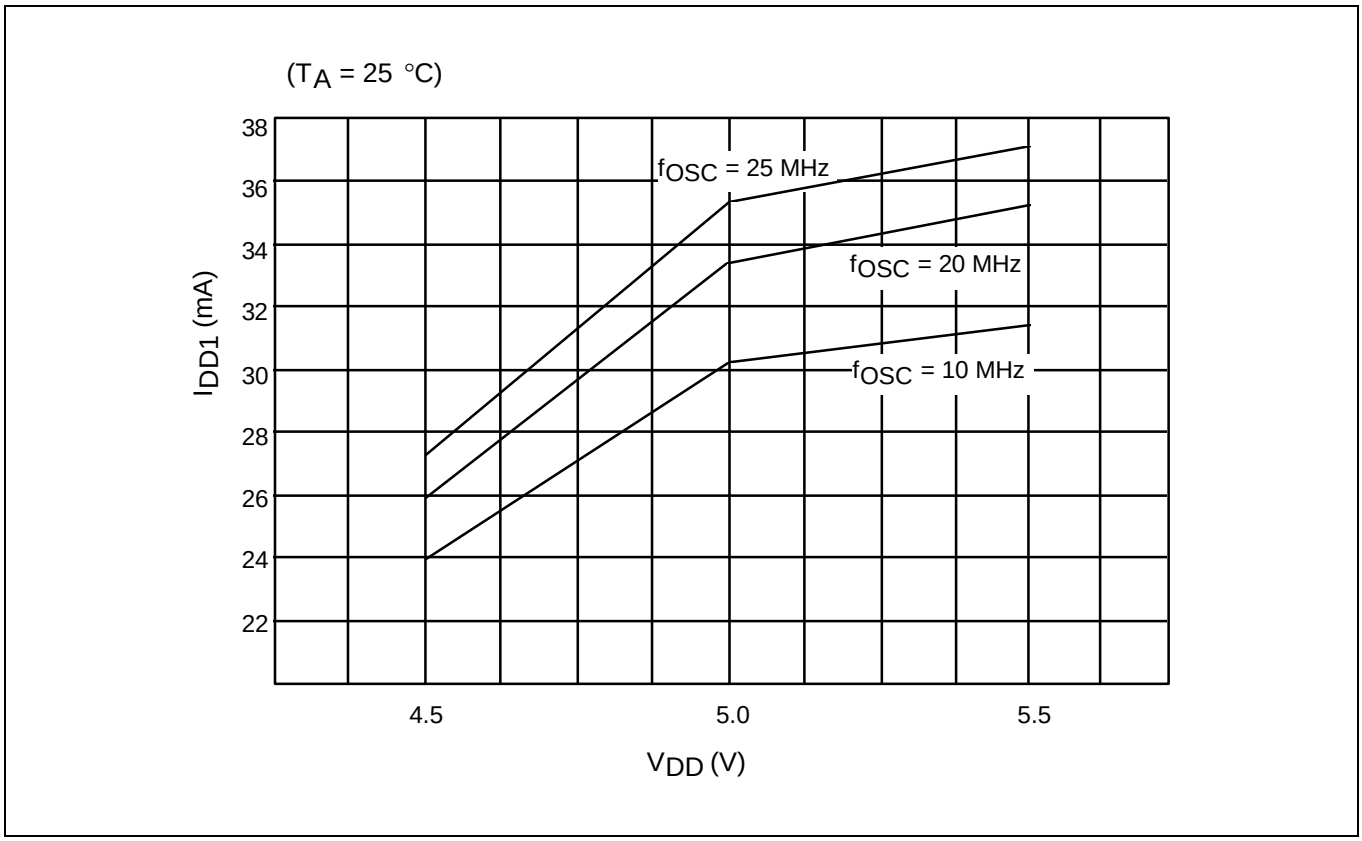


Figure 16–9. IDD1 vs VDD

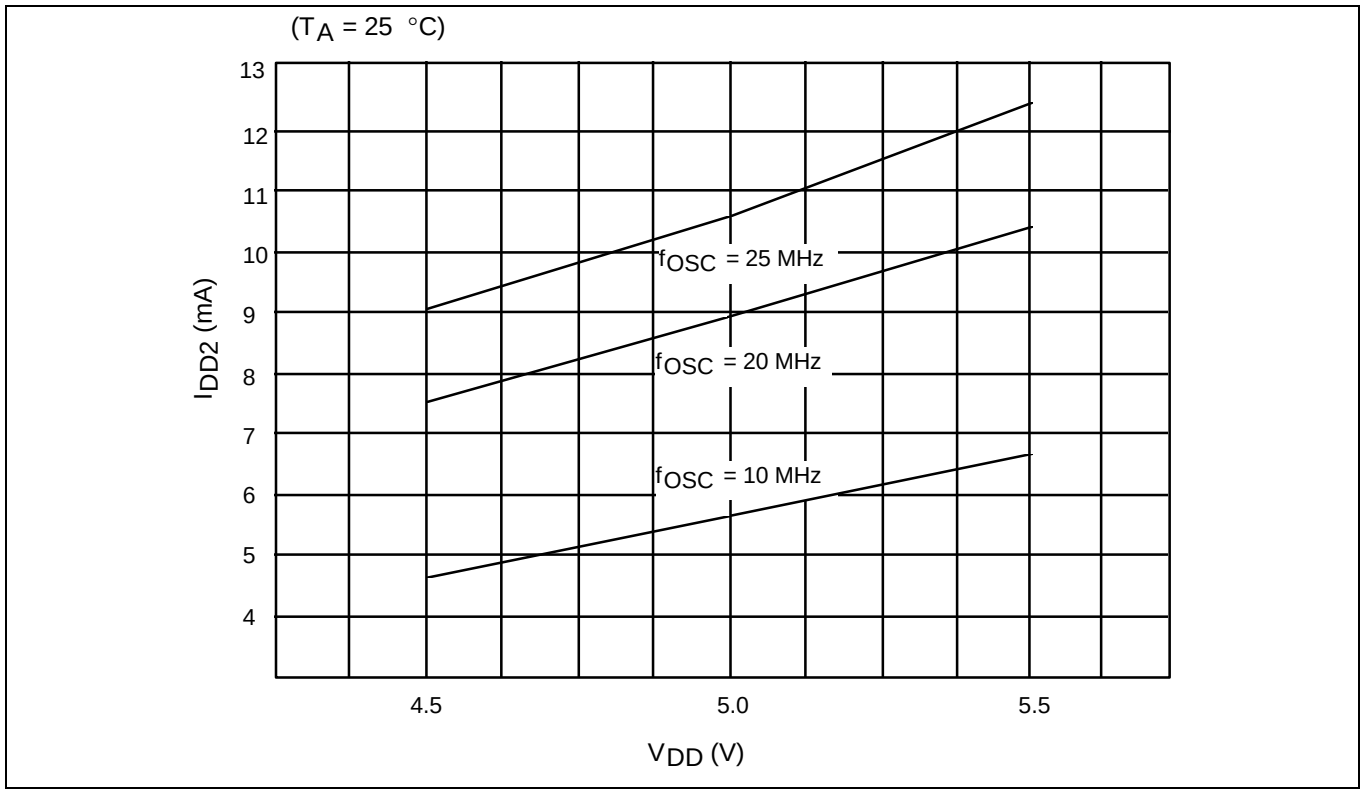


Figure 16–10. IDD2 vs VDD

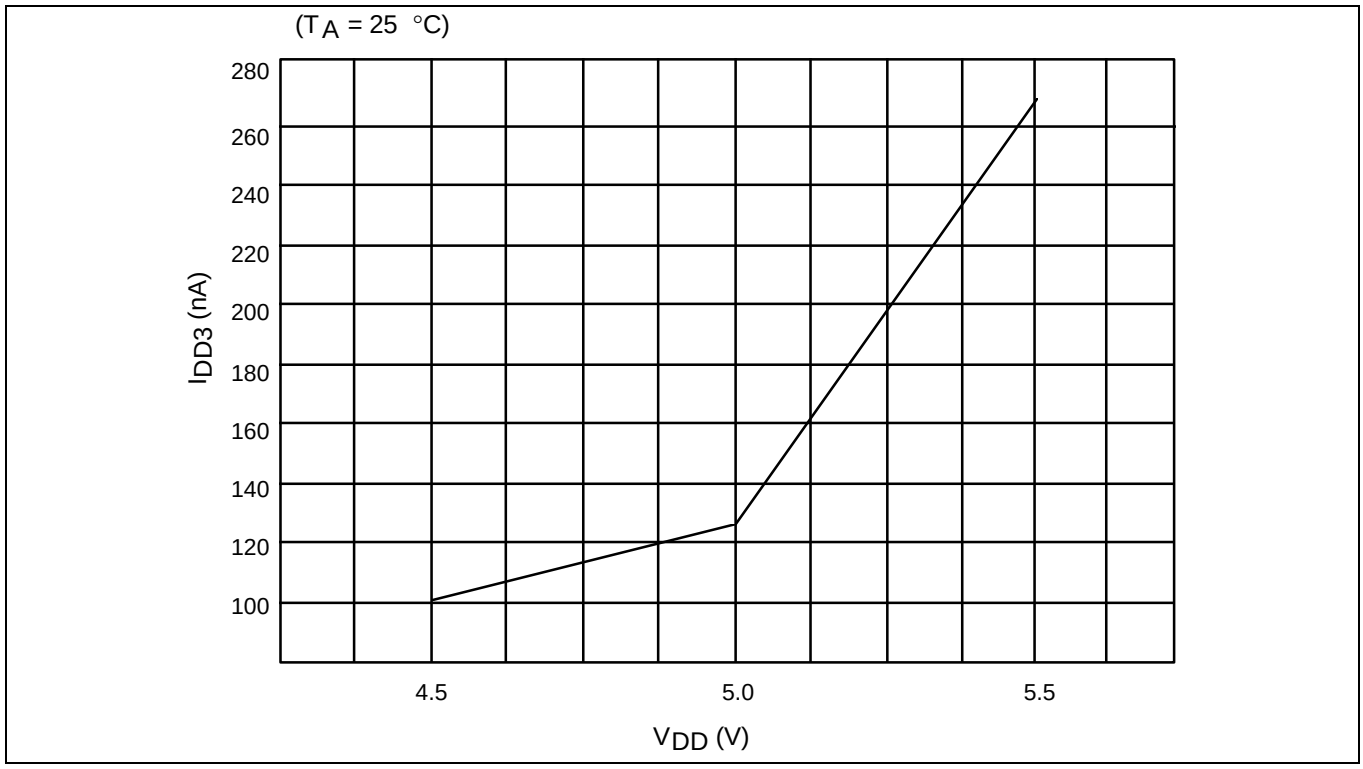


Figure 16–11. IDD3 vs VDD

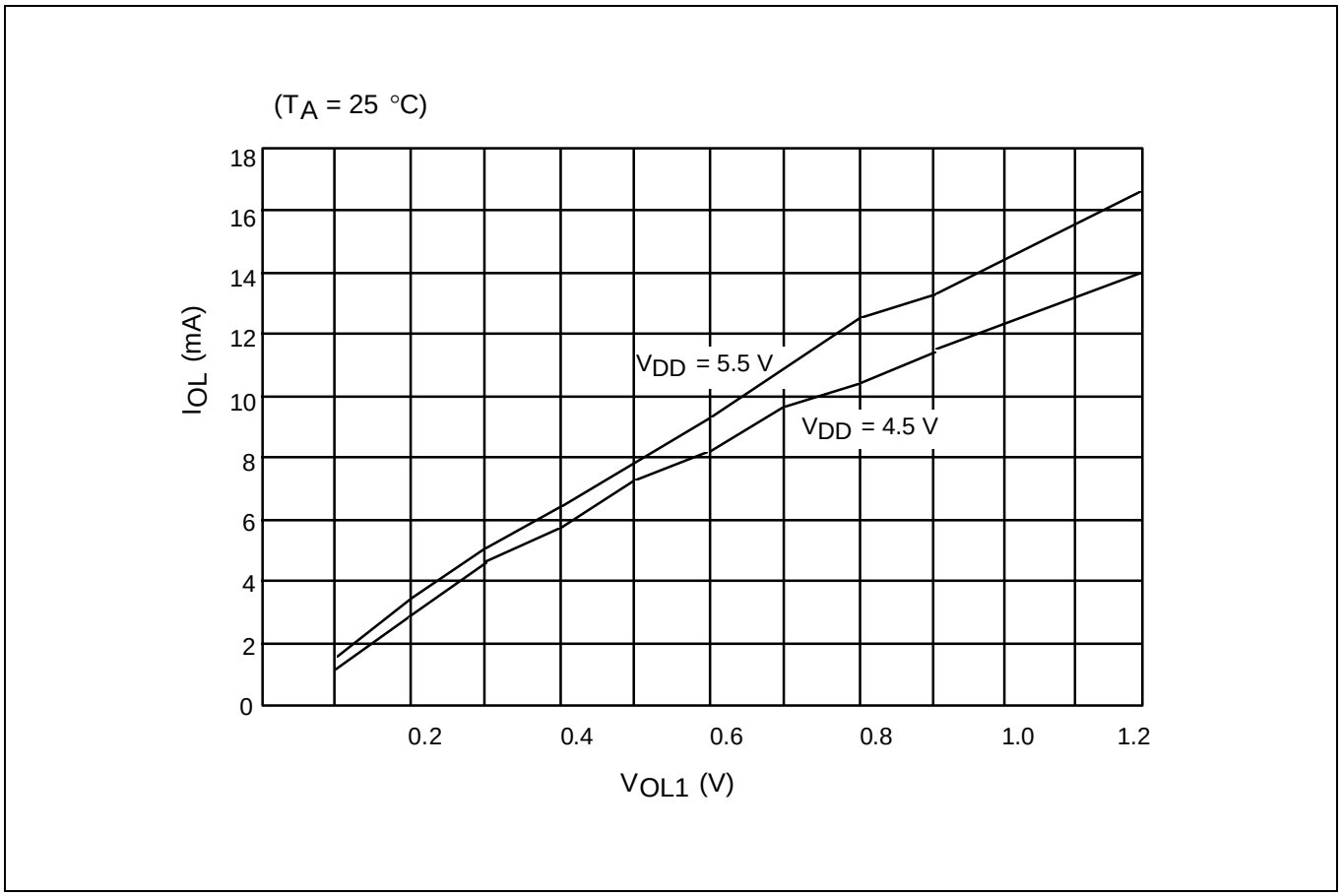


Figure 16–12. IOL vs VOL1

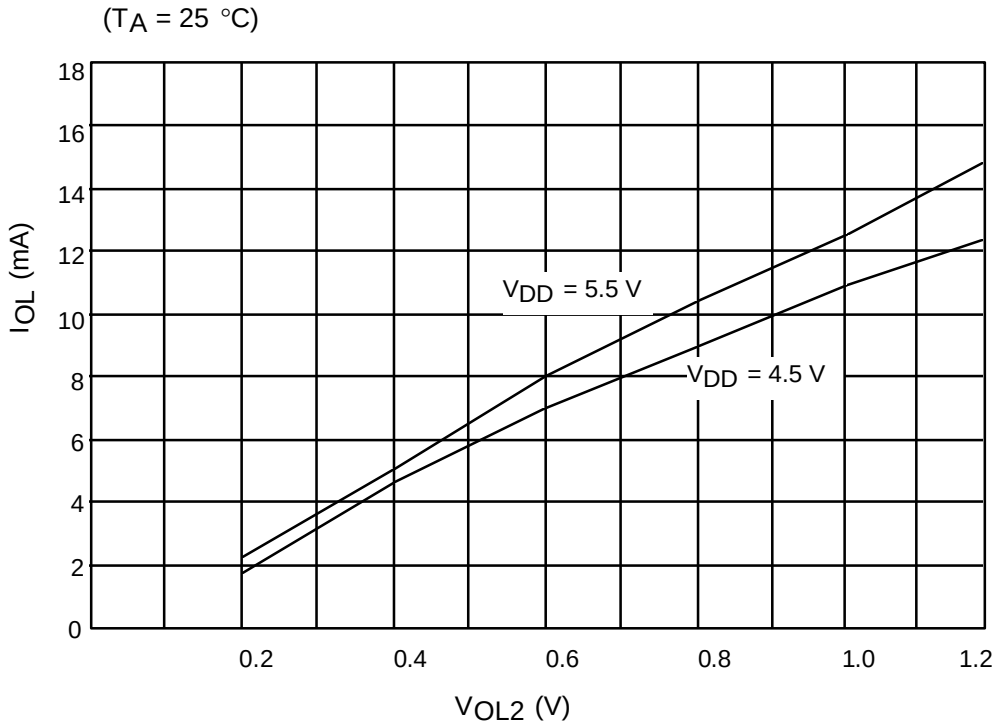


Figure 16–13. IOL vs VOL2

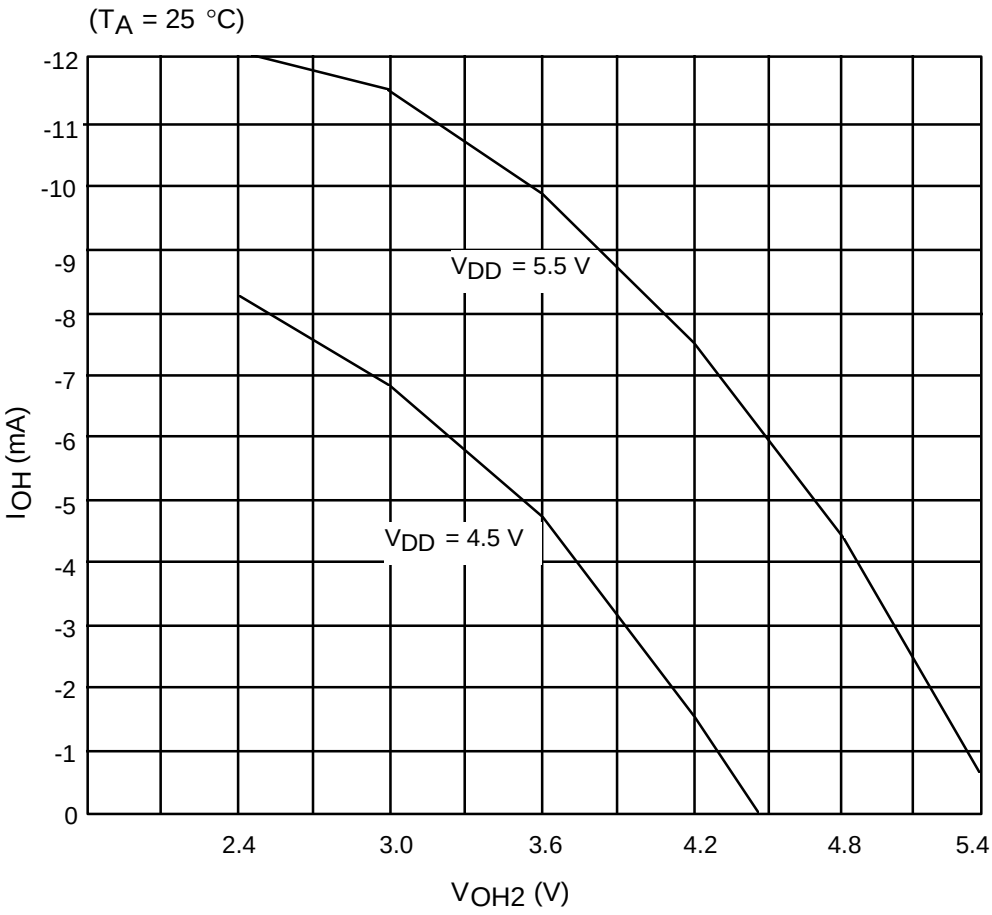
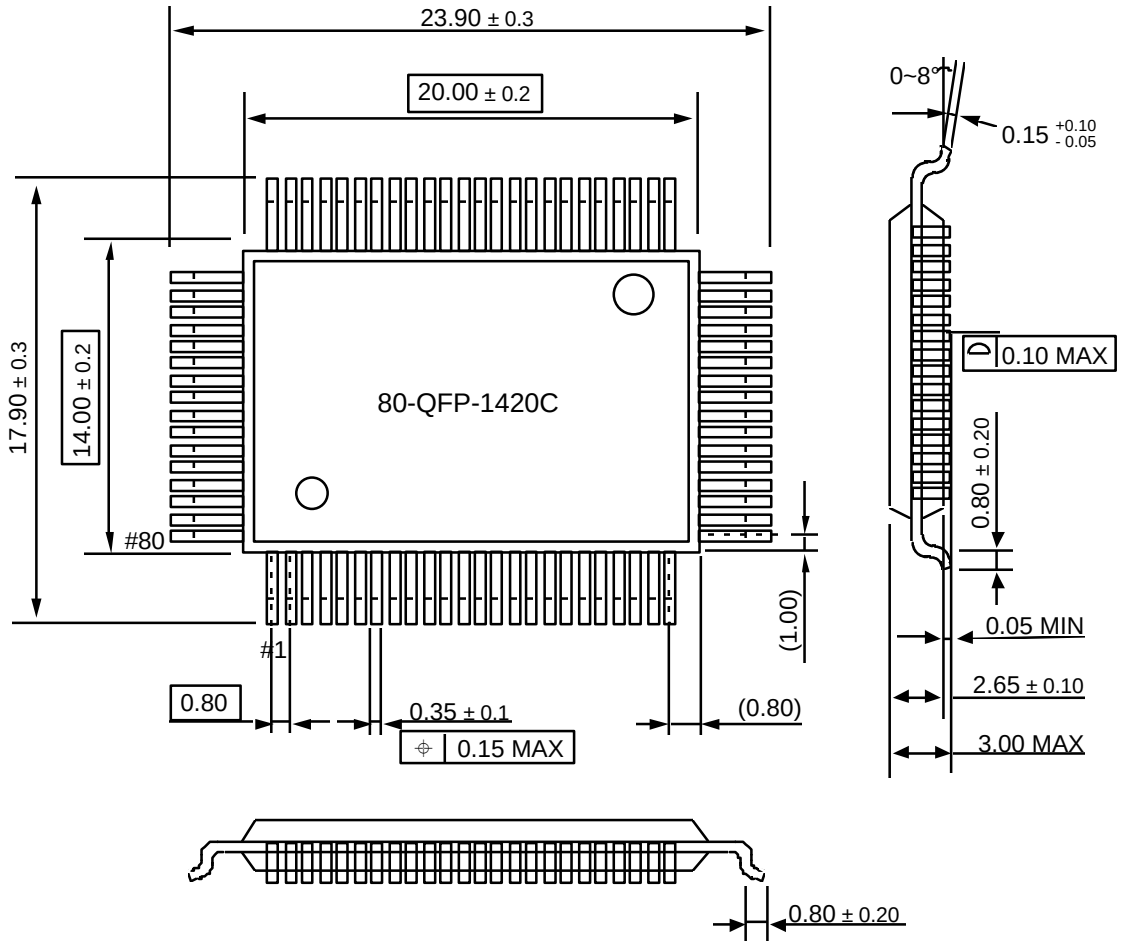


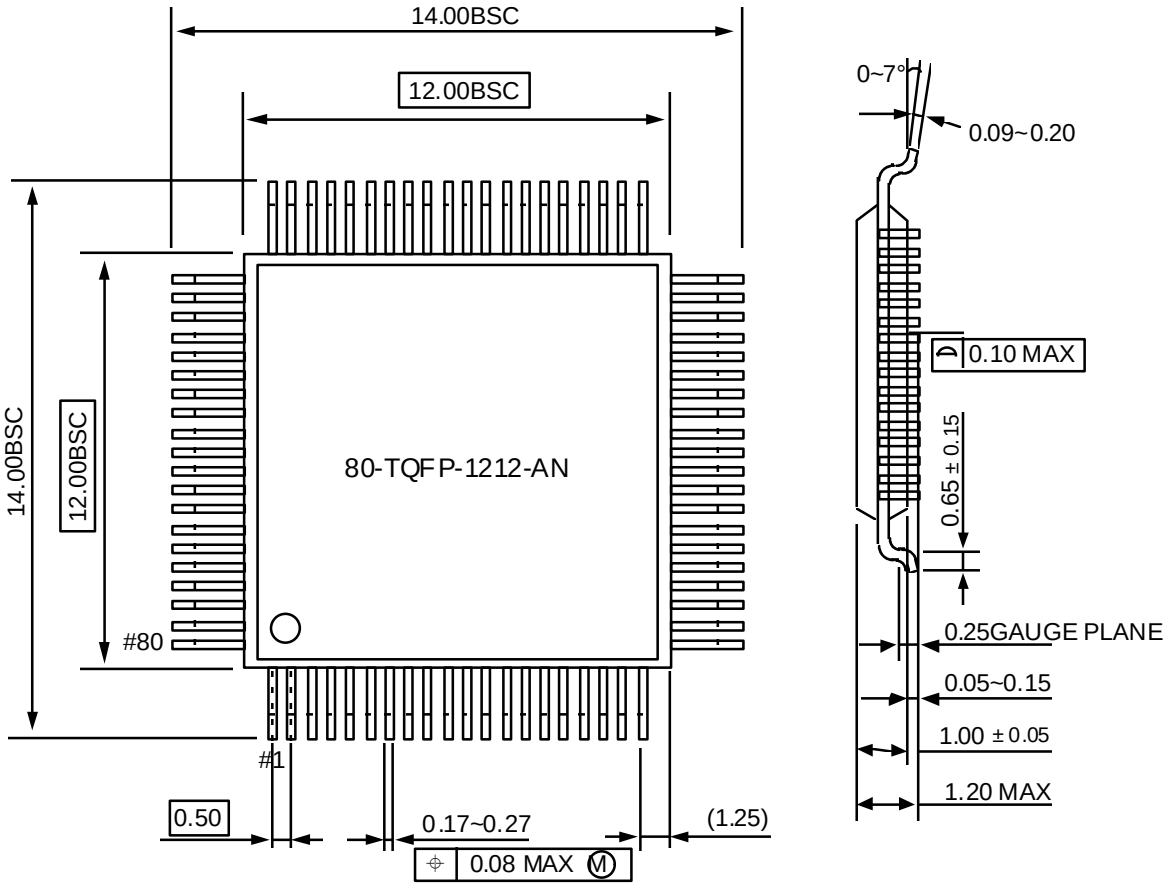
Figure 16–14. IOH vs VOH2

17 MECHANICAL DATA



NOTE: Dimensions are in millimeters.

Figure 17–1. S3C8444 QFP Standard Package Dimensions (in Millimeters)



NOTE: Dimensions are in millimeters.

Figure 17–2. S3C8444 TQFP Standard Package Dimensions (in Millimeters)

18 DEVELOPMENT TOOLS

OVERVIEW

Samsung provides a powerful and easy-to-use development support system in turnkey form. The development support system is configured with a host system, debugging tools, and support software. For the host system, any standard computer that operates with MS-DOS as its operating system can be used. Two types of debugging tools including hardware and software are provided: the in-circuit emulator, SMDS2, developed for S3C1, S3C7, S3C8 families of microcontrollers, and even more sophisticated and powerful in-circuit emulator, SMDS2+, for S3C7, S3C8 families of microcontrollers. The SMDS2+ is a new and improved version of SMDS2. In the future SMDS2+ will replace SMDS2 and eventually SMDS2 will not be supported. Samsung also offers support software that includes debugger, assembler, and a program for setting options.

DEVELOPMENT TOOLS VERSIONS

As of the date of this publication, two versions of the SMDS are being supported:

— SMDS2 Version 5.3 (S/W) and SMDS2 Version 1.3 (H/W); last release: October, 1995.

— SHINE Version 1.0 (S/W) and SMDS2+ Version 1.0 (H/W); last release: January, 1997.

SMDS V5.3

SMDS V5.3 is an assembly level debugger with user-friendly host interfacing that uses in-circuit emulator,SMDS2.

SHINE

Samsung Host Interface for iN-circuit Emulator, SHINE, is a multi-window based debugger for SMDS2+. SHINE provides pull-down and pop-up menus, mouse support, function/hot keys, and context-sensitive hyper-linked help. It has an advanced, multiple-windowed user interface that emphasizes ease of use. Each window can be sized, moved, scrolled, highlighted, added, or removed completely.

SAMA ASSEMBLER

The Samsung Arrangeable Microcontroller (SAM) Assembler, SAMA, is a universal assembler, and generates object code in standard hexadecimal format. Assembled program code includes the object code that is used for ROM data and required SMDS program control data. To assemble programs, SAMA requires a source file and an auxiliary definition (DEF) file with device specific information.

SASM88

The SASM88 is an relocatable assembler for Samsung's S3C8-series microcontrollers. The SASM88 takes a source file containing assembly language statements and translates into a corresponding source code, object code and comments. The SASM88 supports macros and conditional assembly. It runs on the MS-DOS operating system. It produces the relocatable object code only, so the user should link object file. Object files can be linked with other object files and loaded into memory.

HEX2ROM

HEX2ROM file generates ROM code from HEX file which has been produced by assembler. ROM code must be needed to fabricate a microcontroller which has a mask ROM. When generating the ROM code (.OBJ file) by HEX2ROM, the value 'FF' is filled into the unused ROM area upto the maximum ROM size of the target device automatically.

TARGET BOARDS

Target boards are available for all S3C8-series microcontrollers. All required target system cables and adapters are included with the device-specific target board.

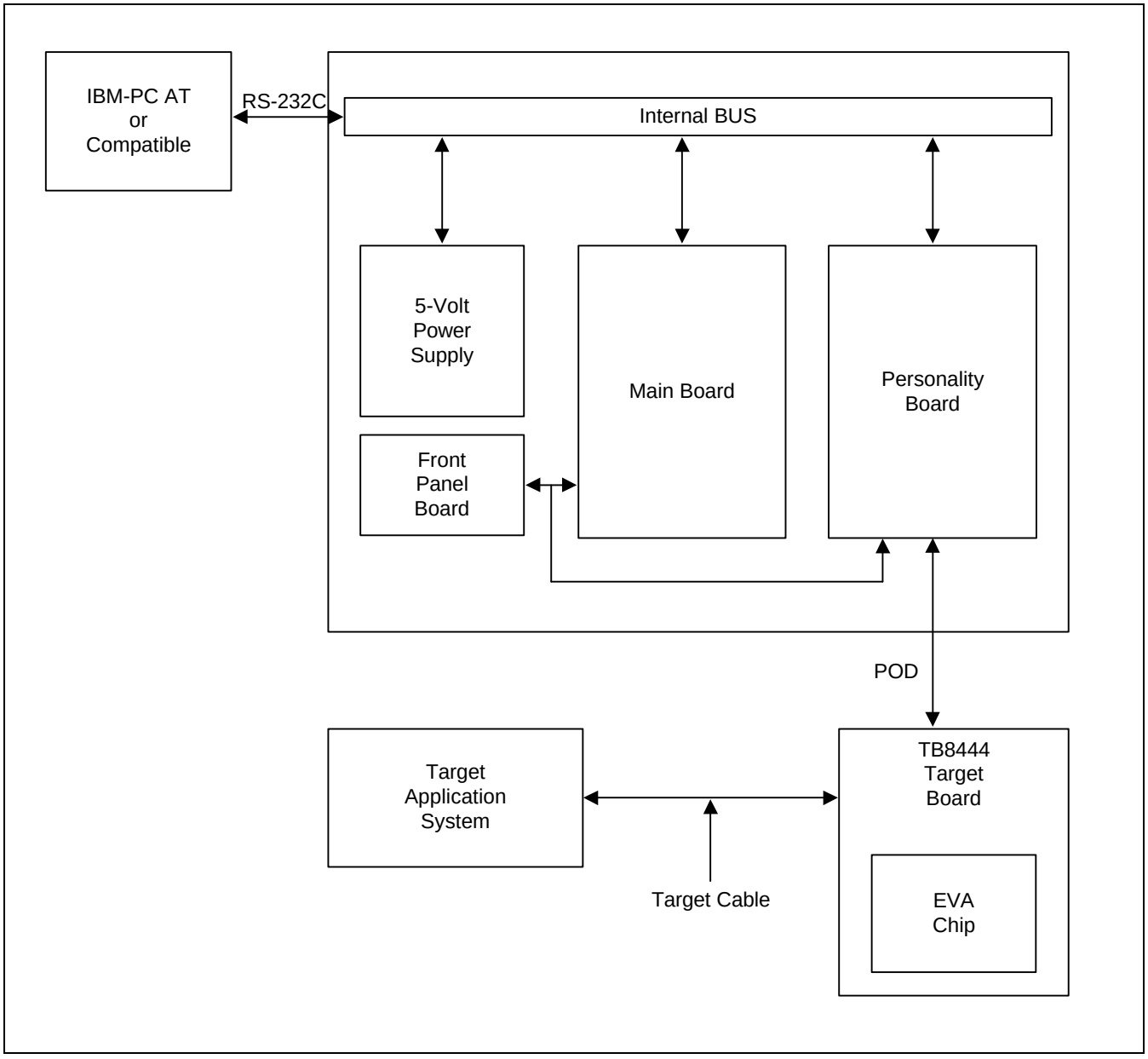


Figure 18–1. SMDS Product Configuration (SMDS2)

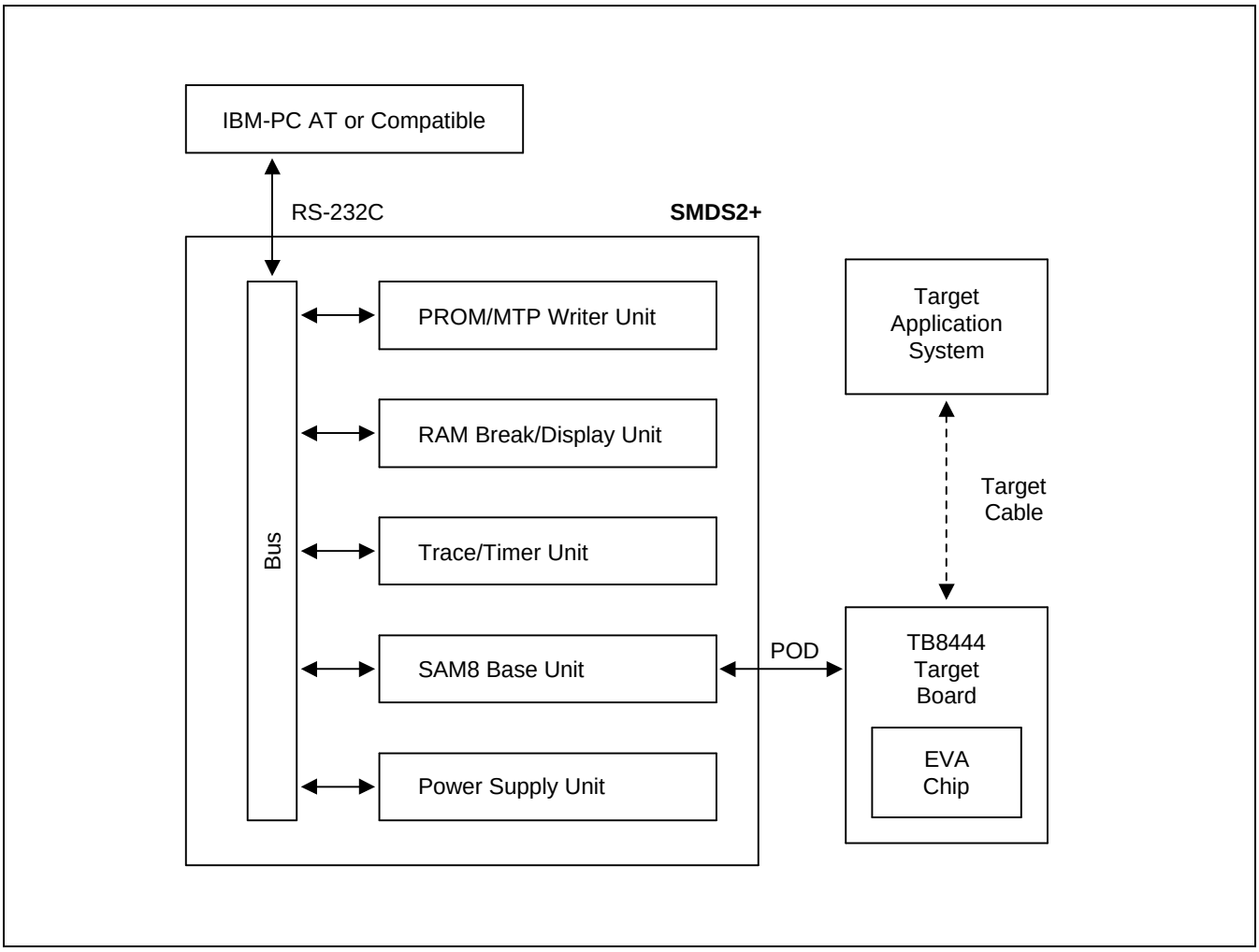


Figure 18–2. SMDS Product Configuration (SMDS2+)

TB8444 TARGET BOARD

The TB8444 target board is used for the S3C8444 microcontroller. It is supported by the SMDS2 or SMDS2+ development system.

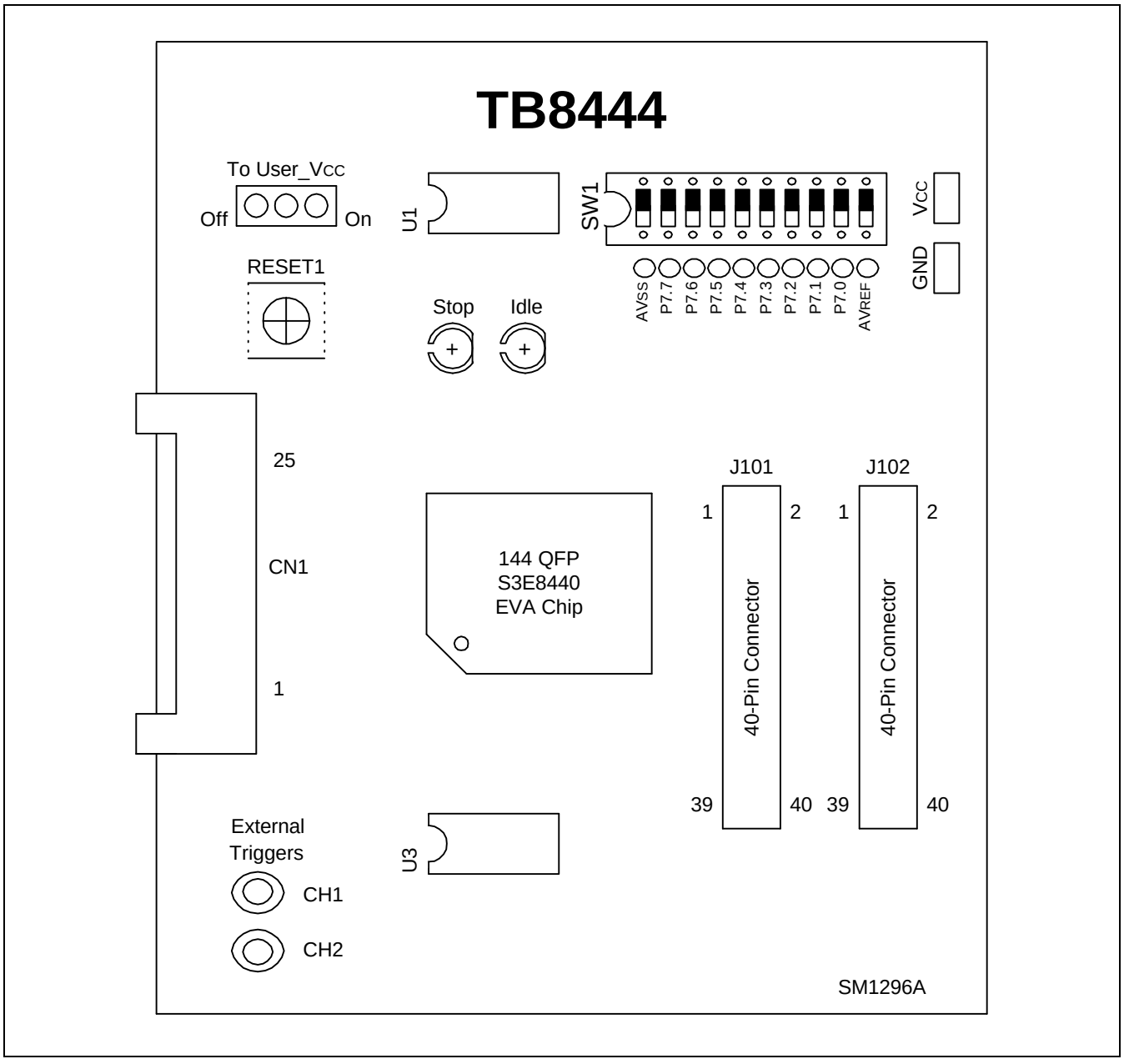
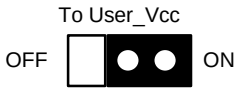
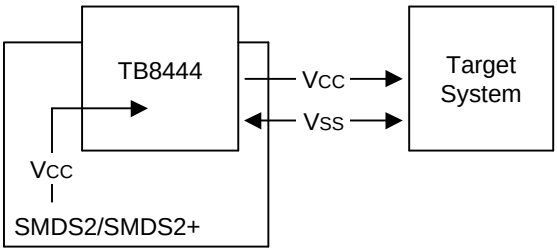
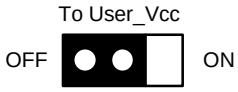
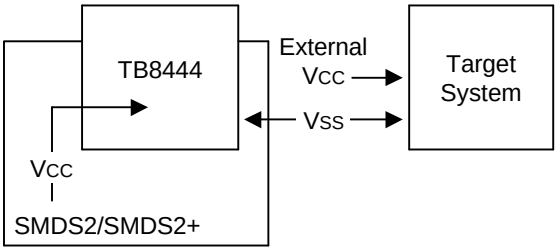


Figure 18–3. TB8444Target Board Configuration

Table 18–1. Power Selection Settings for TB8444

'To User_Vcc' Settings	Operating Mode	Comments
		The SMDS2/SMDS2+ main board supplies V_{CC} to the target board (evaluation chip) and the target system.
		The SMDS2/SMDS2+ main board supplies V_{CC} only to the target board (evaluation chip). The target system must have its own power supply.

NOTE: The following symbol in the 'To User_Vcc' Setting column indicates the electrical short configuration:



Table 18–2. Using Single Header Pins as the Input Path for External Trigger Sources

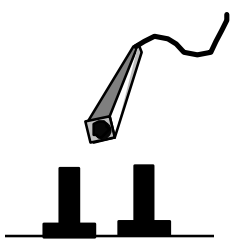
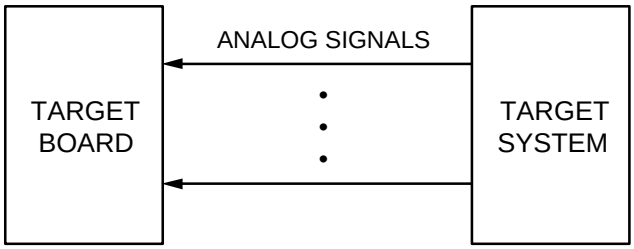
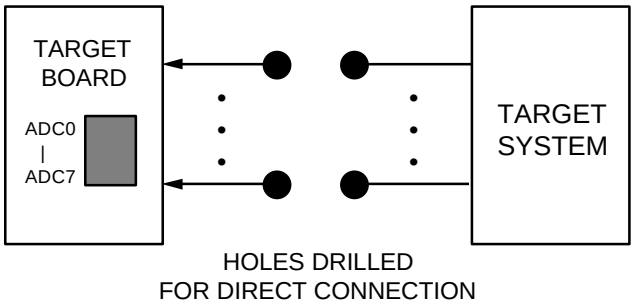
Target Board Part	Comments
EXTERNAL TRIGGERS CH1 CH2	 Connector from external trigger sources of the application system You can connect an external trigger source to one of the two external trigger channels (CH1 or CH2) for the SMDS2/SMDS2+ breakpoint and trace functions.

Table 18–3. Analog Pin Connection Switch Settings (TB8444)

Analog Pin Switch	Operating Mode
DIP SW1: ON 	
DIP SW1: OFF 	

NOTE: Analog signals coming into the target board can easily introduce noise into the analog converter circuit. This can cause invalid conversion results. To reduce noise, you can use the analog pin switches to provide the shortest possible path for analog signals. To do this, turn all DIP switches to the OFF position. Then, connect the analog signal lines directly via the holes of the corresponding analog pins.

IDLE LED

The Green LED is ON when the evaluation chip(S3E8440) is in idle mode.

STOP LED

The Red LED is ON when the evaluation chip(S3E8440) is in stop mode.

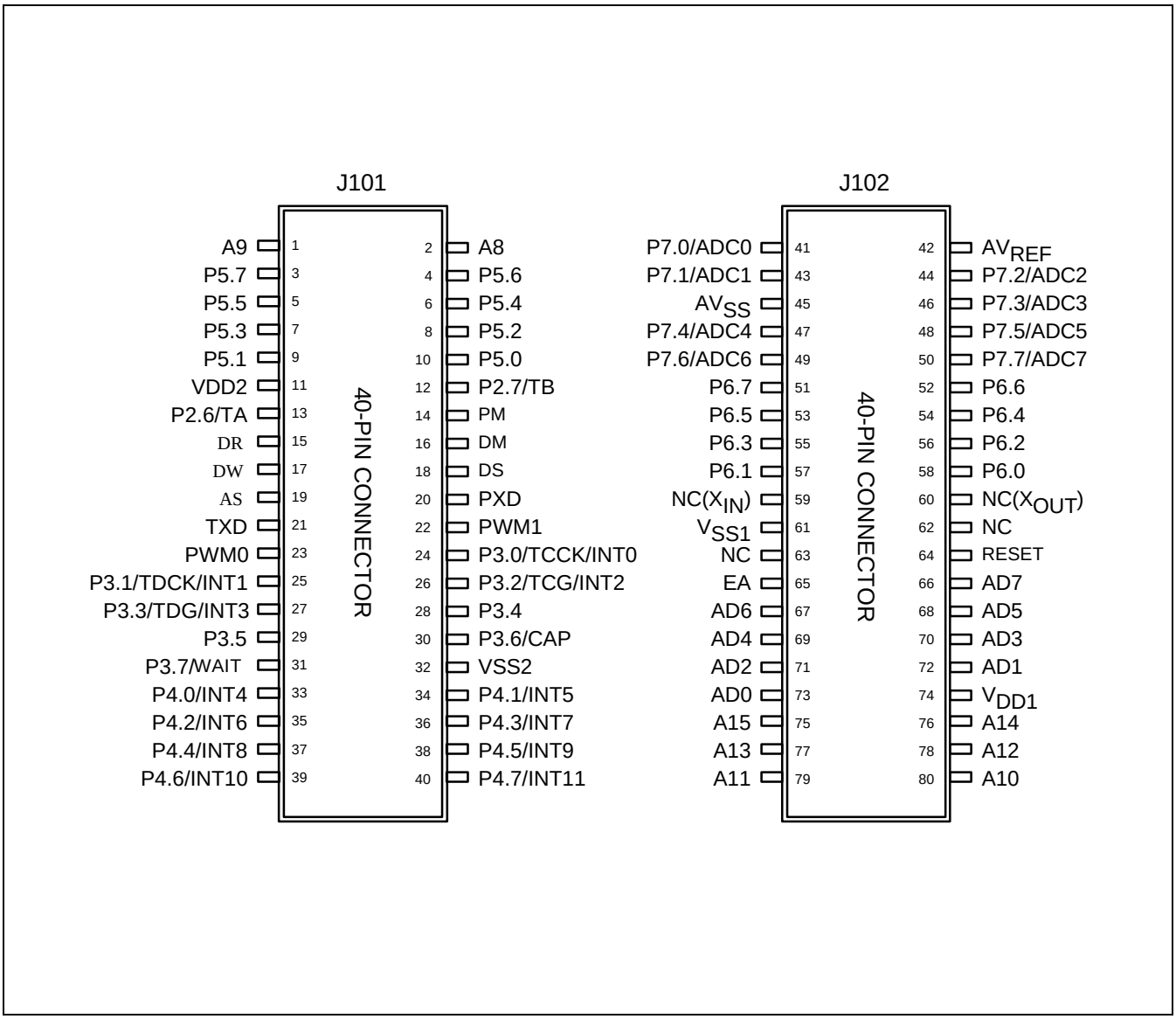
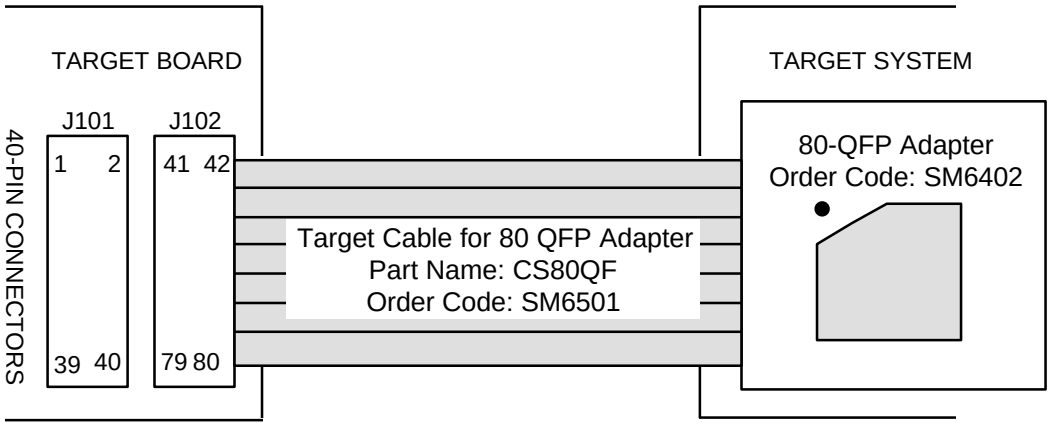


Figure 18–4. 40-Pin Connectors for TB8444 (S3C8444, 80-QFP Package)



NOTE: Two 40-pin flat cables can be used instead of the target cable and the 80-QFP adapter to connect the target board and the target system.

Figure 18–5. TB8444 Cable for 80-QFP Adapter