POWER MANAGEMENT

Description

The SC2616 is a fully integrated DDR power solution providing power for the VDDQ and the VTT rails. The SC2616 also completely adheres to the ACPI sleep state power requirements. A synchronous buck controller provides the high current of the VDDQ at high efficiency, while a linear sink/source regulator provides the termination voltage with 2 Amp Source/Sink capability. This approach makes the best trade-off between cost and performance. Additional logic and UVLOs complete the functionality of this single chip DDR power solution in compliance with SLP_S3 and SLP_S5 motherboard signals.

The SC2616 is capable of sourcing up to 20A at the switcher output, and 2A source/sink at the VTT output. The MLP package provides excellent thermal impedance while keeping small footprint. VDDQ current limit as well as 3 independent thermal shutdown circuits assure safe operation under all fault conditions.

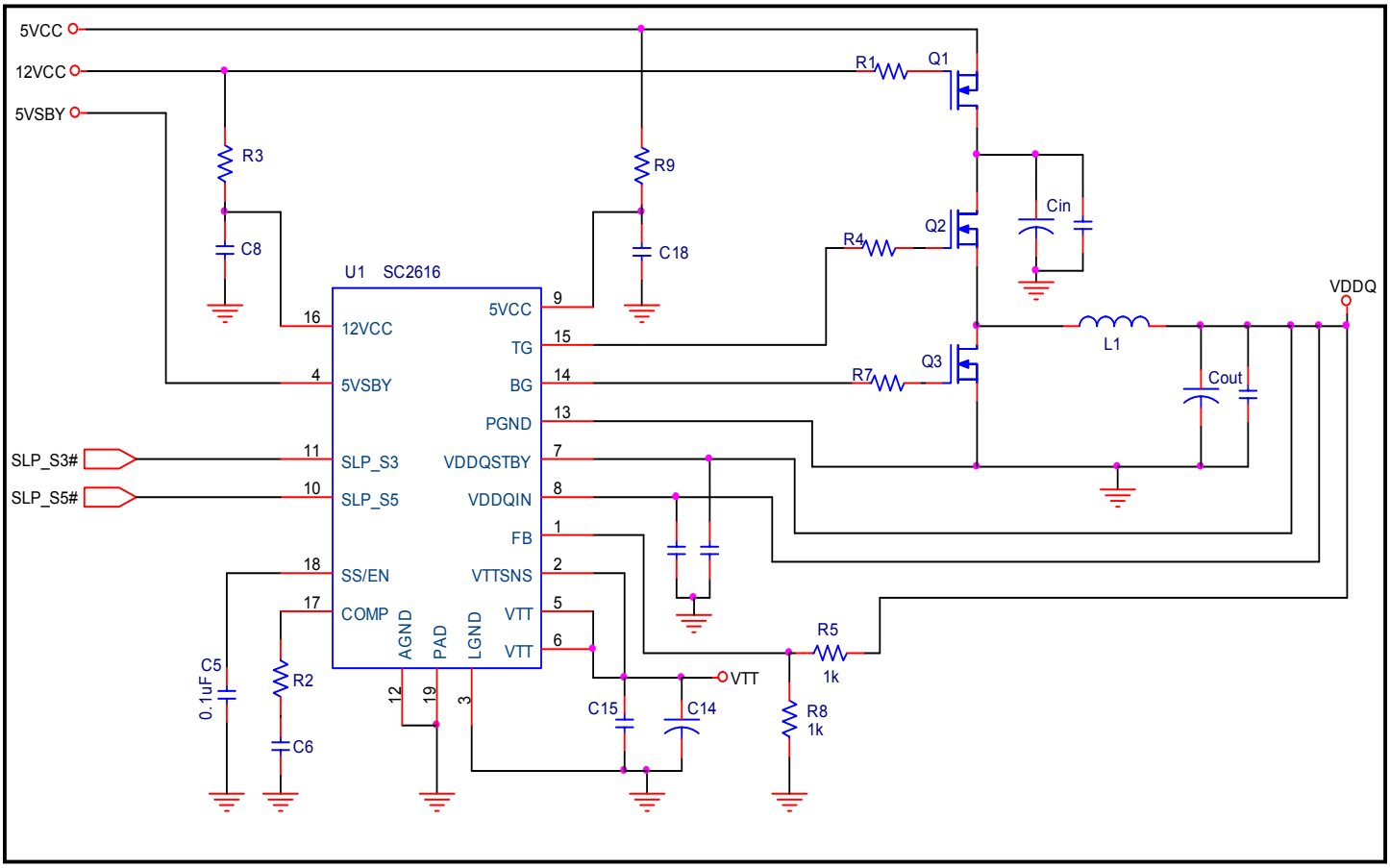
Features

- High efficiency (90%) switcher for VDDQ supplies 20 Amps
- High current gate drives
- Single chip solution complies fully with ACPI power sequencing specifications
- Internal S3 state LDO supplies high standby VDDQ current (0.65 Amp Min.)
- ACPI sleep state controlled
- 2 Amp VTT source/sink capability
- UVLO on 5V and 12V
- Indepent thermal shutdown for VDDQSTBY and VTT
- Fast transient response
- 18 pin MLP package

Applications

- Power solution for DDR memory per ACPI motherboard specification
- High speed data line termination
- Memory cards

Typical Application Circuit



Absolute Maximum Ratings

Exceeding the specifications below may result in permanent damage to the device, or device malfunction. Operation outside of the parameters specified in the Electrical Characteristics section is not implied.

Parameter	Symbol	Maximum	Units
Supply Voltage, 5VCC to AGND	V_{5VCC}	7	V
Supply Voltage, 12VCC to AGND	V_{12VCC}	15	V
Standby Input Voltage	V_{5VSBY}	7	V
Inputs	I/O	5VSTBY +0.3, AGND -0.3	V
AGND to PGND or LGND		0.3	V
VTT Output Current	$I_{O(VTT)}$	±3	A
Operating Ambient Temperature Range	T_A	0 to 70	°C
Operating Junction Temperature	T_J	125	°C
Thermal Resistance Junction to Ambient	θ_{JA}	25	°C/W
Thermal Resistance Junction to Case	θ_{JC}	4	°C/W
Storage Temperature	T_{STG}	-65 to 150	°C
TG/BG DC Voltage		12Vcc + 0.3, AGND -0.5	V
TG/BG AC Voltage, t $\leq$ 100ns		12Vcc + 1.0, AGND -2.0	V
ESD Rating (Human Body Model)	ESD	2	kV

Electrical Characteristics

Unless specified: T_A = 25°C, 12VCC = 12V, 5VCC = 5V, 5VSBY = 5V.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
5V Supply Voltage	V_{5VCC}		4.5	5	5.5	V
12V Supply Voltage	V_{12VCC}		10	12	14	V
5V Standby Voltage	V_{5VSBY}		4.5	5	5.5	V
Quiescent Current	$I_{Q(5VSBY)}$	S0, S5		5.2		mA
		S3, IDDQSTBY = 0		7.8		mA
SLP_S3 Threshold				TTL		V
SLP_S5 Threshold				TTL		V
SLP_S3/SLP_S5 Input Current	$I_{S3,S5}$			50		µA

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Electrical Characteristics (Cont.)

Unless specified: T_A = 25°C, 12VCC = 12V, 5VCC = 5V, 5VSBY = 5V.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
12VCC Under Voltage Lockout	$UVLO_{12VCC}$		8	9.2	10	V
5VCC Under Voltage Lockout	$UVLO_{5VCC}$			2.5		V
Feedback Reference	V_{REF}			1.25		V
Feedback Current	I_{FB}	V_{FB} = 1.25V			0.5	µA
SS/EN Shutdown Threshold	$V_{EN(TH)}$			0.3		V
Thermal Shutdown	T_{J-SHDN}			150		°C
Thermal Shutdown Hysteresis	T_{J-HYST}			10		°C

Switcher						
Load Regulation		I_{VDDQ} = 0A to 10A; S0		0.2		%
Oscillator Frequency	f_{OSC}		225	250	275	KHz
Soft Start Current	I_{SS}			25		µA
Duty Cycle			0		95	%
Overcurrent Trip Voltage	V_{TRIP}	% of VDDQ Setpoint	70	75	80	%
Top Gate Rise Time	TG_R	Gate capacitance = 4000pF		25		nS
Top Gate Fall Time	TG_F	Gate capacitance = 4000pF		25		nS
Bottom Gate Rise Time	BG_R	Gate capacitance = 4000pF		35		nS
Bottom Gate Fall Time	BG_F	Gate capacitance = 4000pF		35		nS
Dead Time	t_d		20	50		nS
Error Amplifier Transconductance	G_M			0.8		mS
Error Amplifier Gain @ DC	A_{EA}	R_{COMP} = open		38		dB
Error Amplifier Bandwidth	G_{BW}			5		MHz
Error Amplifier Source/Sink Current				±60		µA

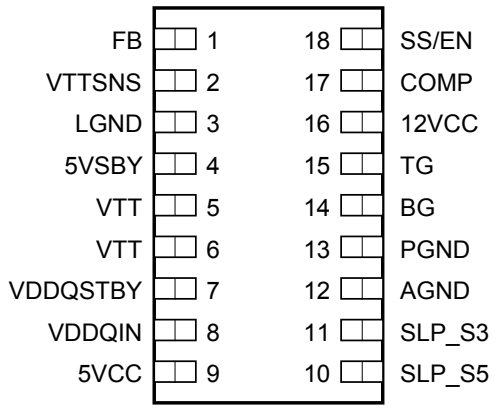
Electrical Characteristics (Cont.)

Unless specified: T_A = 25°C, 12VCC = 12V, 5VCC = 5V, 5VSBY = 5V.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Switcher (Cont.)						
PWM Ramp	V_{RAMP}	Peak to Peak		0.55		V
STBY LDO						
Output Current	$I_{VDDQSTBY}$	DC current	650	750	850	mA
Load Regulation	$\Delta V/\Delta I$	I_{VDDQ} = 0A to 460mA; S3		0.3	0.5	%
Current Limit	I_{LIM}	SLP_S3 = 0		2.3		A
VTT LDO						
Output Voltage	VTT	$V_{VDDQSTBY}$ = 2.500V	1.237	1.250	1.267	V
		I_{VTT} = 1.8A to -1.8A	1.225	1.250	1.275	
Source and Sink Currents	I_{VTT}		±1.8		±2	A
Load Regulation	$\Delta VTT/\Delta I$	I_{VTT} =+1.8A to -1.8A		±0.5	±1.0	%
Error Amplifier Gain	A_{EA_VTT}			75		dB
Current Limit	VTT_{ILIM}	SLP_S3 = high (sink)		3		A
		SLP_S3 = high (source)		3		

Pin Configuration

TOP VIEW



(18 Pin MLP)

Note: Pin 19 is the thermal Pad on the bottom of the device

Ordering Information

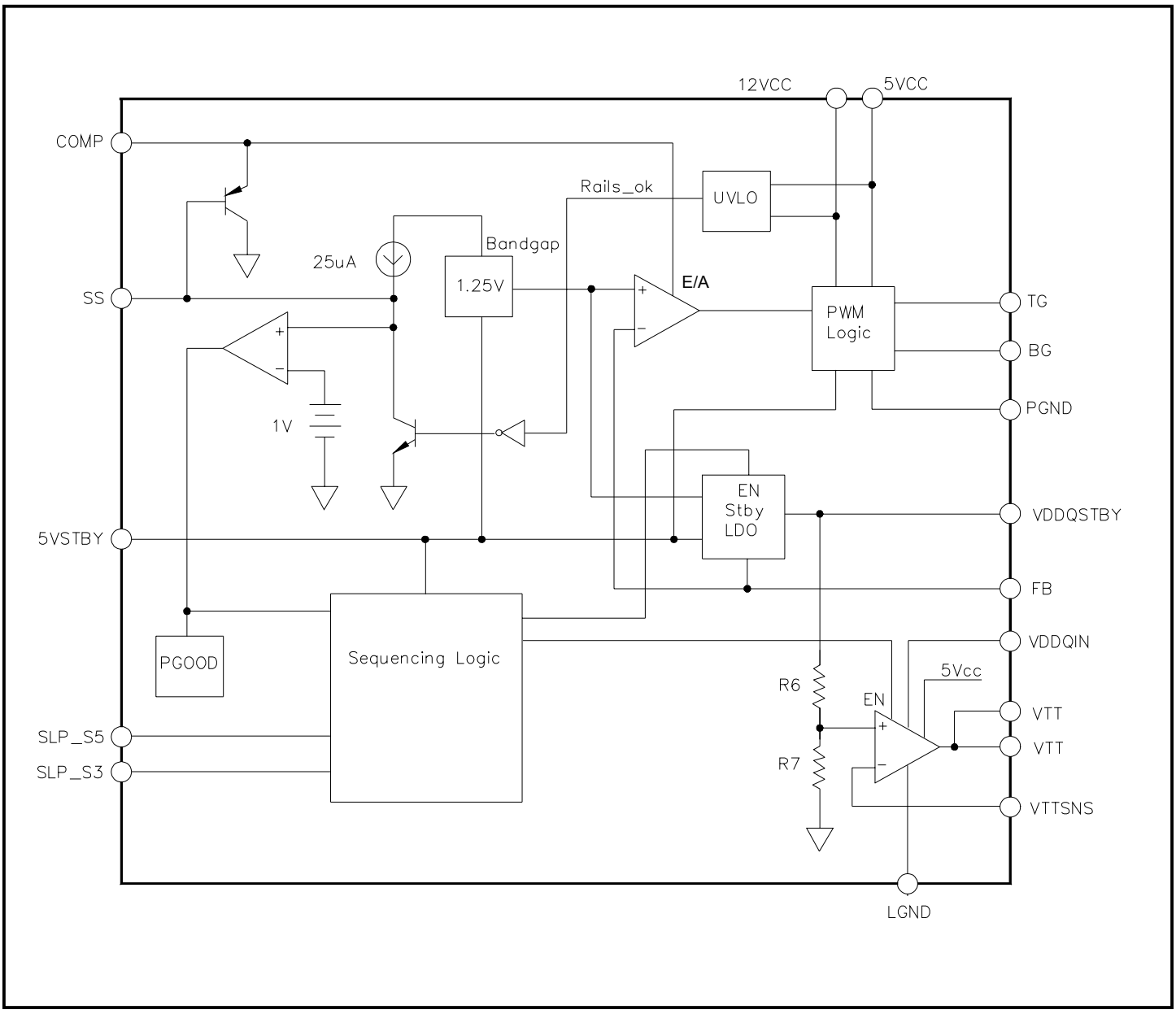
Part Numbers	Package
SC2616MLTR(1)	MLP-18

Note:
(1) Only available in tape and reel packaging. A reel contains 3000 devices.

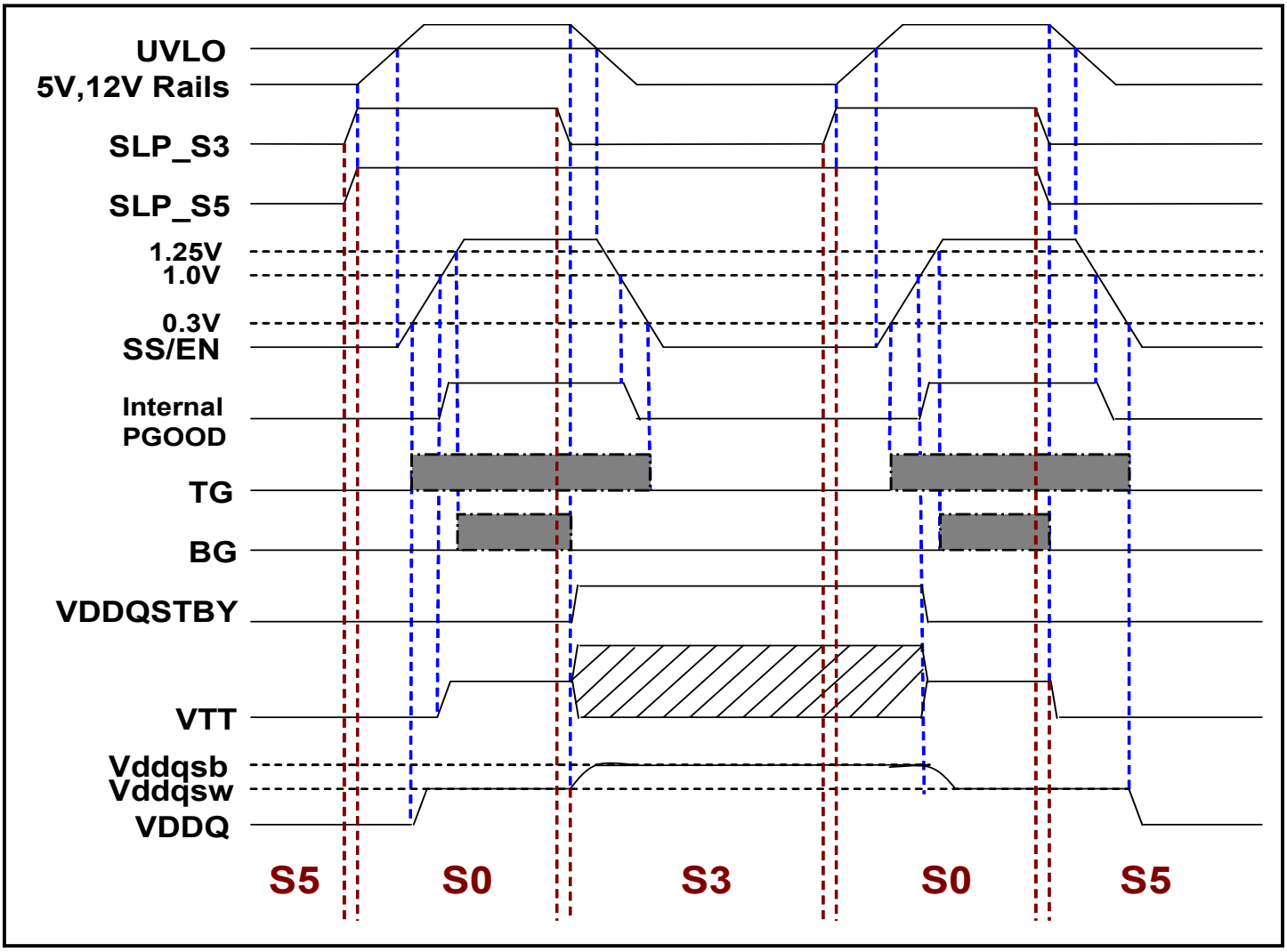
Pin Descriptions

Pin #	Pin Name	Pin Function
1	FB	Feedback for the STBY LDO and the switcher for VDDQ.
2	VTTSNS	VTT LDO feedback and remote sense input.
3	LGND	VTT return. Connect to point of load return. The trace connecting to this pin must be able to carry 2A of current.
4	5VSBY	Bias supply for the chip. Connect to 5V standby.
5, 6	VTT	VTT output. Connect to point of load. The trace connecting to this pin must be able to carry 2A of current
7	VDDQSTBY	S3 VDDQ output. Provision must be made to prevent the VDDQSTBY supply from back feeding the input supply (see typical application schematic). Traces connecting to this pin must be capable of carring 0.85A of current.
8	VDDQIN	VDDQ power input to VTT LDO. The trace connecting to this pin must be able to carry 2 A of current.
9	5VCC	Supply to the Internal logic
10	SLP_S5	Connect to SLP_S5 signal from motherboard.
11	SLP_S3	Connect to SLP_S3 signal from motherboard.
12	AGND	Analog ground.
13	PGND	Gate drive return. Keep this pin close to bottom FET source.
14	BG	Bottom gate drive.
15	TG	Top gate drive.
16	12VCC	Supply to the upper and lower gate drives.
17	COMP	Compensation pin for the PWM transconductance amplifier.
18	SS/EN	Soft start capacitor to AGND. Pull low to less than 0.3V to disable the controller.
19	TH_PAD	Copper pad on bottom of chip used for heatsinking. This pin must be connected to ground plane under IC. (See application information).

Block Diagram



Timing Diagram



Applications Information

Description

The Semtech SC2616 DDR power supply controller offers a switching and linear regulator combination to provide the necessary functions to comply with S3 and S5 sleep state signals generated by the Desktop Computer Motherboards. VDDQ supply, and VTT termination voltage are supplied to the Memory bus during S0 (normal operation) state. During S0, VDDQ is supplied via the Switching regulator, sourcing high output currents to the VDDQ bus as well as supplying the termination supply current. The SC2616 is capable of driving a 4000pf capacitor in 25ns (typical, top gate). This drive capability allows 15-20A DC load on the VDDQ supply. The VTT termination voltage is an internal sink/source linear regulator, which during S0 state receives its power from the VDDQ bus. It is capable of sourcing and sinking 2 Amps (max). The current limit on this pin is set to 3 Amps (typical).

Output Current and PCB layout

The current handling capacity of SC2616 depends upon the amount of heat the PC board can sink from the SC2616 thermal pad. (See thermal considerations). The PC board layout must take into consideration the high current paths, and ground returns for both the VDDQ and VTT supply pins. VTT, LGND, VDDQ, 5VCC and PGND traces must also be routed using wide traces to minimize power loss and heat in these traces, based on the current handling requirements.

S3 and S5 States

During S3 and S5 sleep states, the operation of the VDDQ and VTT supplies is governed by the internal sequencing logic in strict adherence with motherboard specifications. The timing diagram demonstrates the state of the controller, and each of the VDDQ and VTT supplies during S3 and S5 transitions. When SLP_S3 is low, the VDDQ supplies the “Suspend To RAM” current of 650 mA (min) to maintain the information in memory while in standby mode. The VTT termination voltage is not needed during this state, and is thus tri-stated during S3. Once SLP_S3 goes high, the VDDQ switcher recovers and takes control of the VDDQ supply voltage. When SLP_S5 and SLP_S3 are both pulled low, all supplies shut down. The SS/EN pin must be pulled low (<0.3V) and high again to restart the SC2616. This can be achieved by cycling the input supplies(5V and 12V), since both supplies have to be higher than their UVLO thresholds for proper start-up.

Initial Conditions and Event Sequencing

The main switcher will start-up in Asynchronous Mode when the voltage on SS/EN pin is greater than ~0.3V. The SS/EN will go high only after the 5Vcc and 12Vcc are higher than their respective UVLO thresholds. The switcher achieves maximum duty cycle when SS/EN reaches 0.8V. When the SS/EN equals 1.25V, the synchronous FET will also be activated.

When the SLP_S5 and SLP_S3 go high for the first time, the VDDQ is supplied by the switcher, thus removing the burden of charging the output capacitors via the linear regulator. An internal latch guarantees that the supply goes through S0 state for the first time.

During a transition from S3 to S0, where the 5V and 12V rails and subsequently the SS/EN pin go high, the internal VDDQ standby supply will remain ”on” until SS/EN has reached 1V, at which point only the switcher is supplying VDDQ , and the internal “power good” indicator goes high.

The “Memory” activity should be slaved off the “Power OK” signal from the Silver Box supply, and since the “Power OK” is asserted after all supplies are within close tolerance of their final values, the VDDQ switcher should have been running for some time before the memory is activated. This is true for typical SS/EN capacitor values (10nf to 220nf). Thus during transitions from S3 to S0, the concern that the VDDQ Standby supply may have to provide high currents before the switcher is activated is alleviated.

The logic inputs to SLP_S3 and SLP_S5 pins must be defined before application of power to the SC2616. This can be guaranteed by pulling up the SLP_S3 and SLP_S5 inputs to 5VStandby. If the chipset that asserts these signals is powered after the SC2616 powers up, and SLP_S3 and SLP_S5 are not pulled up, erroneous startup and operation can result.

Care must be taken not to exceed the maximum voltage/ current specifications of the interface inputs supplying these signals. The pullup voltage and resistor must be chosen such that when high, the S3 and S5 do not “back drive” the interface chipset (Southbridge, etc.) and the

Applications Information (Cont.)

maximum voltage applied to these pins do not exceed the chipsets specifications. A separate lower pullup supply may be necessary to avoid damage to the chipset.

"Back Feeding" the Input Supply

When in S3 state, VDDQ is supplied by the linear regulator and current can flow back from the VDDQ supply through the body diode of the Top switching MOSFET to the 5V supply of the Silver Box, which is off during the S3 state. This in turn shorts out the VDDQ supply and is not acceptable.

An addittional MOSFET should be addded to avoid the reverse current flow. The MOSFETs should have the drains *to each other(common- Drain)*.

During S0 to S3 transition, As soon as SLP_S3 signal goes low, BG signal stops chopping. This can prevent the inductor to build up its current in the reverse direction.

To avoid the MOSFET damaged by overshoot, the input bulk capacitor must be added to the node of common - Drain.

Current Limit

Current limit is implemented by sensing the VDDQ voltage. If it falls to 75% off its nominal voltage, as sensed by the FB pin, the TG and BG pins are latched off and the switcher and the linear converters are shut down. To recover from the current limit condition, either the power rails, 5VCC or 12VCC have to be recycled, or the SS/EN pin must be pulled low and released to restart switcher operation.

Thermal Shutdown

There are three independent Thermal Shutdown protection circuits in the SC2616: the VDDQ linear regulator, the VTT source regulator, and the VTT sink regulator. If any of the three regulators' temperature rises above the threshold, that regulator will turn off independently, until the temperature falls below the thermal shutdown limit.

OUTPUT INDUCTOR - A good starting point for output filter component selection is to choose an inductor value that will give an inductor ripple current of approximately 20% of max. output current.
Inductor ripple current is given by:-

$$I_{LRIPPLE} = \frac{V_O \cdot \left(1 - \frac{V_O}{V_{IN}}\right)}{L \cdot f_{OSC}}$$

So choose inductor value from:-

$$L = \frac{5 \cdot V_O \cdot \left(1 - \frac{V_O}{V_{IN}}\right)}{I_O \cdot f_{OSC}}$$

OUTPUT CAPACITOR(S) - The output capacitors should be selected to meet output ripple and transient response criteria. Output ripple voltage is caused by the inductor ripple current flowing in the output capacitor's ESR (There is also a component due to the inductor ripple current charging and discharging the output capacitor itself, but this component is usually small and can often be ignored). Given a maximum output voltage ripple requirement, ESR is given by:-

$$R_{ESR} < \frac{L \cdot f_{OSC} \cdot V_{RIPPLE}}{V_O \cdot \left(1 - \frac{V_O}{V_{IN}}\right)}$$

Output voltage transient excursions are a function of load current transient levels, input and output voltages and inductor and capacitor values.

Capacitance and R_{ESR} values to meet a required transient condition can be calculated from

$$R_{ESR} < \frac{V_T}{I_T}$$

$$C > \frac{L \cdot I_T^2}{2 \cdot V_T \cdot V_A}$$

where

$V_A = V_{IN} - V_O$ for negative transients (load application)

and

$V_A = V_O$ for positive transients (load release)

values for positive and negative transients must be calculated seperately and the worst case value chosen. For Capacitor values, the calculated value should be doubled to allow for duty cycle limitation and voltage drop issues.

Applications Information (Cont.)

Compensation Components

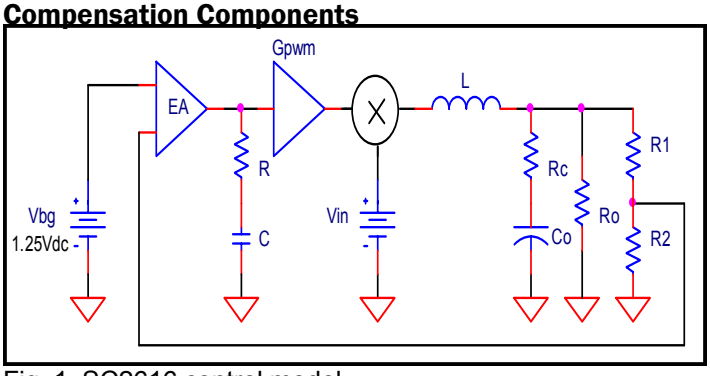


Fig. 1. SC2616 control model.

The control model of SC2616 can be depicted in Fig. 1. This model can also be used in Spice kind of simulator to generate loop gain Bode plots. The bandgap reference is 1.25 V and trimmed to +/-1% accuracy. The desired output voltage can be achieved by setting the resistive divider network, R1 and R2.

The error amplifier is transconductance type with fixed gain of:

$$G_m := \frac{0.0008\,A}{V}$$

The compensation network includes a resistor and a capacitor in series, which terminates from the output of the error amplifier to the ground.

This device uses voltage mode control with input voltage feed forward. The peak-to-peak ramp voltage is proportional to the input voltage, which results in an excellent performance to reject input voltage variation. The PWM gain is inversion of the ramp amplitude, and this gain is given by:

$$G_{pwm} := \frac{1}{V_{ramp}}$$

where the ramp amplitude (peak-to-peak) is 0.55 volts when input voltage is 5 volts.

The total control loop-gain can then be derived as follows:

$$T(s) = T_o \cdot \left(\frac{1 + s \cdot R \cdot C}{s \cdot R \cdot C}\right) \cdot \frac{1 + s \cdot R_c \cdot C_o}{1 + s \cdot \left(R_c \cdot C_o + \frac{L}{R_o}\right) + s^2 \cdot L \cdot C_o \cdot \left(1 + \frac{R_c}{R_o}\right)}$$

where

$$T_o := G_m \cdot G_{pwm} \cdot V_{in} \cdot R \cdot \left(\frac{V_{bg}}{V_o}\right)$$

The task here is to properly choose the compensation network for a nicely shaped loop-gain Bode plot. The following design procedures are recommended to accomplish the goal:

(1) Calculate the corner frequency of the output filter:

$$F_o := \frac{1}{2 \cdot \pi \cdot \sqrt{L \cdot C_o}}$$

(2) Calculate the ESR zero frequency of the output filter capacitor:

$$F_{esr} := \frac{1}{2 \cdot \pi \cdot R_c \cdot C_o}$$

(3) Check that the ESR zero frequency is not too high.

$$F_{esr} < \frac{F_{sw}}{5}$$

If this condition is not met, the compensation structure may not provide loop stability. The solution is to add some electrolytic capacitors to the output capacitor bank to correct the output filter corner frequency and the ESR zero frequency. In some cases, the filter inductance may also need to be adjusted to shift the filter corner frequency. It is not recommended to use only high frequency multi-layer ceramic capacitors for output filter.

(4) Choose the loop gain cross over frequency (0 dB frequency). It is recommended that the crossover frequency is always less than one fifth of the switching frequency :

$$F_{x_over} \le \frac{F_{sw}}{5}$$

If the transient specification is not stringent, it is better to choose a crossover frequency that is less than one tenth of the switching frequency for good noise immunity. The resistor in the compensation network can then be calculated as:

$$R := \frac{1}{G_{pwm} \cdot V_{in} \cdot G_m} \cdot \left(\frac{F_{esr}}{F_o}\right)^2 \cdot \left(\frac{F_{x_over}}{F_{esr}}\right) \cdot \left(\frac{V_o}{V_{bg}}\right)$$

when

$$F_o < F_{esr} < F_{x_over}$$

Applications Information (Cont.)

or

$$R := \frac{1}{G_{pwm} \cdot V_{in} \cdot G_m} \cdot \left(\frac{F_o}{F_{esr}} \right)^2 \cdot \left(\frac{F_{x_over}}{F_o} \right) \cdot \left(\frac{V_o}{V_{bg}} \right)$$

when

$$F_{esr} < F_o < F_{x_over}$$

(5) The compensation capacitor is determined by choosing the compensator zero to be about one fifth of the output filter corner frequency:

$$F_{zero} := \frac{F_o}{5}$$

$$C := \frac{1}{2 \cdot \pi \cdot R \cdot F_{zero}}$$

(6) The final step is to generate the Bode plot, either by using the simulation model in Fig. 1 or using the equations provided here with Mathcad. The phase margin can then be checked using the Bode plot. Usually, this design procedure ensures a healthy phase margin.

An example is given below to demonstrate the procedure introduced above. The parameters of the power supply are given as:

$V_{in} := 5$ V

$V_o := 2.5$ V

$I_o := 20$ A

$F_{sw} := 250$ KHz

$L := 3$ µH

$C_o := 6600$ µF

$R_c := 0.006$ Ω

$R_1 := 1.0$ KΩ

$R_2 := 1.0$ KΩ

Step 1. Output filter corner frequency

F_o = 1.13 KHz

Step 2. ESR zero frequency:

F_{esr} = 4.019 KHz

Step 3. Check the following condition:

$$F_{esr} < \frac{F_{sw}}{5}$$

Which is satisfied in this case.

Step 4. Choose crossover frequency and calculate compensator R:

F_{x_over} = 50 KHz

R = 43.197 KΩ

Step 5. Calculate the compensator C:

C = 16.287 nF

Step 6. Generate Bode plot and check the phase margin. In this case, the phase margin is about 85°C that ensures the loop stability. Fig. 2 shows the Bode plot of the loop.

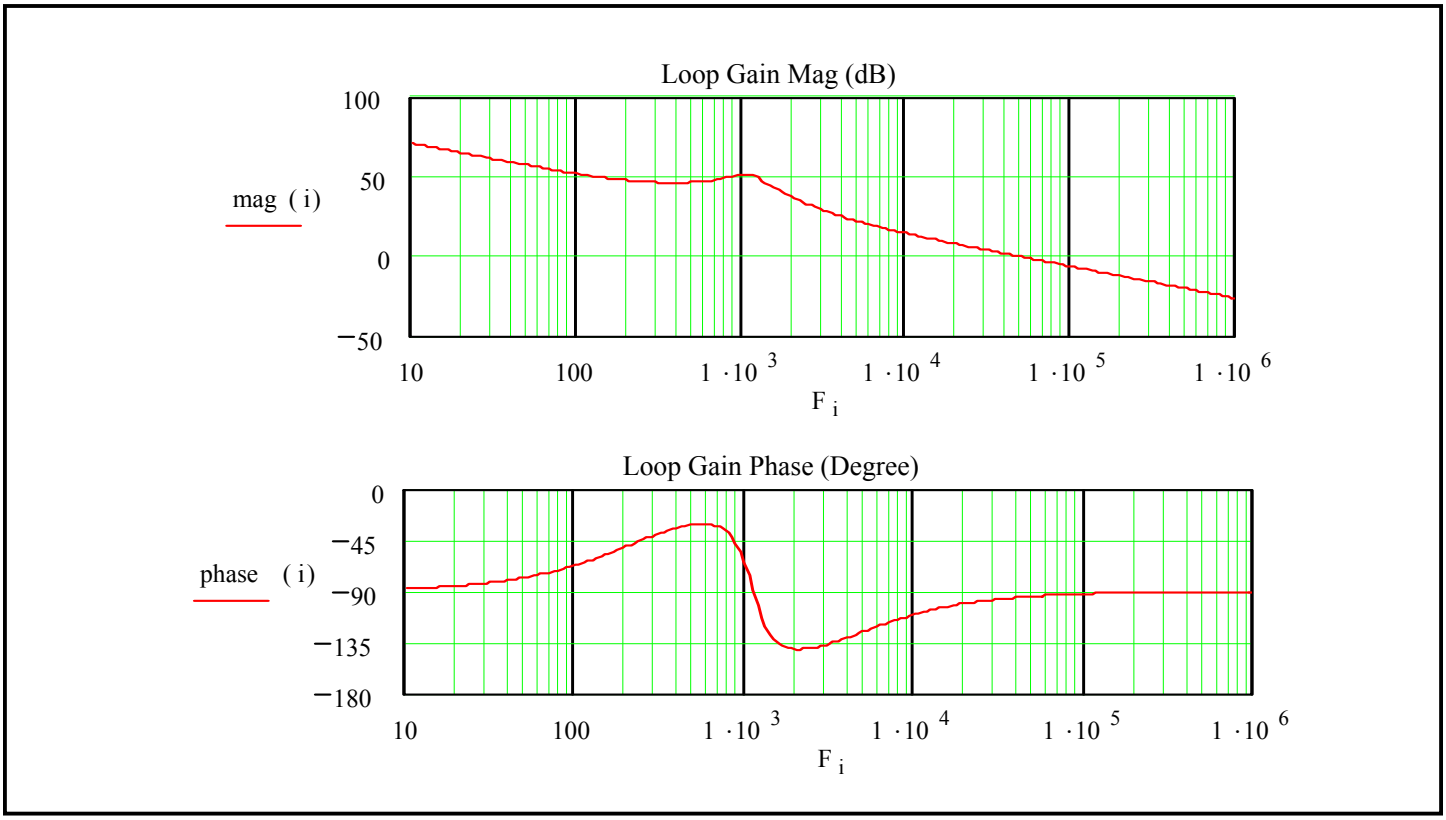
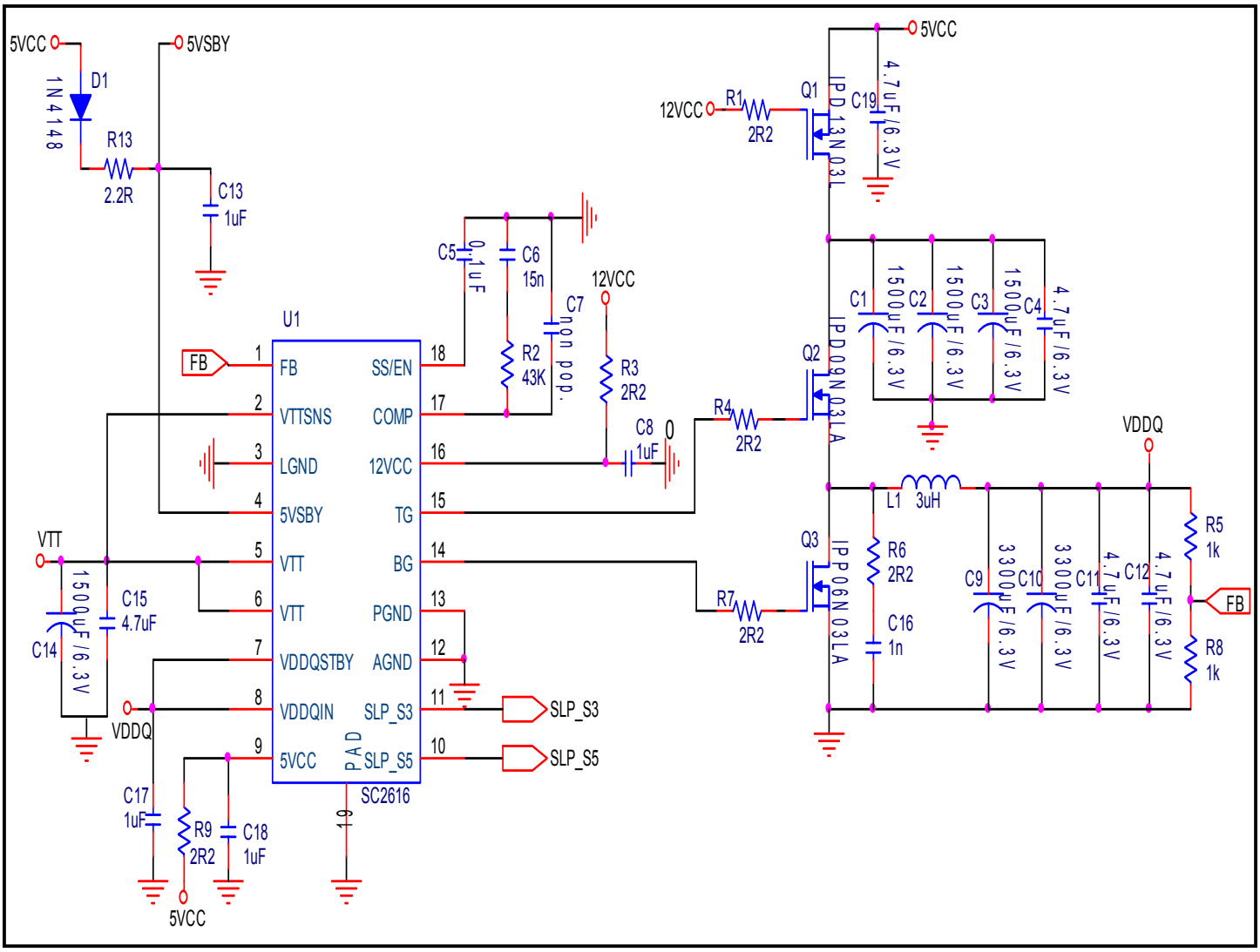


Fig. 2. Bode plot of the loop

Evaluation Board Schematic



Guidelines for Layout of DDR Supply Using SC2616 DDR Controllers on Typical Motherboards

Signals of arbitrary importance (signals that can be routed last, such as SLP_S3, SLP_S5, 5VCC) have been omitted for simplicity.

Parameters of importance in the Layout of the DDR power section are as follows (in order of importance):

1. The VTT decoupling cap,C15, must be placed less than 0.25 inch from Controller.
2. The power rail decoupling cap,C4, must be placed less than 0.25 inch from Q2 drain.
3. The decoupling caps for 5VSBY AND 12Vcc,C13 and C8, must be placed very close to the controller(0.25inch or less)
4. The VDDQ sense lines must be routed from a distant load point (do not connect to the inductor output at the VDDQ plane near the controller/FETS. Place the voltage divider at the load point and route the divider center and the sense ground close together as a differential pair. Connect the AGND and the sensed ground and LGND at the chip.
5. The VTTSNS must be connected to a distant load point.
6. Adequate copper area must be allocated to both VDDQ and VTT. The copper coverage must be uniform, i. e. it provides low resistance to all areas around the DIMMs. VDDQIN traces (and vias if used to carry current) must be adequate for 2.0Amps.
7. Make the phase node area, which connects the Inductor, Top FET and the Bottom FET, as small as possible to prevent EMI, and ringing. Avoid making this

Applications Information (Cont.)

connection using Vias, to minimize inductance.
8. Route gate drive traces on the Top layer as much as possible, with traces 25 mil or wider. If Vias are used, use multiple vias. While gate drive resistors are not required, they may be needed to reduce ringing if the traces are long and inductive.
9. Place components R2,C5, C6 and C7 near the controller, preferably on an analog ground island.
10. Keep Input electrolytic capacitors near the FETs, to minimize AC current loops.

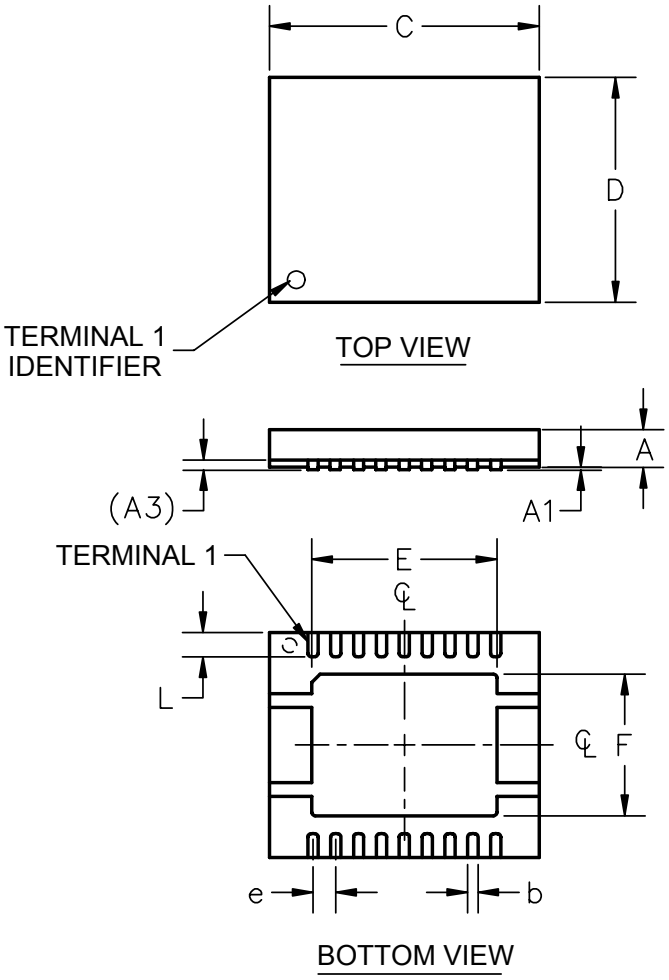
The traces connecting to pins 9, 10, 11 are not critical, since low currents flow in these paths.

Thermal considerations

11. The controller must be placed on a copper land, with at least 0.5" square area. Remove the Soldermask under the IC, as shown in the recommend landing pattern in this datasheet. The Solder-mask cutout area(also referred as stencil aperture) allows the Ground contact at the bottom of the controller (pin 19) to be directly soldered to the PC board for heatsinking to the PC board. There must be at least 5 vias connecting the top and bottom layers on this plane to reduce thermal resistance. These thermal vias must be minimum diameter for the PCB process(12mil drill for 62mil thick PCB). Also it is better to plug the vias by copper plating and solder plating. Making the soldermask cutout area too large will add to the risk of solder flowing near the pins and causing shorted connections.

12. The FETs must be placed on a copper area large enough to adequately transfer heat from the FETs to the PC board. Multiple vias aid in cooling the copper area surrounding the FETs, thus reducing the FETs' junction to ambient thermal resistance.

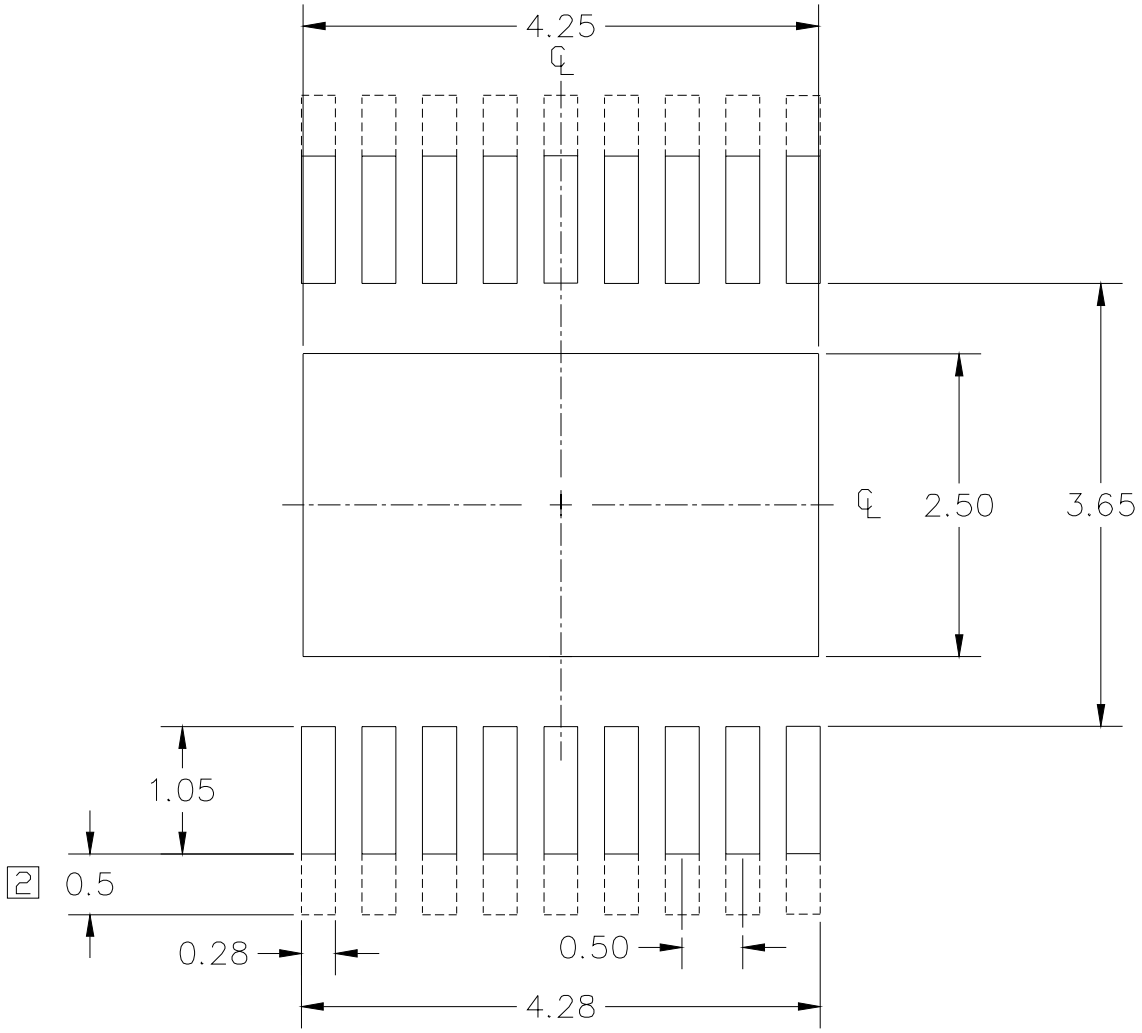
Outline Drawing - MLP-18



DIMENSIONS					
DIM	INCHES		MM		NOTE
	MIN	MAX	MIN	MAX	
A	.032	.039	0.80	1.00	–
A1	0	.002	0	0.05	–
A3	–	.008	–	0.20	REF
b	.007	.012	0.18	0.30	–
C	.236		6.00		NOM
D	.197		5.00		NOM
E	.157	.167	4.00	4.25	–
F	.118	.128	3.00	3.25	–
e	.020 BSC		0.50 BSC		–
L	.017	.026	0.45	0.65	–

[1] CONTROLLING DIMENSIONS: MILLIMETERS

Recommended Land Pattern - MLP-18



[2] PAD LENGTHS MAY BE EXTENDED BY DASHED LINE DIMENSIONS FOR EASE OF REWORK.

[1] CONTROLLING DIMENSIONS: MILLIMETERS.

Contact Information

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