Features

- Supply voltage range VDD 4.5V to 5.5V
- Low standby current (typical < 1µA)
- Serial structure for direct µC interfacing
- Cascadable
- Output status detection
- TTL - compatible input levels with threshold hysteresis
- 8 high current outputs (R_{ON} typ. 1.5 Ω / I_{max}=350mA)
- Wide output operating voltage range (5.5 to 25.5V)
- Output open- and short - circuit detection
- Individual output short - circuit protection
- Clamped output for inductive loads
- Thermal overload protection

Applications

- Relays
- Lamps / LEDs
- DC and stepper motors

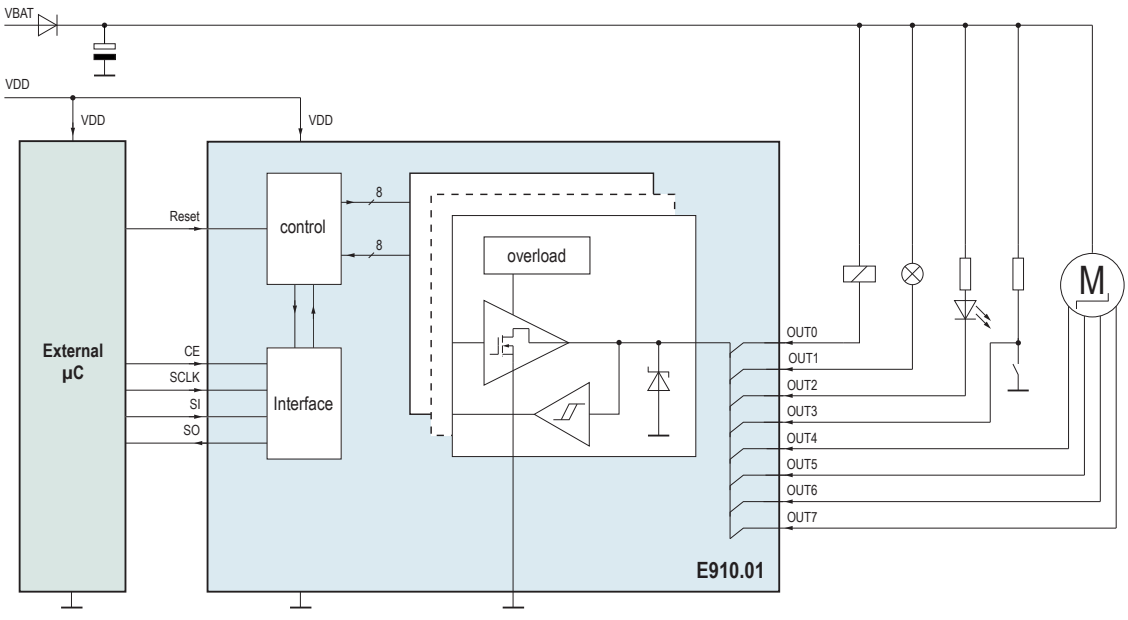
General Description

The IC is developed for automotive applications and can also be used in several other application areas. The IC is well suited to drive relays, lamps, bus systems etc. with medium power consumption.

The device provides a serial data bus for comunication with a µC and 8 identical power drivers. All outputs are short circuit protected. A thermal shut-off protects the device against thermal overload. Readback capability enables fault detection as well as simple switch monitoring.

Ordering Information

Product ID	Temp. Range	Package
E910.01	-40°C to +125°C	SOIC20



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1 Pinout

1.1 Pin Description

Pin-No.	Name	Type [1)]	Description
1	GND		Ground
2	TEST	AI	Test mode enable - Active HIGH > 3V : Test Mode 1 Test mode enable - Active HIGH > 16V: Test Mode 2 for application use : Connect to ground
3	OUT3	AO	Open - drain low - side driver
4	OUT2	AO	Open - drain low - side driver
5	OUT1	AO	Open - drain low - side driver
6	OUT0	AO	Open - drain low - side driver
7	CE	DI	Chip enable - active low (output data is read back on the falling edge of the pulse and only after 8 x n falling edges on SCLK is the output data clocked on the next rising edge)
8	SCLK	DI	Serial data input/output clock (Data are clocked by the falling edge of the pulse.)
9	SI	DI	Serial data input
10	GND		Ground
11	GND		Ground
12	SO	DO	Serial data output (high impedance when CE = High)
13	VDD	DS	Supply voltage
14	RESET	DI	External reset - active low (= internal power on reset)
15	OUT7	AO	Open - drain low - side driver
16	OUT6	AO	Open - drain low - side driver
17	OUT5	AO	Open - drain low - side driver
18	OUT4	AO	Open - drain low - side driver
19	NC		Not connected
20	GND		Ground

1) D = Digital, A = Analog, S = Supply, I = Input, O = Output, HV = High Voltage (max. 40V)

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1.2 Package Pinout

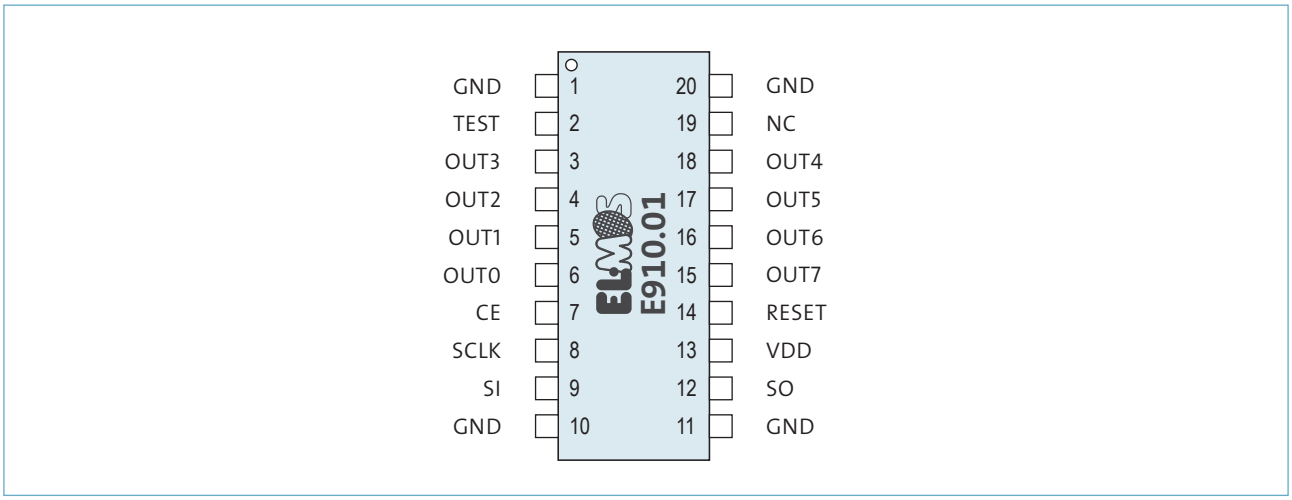


Figure 1: Pinout SOIC20

1.3 Package Reference

Package outline and dimensions are according to JEDEC MS-013-E, version AC. (SOIC20)

2 Operating Conditions

2.1 Absolute Maximum Ratings

Operation of the device at those limits or at values exceeding the limits is not permitted.

Parameter	Condition	Symbol	Min.	Max.	Unit
Logic supply voltage		VDD	-0.3	7.0	V
Transient Output Voltage (Maximum 500 ms) (Maximum 500 µs)		 VOUT VOUT	 - -	 40 50	 V V
Output current		IOUT	-	350	mA
Output current (Schaffner Pulses Type 2)		IOUT P	-	600	mA
Input Voltage		VIN	-0.3	VDD+0.3	V
Power dissipation SO 20 TA = 85°C		P0	-	800	mW
Thermal resistance SO 20 (junction to Ambient)		R_{ThJ-A}	-	80	K/W
Junction temperature		T_J		+150	°C
Operating temperature range		T_{OPT}	-40	+125	°C
Storage temperature range		T_{STG}	-55	+150	°C

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2.2 Recommended Operating Conditions

The following conditions apply unless otherwise stated.

All of the following parameters are valid for an operating temperature range of -40°C up to +105°C (production test max limit is at +85°C), a supply voltage range of 4.5V < VDD < 5.5V, an output current IOUT ≤ 300mA and an output voltage range of 5.5V to 25V, unless otherwise specified.
Voltage reference is GND, if not otherwise specified.
The current values are positive, if flowing into the circuit.

3 Detailed Electrical Specification

3.1 Parameter

3.1.1 DC Parameters

No.	Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
1	Power Supply Current	I_{VDD}		-	-	2	mA
2	Power Supply Current (Sleep Mode)	I_{VDD}	VOUTX > 1V	-	<1	5	µA
3	Power On Reset Threshold	POR_{on}	VDD : 0V --> 5V [3]	-	-	3.6	V
4	Thermal Cut-Off Threshold	T_{HSoff}	$T_J > T_{HS}$ [2) 3)]	+150	+165	+185	°C
5	Thermal Cut-Off Reset Threshold	T_{HSon}	$T_J > T_{HS}$ [2) 3)]	+125	+140	+155	°C
6	Thermal Surveillance Hysteresis	T_{HShys}	[3]	+20	+40	+60	°C

3.1.1.1 Input Parameters

No.	Pin	LOW-Level		HIGH-Level		Hysteresis [3]		Pull up		Pull down	
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.
1	SI	-0.3V	0.3VDD	0.75VDD	VDD+0.3V	0.9V	1.7V	-	1µA		1µA
2	SCLK	-0.3V	0.3VDD	0.75VDD	VDD+0.3V	0.9V	1.7V	-	1µA		1µA
3	CE	-0.3V	0.3VDD	0.75VDD	VDD+0.3V	0.9V	1.7V	-	1µA		1µA
4	RESET	-0.3V	0.3VDD	0.75VDD	VDD+0.3V	0.9V	1.7V	-	-	10µA	50µA
5	TEST	-0.3V	0.3VDD	0.75VDD	8V [4]	-	-	-	-	10µA	50µA
6				16V	17V [5]	-	-				
7	OUTx	-0.3V	2.5V	3.5V	V_{OUT}	-	-	-	-	30µA	90µA

2) As long as the thermal cut-off threshold THS is exceeded, all output drivers are in a high impedance condition. The contents of the latch are unaffected.
3) Not tested in production.
4) Test Mode 1
5) Test Mode 2

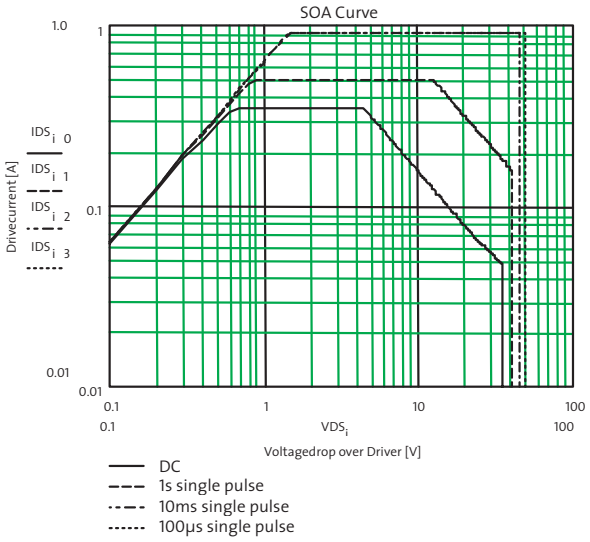
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3.1.1.2 Output Parameters

No.	Pin	Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
1	SO	LOW Level Output Voltage	V_{SOL}	I_{SO} = 1.6mA	-	-	0.4	V
2		HIGH Level Output Voltage	V_{SOH}	I_{SO} = -1mA	V_{DD}-1.3V	-	V_{DD}	V
3		Tristate-Leakage Current	I_{SOtri}	$0 \le V_{SO} \le V_{DD}$	-5	-	5	µA
4	OUTx	Short Circuit Output Current	I_{SC}	VOUTX = 3V T_{SCL} = 20ms	0.35	0.6	0.9	A
5		Output Voltage Limit	V_{OUTx}	OUT = HIGH	36	-	50	V
6		Output Resistance	R_{OUT}	OUT = LOW, $0 < I_{OUT} < 200mA$	-	1.5	3	Ω
7		Residual Output Current	I_{OUTLx}	OUT = HIGH	0	1	10	µA

3.1.2 Safe Operating Area of OUTx

Only one driver active (T=25°C):



All drivers active (T=25°C):

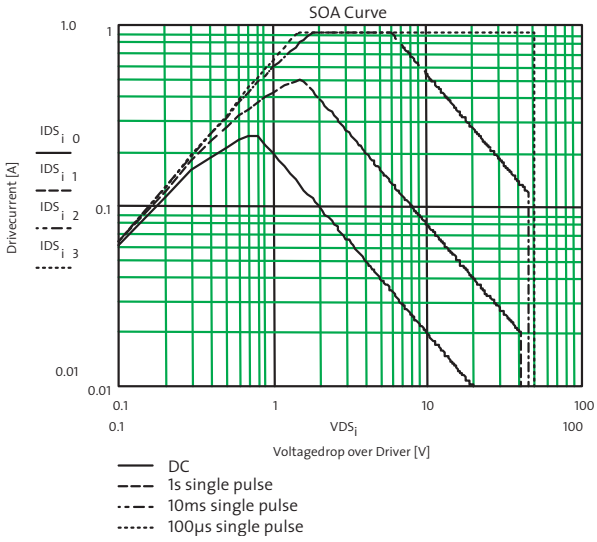


Figure 2: Operating diagrams

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3.1.3 AC Parameters

No.	Pin	Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
1	SCLK SI RESET CE TEST	Input capacitance		3)	-	-	5	pF
2	SO	Output marginal delay		3)	-	-	0.5	ns/pF
3	RESET	RESET Pulse Width	t_{RESon}	RESET --> L	0.31	0.62	0.93	ms
4	OUTx	Rate of Change of Output Voltage	dV_{OUT}/dt	R_L = 1kΩ 3)	-	10	-	V/µs
5		Output Capacitance	C_{OUT}	OUT = HIGH, V_{OUT} = 5V 3)	-	40	60	pF
6				OUT = HIGH, V_{OUT} = 15V 3)	-	30	45	pF
7		Duration of Output Short Circuit Limit	T_{SCL}	$I_{OUT} > I_{SCL}$ 1)	18.5	37	55.5	ms
8		Propagation Delay Time CE --> OUTx	t_N	see Fig. 9 R_L = 1kΩ 3)	-	10	20	µs
9	SCLK	Clock frequency	f_{SCLK}	3)	-	-	2	MHz

1) When the output current exceeds the value of ISCL an internal timer is initiated and the current limit is activated. If the current limit is still active after the time TSCL the individual output is disabled by resetting the input latch.
3) Not tested in production.

3.1.3.1 Interface Timing

Symbol	Parameter	Min. 3)	Max. 3)	Unit
T_{LSO}	Time between falling edge (10%) or rising edge (90%) of the CE signal and active (90%) or high impedance state of the SO output. Load capacitance at SO < 20pF.	20	100	ns
T_{LCF}	Time between falling edge (10%) of the CE signal and the first rising edge (10%) of the SCLK clock.	150		ns
T_{CSO}	Time between rising edge (10%) of the SCLK clock and the new data at SO output (10% or 90%). Load capacitance at SO < 20pF.	10	60	ns
T_{DS}	Time between stable data at SI (90% or 10%) and falling edge at SCLK (90%) to clock the data in: Data setup time.	40		ns
T_{DH}	Time between falling edge at SCLK (90%) and changing of the data at SI (10% or 90%): data hold time	20		ns
T_{LL}	Time between two load cycles: CE at high level (90%)	150		ns
T_{LCR}	Time between falling edge of SCLK (90%) and rising edge of CE (90%) signal.	20		ns

3) Not tested in production.

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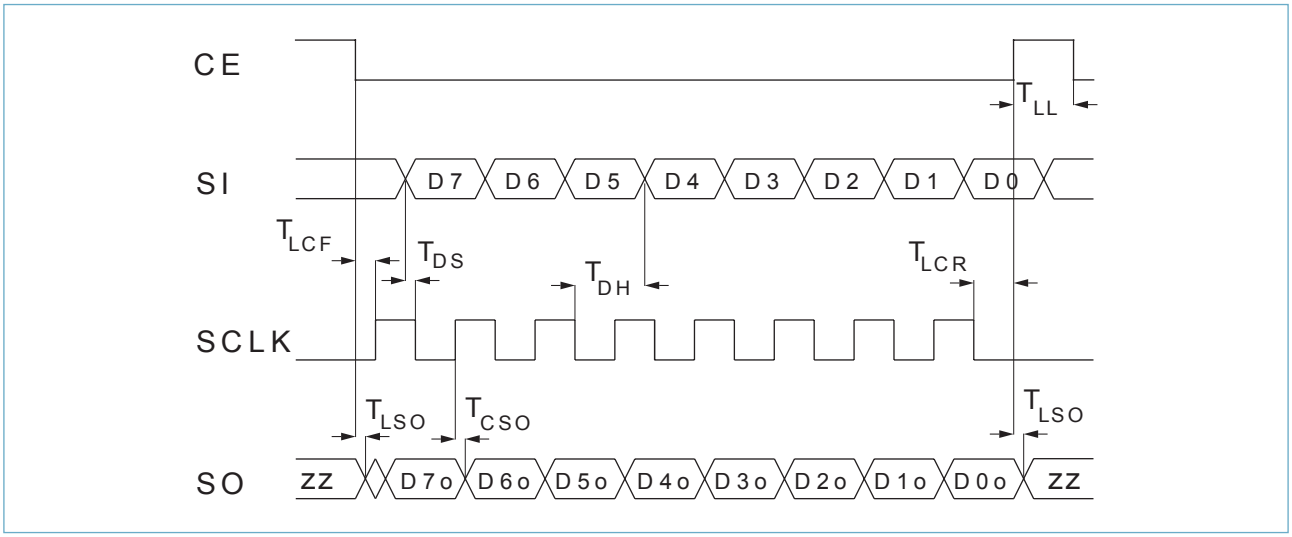


Figure 3: Timing diagram

4 Functional Description

4.1 Block diagram

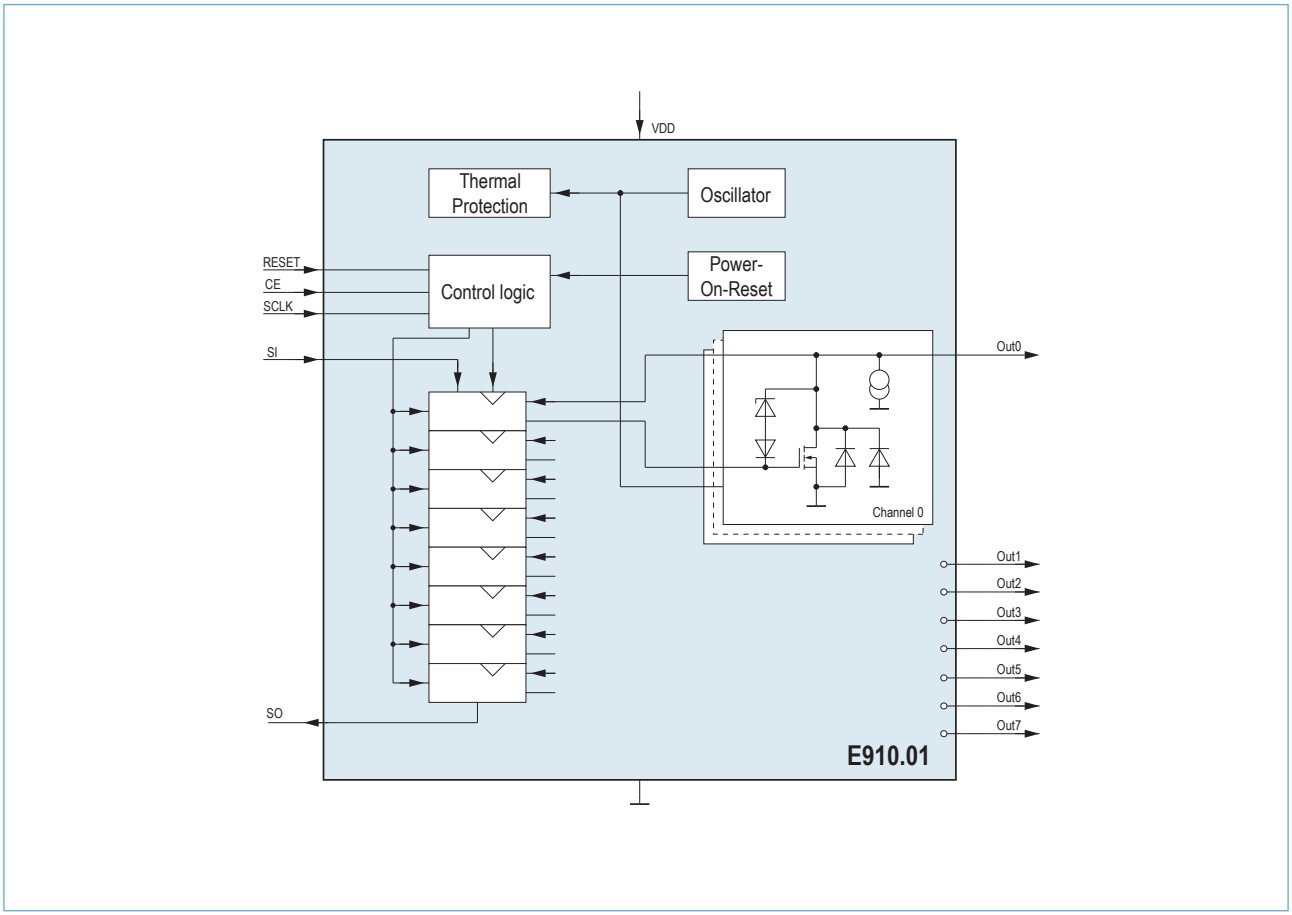


Figure 4: Block diagram

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4.2 Detailed Functional Description

This IC was specially developed for Automobile applications. Application areas include driving relays, Lamps, bus systems etc. with medium power consumption. The E910.01 comprises a serial data bus and 8 identical power drivers. All outputs are short circuit protected, and a thermal cut-off protects the devices from thermal overstress.

By means of the RESET signal (RESET=Low) the IC can be switched into a low current consumption mode (Sleep Mode). In this mode all current consumption is disabled.

There are two possible data transfer protocols:

a) Parallel data input (see Figure 5 and Figure 9)

SI and SO are tied together and the device is activated by means of the chip enable (CE) line. On the falling edge of the CE signal the data is loaded into the shift register and SO goes to the low impedance state. With each rising edge of SCLK the data beginning with Bit 7 (D7) is clocked out at SO and with each falling edge new data is clocked from SI. On the rising edge of CE the data from the shift register is clocked through to the outputs. SO goes to the high impedance state (Tri-State as long as CE remains inactive HIGH). A LOW level on the input produces a LOW level on the open drain driver which switches to the low impedance state.

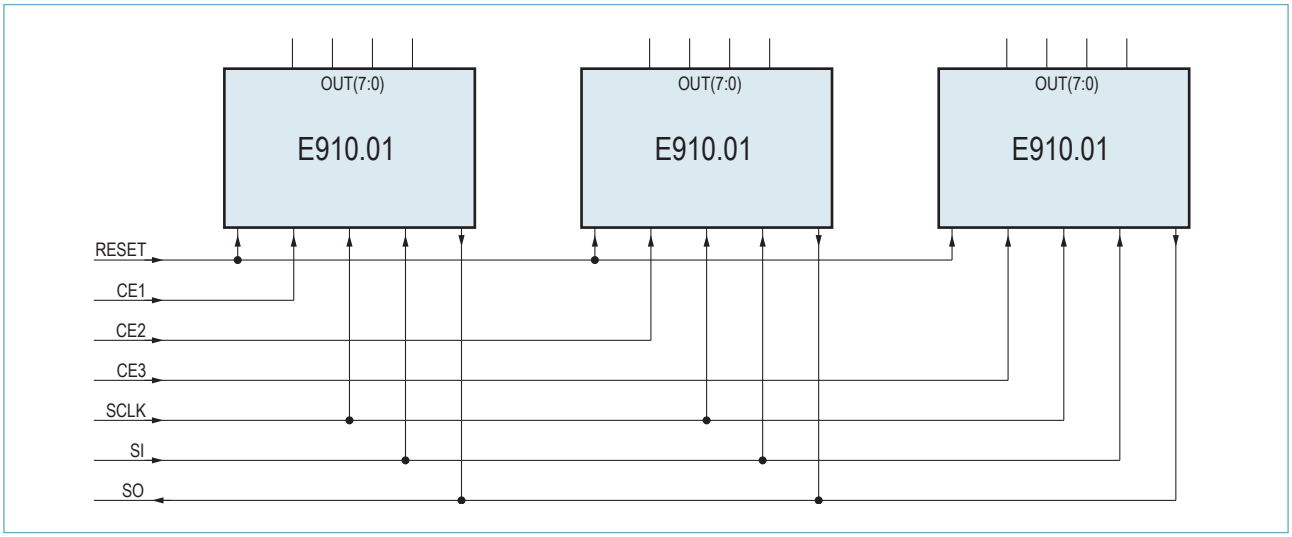


Figure 5: Parallel data input

b) Serial data input (see Figure 6 and Figure 7/8)

The complete Daisy Chain of drivers are enabled in parallel by CE and clocked out by SCLK. On the falling edge of CE the status of each output is clocked into the shift register. On each rising edge of SCLK data is clocked out of SO, and with each falling edge of SCLK new data is clocked into SI. After 8 x n clock cycles new data has been read in and existing data clocked out. On the rising edge of CE new data is clocked through to the outputs. SO goes to the high impedance state (Tri-state as long as CE remains inactive HIGH). A LOW level on the input produces a LOW level on the open drain driver which switches to the low impedance state.

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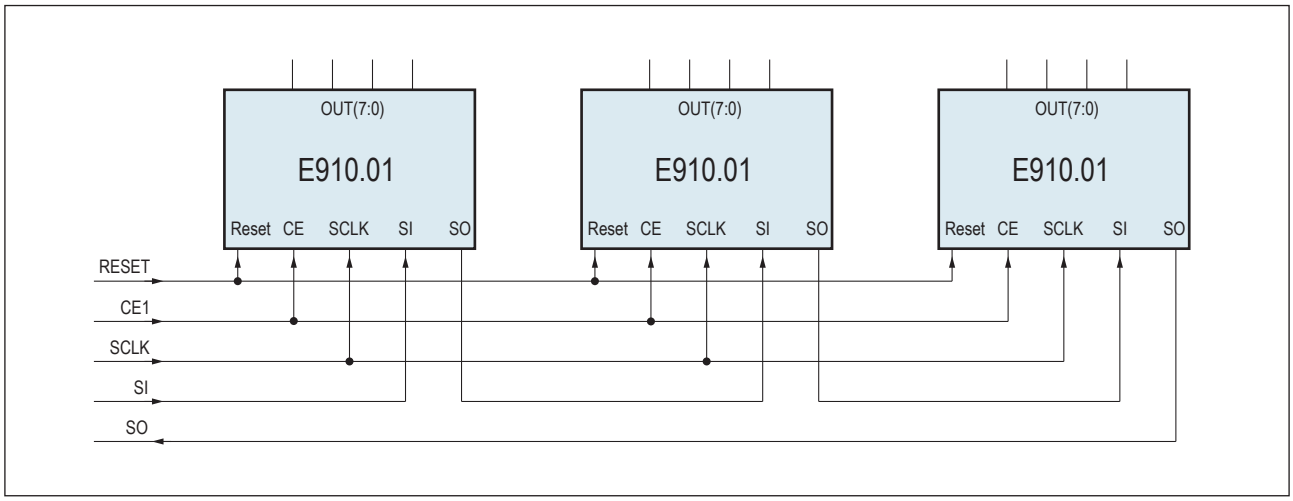


Figure 6: Serial data input

4.3 Protection Functions

In addition to the Power on reset function the IC incorporates three other protection functions; over temperature protection, short-circuit protection and open output recognition. No special failure status bit is provided for indicating failures since this information is not available on the 8 bit interface.

Power-On-Reset: After the application of the supply voltage all data latches and the timer are reset, and the outputs are disabled (inactive HIGH). The internal Power On Reset is OR'd with the external RESET input. In the RESET Mode the serial data output SO is inactive (LOW), as long as CE is active (LOW). Whereas SO goes into the high impedance Tri-State, if CE is inactive (HIGH). The external RESET is only invoked, if the pulse width exceeds the time tRESon.(see Figure 10)

Short Circuit Protection: If the voltage drop across the output driver exceeds the short circuit threshold of 1V (RDSON typ. 1.5Ω), the current limit is activated and after approximately 40ms, the output is disabled. After disabling the output, the short circuit memory is cleared and it is possible to re-activate the outputs by writing LOW bits into the shift register via the serial data input SI. In the event that a short circuit is still present the current limit is again activated and the output is again disabled after 40 ms.

After output disable due to the presence of a short circuit (OUTx = inactive HIGH) the serial output SO goes to a HIGH level, since SO always indicates the actual output status. Interrogating the SO status is the only way of establishing if a short circuit exists. When the output OUTx is selected by a LOW level on the SI serial data input (output OUTx enabled) and a HIGH level appears on the data output SO the presence of a short circuit on the enabled output is clear.

At switch on the output is operated as a constant current source by the internal limiting. When used with lamps they may be safely switched on because the internal limit operates for approximately 40 ms and disables the outputs. (see Figure 12)

Open Output Recognition: In the event of an open output the output voltage of OUTx is set to definite LOW level by the pull down transistor (OUTx = LOW). A LOW level also appears at the data output SO:

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The actual method of establishing that an output is open is by interrogating the state of the data output SO. When an output OUTx is selected by means of a HIGH level on the SI pin (output OUTx disabled) a LOW level appears on the SO pin. Thus the open condition of the output is indicated. This function is the inverse of the short circuit condition above.

Over temperature Protection: If the chip temperature exceeds the protection threshold of typically 165°C all output drivers are disabled and the data stored in the latches are retained. When the temperature drops below the protection threshold of typically 140°C the previously stored condition is restored providing no new data have been loaded into the shift register by SI during this protection condition otherwise the stored data is overridden. This is also the case, when a RESET signal is received or when a falling edge on CE causes the shift register to be read. (see Figure 11)

The actual method of establishing that the device is in thermal protection shut down is by interrogating the state of the data output SO. When an output OUTx is selected by means of a LOW level on the SI pin (output OUTx enabled) a HIGH level appears on the SO pin for all outputs. Thus the thermal shutdown condition is indicated. It is highly unlikely that a short circuit condition can occur in all outputs simultaneously.

Test Modes:
If a voltage of greater than 3V and lower than 8V is applied to the TEST input, the device will switch into the Test Mode 1. In this mode the counter chain following the internal RC oscillator is shortened. The oscillator signal (divided by 2) appears on the output SO.
Test mode 2: If the voltage at the TEST input is greater than 16V additionally the over temperature protection circuit is set between +25°C and +85°C.

4.4 Application Circuit

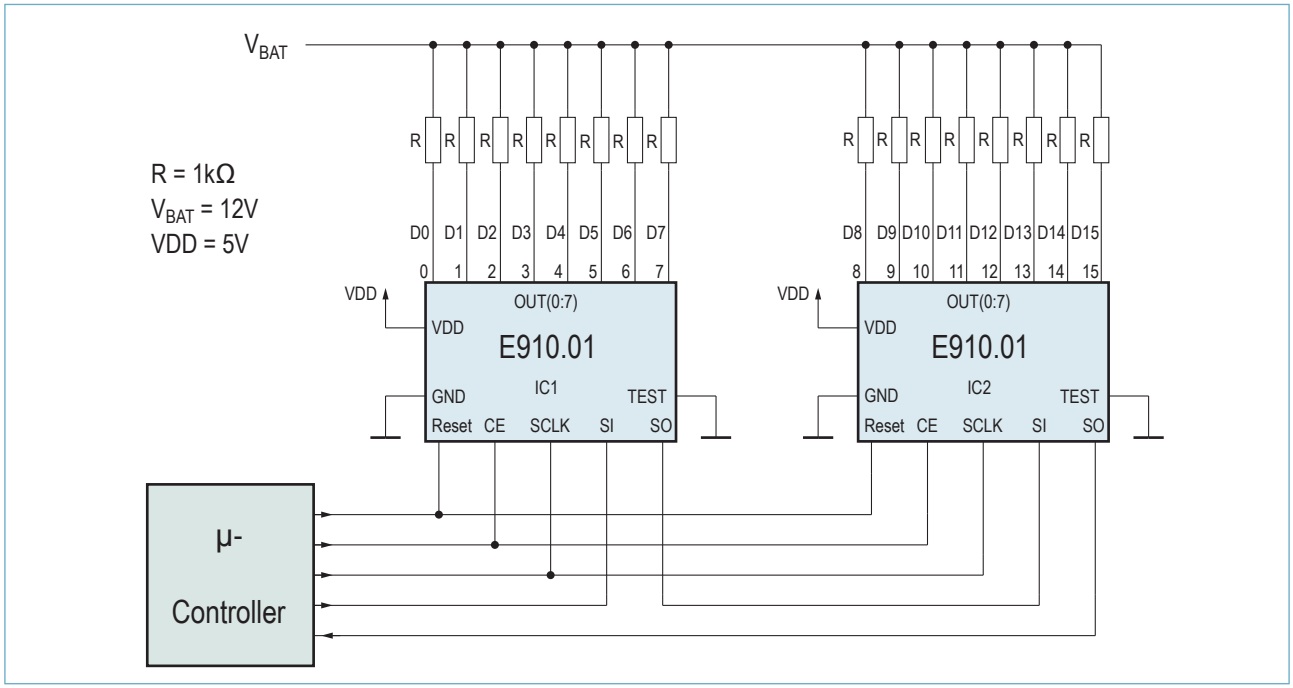


Figure 7: Typical application circuit

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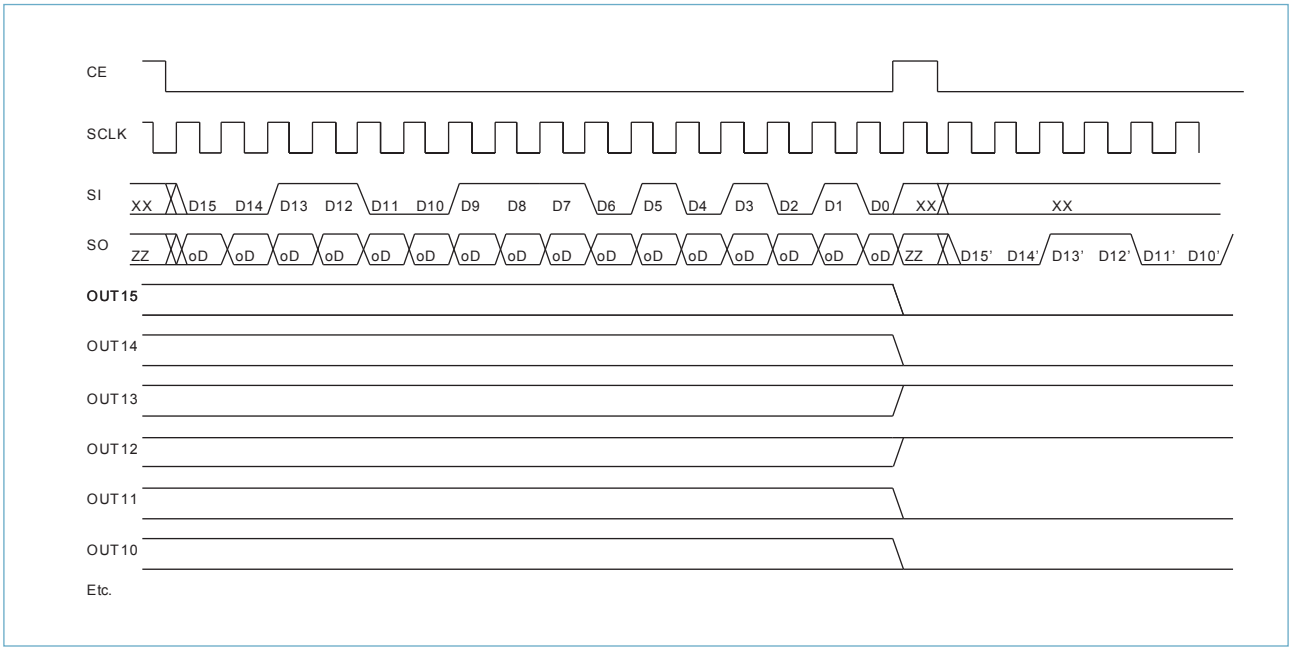


Figure 8: Timing diagram example

4.5 Timing Diagram

4.5.1 Operating Mode

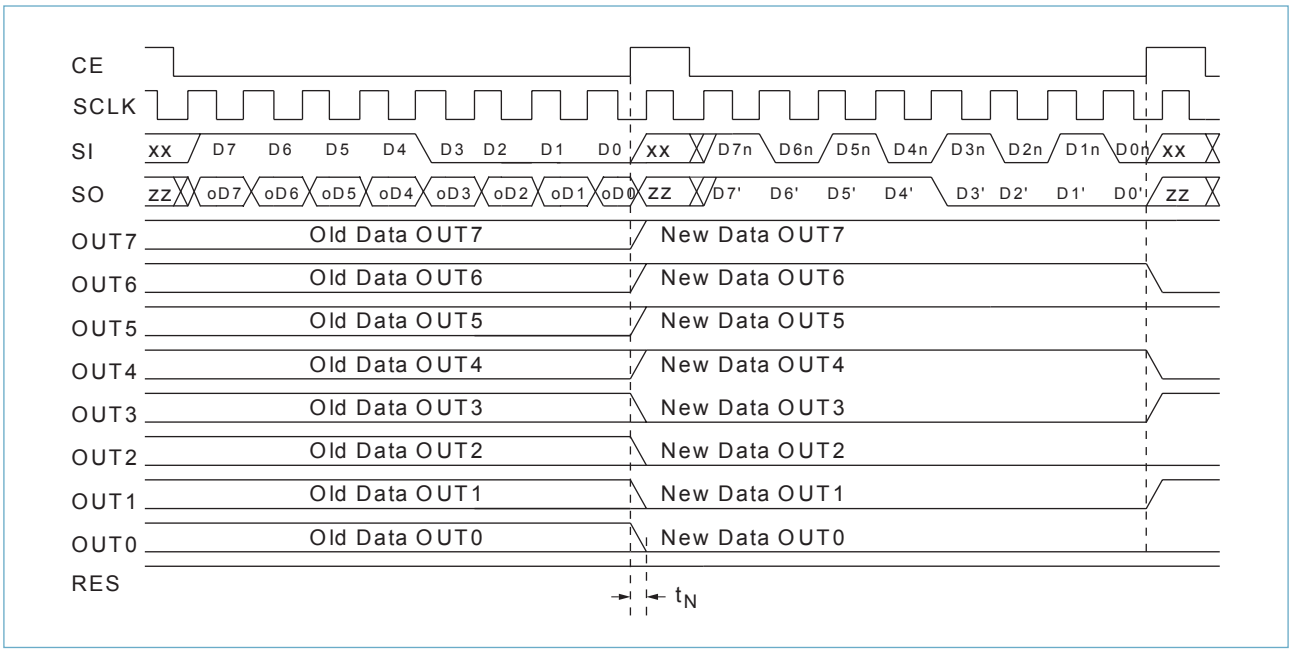


Figure 9: Timing diagram operating mode

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4.5.2 RESET Mode (Sleep Mode)

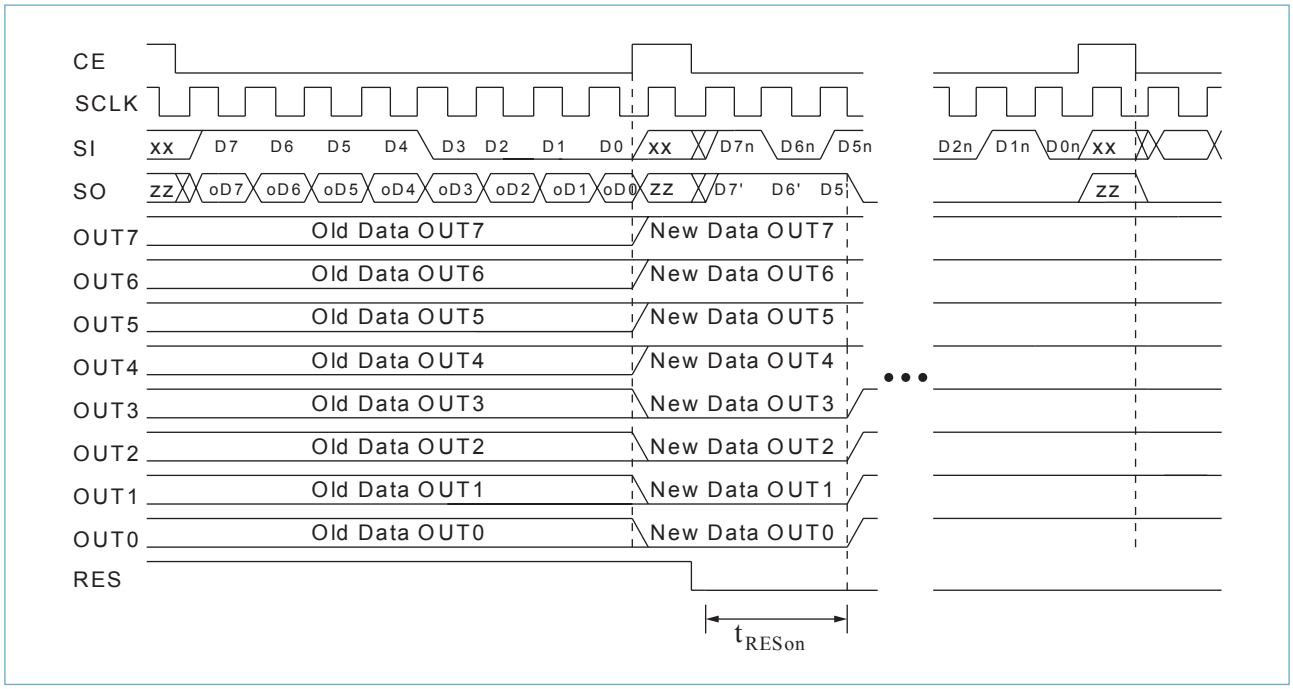


Figure 10: Timing diagram RESET mode

4.5.3 Thermal Cut-off

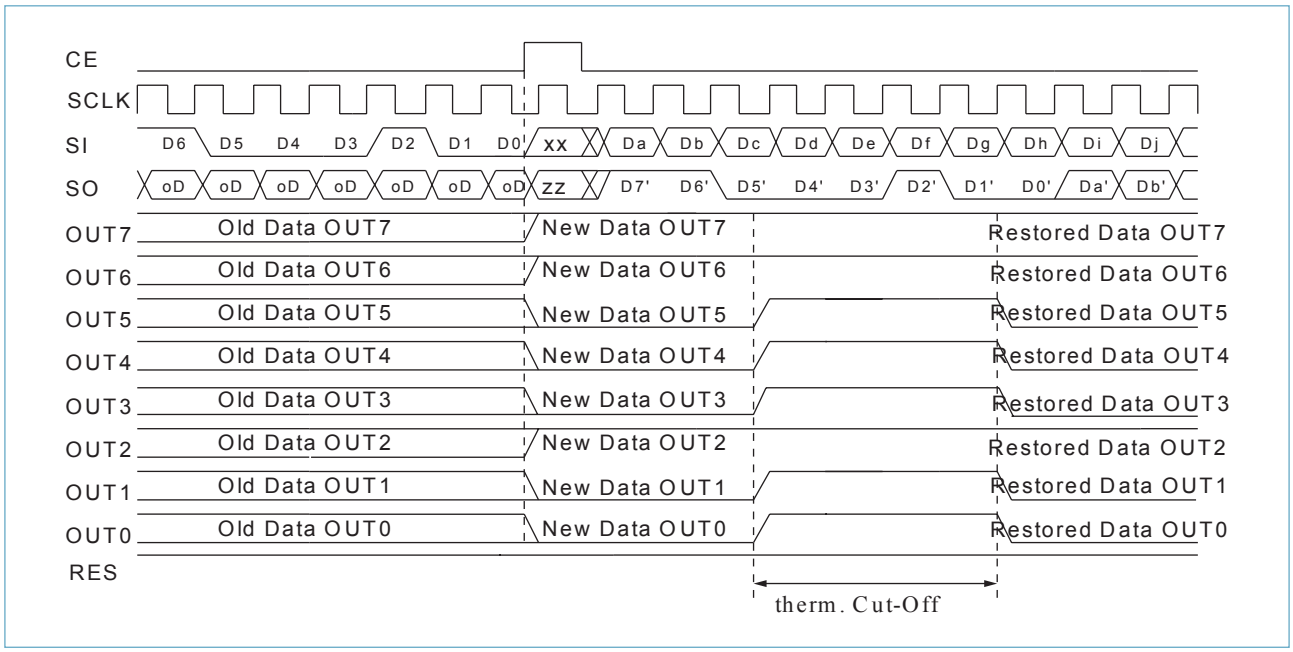


Figure 11: Timing diagram thermal cut-off

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4.5.4 Short Circuit Condition

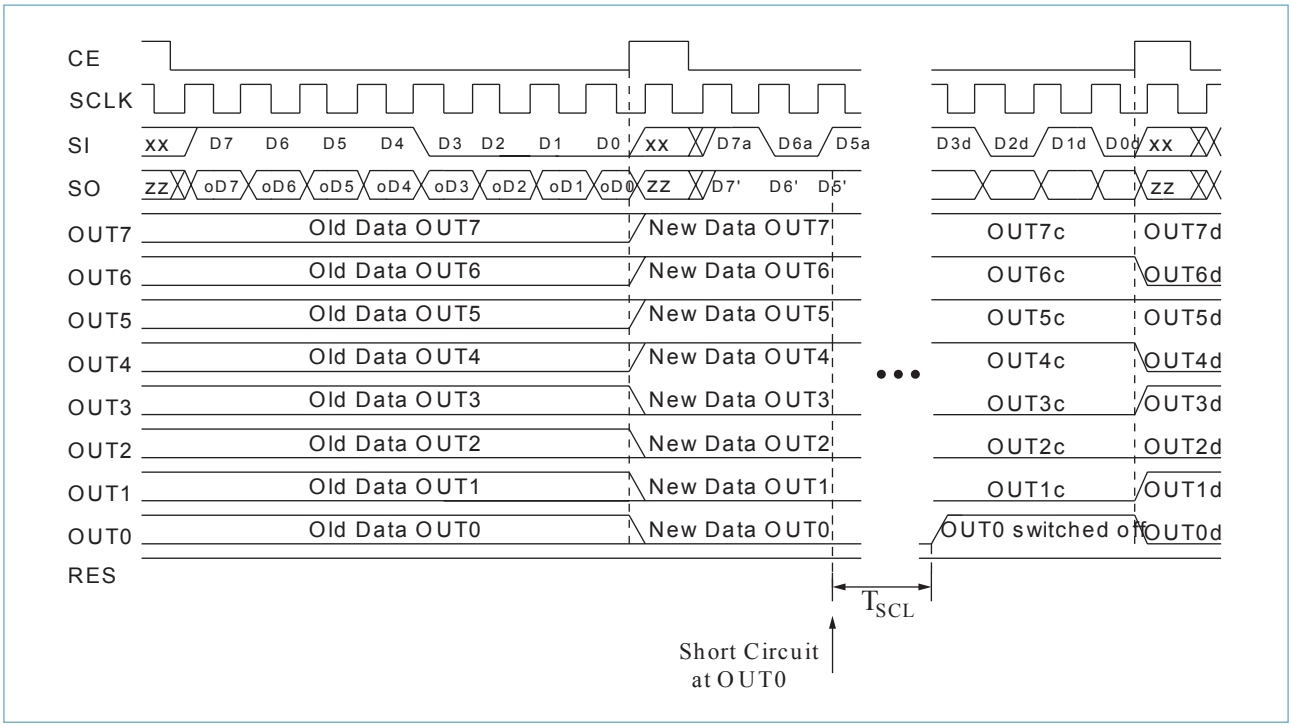


Figure 12: Timing diagram short circuit condition

4.6 Noise Immunity

The E910.01 device meets the following requirements of DIN 40 839 part 1, when used in an application according to this specification :

Parameter	Condition	
Test pulse 1	t_1 = 5s / U_S = -100V	100 pulses
Test pulse 2	t_1 = 0,5s / U_S = 100V	1000 pulses
Test pulse 3a/b	DIN 40 839 Part 3 U_S = -150V / U_S = 100V	1000 bursts
Test pulse 4	U_S = -6V U_a = -5V t_8 = 5s	10 pulses
Test pulse 5	R_i = 2_t_D = 250ms t_r = 0.1ms U_p + U_S = 40V	10 pulses at 1 minute intervals

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4.7 ESD Protection Circuit

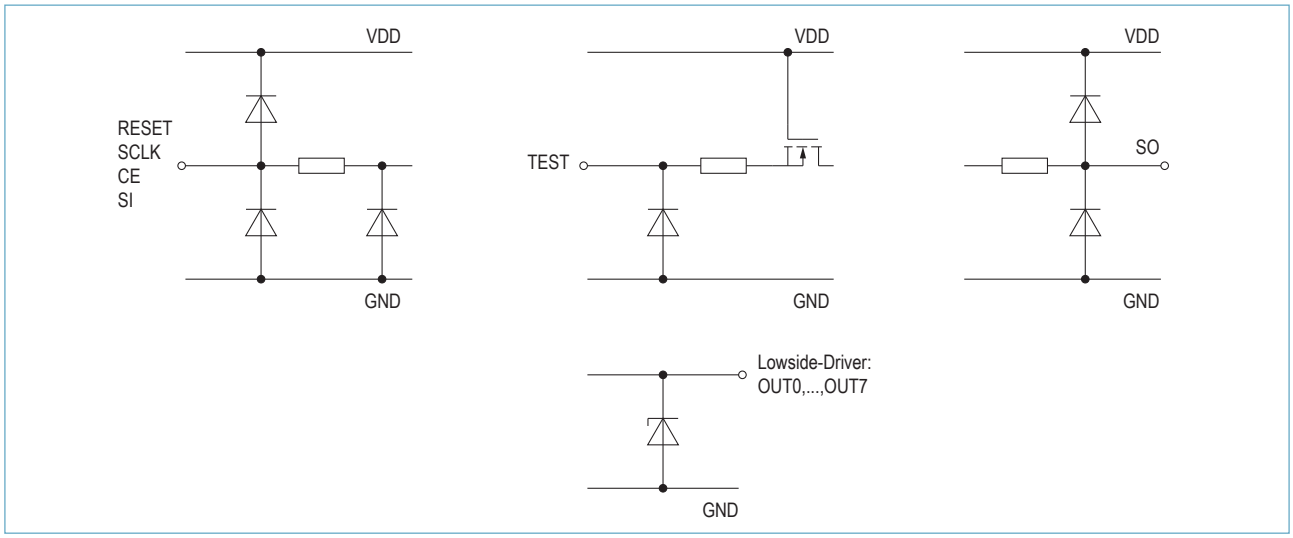


Figure 13: ESD Protection Circuit

4.7.1 Test Method

The ESD Protection circuitry is measured using AEC-Q100-002 chip-level test method with the following conditions :

- VIN = 2000 Volt
- REXT = 1500 Ohm
- CEXT = 100 pF

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