National Semiconductor

May 1995

54F/74F299 Octal Universal Shift/Storage Register with Common Parallel I/O Pins

General Description

The 'F299 is an 8-bit universal shift/storage register with TRI-STATE® outputs. Four modes of operation are possible: hold (store), shift left, shift right and load data. The parallel load inputs and flip-flop outputs are multiplexed to reduce the total number of package pins. Additional outputs, Q_0–Q_7, are provided to allow easy serial cascading. A separate active LOW Master Reset is used to reset the register.

Features

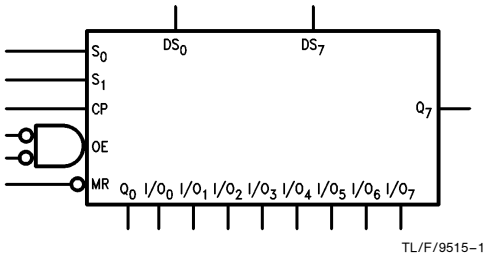
- Common parallel I/O for reduced pin count
- Additional serial inputs and outputs for expansion
- Four operating modes: shift left, shift right, load and store
- TRI-STATE outputs for bus-oriented applications
- Guaranteed 4000V minimum ESD protection

Commercial	Military	Package Number	Package Description
74F299PC		N20A	20-Lead (0.300″ Wide) Molded Dual-In-Line
	54F299DM (Note 2)	J20A	20-Lead Ceramic Dual-In-Line
74F299SC (Note 1)		M20B	20-Lead (0.300″ Wide) Molded Small Outline, JEDEC
74F299SJ (Note 1)		M20D	20-Lead (0.300″ Wide) Molded Small Outline, EIAJ
	54F299FM (Note 2)	W20A	20-Lead Cerpack
	54F299LM (Note 2)	E20A	20-Lead Ceramic Leadless Chip Carrier, Type C

Note 1: Devices also available in 13″ reel. Use suffix = SCX and SJX.

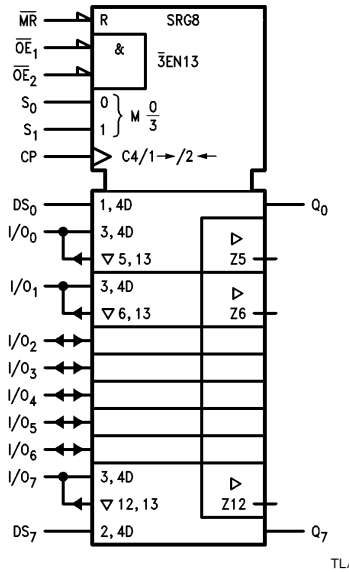
Note 2: Military grade device with environmental and burn-in processing. Use suffix = DMQB, FMQB and LMQB.

Logic Symbols



TL/F/9515–1

IEEE/IEC



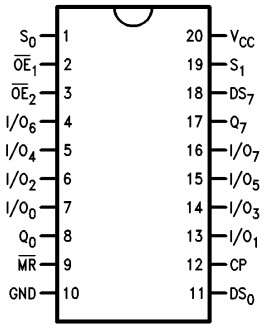
TL/F/9515–4

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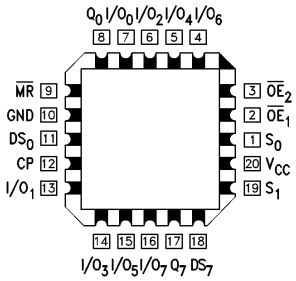
Connection Diagrams

Pin Assignment for DIP, SOIC and Flatpak



TL/F/9515–2

Pin Assignment for LCC



TL/F/9515–3

Unit Loading/Fan Out

Pin Names	Description	54F/74F	
		U.L. HIGH/LOW	Input I_{IH}/I_{IL} Output I_{OH}/I_{OL}
CP	Clock Pulse Input (Active Rising Edge)	1.0/1.0	20 μA/−0.6 mA
DS_0	Serial Data Input for Right Shift	1.0/1.0	20 μA/−0.6 mA
DS_7	Serial Data Input for Left Shift	1.0/1.0	20 μA/−0.6 mA
S_0, S_1	Mode Select Inputs	1.0/2.0	20 μA/−1.2 mA
$\overline{MR}$	Asynchronous Master Reset Input (Active LOW)	1.0/1.0	20 μA/−0.6 mA
$\overline{OE}_1$, $\overline{OE}_2$	TRI-STATE Output Enable Inputs (Active LOW)	1.0/1.0	20 μA/−0.6 mA
I/O_0–I/O_7	Parallel Data Inputs or	3.5/1.083	70 μA/−0.65 mA
	TRI-STATE Parallel Outputs	150/40(33.3)	−3 mA/24 mA (20 mA)
Q_0, Q_7	Serial Outputs	50/33.3	−1 mA/20 mA

Functional Description

The 'F299 contains eight edge-triggered D-type flip-flops and the interstage logic necessary to perform synchronous shift left, shift right, parallel load and hold operations. The type of operation is determined by S_0 and S_1, as shown in the Mode Select Table. All flip-flop outputs are brought out through TRI-STATE buffers to separate I/O pins that also serve as data inputs in the parallel load mode. Q_0 and Q_7 are also brought out on other pins for expansion in serial shifting of longer words.

A LOW signal on $\overline{MR}$ overrides the Select and CP inputs and resets the flip-flops. All other state changes are initiated by the rising edge of the clock. Inputs can change when the clock is in either state provided only that the recommended setup and hold times, relative to the rising edge of CP, are observed.

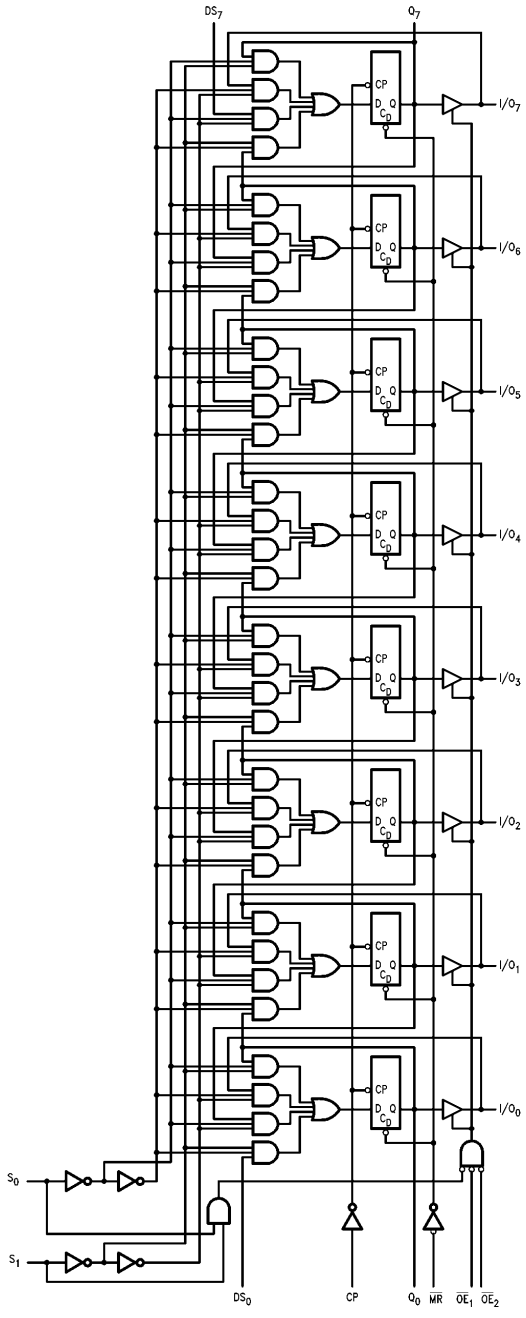
A HIGH signal on either $\overline{OE}_1$ or $\overline{OE}_2$ disables the TRI-STATE buffers and puts the I/O pins in the high impedance state. In this condition the shift, hold, load and reset operations can still occur. The TRI-STATE outputs are also disabled by HIGH signals on both S_0 and S_1 in preparation for a parallel load operation.

Mode Select Table

Inputs				Response
$\overline{MR}$	S_1	S_0	CP	
L	X	X	X	Asynchronous Reset; Q_0–Q_7 = LOW
H	H	H	⌐	Parallel Load; $I/O_n \rightarrow Q_n$
H	L	H	⌐	Shift Right; $DS_0 \rightarrow Q_0$, $Q_0 \rightarrow Q_1$, etc.
H	H	L	⌐	Shift Left; $DS_7 \rightarrow Q_7$, $Q_7 \rightarrow Q_6$, etc.
H	L	L	X	Hold

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
⌐ = LOW-to-HIGH Clock Transition

Logic Diagram



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Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias	−55°C to +175°C
Plastic	−55°C to +150°C
V_{CC} Pin Potential to Ground Pin	−0.5V to +7.0V
Input Voltage (Note 2)	−0.5V to +7.0V
Input Current (Note 2)	−30 mA to +5.0 mA
ESD Last Passing Voltage (Min)	4000V

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

Voltage Applied to Output in HIGH State (with V_{CC} = 0V)	
Standard Output	−0.5V to V_{CC}
TRI-STATE Output	−0.5V to +5.5V
Current Applied to Output in LOW State (Max)	twice the rated I_{OL} (mA)

Recommended Operating Conditions

Free Air Ambient Temperature	
Military	−55°C to +125°C
Commercial	0°C to +70°C
Supply Voltage	
Military	+4.5V to +5.5V
Commercial	+4.5V to +5.5V

DC Electrical Characteristics

Symbol	Parameter		54F/74F Min	54F/74F Typ	54F/74F Max	Units	V_{CC}	Conditions
V_{IH}	Input HIGH Voltage		2.0			V		Recognized as a HIGH Signal
V_{IL}	Input LOW Voltage				0.8	V		Recognized as a LOW Signal
V_{CD}	Input Clamp Diode Voltage				−1.2	V	Min	I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	54F 10% V_{CC}	2.5			V	Min	I_{OH} = −1 mA (Q_0, Q_7, I/O_n)
		54F 10% V_{CC}	2.4					I_{OH} = −3 mA (I/O_n)
		74F 10% V_{CC}	2.5					I_{OH} = −1 mA (Q_0, Q_7, I/O_n)
		74F 10% V_{CC}	2.4					I_{OH} = −3 mA (I/O_n)
		74F 5% V_{CC}	2.7					I_{OH} = −1 mA (Q_0, Q_7, I/O_n)
		74F 5% V_{CC}	2.7					I_{OH} = −3 mA (I/O_n)
V_{OL}	Output LOW Voltage	54 10% V_{CC}			0.5	V	Min	I_{OL} = 20 mA
		74 10% V_{CC}			0.5			I_{OL} = 20 mA (Q_0, Q_7)
		74 10% V_{CC}			0.5			I_{OL} = 24 mA (I/O_n)
I_{IH}	Input HIGH Current	54F			20.0	μA	Max	V_{IN} = 2.7V ($\overline{CP}$, $\overline{DS_0}$, $\overline{DS_7}$, S_0, S_1, $\overline{MR}$, $\overline{OE_1}$, $\overline{OE_2}$)
		74F			5.0			
I_{BVI}	Input HIGH Current Breakdown Test	54F			100	μA	Max	V_{IN} = 7.0V ($\overline{CP}$, $\overline{DS_0}$, $\overline{DS_7}$, S_0, S_1, $\overline{MR}$, $\overline{OE_1}$, $\overline{OE_2}$)
		74F			7.0			
I_{BVIT}	Input HIGH Current Breakdown Test (I/O)	54F			1.0	mA	Max	V_{IN} = 5.5V (I/O_n)
		74F			0.5			
I_{CEX}	Output HIGH Leakage Current	54F			250	μA	Max	V_{OUT} = V_{CC}
		74F			50			
V_{ID}	Input Leakage Test	74F	4.75			V	0.0	I_{ID} = 1.9 μA All Other Pins Grounded
I_{OD}	Output Leakage Circuit Current	74F			3.75	μA	0.0	V_{IOD} = 150 mV All Other Pins Grounded
I_{IL}	Input LOW Current				−0.6	mA	Max	V_{IN} = 0.5V (CP, $\overline{DS_0}$, $\overline{DS_7}$, $\overline{MR}$, $\overline{OE_1}$, $\overline{OE_2}$)
					−1.2			V_{IN} = 0.5V (S_0, S_1)
I_{IH} + I_{OZH}	Output Leakage Current				70	μA	Max	$V_{I/O}$ = 2.7V (I/O_n)
I_{IL} + I_{OZL}	Output Leakage Current				−650	μA	Max	$V_{I/O}$ = 0.5V (I/O_n)
I_{OS}	Output Short-Circuit Current		−60		−150	mA	Max	V_{OUT} = 0V
I_{ZZ}	Bus Drainage Test				500	μA	0.0V	V_{OUT} = 5.25V
I_{CCH}	Power Supply Current			68	95	mA	Max	V_O = HIGH
I_{CCL}	Power Supply Current			68	95	mA	Max	V_O = LOW
I_{CCZ}	Power Supply Current			68	95	mA	Max	V_O = HIGH Z

AC Electrical Characteristics

Symbol	Parameter	74F $T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50$ pF			54F T_A, V_{CC} = Mil $C_L = 50$ pF		74F T_A, V_{CC} = Com $C_L = 50$ pF		Units
		Min	Typ	Max	Min	Max	Min	Max	
f_{max}	Maximum Input Frequency	70	100		85		70		MHz
t_{PLH} t_{PHL}	Propagation Delay CP to Q_0 or Q_7	4.0 4.5	7.0 6.5	8.0 8.0	4.0 4.5	9.0 9.5	4.0 4.5	8.5 8.5	ns
t_{PLH} t_{PHL}	Propagation Delay CP to I/O_n	3.5 4.0	7.0 8.5	9.0 9.0	3.5 4.0	10.0 11.0	3.5 4.0	10.0 10.0	
t_{PHL}	Propagation Delay $\overline{MR}$ to Q_0 or Q_7	5.5	7.5	9.5	5.5	12.5	5.5	10.5	ns
t_{PHL}	Propagation Delay $\overline{MR}$ to I/O_n	5.5	11.0	10.0	5.5	12.0	5.5	10.5	
t_{PZH} t_{PZL}	Output Enable Time $\overline{OE}$ to I/O_n	3.5 4.0	6.0 7.0	8.0 10.0	3.0 4.0	9.5 13.0	3.5 4.0	9.0 11.0	ns
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{OE}$ to I/O_n	2.0 1.0	4.5 4.0	6.0 5.5	1.5 1.0	7.0 6.5	2.0 1.0	7.0 6.5	
t_{PZH} t_{PZL}	Output Enable Time S_n to I/O_n	3.5 4.0		9.0 10.0	3.0 4.0	10.5 13.0	3.5 4.0	10.0 11.0	ns
t_{PHZ} t_{PLZ}	Output Disable Time S_n to I/O_n	2.5 1.5		6.0 5.5	1.5 1.0	7.0 6.5	2.5 1.5	7.0 6.5	ns

AC Operating Requirements

Symbol	Parameter	74F $T_A = +25°C$ $V_{CC} = +5.0V$		54F T_A, V_{CC} = Mil		74F T_A, V_{CC} = Com		Units
		Min	Max	Min	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW S_0 or S_1 to CP	8.5 8.5		10.0 7.5		8.5 8.5		ns
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW S_0 or S_1 to CP	0 0		0 0		0 0		
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW I/O_n, DS_0 or DS_7 to CP	5.0 5.0		5.0 5.0		5.0 5.0		ns
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW I/O_n, DS_0 or DS_7 to CP	2.0 2.0		2.0 2.0		2.0 2.0		
$t_w(H)$ $t_w(L)$	CP Pulse Width HIGH or LOW	5.0 5.0		5.0 5.0		5.0 5.0		ns
$t_w(L)$	$\overline{MR}$ Pulse Width, LOW	5.0		6.0		5.0		ns
t_{rec}	Recovery Time, $\overline{MR}$ to CP	7.0		12.0		7.0		ns

Ordering Information

The device number is used to form part of a simplified purchasing code where the package type and temperature range are defined as follows:

74F 299 S C X

Temperature Range Family
- 74F = Commercial
- 54F = Military

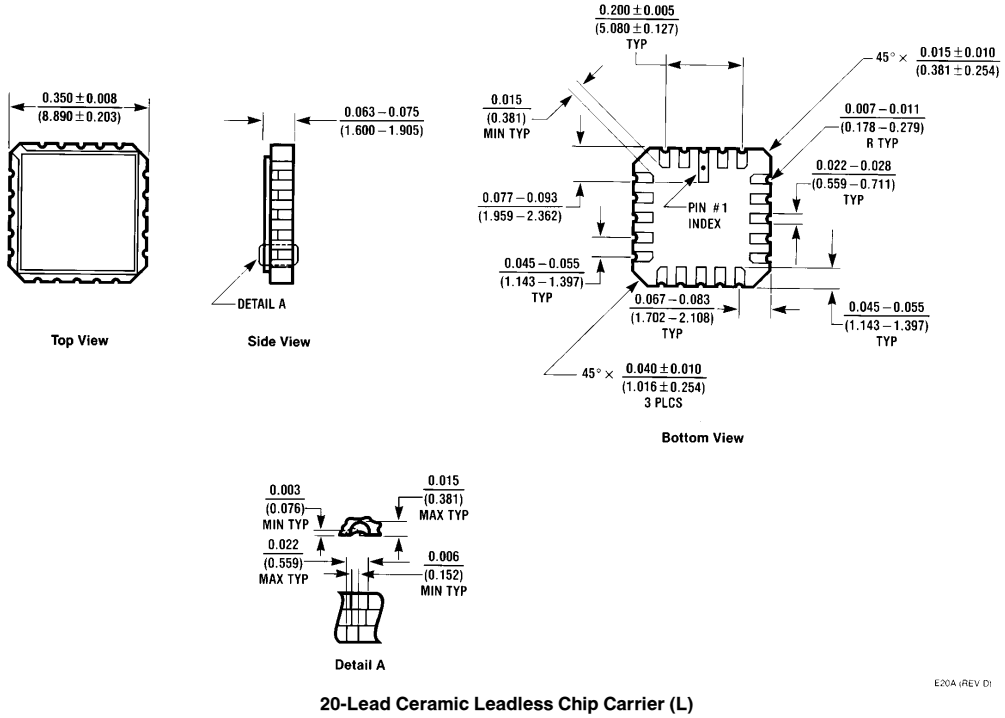
Device Type

Package Code
- P = Plastic DIP
- D = Ceramic DIP
- S = Small Outline SOIC JEDEC
- SJ = Small Outline SOIC EIAJ
- F = Flatpak
- L = Leadless Chip Carrier (LCC)

Temperature Range
- C = Commercial (0°C to +70°C)
- M = Military (−55°C to +125°C)

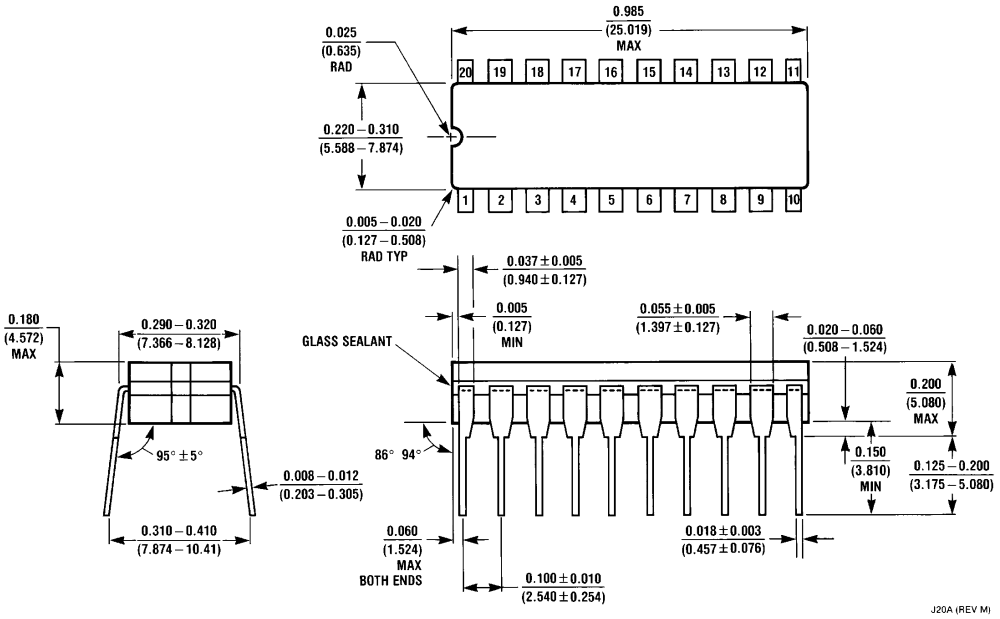
Special Variations
- QB = Military grade device with environmental and burn-in processing
- X = Devices shipped in 13″ reel

Physical Dimensions inches (millimeters)

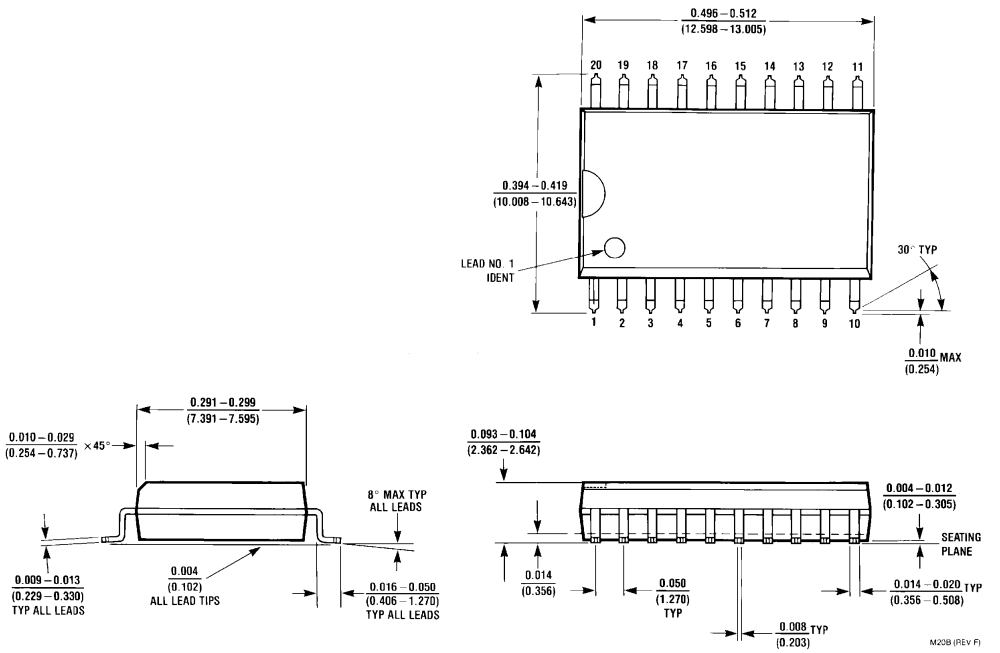


20-Lead Ceramic Leadless Chip Carrier (L)
NS Package Number E20A

Physical Dimensions inches (millimeters) (Continued)

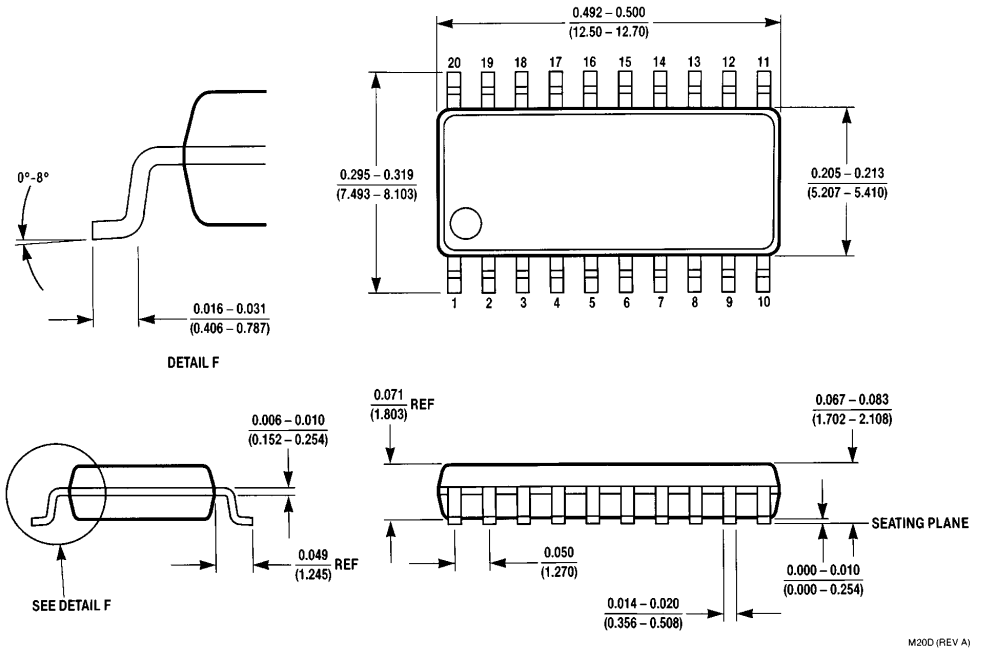


20-Lead Ceramic Dual-In-Line Package (D)
NS Package Number J20A

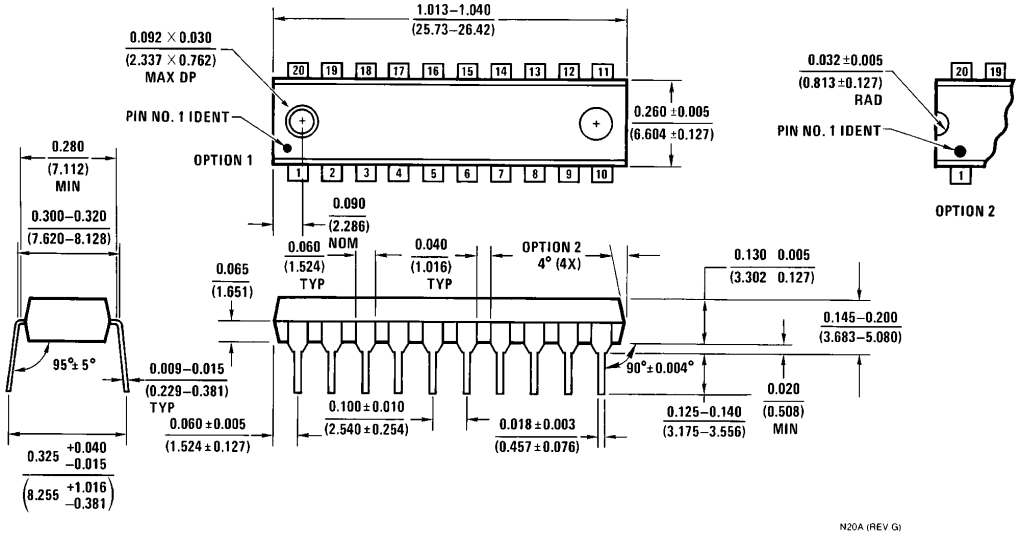


20-Lead (0.300″ Wide) Molded Small Outline Package, JEDEC (S)
NS Package Number M20B

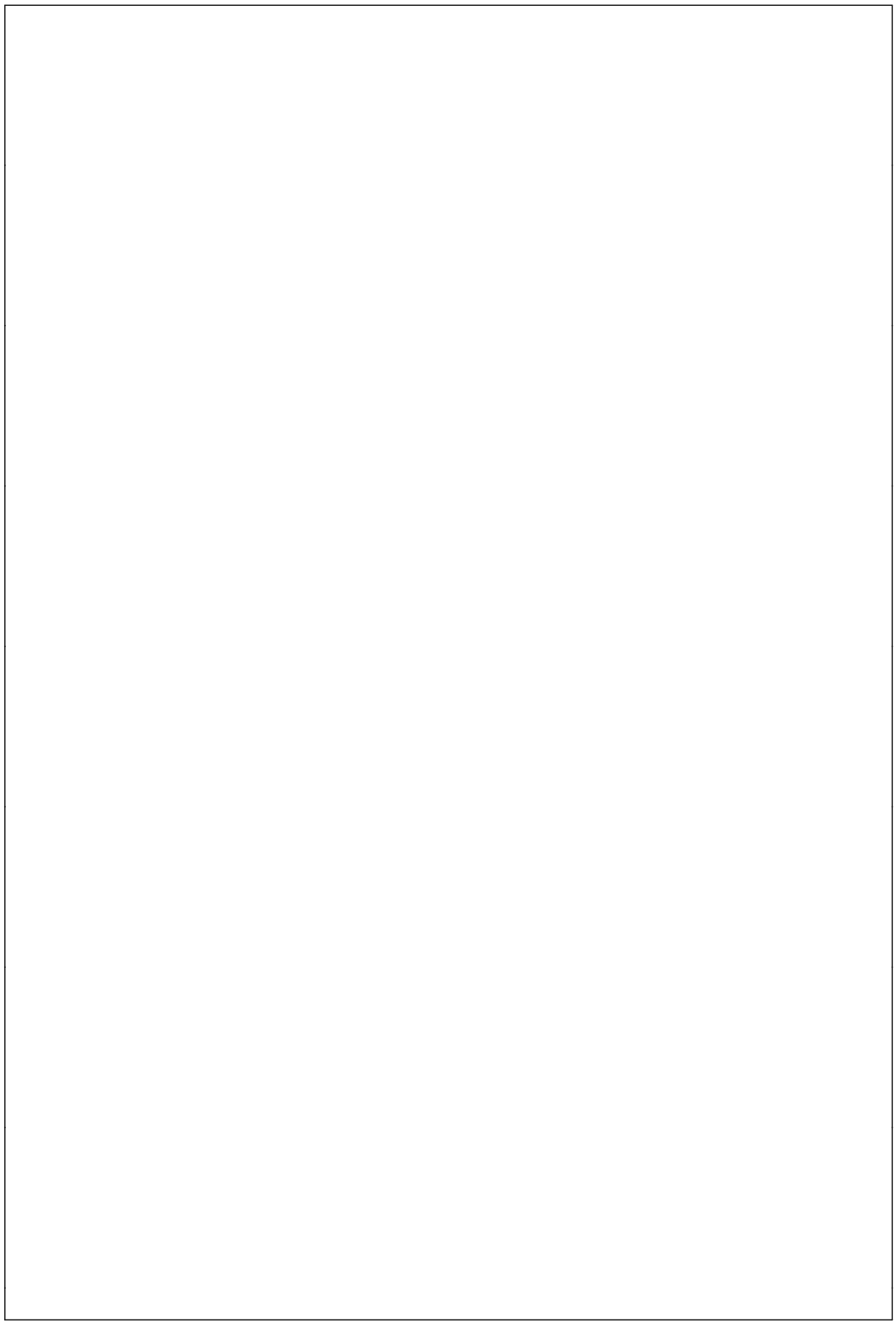
Physical Dimensions inches (millimeters) (Continued)



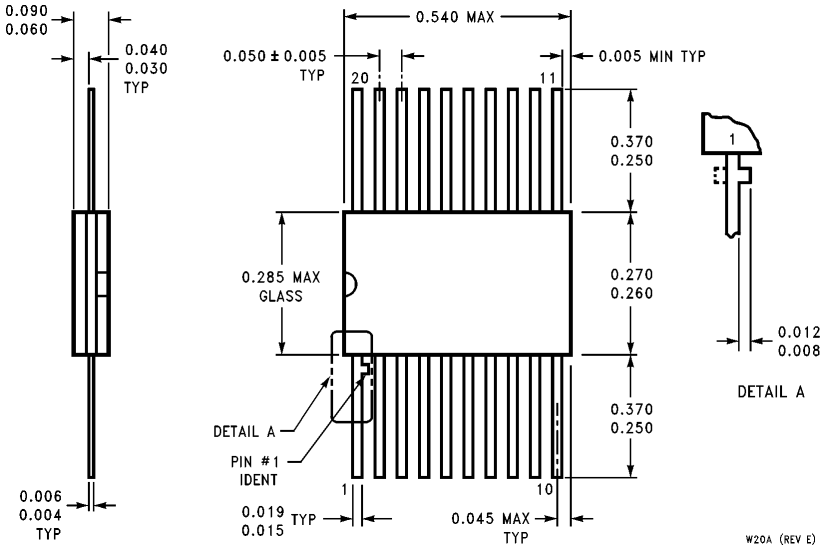
20-Lead (0.300″ Wide) Molded Small Outline Package, EIAJ (SJ)
NS Package Number MD20D



20-Lead (0.300″ Wide) Molded Dual-In-Line Package (P)
NS Package Number N20A



Physical Dimensions inches (millimeters) (Continued)



20-Lead Cerpack
NS Package Number W20A

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