GPIO ICs Series

Key Encoder IC

BU1851GUW

No.09098EAT03

●Description

Key Encoder IC can monitor up to 8x8 matrix (64 keys), which means to be adaptable to Qwerty keyboard. We adopt the architecture that the information of the only key which status is changed, like push or release, is encoded into the 8 bits data. This can greatly reduce the CPU load which tends to become heavier as the number of keys increase.
(Previously, all key's status is stored in the registers.)
Furthermore, auto sleep function contribute to low power consumption, when no keys are pressed. It is also equipped with the various functions such as ghost key rejection, N-key Rollover, Built-in power on reset and oscillator.

●Features

1) Monitor up to 64-matrix keys
2) Under 5μA Stand-by Current
3) Built-in Power On Reset
4) Ghost key rejection

●Absolute maximum ratings

(Ta=25℃)

Item	Symbol	Value	Unit	comment
Supply Voltage*1	VDD	-0.3 ~ +4.5	V	
Input voltage	VI	-0.3 ~ VDD +0.3*1	V	
Storage temperature range	Tstg	-55 ~ +125	℃	
Package power	PD	272*2	mW	

This IC is not designed to be X-ray proof.

*1 It is prohibited to exceed the absolute maximum ratings even including +0.3 V.

*2 Package dissipation will be reduced each 2.72mW/°C when the ambient temperature increases beyond 25°C.

●Operating Conditions

Item	Symbol	Limit			Unit	Condition
		Min	Typ	Max		
Supply voltage range（VDD）	VDD	2.20	3.30	3.60	V	
Input voltage range	V_{IN}	-0.2	-	VDD+0.2	V	
Operating temperature range	Topr	-30	25	+85	℃	
External clock	Fclk	0.8	1.0	1.2	MHz	CLKSEL=VDD
External resistor	Rxi	118.8	120	121.2	kΩ	To Xi pin, when CLKSEL=VSS

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● Package Specification

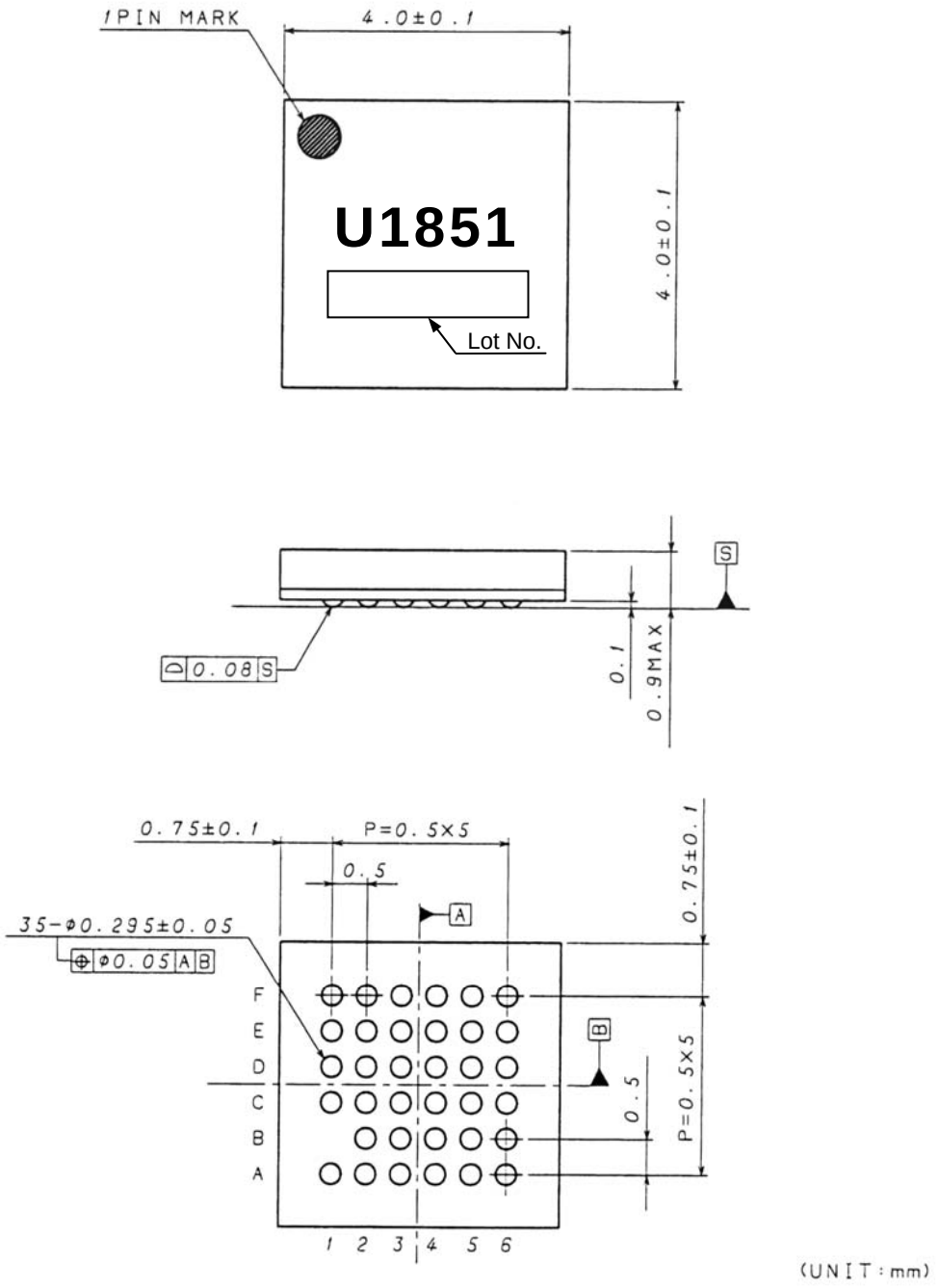


Fig.1 Package Specification（VBGA035W040）

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● Pin Assignment

	1	2	3	4	5	6
A	TESTM0	XRST	XO	XI	ROW0	TESTM3
B		CLKSEL	VDD	VDD	ROW2	ROW1
C	KINT	VDD	VSS	PORENB	ROW4	ROW3
D	KSDA	VDD	VSS	VSS	ROW6	ROW5
E	KSCL	COL6	COL4	COL2	COL0	ROW7
F	TESTM1	COL7	COL5	COL3	COL1	TESTM2

Fig.2 Pin Diagram（Top View）

● Block Diagram

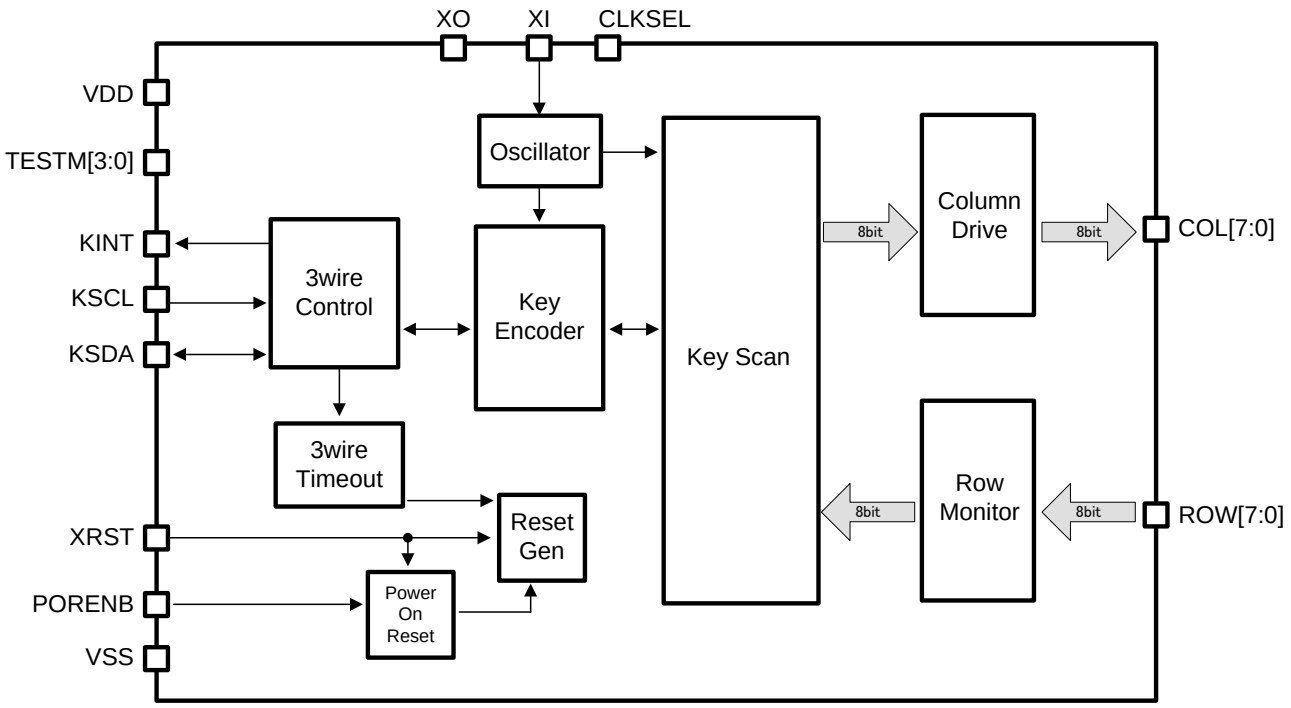


Fig.3 Functional Block Diagram

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● Pin-out Functional Descriptions

PIN name	I/O	Function	Init	Cell Type
VDD	-	Power supply (Core, I/O)	-	-
VSS	-	GND	-	-
XRST	I	Reset（Low Active）	I	A
CLKSEL	I	H: External clock is used L: Internal CR oscillator is used	I	B
XI	I	External clock input when “CLKSEL” is H. 120kΩ is attached up to VDD when “CLKSEL” is L.	I	G
XO	O	Test pin[*1]	L	C
KINT	O	Key Interrupt	H	C
KSCL	I	Clock for serial interface	I	A
KSDA	I/O	Serial data inout for serial interface	I	D
ROW0	I	Row input from key matrix (Pull-up)	I Pull-up	E
ROW1	I			
ROW2	I			
ROW3	I			
ROW4	I			
ROW5	I			
ROW6	I			
ROW7	I			
COL0	O	Column output to key matrix	L	C
COL1	O			
COL2	O			
COL3	O			
COL4	O			
COL5	O			
COL6	O			
COL7	O			
PORENB	I	Power on reset enable (Low Active)	I	B
TESTM0	I	Test Pin[*2]	I	F
TESTM1	I			
TESTM2	I			
TESTM3	I			

[*1] Note: This pin must be open in normal operation.
[*2] Note: All these pins must be tied down to GND in normal operation.

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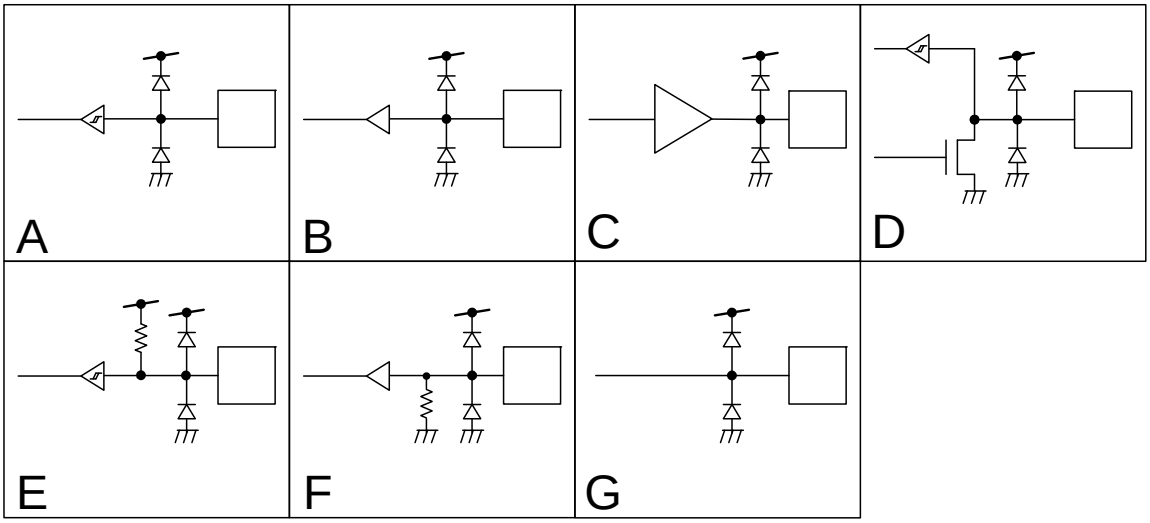


Fig.4 Equivalent IO circuit diagram

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● Functional Description

1. Power mode

The device enters the state of Power Down when XRST=”Low”. When XRST=High after powered, the device enters the standby state.

Power On Reset

A Power On Reset logic is implemented in this device. Therefore, it will operate correctly even if the XRST port is not used. In this case, the XRST port must be connected to high (VDD), and the PORENB port must be connected to low (VSS). If you don’t want to use Power On reset, you must connect PORENB port to high (VDD).

Power Down State

The device enters Power Down state by XRST=”Low”. An internal circuit is initialized, and key encoding and 3wire interface are invalid. Power On Reset becomes inactive during this state.

Stand-by State

The device enters the stand-by state by setting XRST to "High". In this state, the device is waiting for keys pressed. When a key is pressed, the state will change to operation. Power On Reset is active in this state if PORENB = low.

Operating State

The device enters the operating state by pressing keys. The device will scan the key matrix and encode the key code, and then the 3wire interface tries to start communication by driving KINT “Low”. See sec.2 for the details. After communicating with host device, when no keys are pressed, the device returns to the stand-by state. Power On Reset is active in this state if PORENB=low.

2. 3wire Interface

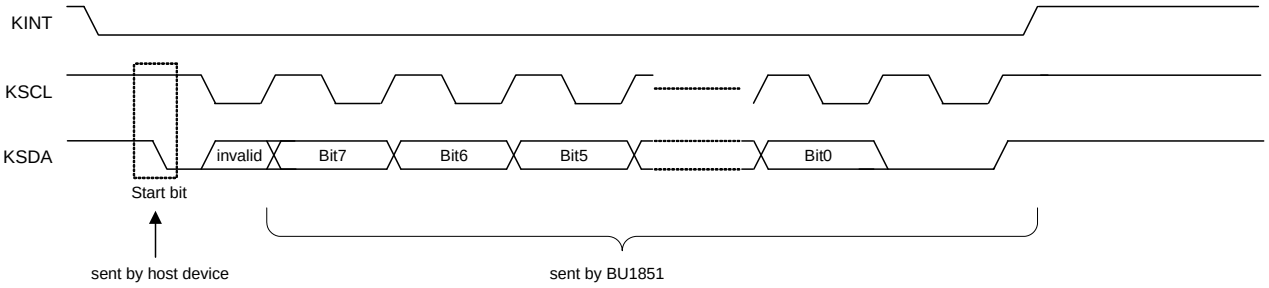


Fig.5 Protocol

Figure 5 shows the protocol of BU1851. BU1851 protocol basically consists of 3 wire configuration (KINT, KSCL, and KSDA) as shown above. Note that this 3wire interface is completely different from I2C and other standard bus interface.

Procedure

1. When BU1851 detects key events, KINT interrupt is generated to host with driving Low.
2. After the host detects KINT interrupt, the host is supposed to send start bit.
3. After BU1851 detects start bit, the 8bit data (key code) transmission on KSDA will start synchronized with the rising edge of KSCL clock signal, which is sent from the host.
4. 8 bit data are followed by “0” (9^{th} bit is always “0”), and then BU1851 drives High on KINT line.

timeout

Fig.6 shows the 3wire timeout sequence. It is suppose to happen when Host doesn’t response anything in a certain time.

1. bu1851 generates KINT interrupt.
2. But Host doesn’t response within 500ms.
3. BU1851 stops KINT, and tries to communicate again by generating KINT.
4. BU1851 will go into the stand-by state when the communication fails five times.

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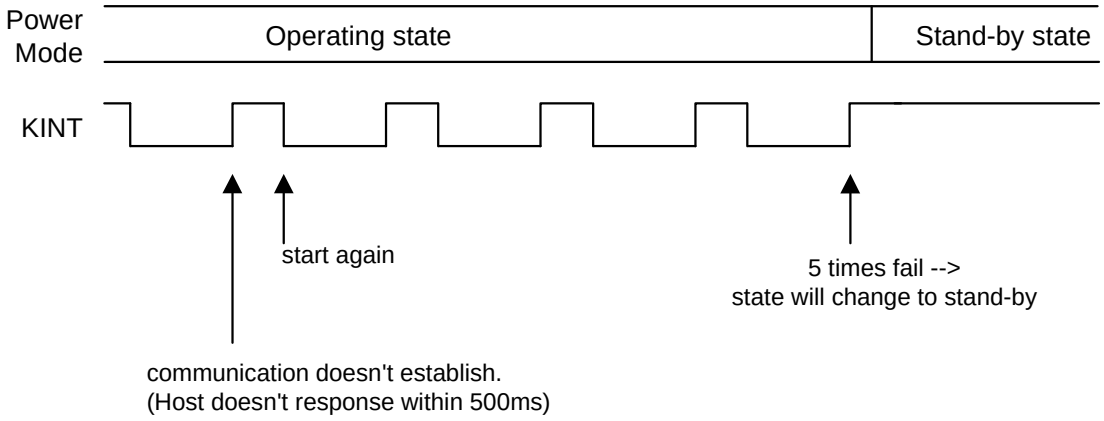


Fig.6 3wire timeout

See also “3wire interface AC characteristics”.

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3. Key code Assignment
Table 1 shows the key code assignment. These key codes are sent through KSDA line corresponding to the pushed or released keys as indicated in section 2.

Table.1 Key code

		ROW0	ROW1	ROW2	ROW3	ROW4	ROW5	ROW6	ROW7
COL0	M	0x01	0x11	0x21	0x31	0x41	0x51	0x61	0x71
	B	0x81	0x91	0xA1	0xB1	0xC1	0xD1	0xE1	0xF1
COL1	M	0x02	0x12	0x22	0x32	0x42	0x52	0x62	0x72
	B	0x82	0x92	0xA2	0xB2	0xC2	0xD2	0xE2	0xF2
COL2	M	0x03	0x13	0x23	0x33	0x43	0x53	0x63	0x73
	B	0x83	0x93	0xA3	0xB3	0xC3	0xD3	0xE3	0xF3
COL3	M	0x04	0x14	0x24	0x34	0x44	0x54	0x64	0x74
	B	0x84	0x94	0xA4	0xB4	0xC4	0xD4	0xE4	0xF4
COL4	M	0x05	0x15	0x25	0x35	0x45	0x55	0x65	0x75
	B	0x85	0x95	0xA5	0xB5	0xC5	0xD5	0xE5	0xF5
COL5	M	0x06	0x16	0x26	0x36	0x46	0x56	0x66	0x76
	B	0x86	0x96	0xA6	0xB6	0xC6	0xD6	0xE6	0xF6
COL6	M	0x07	0x17	0x27	0x37	0x47	0x57	0x67	0x77
	B	0x87	0x97	0xA7	0xB7	0xC7	0xD7	0xE7	0xF7
COL7	M	0x08	0x18	0x28	0x38	0x48	0x58	0x68	0x78
	B	0x88	0x98	0xA8	0xB8	0xC8	0xD8	0xE8	0xF8

M: Make Key (the code when the key is pressed)
B: Break Key (the code when the key is released)

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4. Ghost Key Rejection

Ghost key is an inevitable phenomenon as long as key-switch matrices are used. When three switches located at the corners of a certain matrix rectangle are pressed simultaneously, the switch that is located at the last corner of the rectangle (the ghost key) also appears to be pressed, even though the last key is not pressed. This occurs because the ghost key switch is electrically shorted by the combination of the other three switches (Fig.7). Because the key appears to be pressed electrically, it is impossible to distinguish which key is the ghost key and which key is pressed. The BU1851 solves the ghost key problem to use the simple method. If BU1851 detects any three-key combination that generates a fourth ghost key, and BU1851 does not report anything, indicating the ghost keys are ignored. This means that many combinations of three keys are also ignored when pressed at the same time. Applications requiring three-key combinations (such as <Ctrl><Alt><Del>) must ensure that the three keys are not wired in positions that define the vertices of a rectangle (Fig. 8). There is no limit on the number of keys that can be pressed simultaneously as long as the keys do not generate ghost key events.

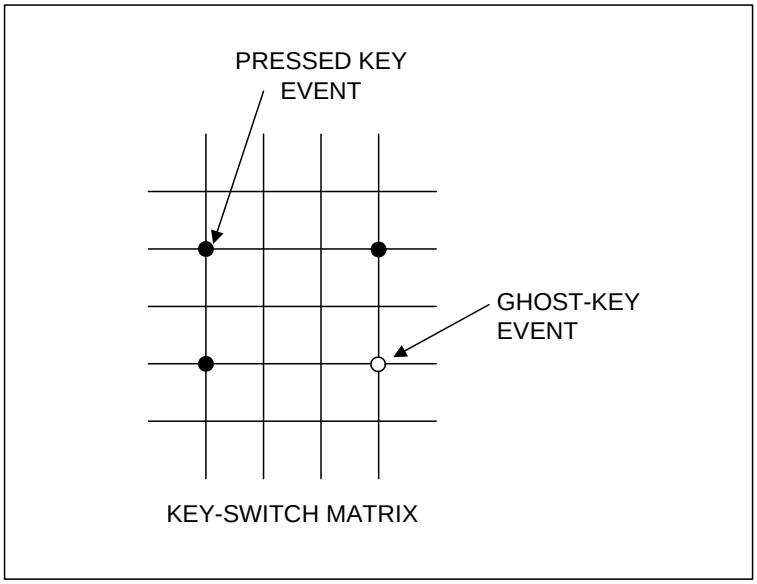


Fig.7 Ghost key phenomenon

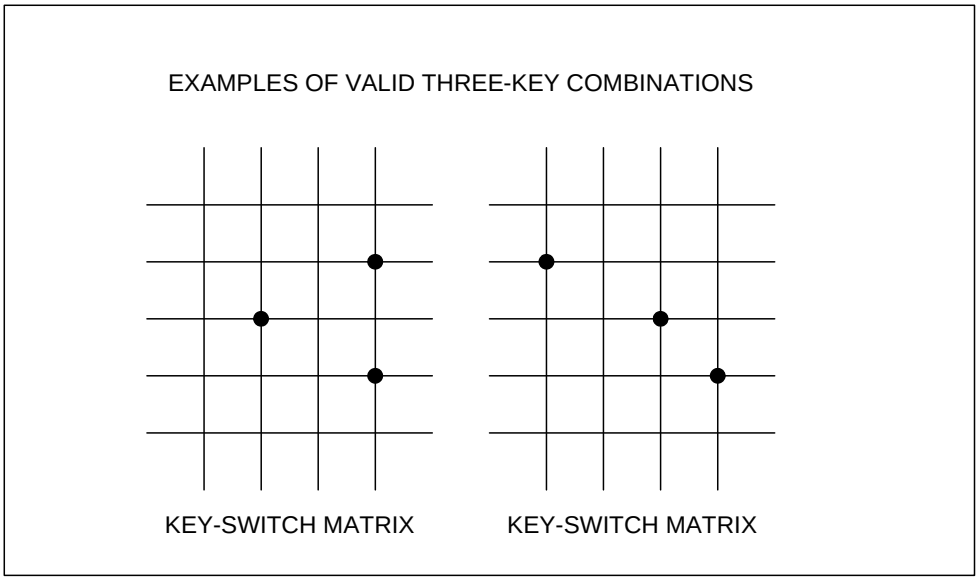


Fig.8 Valid three key combinations

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● 3wire Interface AC characteristics

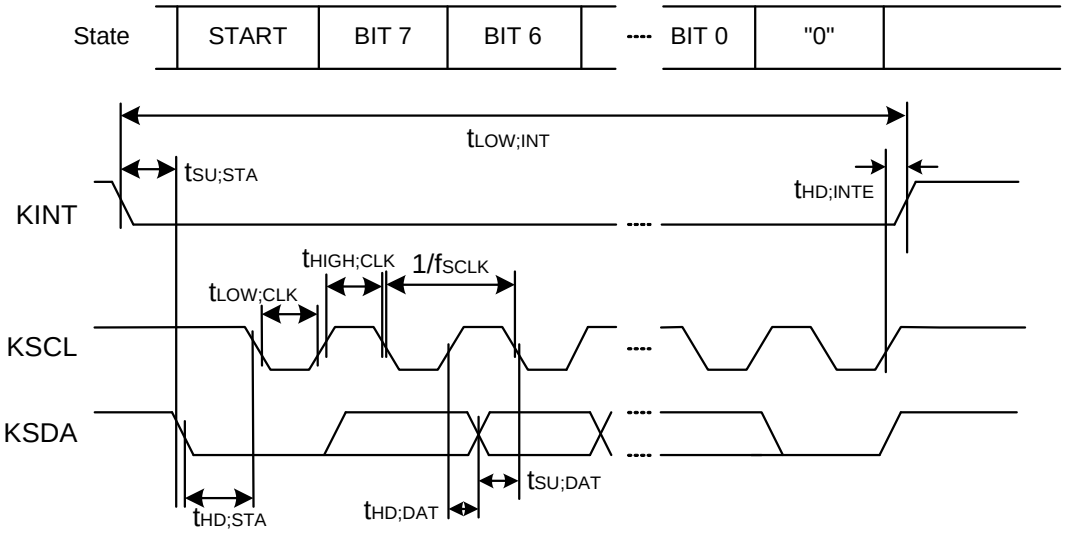


Fig.9 3wire interface AC timing

VDD=3.30V, Topr=25℃, CLKSEL=H (Sysclk = External Clock)

Item	Symbol	Min	Typ	Max	Unit	Condition
KSCL Clock Frequency	f_{SCLK}	-	-	21.5	kHz	
START Condition Setup Time	$t_{SU;STA}$	0.030	-	500	ms	
START Condition Hold Time	$t_{HD;STA}$	20	-	-	μs	
KSCL Low Time	$t_{LOW;CLK}$	23	-	-	μs	
KSCL High Time	$t_{HIGH;CLK}$	23	-	-	μs	
Data Setup Time	$t_{SU;DAT}$	$t_{HIGH;CLK}$ – (1/Sysclk)x12	-	$t_{HIGH;CLK}$ – (1/Sysclk)x10	μs	
Data Hold Time	$t_{HD;DAT}$	(1/Sysclk)x10	-	(1/Sysclk)x12	μs	
KINT End Hold Time	$t_{HD;INTE}$	(1/Sysclk)x3	-	(1/Sysclk)x5	μs	
KINT Low Time	$t_{LOW;INT}$	500	-	1200	ms	

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● Application circuit example

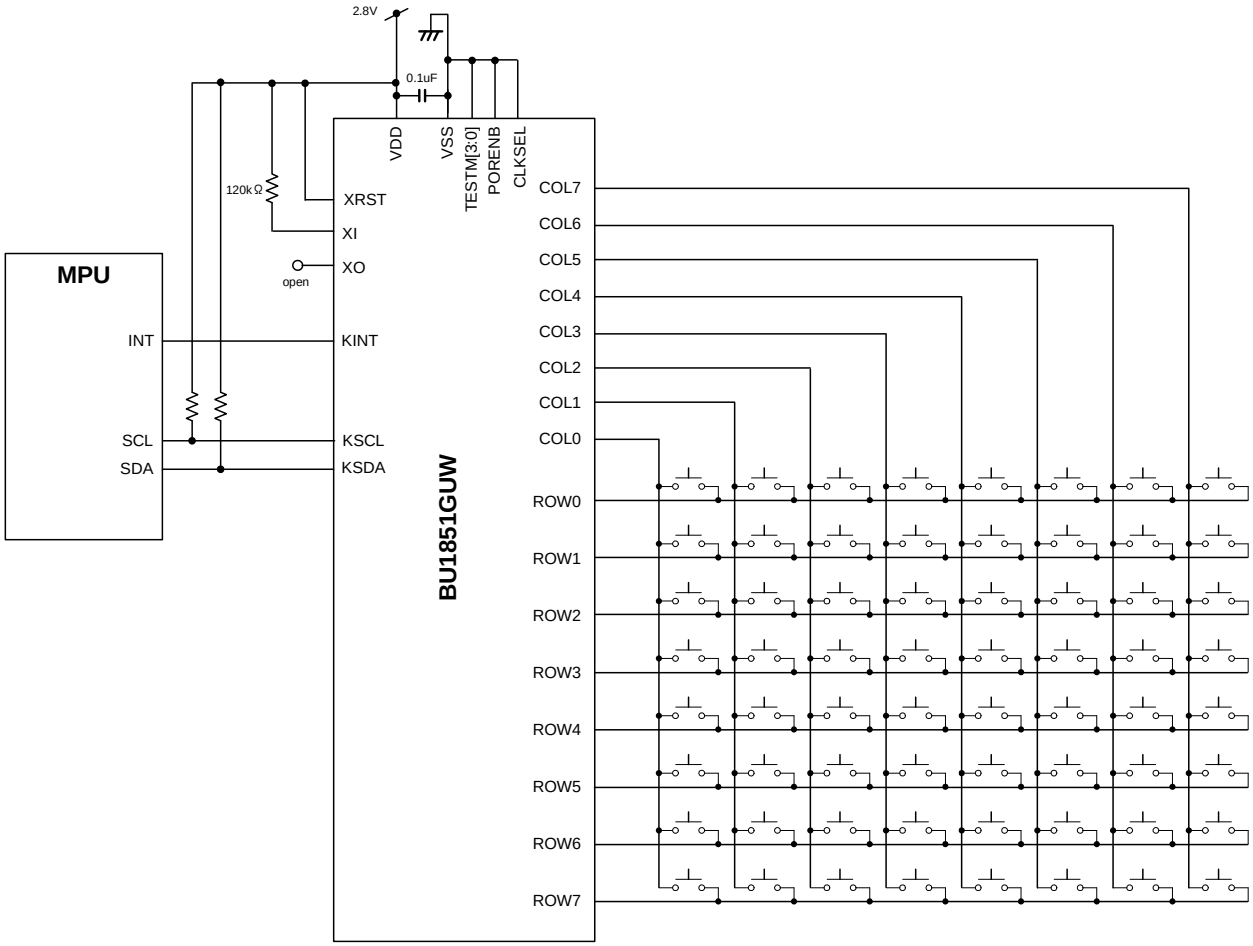


Fig. 10 Application circuit example

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●Ordering part number

B	U	1	8	5	1	G	U	W	-	E	2

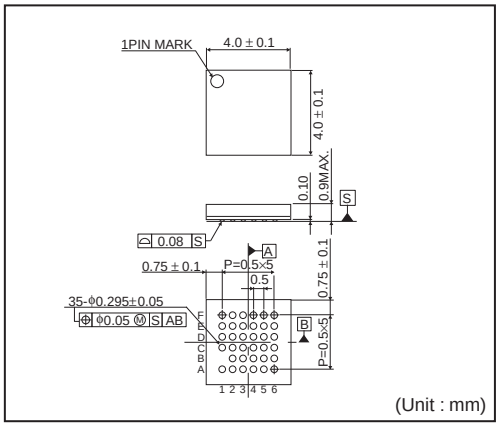
Part No. (BU)

Part No. (1851)

Package
GUW:
VBGA035W040

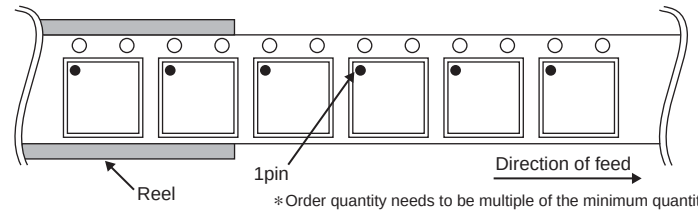
Packaging and forming specification
E2: Embossed tape and reel

VBGA035W040



<Tape and Reel information>

Tape	Embossed carrier tape (with dry pack)
Quantity	2500pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



∗Order quantity needs to be multiple of the minimum quantity.

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