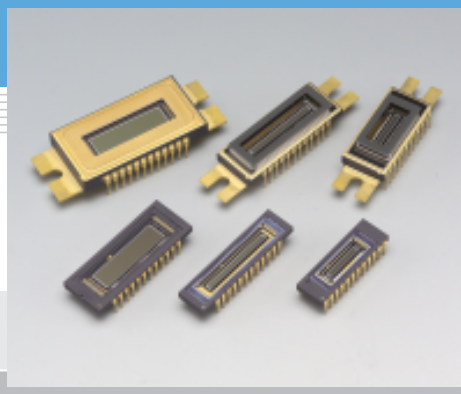


# CCD area image sensor S9970/S9971 series

Low dark signal · low readout noise/front-illuminated FFT-CCD



The S9970/S9971 series are families of FFT-CCD image sensors specifically designed for low-light-level detection in scientific applications. The S9970/S9971 series offer lower dark current and lower readout noise than the S7010/S7011 series that have been marketed. By using the binning operation, the S9970/S9971 series can be used as a linear image sensor having a long aperture in the direction of the device length. This makes the S9970/S9971 series ideally suited for use in spectrophotometry. The binning operation offers significant improvement in S/N and signal processing speed compared with conventional methods by which signals are digitally added by an external circuit. The S9970/S9971 series also feature low noise and low dark signal (MPP mode operation). This enables low-light-level detection and long integration time, thus achieving a wide dynamic range.

The S9970/S9971 series have an effective pixel size of  $24 \times 24 \mu\text{m}$  and are available in image areas ranging from  $12.288 \text{ (H)} \times 1.44 \text{ (V)} \text{ mm}^2$  ( $512 \times 60$  pixels) up to a large image area of  $24.576 \text{ (H)} \times 6.048 \text{ (V)} \text{ mm}^2$  ( $1024 \times 252$  pixels). S9970/S9971 series are pin compatible with S7010/S7011 series. (Operating conditions are a little bit changed from S7010/S7011 series.)

## Features

- Low dark signal:  $10 \text{ e}^-/\text{pixel/s}$  Typ. ( $0^\circ\text{C}$ , MPP mode)
- Low readout noise:  $4 \text{ e}^-_{\text{rms}}$  Typ.
- $512 \text{ (H)} \times 60 \text{ (V)}$  to  $1024 \text{ (H)} \times 252 \text{ (V)}$  pixel format
- Pixel size:  $24 \times 24 \mu\text{m}$
- Line/pixel binning
- 100 % fill factor
- Wide dynamic range
- MPP operation

## Applications

- Fluorescence spectrometer, ICP
- Raman spectrometer
- Industrial inspection requiring
- Semiconductor inspection
- DNA sequencer
- Low-light-level detection

## Selection guide

| Type no.   | Cooling             | Number of total pixels | Number of active pixels | Active area [mm (H) × mm (V)] | Applicable multichannel detector head |
|------------|---------------------|------------------------|-------------------------|-------------------------------|---------------------------------------|
| S9970-0906 | Non-cooled          | $532 \times 64$        | $512 \times 60$         | $12.288 \times 1.440$         | C7020                                 |
| S9970-1006 |                     | $1044 \times 64$       | $1024 \times 60$        | $24.576 \times 1.440$         |                                       |
| S9970-1007 |                     | $1044 \times 128$      | $1024 \times 124$       | $24.576 \times 2.976$         |                                       |
| S9970-1008 |                     | $1044 \times 256$      | $1024 \times 252$       | $24.576 \times 6.048$         |                                       |
| S9971-0906 | One-stage TE-cooled | $532 \times 64$        | $512 \times 60$         | $12.288 \times 1.440$         | C7021                                 |
| S9971-1006 |                     | $1044 \times 64$       | $1024 \times 60$        | $24.576 \times 1.440$         |                                       |
| S9971-1007 |                     | $1044 \times 128$      | $1024 \times 124$       | $24.576 \times 2.976$         |                                       |
| S9971-1008 |                     | $1044 \times 256$      | $1024 \times 252$       | $24.576 \times 6.048$         | C7025                                 |

## General ratings

| Parameter              | S9970 series                                       | S9971 series                                                       |
|------------------------|----------------------------------------------------|--------------------------------------------------------------------|
| Pixel size             | $24 \text{ (H)} \times 24 \text{ (V)} \mu\text{m}$ |                                                                    |
| Vertical clock phase   | 2-phase                                            |                                                                    |
| Horizontal clock phase | 2-phase                                            |                                                                    |
| Output circuit         | One-stage MOSFET source follower                   |                                                                    |
| Package                | 24 pin ceramic DIP (refer to dimensional outlines) |                                                                    |
| Window*1               | Quartz glass                                       | S9971-0906/-1006/-1007: sapphire<br>S9971-1008: AR-coated sapphire |

\*1: Temporary window type (ex. S9970-0906N) and UV coat type (ex. S9970-0906UV) are available upon request.  
(On the temporary window type, a window is temporarily attached by tape to protect the CCD chip and wires.)

■ Absolute maximum ratings (Ta=25 °C)

| Parameter                | Symbol       | Min. | Typ. | Max. | Unit |
|--------------------------|--------------|------|------|------|------|
| Operating temperature    | Topr         | -50  | -    | +30  | °C   |
| Storage temperature      | Tstg         | -50  | -    | +70  | °C   |
| OD voltage               | VOD          | -0.5 | -    | +25  | V    |
| RD voltage               | VRD          | -0.5 | -    | +18  | V    |
| ISV voltage              | VISV         | -0.5 | -    | +18  | V    |
| ISH voltage              | VISH         | -0.5 | -    | +18  | V    |
| IGV voltage              | VIG1V, VIG2V | -15  | -    | +15  | V    |
| IGH voltage              | VIG1H, VIG2H | -15  | -    | +15  | V    |
| SG voltage               | VSG          | -15  | -    | +15  | V    |
| OG voltage               | VOG          | -15  | -    | +15  | V    |
| RG voltage               | VRG          | -15  | -    | +15  | V    |
| TG voltage               | VTG          | -15  | -    | +15  | V    |
| Vertical clock voltage   | VP1V, VP2V   | -15  | -    | +15  | V    |
| Horizontal clock voltage | VP1H, VP2H   | -15  | -    | +15  | V    |

■ Operating conditions (MPP mode, Ta=25 °C)

| Parameter                               | Symbol       | Min.         | Typ. | Max. | Unit |
|-----------------------------------------|--------------|--------------|------|------|------|
| Output transistor drain voltage         | VOD          | 18           | 20   | 22   | V    |
| Reset drain voltage                     | VRD          | 11.5         | 12   | 12.5 | V    |
| Output gate voltage                     | VOG          | 1            | 3    | 5    | V    |
| Substrate voltage                       | VSS          | -            | 0    | -    | V    |
| Test point (vertical input source)      | VISV         | -            | VRD  | -    | V    |
| Test point (horizontal input source)    | VISH         | -            | VRD  | -    | V    |
| Test point (vertical input gate)        | VIG1V, VIG2V | -8           | 0    | -    | V    |
| Test point (horizontal input gate)      | VIG1H, VIG2H | -8           | 0    | -    | V    |
| Vertical shift register clock voltage   | High         | VP1VH, VP2VH | 0    | 4    | V    |
|                                         | Low          | VP1VL, VP2VL | -9   | -8   |      |
| Horizontal shift register clock voltage | High         | VP1HH, VP2HH | 0    | 4    | V    |
|                                         | Low          | VP1HL, VP2HL | -9   | -8   |      |
| Summing gate voltage                    | High         | VSGH         | 0    | 4    | V    |
|                                         | Low          | VSGL         | -9   | -8   |      |
| Reset gate voltage                      | High         | VRGH         | 0    | 4    | V    |
|                                         | Low          | VRGL         | -9   | -8   |      |
| Transfer gate voltage                   | High         | VTGH         | 0    | 4    | V    |
|                                         | Low          | VTGL         | -9   | -8   |      |
| External load resistance                | RL           | 20           | 22   | 24   | kΩ   |

■ Electrical characteristics (Ta=25 °C)

| Parameter                             | Symbol           | Min.    | Typ.    | Max. | Unit |
|---------------------------------------|------------------|---------|---------|------|------|
| Signal output frequency               | fc               | -       | 0.1     | 1    | MHz  |
| Vertical shift register capacitance   | S9970/S9971-0906 | -       | 750     | -    | pF   |
|                                       | S9970/S9971-1006 | -       | 1500    | -    |      |
|                                       | S9970/S9971-1007 | -       | 3000    | -    |      |
|                                       | S9970/S9971-1008 | -       | 6000    | -    |      |
| Horizontal shift register capacitance | S9970/S9971-0906 | -       | 100     | -    | pF   |
|                                       | S9970/S9971-1006 | -       | 180     | -    |      |
|                                       | S9970/S9971-1007 | -       | 180     | -    |      |
|                                       | S9970/S9971-1008 | -       | 180     | -    |      |
| Summing gate capacitance              | CSG              | -       | 7       | -    | pF   |
| Reset gate capacitance                | CRG              | -       | 7       | -    | pF   |
| Transfer gate capacitance             | S9970/S9971-0906 | -       | 60      | -    | pF   |
|                                       | S9970/S9971-1006 | -       | 100     | -    |      |
|                                       | S9970/S9971-1007 | -       | 100     | -    |      |
|                                       | S9970/S9971-1008 | -       | 100     | -    |      |
| Transfer efficiency*2                 | CTE              | 0.99995 | 0.99999 | -    | -    |
| DC output level                       | Vout             | 12      | 15      | 18   | V    |
| Output impedance                      | Zo               | -       | 5       | -    | kΩ   |
| Power dissipation*3                   | P                | -       | 15      | -    | mW   |

\*2: Charge transfer efficiency per pixel, measured at half of the full well capacity

\*3: Power dissipation of the on-chip amplifier plus load resistance

■ Electrical and optical characteristics (Ta=25 °C, unless otherwise noted)

| Parameter                       |                    | Symbol | Min.  | Typ.        | Max. | Unit                    |
|---------------------------------|--------------------|--------|-------|-------------|------|-------------------------|
| Saturation output voltage       |                    | Vsat   | -     | Fw × Sv     | -    | V                       |
| Full well capacity              | Vertical           | Fw     | 150   | 300         | -    | ke <sup>-</sup>         |
|                                 | Horizontal         |        | 300   | 600         | -    |                         |
| CCD node sensitivity*4          |                    | Sv     | -     | 3.5         | -    | μV/e <sup>-</sup>       |
| Dark current*5<br>(MPP mode)    | +25 °C             | DS     | -     | 200         | 3000 | e <sup>-</sup> /pixel/s |
|                                 | 0 °C               |        | -     | 10          | 150  |                         |
| Readout noise*6                 |                    | Nr     | -     | 4           | 18   | e <sup>-</sup> rms      |
| Dynamic range*7                 | Line binning       | DR     | 75000 | 150000      | -    | -                       |
|                                 | Area scanning      |        | 37500 | 75000       | -    |                         |
| Spectral response range         |                    | λ      | -     | 400 to 1100 | -    | nm                      |
| Photo response non-uniformity*8 |                    | PRNU   | -     | -           | ±10  | %                       |
| Blemish                         | Point defects*9    | -      | -     | -           | 0    | -                       |
|                                 | Cluster defects*10 |        | -     | -           | 0    |                         |
|                                 | Column defects*11  |        | -     | -           | 0    |                         |

\*4: VOD=20 V , Load resistance=22 kΩ

\*5: Dark current nearly doubles for every 5 to 7 °C increase in temperature.

\*6: -40 °C, operating frequency is 80 kHz.

\*7: Dynamic range (DR) = Full well capacity / Readout noise

\*8: Measured at one-half of the saturation output (full well capacity) using LED light (peak emission wavelength: 560 nm)

$$\text{Photo response non-uniformity} = \frac{\text{Fixed pattern noise (peak to peak)}}{\text{Signal}} \times 100 \quad [\%]$$

\*9: White spots

Pixels that generate dark current higher than 3% of the saturation. (Measured at 0 °C, Ts=1 s)

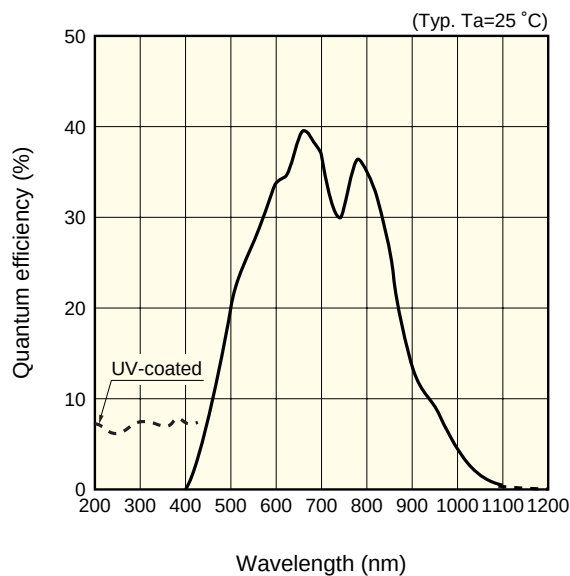
Black spots

Pixels whose sensitivity is lower than one-half of the average pixel output. (Measured with uniform light producing one-half of the saturation charge)

\*10: 2 to 9 contiguous defective pixels

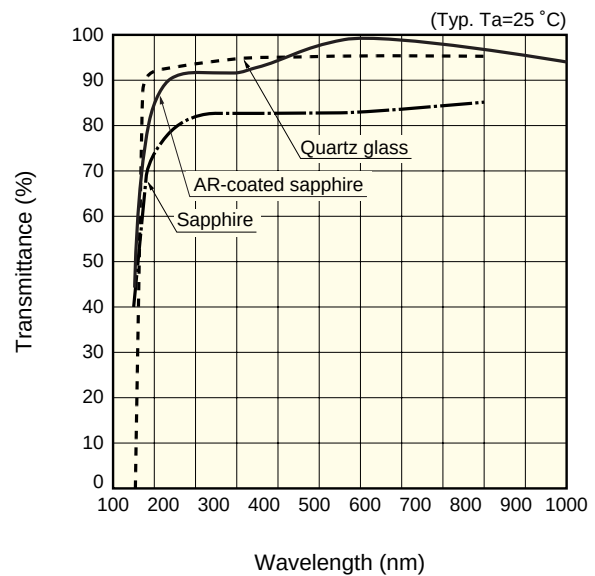
\*11: 10 or more contiguous defective pixels

■ Spectral response (without window)\*12



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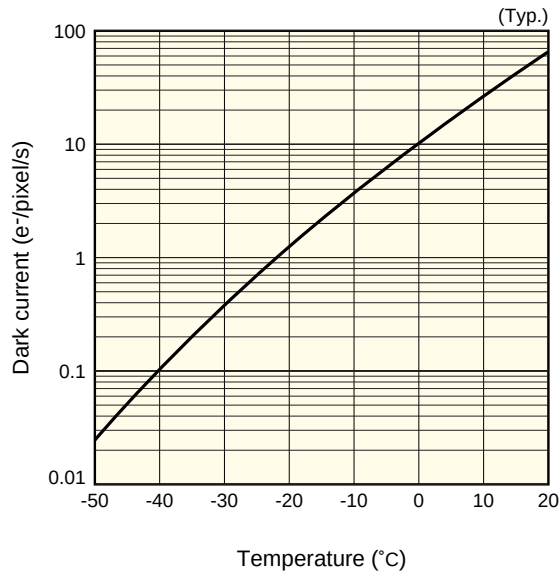
■ Spectral transmittance characteristics of window material



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\*12: Spectral response with sapphire or AR-coated sapphire is decreased according to the spectral transmittance characteristic of window material.

## ■ Dark current vs. temperature



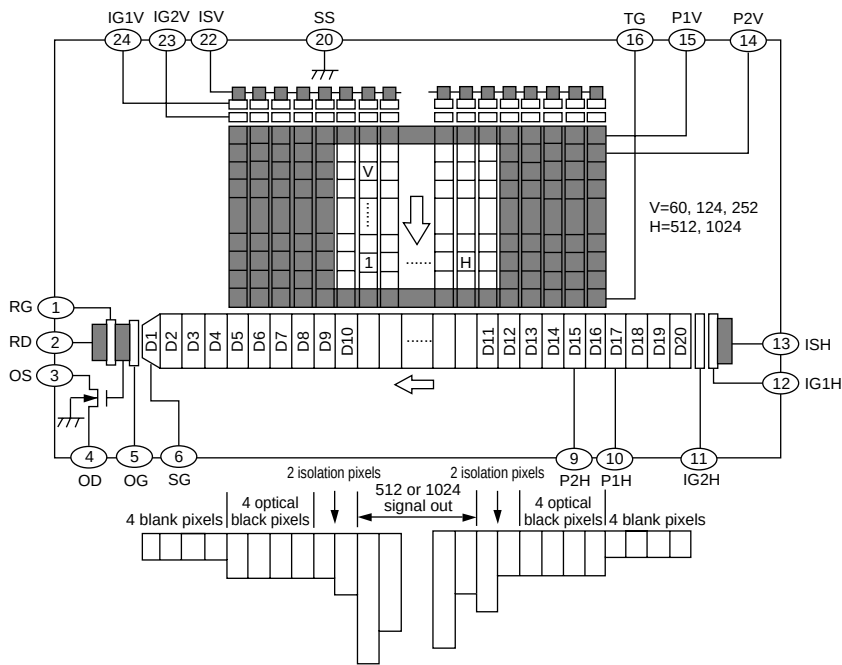
## ■ Window material

| Type No.               | Window material                                            |
|------------------------|------------------------------------------------------------|
| S9970 series           | Quartz glass* <sup>13</sup><br>(option: window-less)       |
| S9971-0906/-1006/-1007 | Sapphire* <sup>14</sup><br>(option: window-less)           |
| S9971-1008             | AR-coated sapphire* <sup>14</sup><br>(option: window-less) |

\*13: Resin sealing

\*14: Hermetic sealing

## ■ Device structure (conceptual drawing of top view in dimensional outlines)



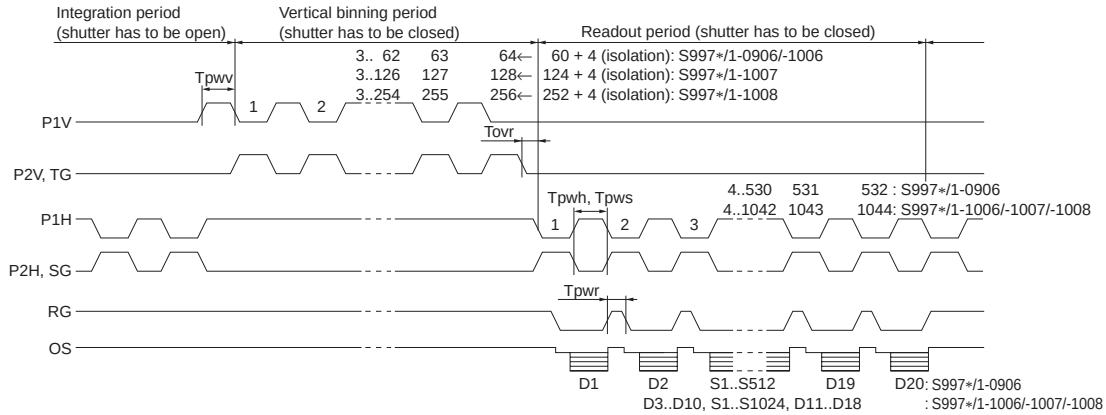
## Pixel format

| Left ← Horizontal Direction → Right |               |           |             |           |               |       |
|-------------------------------------|---------------|-----------|-------------|-----------|---------------|-------|
| Blank                               | Optical Black | Isolation | Effective   | Isolation | Optical Black | Blank |
| 4                                   | 4             | 2         | 512 or 1024 | 2         | 4             | 4     |

| Top ← Vertical Direction → Bottom |                |           |
|-----------------------------------|----------------|-----------|
| Isolation                         | Effective      | Isolation |
| 2                                 | 60, 124 or 252 | 2         |

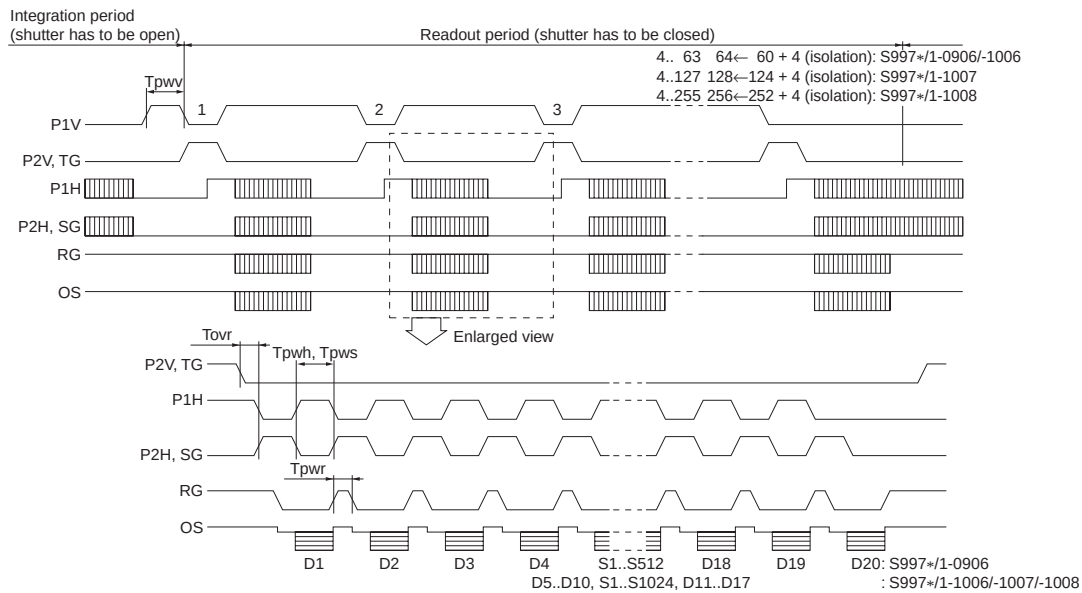
## ■ Timing chart

### Line binning



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### Area scanning (large full well mode)



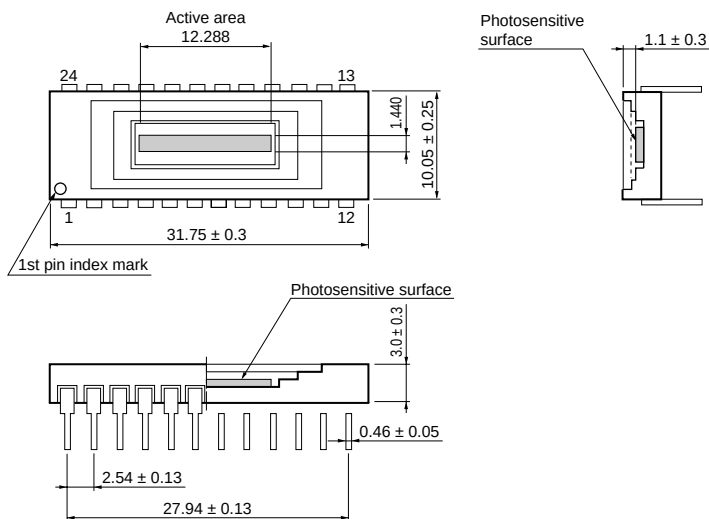
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| Parameter    |                        |                  | Symbol       | Min. | Typ. | Max. | Unit |
|--------------|------------------------|------------------|--------------|------|------|------|------|
| P1V, P2V, TG | Pulse width*15         | S9970/S9971-0906 | Tpww         | 1.5  | 4.5  | -    | μs   |
|              |                        | S9970/S9971-1006 |              | 3.0  | 9.0  | -    |      |
|              |                        | S9970/S9971-1007 |              | 6.0  | 18   | -    |      |
|              |                        | S9970/S9971-1008 |              | 12   | 36   | -    |      |
|              | Rise and fall times    |                  | Tprv, Tpfv   | 200  | -    | -    | ns   |
| P1H, P2H     | Pulse width            |                  | Tpwh         | 500  | 5000 | -    | ns   |
|              | Rise and fall times*15 |                  | Tprh, Tpfh   | 10   | -    | -    | ns   |
|              | Duty ratio             |                  | -            | -    | 50   | -    | %    |
| SG           | Pulse width            |                  | Tpws         | 500  | 5000 | -    | ns   |
|              | Rise and fall times    |                  | Tprs, Tpfss  | 10   | -    | -    | ns   |
|              | Duty ratio             |                  | -            | -    | 50   | -    | %    |
| RG           | Pulse width            |                  | Tpwr         | 100  | 500  | -    | ns   |
|              | Rise and fall times    |                  | Tprrr, Tpfrr | 5    | -    | -    | ns   |
| TG - P1H     | Overlap time           |                  | Tovrr        | 3    | 6    | -    | μs   |

\*15: Symmetrical clock pulses should be overlapped at 50% of maximum amplitude.

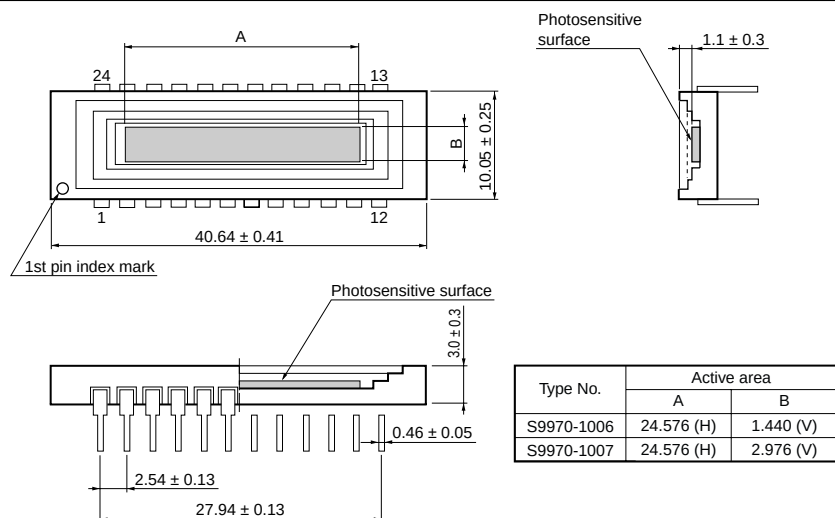
## ■ Dimensional outlines (unit: mm)

### S9970-0906



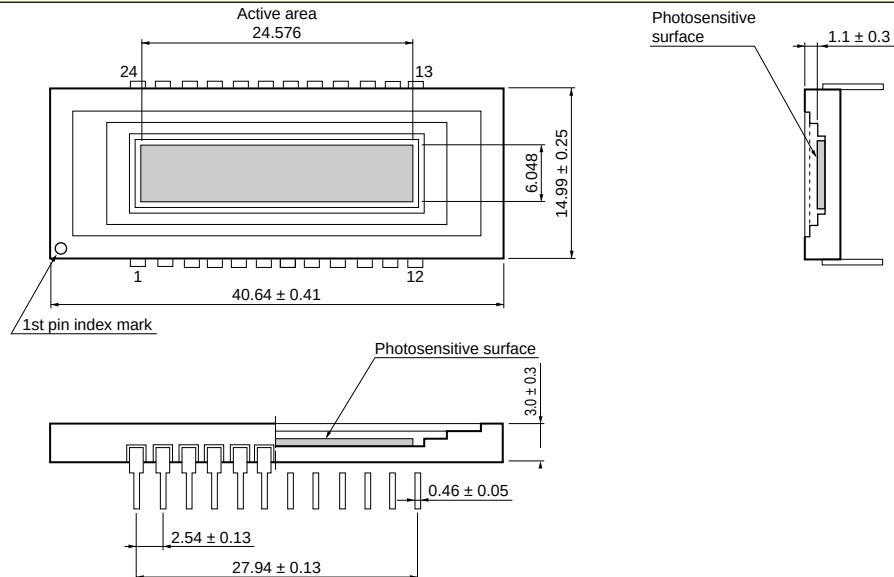
KMPDA0193EB

### S9970-1006/-1007



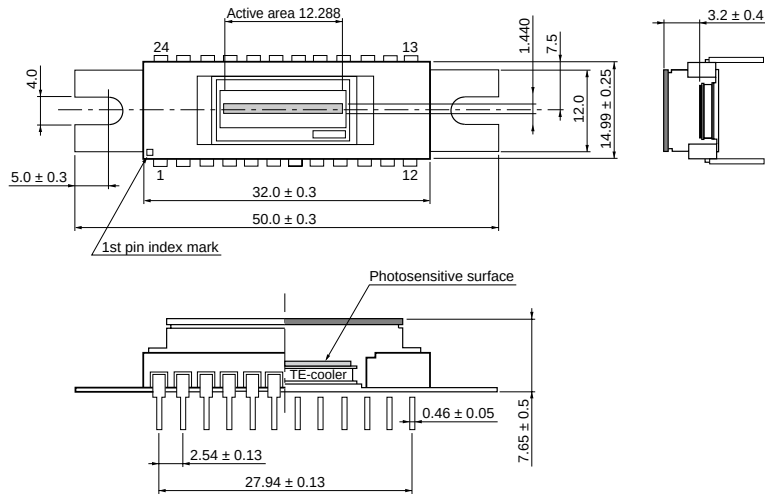
KMPDA0194EB

### S9970-1008



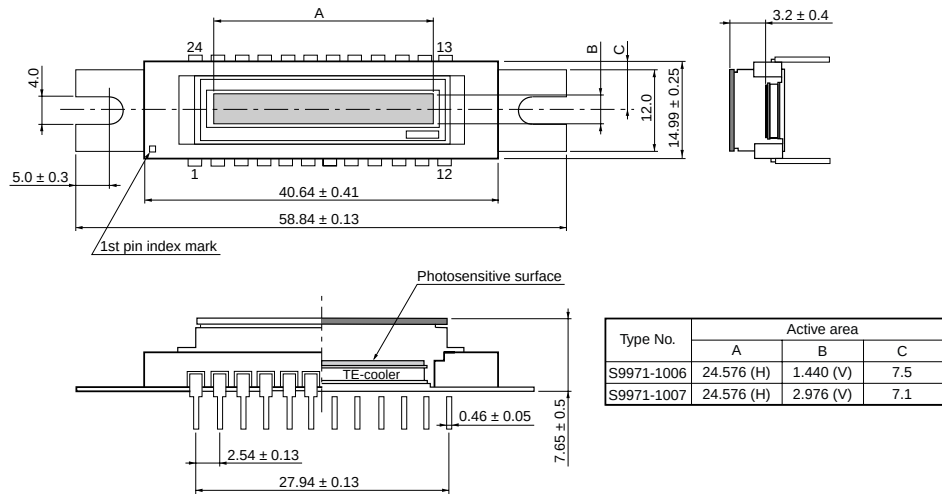
KMPDA0195EB

## S9971-0906



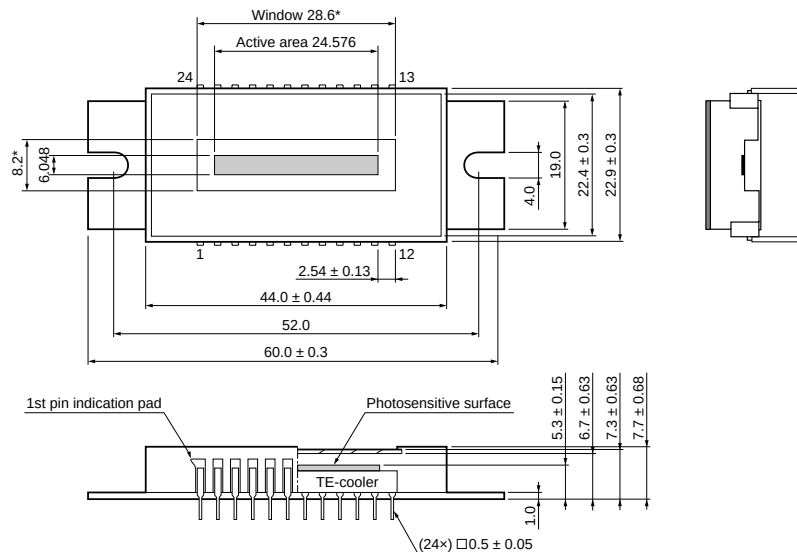
KMPDA0196EB

## S9971-1006/-1007



KMPDA0197EB

## S9971-1008



\* Size of window that guarantees the transmittance in the "Spectral transmittance characteristics of window material" graph

KMPDA0198EB

■ Pin connections

| Pin No. | S9970 series |                                      | S9971 series |                                      | Remark<br>(standard operation) |
|---------|--------------|--------------------------------------|--------------|--------------------------------------|--------------------------------|
|         | Symbol       | Description                          | Symbol       | Description                          |                                |
| 1       | RG           | Reset gate                           | RG           | Reset gate                           |                                |
| 2       | RD           | Reset drain                          | RD           | Reset drain                          | +12 V                          |
| 3       | OS           | Output transistor source             | OS           | Output transistor source             | RL=22 kΩ                       |
| 4       | OD           | Output transistor drain              | OD           | Output transistor drain              | +20 V                          |
| 5       | OG           | Output gate                          | OG           | Output gate                          | +3 V                           |
| 6       | SG           | Summing gate                         | SG           | Summing gate                         | Same timing as P2H             |
| 7       | -            |                                      | Th1          | Thermistor                           |                                |
| 8       | -            |                                      | Th2          | Thermistor                           |                                |
| 9       | P2H          | CCD horizontal register clock-2      | P2H          | CCD horizontal register clock-2      |                                |
| 10      | P1H          | CCD horizontal register clock-1      | P1H          | CCD horizontal register clock-1      |                                |
| 11      | IG2H         | Test point (horizontal input gate-2) | IG2H         | Test point (horizontal input gate-2) | 0 V                            |
| 12      | IG1H         | Test point (horizontal input gate-1) | IG1H         | Test point (horizontal input gate-1) | 0 V                            |
| 13      | ISH          | Test point (horizontal input source) | ISH          | Test point (horizontal input source) | Shorted to RD                  |
| 14      | P2V          | CCD vertical register clock-2        | P2V          | CCD vertical register clock-2        |                                |
| 15      | P1V          | CCD vertical register clock-1        | P1V          | CCD vertical register clock-1        |                                |
| 16      | TG*16        | Transfer gate                        | TG*16        | Transfer gate                        | Same timing as P2V             |
| 17      | -            |                                      | -            |                                      |                                |
| 18      | -            |                                      | P-           | TE-cooler-                           |                                |
| 19      | -            |                                      | P+           | TE-cooler+                           |                                |
| 20      | SS           | Substrate (GND)                      | SS           | Substrate (GND)                      | GND                            |
| 21      | -            |                                      | -            |                                      |                                |
| 22      | ISV          | Test point (vertical input source)   | ISV          | Test point (vertical input source)   | Shorted to RD                  |
| 23      | IG2V         | Test point (vertical input gate-2)   | IG2V         | Test point (vertical input gate-2)   | 0 V                            |
| 24      | IG1V         | Test point (vertical input gate-1)   | IG1V         | Test point (vertical input gate-1)   | 0 V                            |

\*16: TG is an isolation gate between vertical register and horizontal register. In standard operation, the same pulse as P2V should be applied to TG.

■ Specifications of built-in TE-cooler (Typ.)

| Parameter                       | Symbol           | Condition         | S9971-0906 | S9971-1006/-1007 | S9971-1008 | Unit |
|---------------------------------|------------------|-------------------|------------|------------------|------------|------|
| Internal resistance             | Rint             | Ta=25 °C          | 2.8        | 6.0              | 1.2        | Ω    |
| Maximum current*17              | I <sub>max</sub> | Tc*18=Th*19=25 °C | 1.5        | 1.5              | 3.0        | A    |
| Maximum voltage                 | V <sub>max</sub> | Tc*18=Th*19=25 °C | 4.4        | 8.8              | 3.6        | V    |
| Maximum heat absorption*20      | Q <sub>max</sub> |                   | 3.4        | 6.7              | 5.1        | W    |
| Maximum temperature of hot side | -                |                   | 70         |                  |            | °C   |

\*17: If the current is greater than I<sub>max</sub>, the heat absorption begins to decrease due to the Joule heat. It should be noted that this value is not a damage threshold. To protect the thermoelectric cooler and maintain stable operation, the supply current should be less than 60 % of this maximum current.

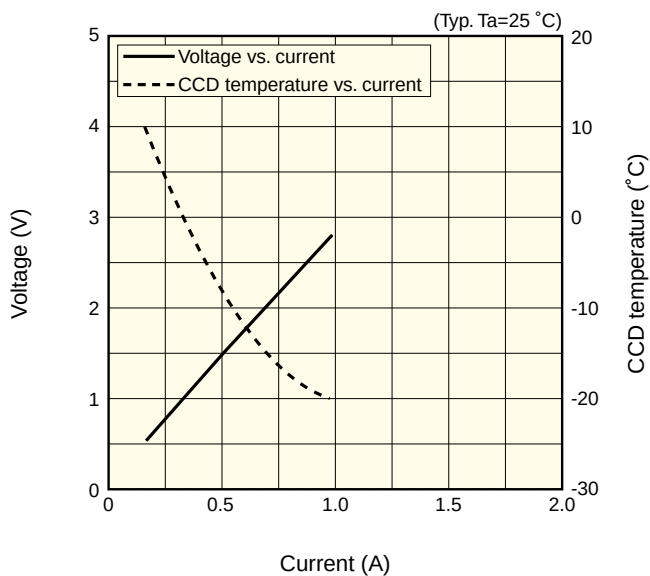
\*18: Temperature of cool side of thermoelectric cooler

\*19: Temperature of hot side of thermoelectric cooler

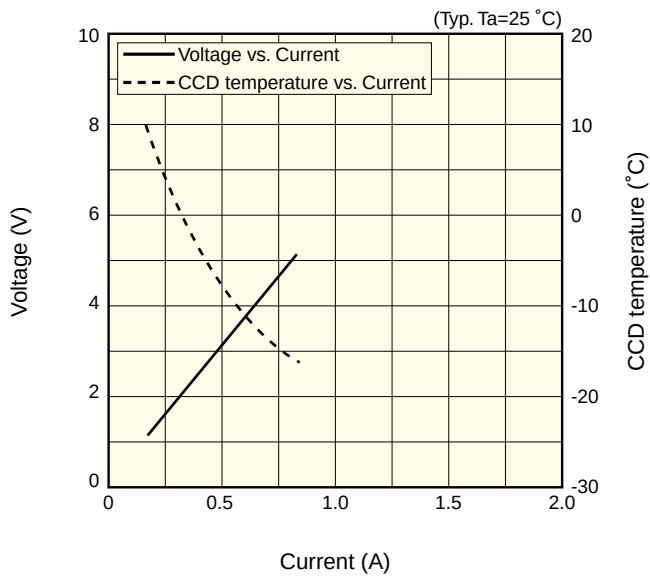
\*20: This is a heat absorption when the maximum current is supplied to the TE-cooler.

## TE-cooler characteristics

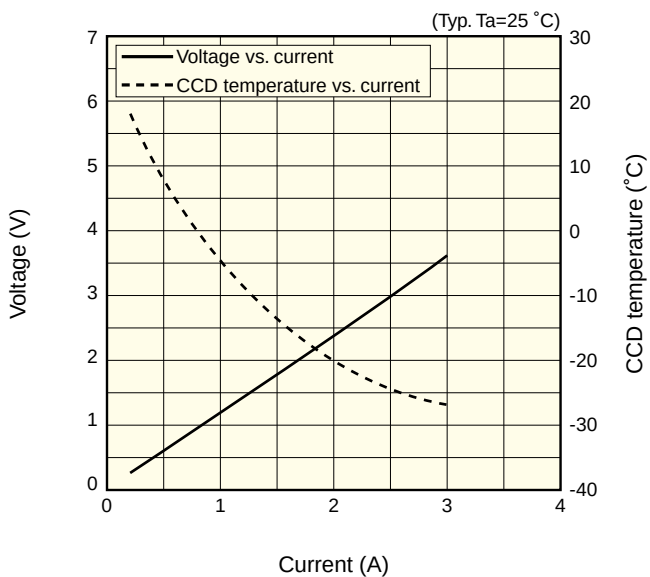
S9971-0906



S9971-1006/-1007



S9971-1008



## ■ Specifications of built-in temperature sensor

A chip thermistor is built in the same package with a CCD chip, and the CCD chip temperature can be monitored with it. A relation between the thermistor resistance and absolute temperature is expressed by the following equation.

$$R_{T1} = R_{T2} \times \exp B_{T1/T2} (1/T1 - 1/T2)$$

$R_{T1}$ : Resistance at absolute temperature  $T1$  [K]

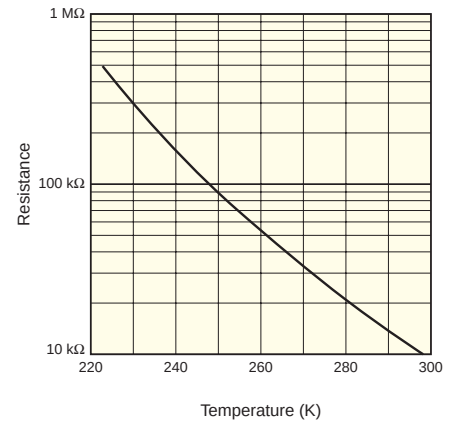
$R_{T2}$ : Resistance at absolute temperature  $T2$  [K]

$B_{T1/T2}$ : B constant [K]

The characteristics of the thermistor used are as follows.

$R_{298}=10\text{ k}\Omega$

$B_{298/323}=3450\text{ K}$



KMPD80111EB

## ■ Precaution for use (Electrostatic countermeasures)

- Handle these sensors with bare hands or wearing cotton gloves. In addition, wear anti-static clothing or use a wrist strap, in order to prevent electrostatic damage due to electrical charges from friction.
- Avoid directly placing these sensors on a work-desk or work-bench that may carry an electrostatic charge.
- Provide ground lines or ground connection with the work-floor, work-desk and work-bench to allow static electricity to discharge.
- Ground the tools used to handle these sensors, such as tweezers and soldering irons.

It is not always necessary to provide all the electrostatic measures stated above. Implement these measures according to the amount of damage that occurs.

## ■ Element cooling/heating temperature gradient rate

When using an external cooler, the element cooling/heating temperature gradient rate should be set at less than 5 K/min.

### Multichannel detector head (C7020, C7021, C7025)

#### Features

- C7020: for S9970 series
- C7021: for S9971-0906/-1006/-1007
- C7025: for S9971-1008
- Area scanning or full line-binning operation
- Readout frequency: 250 kHz
- Readout noise: 20 e<sup>-</sup>rms
- $\Delta T=50\text{ }^{\circ}\text{C}$  ( $\Delta T$  changes by radiation method.)

| Input          | Symbol      | Value                          |
|----------------|-------------|--------------------------------|
| Supply voltage | $V_{D1}$    | +5 Vdc, 200 mA                 |
|                | $V_{A1+}$   | +15 Vdc, +100 mA               |
|                | $V_{A1-}$   | -15 Vdc, -100 mA               |
|                | $V_{A2}$    | +24 Vdc, 30 mA                 |
|                | $V_{D2}$    | +5 Vdc, 30 mA (C7021, C7025)   |
|                | $V_p$       | +5 Vdc, 2.5 A (C7021, C7025)   |
|                | $V_F$       | +12 Vdc, 100 mA (C7021, C7025) |
| Master start   | $\phi_{ms}$ | HCMOS logic compatible         |
| Master clock   | $\phi_{mc}$ | HCMOS logic compatible, 1 MHz  |



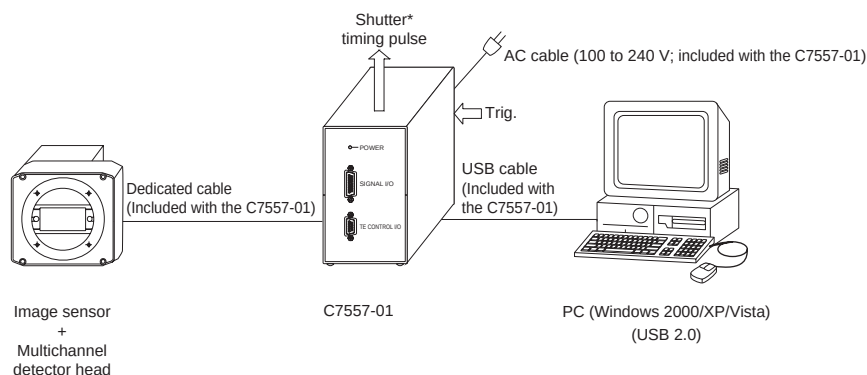
## Multichannel detector head controller

| Type no. | Interface | Photo                                                                             | Accessories                                                                                                                                                                                                                                                |
|----------|-----------|-----------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| S7557    | SCSI      |  | <ul style="list-style-type: none"> <li>·SCSI terminator</li> <li>·Fuse (2.5 A)</li> <li>·Detector head connection cable</li> <li>·AC cable</li> <li>·Software (compatible OS: Windows 98/ME*21)</li> <li>·Operation manual</li> </ul>                      |
| S7557-01 | USB2.0    |  | <ul style="list-style-type: none"> <li>·USB cable</li> <li>·Fuse (2.5 A)</li> <li>·Detector head connection cable</li> <li>·AC cable</li> <li>·Software (compatible OS: Windows 2000/XP/Vista)</li> <li>·Operation manual</li> <li>·MOS adapter</li> </ul> |

Note: SCSI cable and SCSI board (card) are not supplied with the C7557

\*21: This software may be run on Windows 2000/NT/XP with a simple task. For information on how to do this, please consult with our sales office.

### ■ Connection example



\* Shutter, etc. are not available.

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# HAMAMATSU

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