MJF18002 (See MJE18002)
MJF18004 (See MJE18004)
MJF18006 (See MJE18006)
MJF18008 (See MJE18008)

SCANSWITCH™

NPN Bipolar Power Deflection Transistor For High and Very High Resolution Monitors

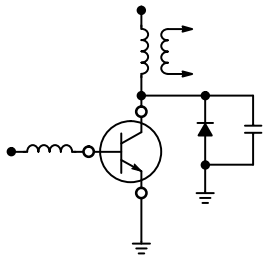
MJW16212*

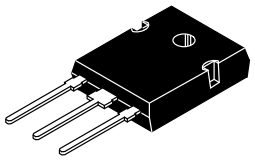
*Motorola Preferred Device

The MJW16212 is a state–of–the–art SWITCHMODE™ bipolar power transistor. It is specifically designed for use in horizontal deflection circuits for 20 mm diameter neck, high and very high resolution, full page, monochrome monitors.

- 1500 Volt Collector–Emitter Breakdown Capability
- Typical Dynamic Desaturation Specified (New Turn–Off Characteristic)
- Application Specific State–of–the–Art Die Design
- Fast Switching:
  200 ns Inductive Fall Time (Typ)
  2000 ns Inductive Storage Time (Typ)
- Low Saturation Voltage:
  0.15 Volts at 5.5 Amps Collector Current and 2.5 A Base Drive
- Low Collector–Emitter Leakage Current — 250 μA Max at 1500 Volts — V_{CES}
- High Emitter–Base Breakdown Capability For High Voltage Off Drive Circuits — 8.0 Volts (Min)

POWER TRANSISTOR
10 AMPERES
1500 VOLTS – V_{CES}
50 AND 150 WATTS





CASE 340F–03
TO–247AE

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Breakdown Voltage	V_{CES}	1500	Vdc
Collector–Emitter Sustaining Voltage	$V_{CEO(sus)}$	650	Vdc
Emitter–Base Voltage	V_{EBO}	8.0	Vdc
RMS Isolation Voltage (2) (for 1 sec, T_A = 25°C, Per Fig. 14 Rel. Humidity < 30%) Per Fig. 15	V_{ISOL}	 — —	V
Collector Current — Continuous — Pulsed (1)	I_C I_{CM}	10 15	Adc
Base Current — Continuous — Pulsed (1)	I_B I_{BM}	5.0 10	Adc
Maximum Repetitive Emitter–Base Avalanche Energy	W (BER)	0.2	mJ
Total Power Dissipation @ T_C = 25°C @ T_C = 100°C Derated above T_C = 25°C	P_D	150 39 1.49	Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	–55 to 125	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance — Junction to Case	$R_{\theta JC}$	0.67	°C/W
Lead Temperature for Soldering Purposes 1/8″ from the case for 5 seconds	T_L	275	°C

(1) Pulse Test: Pulse Width = 5.0 ms, Duty Cycle ≤ 10%.
(2) Proper strike and creepage distance must be provided.

Preferred devices are Motorola recommended choices for future use and best overall value.

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ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS (2)					
Collector Cutoff Current (V_{CE} = 1500 V, V_{BE} = 0 V) (V_{CE} = 1200 V, V_{BE} = 0 V)	I_{CES}	— —	— —	250 25	μAdc
Emitter–Base Leakage (V_{EB} = 8.0 Vdc, I_C = 0)	I_{EBO}	—	—	25	μAdc
Emitter–Base Breakdown Voltage (I_E = 1.0 mA, I_C = 0)	$V_{(BR)EBO}$	8.0	11	—	Vdc
Collector–Emitter Sustaining Voltage (Table 1) (I_C = 10 mAdc, I_B = 0)	$V_{CEO(sus)}$	650	—	—	Vdc
ON CHARACTERISTICS (2)					
Collector–Emitter Saturation Voltage (I_C = 5.5 Adc, I_B = 2.2 Adc) (I_C = 3.0 Adc, I_B = 400 mAdc)	$V_{CE(sat)}$	— —	0.15 0.14	1.0 1.0	Vdc
Base–Emitter Saturation Voltage (I_C = 5.5 Adc, I_B = 2.2 Adc)	$V_{BE(sat)}$	—	0.9	1.5	Vdc
DC Current Gain (I_C = 1.0 A, V_{CE} = 5.0 Vdc) (I_C = 10 A, V_{CE} = 5.0 Vdc)	h_{FE}	— 4.0	24 6.0	— 10	—
DYNAMIC CHARACTERISTICS					
Dynamic Desaturation Interval (I_C = 5.5 A, I_{B1} = 2.2 A, LB = 1.5 μH)	t_{ds}	—	350	—	ns
Output Capacitance (V_{CE} = 10 Vdc, I_E = 0, f_{test} = 100 kHz)	C_{ob}	—	180	350	pF
Gain Bandwidth Product (V_{CE} = 10 Vdc, I_C = 0.5 A, f_{test} = 1.0 MHz)	f_T	—	2.75	—	MHz
Emitter–Base Turn–Off Energy ($EB_{(avalanche)}$ = 500 ns, R_{BE} = 22 Ω)	$EB_{(off)}$	—	35	—	μJ
Collector–Heatsink Capacitance — MJF16212 Isolated Package (Mounted on a 1″ x 2″ x 1/16″ Copper Heatsink, V_{CE} = 0, f_{test} = 100 kHz)	$C_{c–hs}$	—	5.0	—	pF
SWITCHING CHARACTERISTICS					
Inductive Load (I_C = 5.5 A, I_B = 2.2 A), High Resolution Deflection Simulator Circuit Table 2 Storage Fall Time	 t_{sv} t_{fi}	 — —	 2000 200	 4000 350	ns

(2) Pulse Test: Pulse Width = 300 μs, Duty Cycle ≤ 2.0%.

SAFE OPERATING AREA

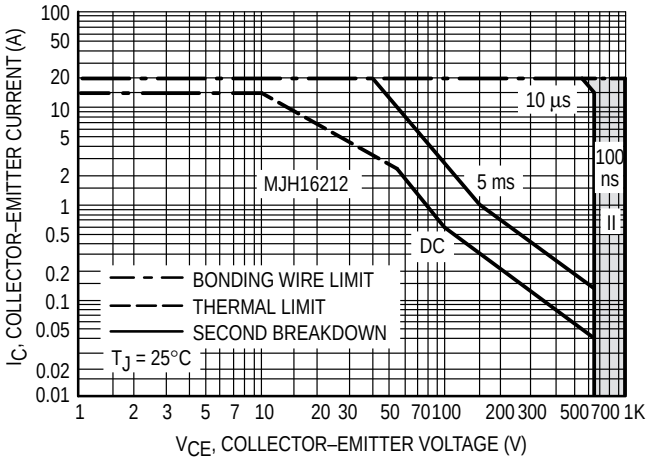


Figure 1. Maximum Forward Bias Safe Operating Area

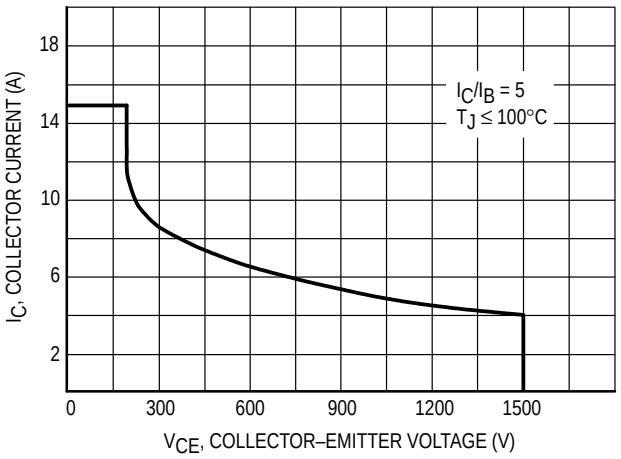


Figure 2. Maximum Reverse Bias Safe Operating Area

SAFE OPERATING AREA (continued)

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 1 is based on $T_C = 25°C$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25°C$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 1 may be found at any case temperature by using the appropriate curve on Figure 3.

At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

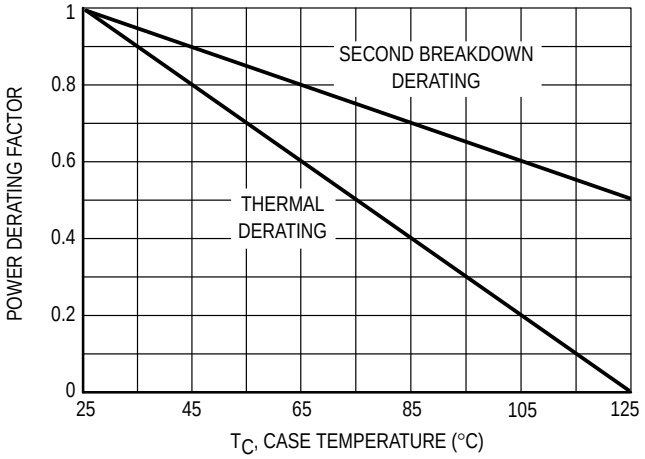


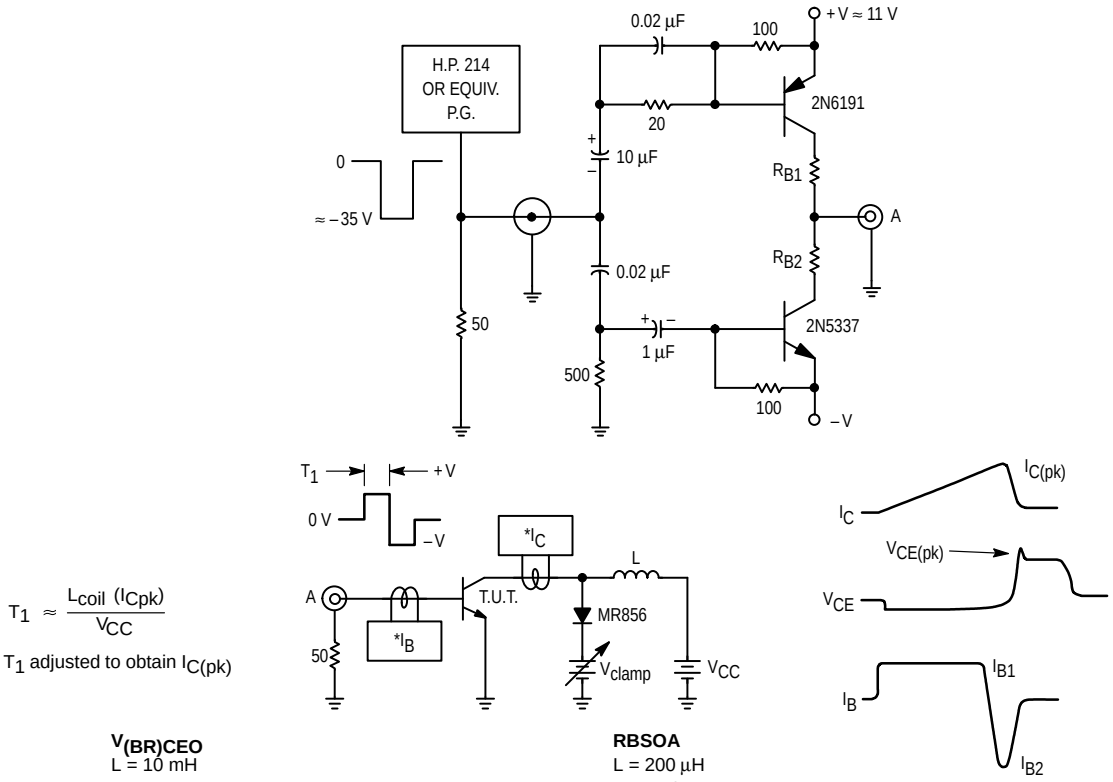
Figure 3. Power Derating

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn–off, in most cases, with the base–to–emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc.

The safe level for these devices is specified as Reverse Biased Safe Operating Area and represents the voltage–current condition allowable during reverse biased turnoff. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 2 gives the RBSOA characteristics.

Table 1. RBSOA/$V_{(BR)CEO(SUS)}$ Test Circuit



$$T_1 \approx \frac{L_{coil}\ (I_{Cpk})}{V_{CC}}$$

T_1 adjusted to obtain $I_{C(pk)}$

$V_{(BR)CEO}$
L = 10 mH
$R_{B2} = \infty$
V_{CC} = 20 Volts

*Tektronix
P–6042 or
Equivalent

RBSOA
L = 200 µH
$R_{B2} = 0$
V_{CC} = 20 Volts
R_{B1} selected for desired I_{B1}

Note: Adjust –V to obtain desired $V_{BE(off)}$ at Point A.

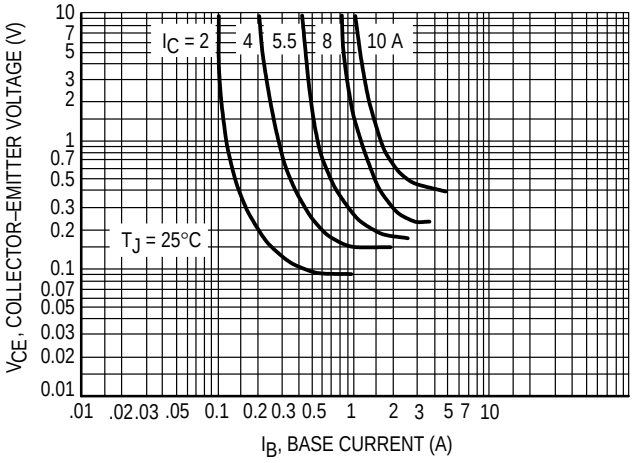


Figure 4. Typical Collector–Emitter Saturation Region

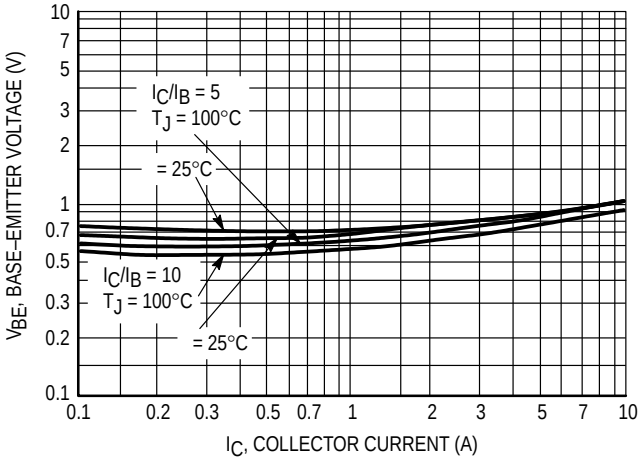


Figure 5. Typical Emitter–Base Saturation Voltage

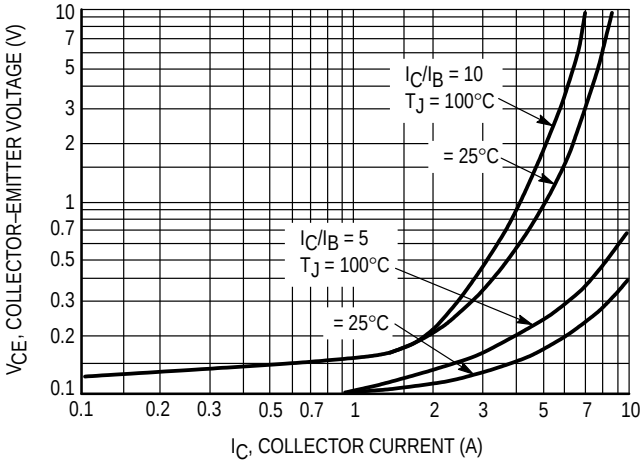


Figure 6. Typical Collector–Emitter Saturation Voltage

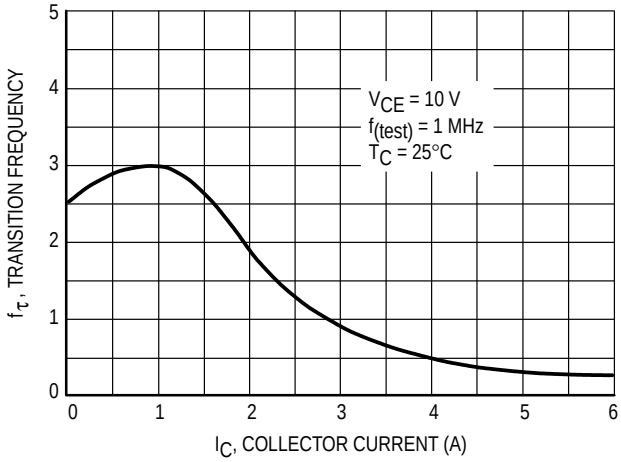


Figure 7. Typical Transition Frequency

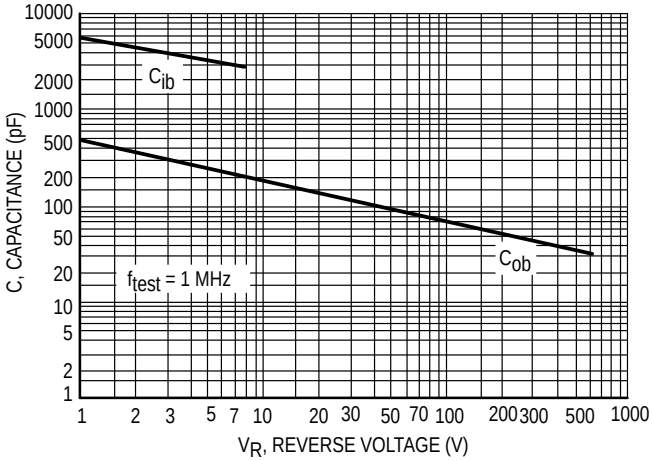
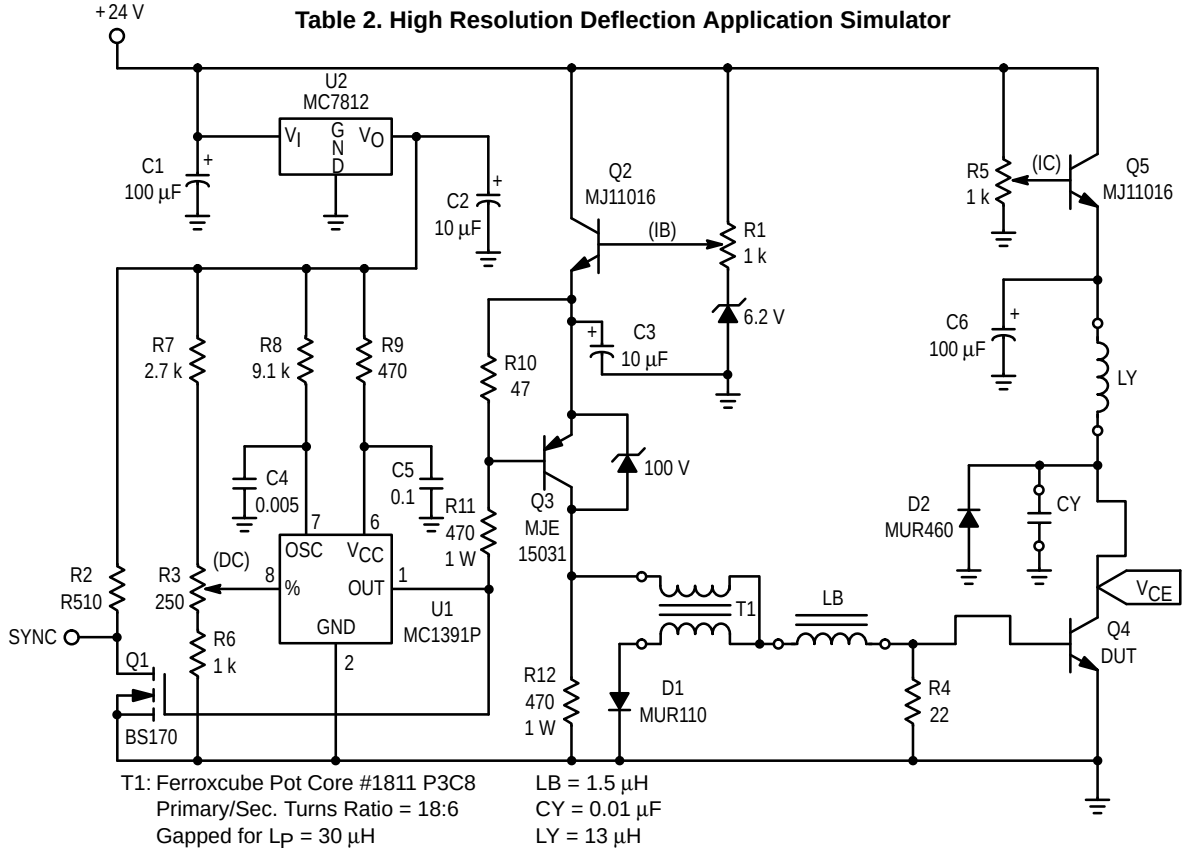


Figure 8. Typical Capacitance

DYNAMIC DESATURATIION

The SCANSWITCH series of bipolar power transistors are specifically designed to meet the unique requirements of horizontal deflection circuits in computer monitor applications. Historically, deflection transistor design was focused on minimizing collector current fall time. While fall time is a valid figure of merit, a more important indicator of circuit performance as scan rates are increased is a new characteristic, “dynamic desaturation.” In order to assure a linear collector current ramp, the output transistor must remain in hard saturation during storage time and exhibit a rapid turn–off transition. A sluggish transition results in serious consequences. As the saturation voltage of the output transistor increases, the voltage across the yoke drops. Roll off in the collector current ramp results in improper beam deflection and distortion of the image at the right edge of the screen. Design changes have been made in the structure of the SCANSWITCH series of devices which minimize the dynamic desaturation interval. Dynamic desaturation has been defined in terms of the time required for the V_{CE} to rise from 1.0 to 5.0 volts (Figures 9 and 10) and typical performance at optimized drive conditions has been specified. Optimization of device structure results in a linear collector current ramp, excellent turn–off switching performance, and significantly lower overall power dissipation.

Table 2. High Resolution Deflection Application Simulator



T1: Ferroxcube Pot Core #1811 P3C8
Primary/Sec. Turns Ratio = 18:6
Gapped for L_P = 30 µH

LB = 1.5 µH
CY = 0.01 µF
LY = 13 µH

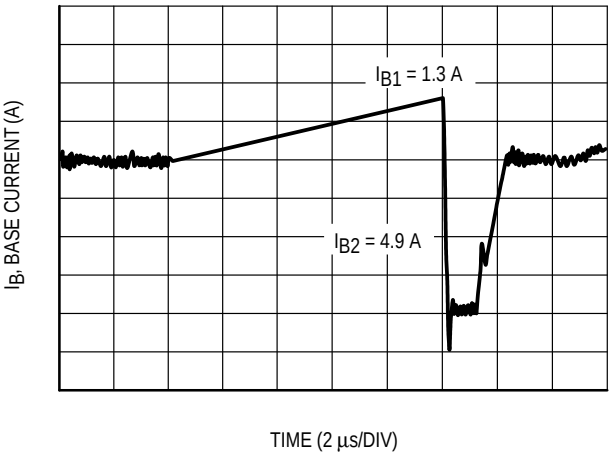


Figure 9. Deflection Simulator Circuit Base Drive Waveform

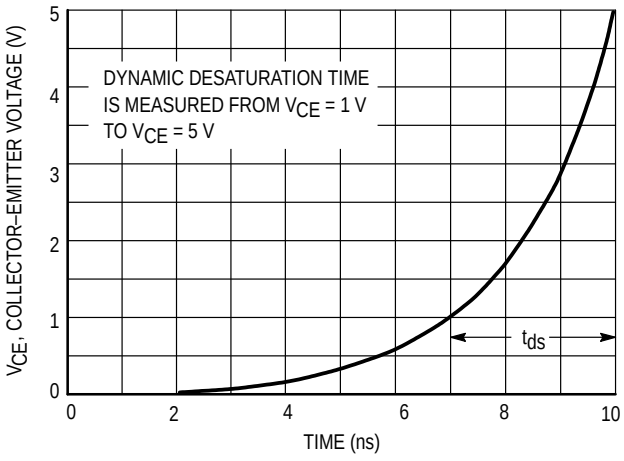


Figure 10. Definition of Dynamic Desaturation Measurement

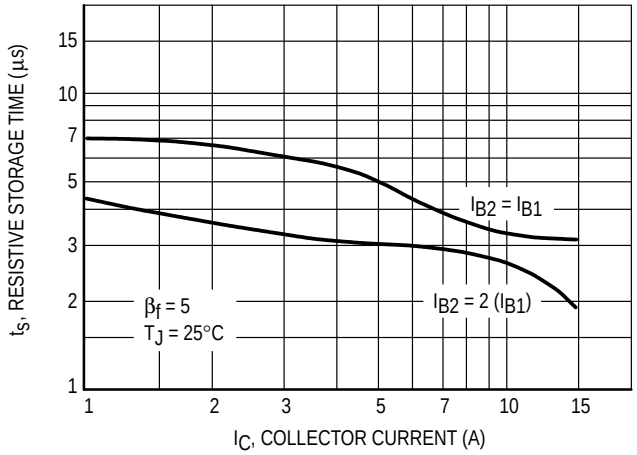


Figure 11. Typical Resistive Storage Time

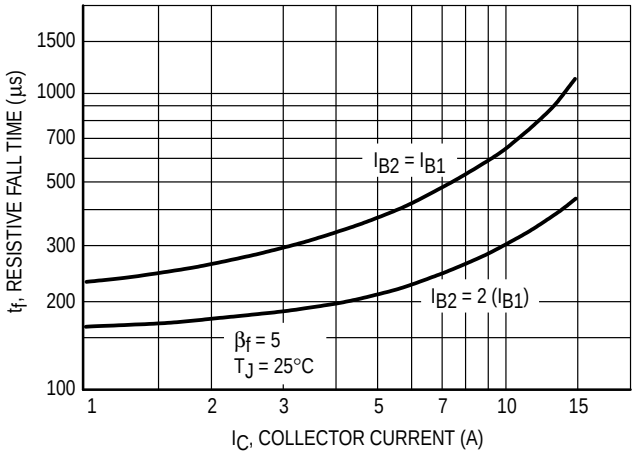
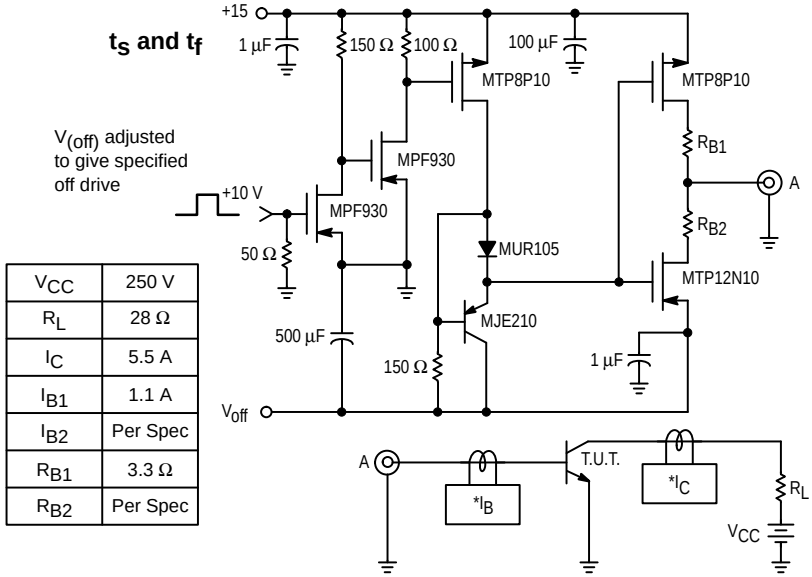


Figure 12. Typical Resistive Fall Time

Table 3. Resistive Load Switching

t_S and t_f



V_{CC}	250 V
R_L	28 Ω
I_C	5.5 A
I_{B1}	1.1 A
I_{B2}	Per Spec
R_{B1}	3.3 Ω
R_{B2}	Per Spec

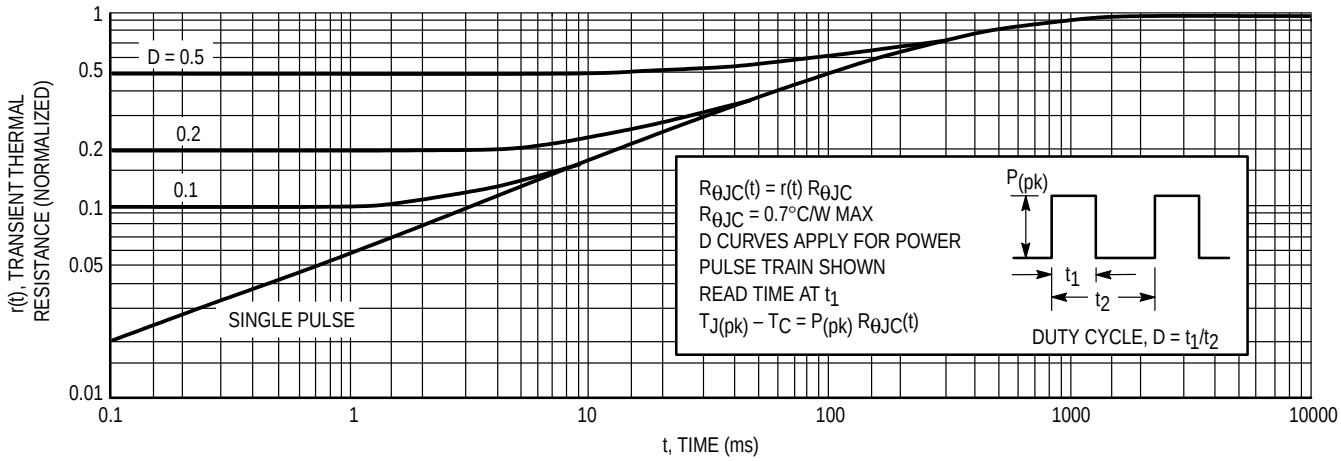


Figure 13. Thermal Response

EMITTER–BASE TURN–OFF ENERGY, $EB_{(off)}$

Emitter–base turn–off energy is a new specification included on the SCANSWITCH data sheets. Typical techniques for driving horizontal outputs rely on a pulse transformer to supply forward base current, and a turnoff network that includes a series base inductor to limit the rate of transition from forward to reverse. An alternate drive scheme has been used to characterize the SCANSWITCH series of devices (see Figure 2). This circuit ramps the base drive to eliminate the heavy overdrive at the beginning of the collector current ramp and underdrive just prior to turn–off observed in typical drive topologies. This high performance drive has two additional important advantages. First, the configuration of T1 allows L_b to be placed outside the path of forward base current making it unnecessary to expend energy to reverse the current flow as in a series based inductor. Second, there is no base resistor to limit forward base current and hence no power loss associated with setting the value of the forward base current. The ramp generating process stores rather than dissipates energy. Tailoring the amount of energy stored in T1 to the amount of energy, $EB_{(off)}$, that is required to turn the output transistor off results in essentially lossless operation. [Note: B+ and the primary inductance of T1 (L_P) are chosen such that $1/2L_PI_b^2 = EB_{(off)}$.]

TEST CONDITIONS FOR ISOLATION TESTS* (MJF16212 ONLY)

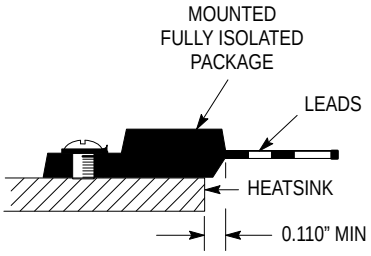


Figure 14. Screw or Clip Mounting Position for Isolation Test Number 1

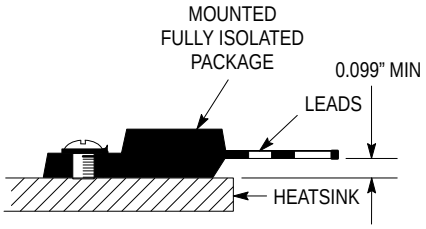


Figure 15. Screw or Clip Mounting Position for Isolation Test Number 2

* Measurement made between leads and heatsink with all leads shorted together

MOUNTING INFORMATION** (MJF16212 ONLY)

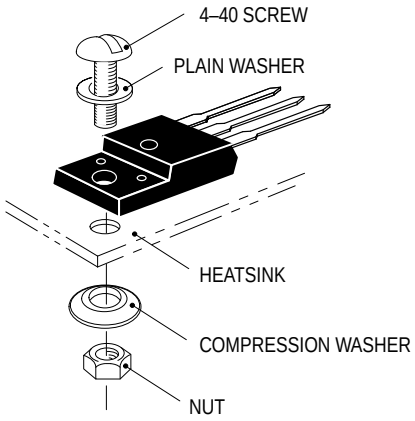


Figure 16a. Screw–Mounted

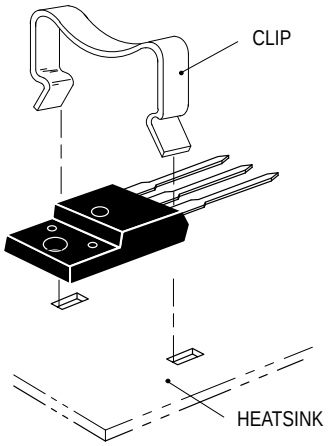


Figure 16b. Clip–Mounted

Figure 16. Typical Mounting Techniques*

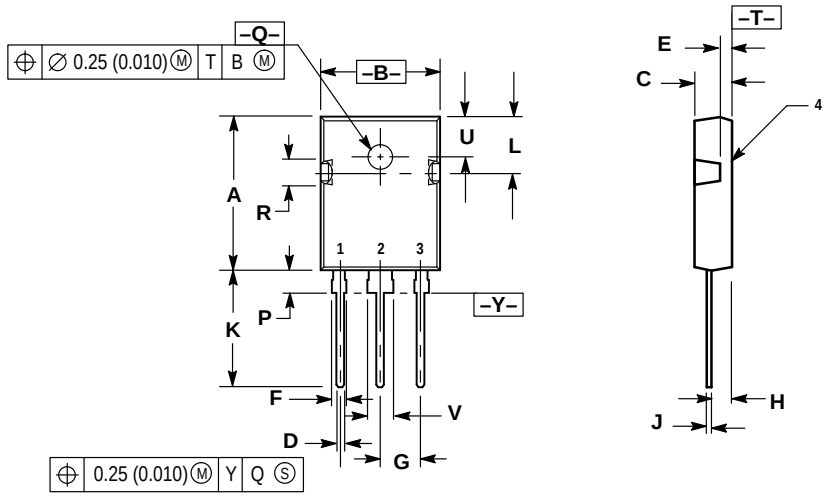
Laboratory tests on a limited number of samples indicate, when using the screw and compression washer mounting technique, a screw torque of 6 to 8 in · lbs is sufficient to provide maximum power dissipation capability. The compression washer helps to maintain a constant pressure on the package over time and during large temperature excursions.

Destructive laboratory tests show that using a hex head 4-40 screw, without washers, and applying a torque in excess of 20 in · lbs will cause the plastic to crack around the mounting hole, resulting in a loss of isolation capability.

Additional tests on slotted 4-40 screws indicate that the screw slot fails between 15 to 20 in · lbs without adversely affecting the package. However, in order to positively ensure the package integrity of the fully isolated device, Motorola does not recommend exceeding 10 in · lbs of mounting torque under any mounting conditions.

** For more information about mounting power semiconductors see Application Note AN1040.

PACKAGE DIMENSIONS



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	20.40	20.90	0.803	0.823
B	15.44	15.95	0.608	0.628
C	4.70	5.21	0.185	0.205
D	1.09	1.30	0.043	0.051
E	1.50	1.63	0.059	0.064
F	1.80	2.18	0.071	0.086
G	5.45 BSC		0.215 BSC	
H	2.56	2.87	0.101	0.113
J	0.48	0.68	0.019	0.027
K	15.57	16.08	0.613	0.633
L	7.26	7.50	0.286	0.295
P	3.10	3.38	0.122	0.133
Q	3.50	3.70	0.138	0.145
R	3.30	3.80	0.130	0.150
U	5.30 BSC		0.209 BSC	
V	3.05	3.40	0.120	0.134

STYLE 3:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

CASE 340F–03
TO–247AE
ISSUE E

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