

40 CH Driver for Dot Matrix LCD

FEATURES

- Display driving bias ; static-1/5
- Power supply voltage ; $V_{DD} = +5V \pm 10\%$
 $V_{DD} = +3V \pm 10\%$
- Supply voltage range for display : $\leq 10V$
- Negative display voltage :
 $0 \geq V_{EE} \geq V_{DD} - 10V$
- Interface

Driver (cascade connection)	Controller
Other APU0065	APU0066

APPLICATIONS

- Dot matrix LCD driver with 40 channel output.
- Selectable function to use Common / Segment drivers simultaneously.
- Input / Output signal
- Output ; 20×2 channel waveform for LCD driving
- Input ; - Serial display data and control pulse from the controller LSI .
- Bias voltage ($V_1 - V_6$)
- QFP64 and bare chip available

GENERAL DESCRIPTION

The APU0065 is a LCD driver LSI that is fabricated by low power CMOS technology. Basically this LSI consists of 20×2 bit bi-directional shift register, 20×2 bit data latch and 20×2 bit driver. This LSI can be CMOS Process used a Common or Segment driver.

ORDERING INFORMATION

APU0065 □ E - □ Handling Code Package Type	Package Type Q : QFP Y : Chip Handling Code TY : Tray
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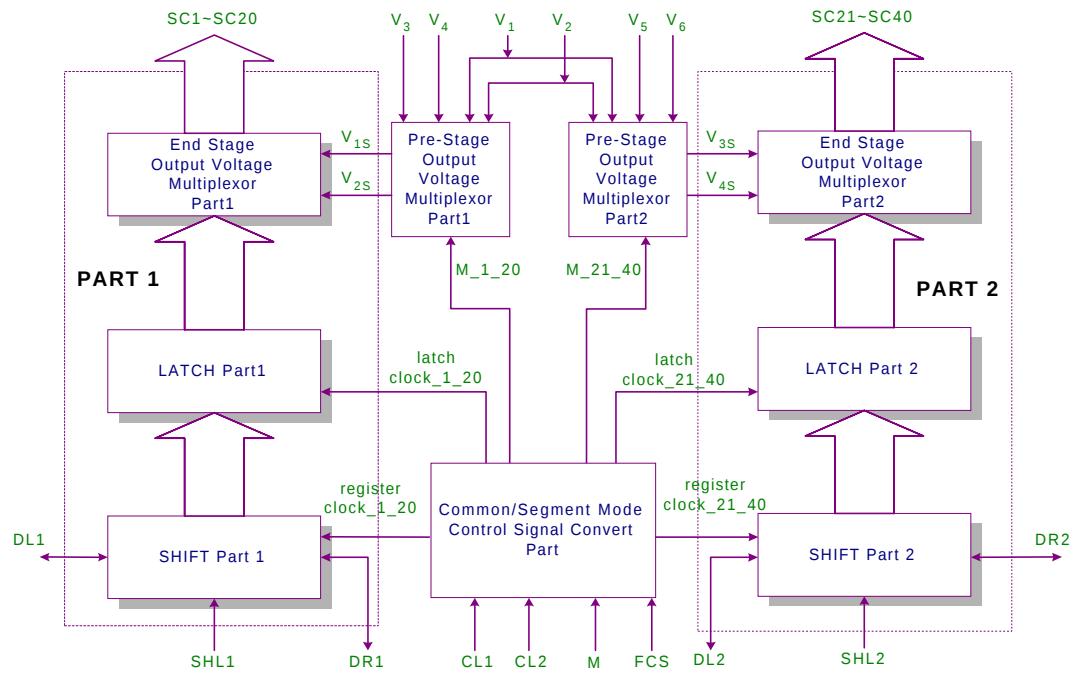


Figure 1. Block diagram of APU0065

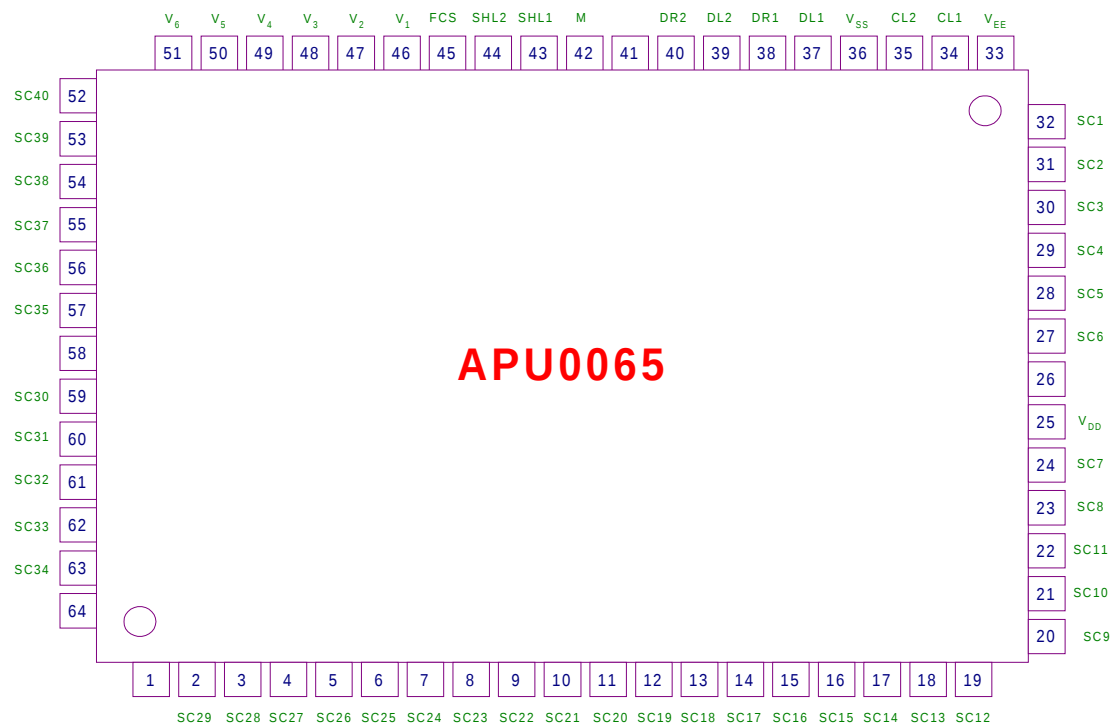


Figure 2. QFP 64 Top View

PIN DESCRIPTION-QFP100

PAD (NO.)	INPUT/OUTPUT	NAME	DESCRIPTION	INTERFACE												
V _{EE} (33)	Power	Negative Supply Voltage	For LCD driver circuit(0 ≥ V _{EE} ≥ V _{DD} -10V)	Power Supply												
V _{DD} (25)	Power	Operating Voltage	For logical circuit (+5V± 10%, +3V± 10%)	Power Supply												
V _{SS} (36)	Power	Operating Voltage	0V (GND)	Power Supply												
V ₁ ~ V ₆ (46 ~ 51)	Input	Bias Voltage	Bias Voltage level for LCD drive	Power Supply												
M (42)	Input	Altemated signal for LCD driver output	This is the signal for LCD twisting	Controller												
CL1, CL2 (34, 35)	Input	Data shift / latch clock	These signal control the shift and latch of driver. More detail scription in next line FCS .	Controller												
FCS (45)	Input	Mode selection	If FCS equals to V_{SS}, Part1 and Part2 both are segment mode. If FCS equals to V_{DD}, Part1 is segment mode but Part2 is common mode . <table><tr><td>Mode</td><td>CL1</td><td>CL2</td><td>M</td></tr><tr><td>Segment</td><td></td><td></td><td>M</td></tr><tr><td>Common</td><td></td><td></td><td>M̄</td></tr></table>	Mode	CL1	CL2	M	Segment			M	Common			M̄	Controller
Mode	CL1	CL2	M													
Segment			M													
Common			M̄													
SHL1 (43)	Input	Shifting direction control signal of Part1	Selection of the shift directon of Part 1 shift register <table><tr><td>SHL1</td><td>DL1</td><td>DR1</td></tr><tr><td>V_{DD}</td><td>output</td><td>input</td></tr><tr><td>V_{SS}</td><td>input</td><td>output</td></tr></table>	SHL1	DL1	DR1	V _{DD}	output	input	V _{SS}	input	output	Controller			
SHL1	DL1	DR1														
V _{DD}	output	input														
V _{SS}	input	output														
DL1, DR1 (37, 38)	Input Output	Data interface	Data input / output of Part1 shift register	Controller or APU0063												
SC1 ~ SC20	Output	LCD driver	LCD driver output of Part1	LCD												
SHL2 (44)	Input	Shifting direction control signal of Part2	Selection of the shift directon of Part 2 shift register <table><tr><td>SHL2</td><td>DL2</td><td>DR2</td></tr><tr><td>V_{DD}</td><td>output</td><td>Input</td></tr><tr><td>V_{SS}</td><td>Input</td><td>output</td></tr></table>	SHL2	DL2	DR2	V _{DD}	output	Input	V _{SS}	Input	output	Controller			
SHL2	DL2	DR2														
V _{DD}	output	Input														
V _{SS}	Input	output														
DL2, DR2 (39, 40)	Input Output	Data interface	Data input / output of Part 2 shift register	Controller or APU0063												
SC21 ~ SC40	Output	LCD driver	LCD driver output of Part2	LCD												

Note : Input pin can not be floated, or it will cause large leakage current.

SEGMENT MODE

When Part1 or Part2 be selected to work in segment mode (FCS pin = V_{SS}), these are the liquid crystal segment drive outputs. A signal of driving pin in segment mode is the one of V_1 , V_2 , V_3 or V_4 . These selecting are following.

Data of latch	M	Output voltage
High	High	V_1
High	Low	V_2
Low	High	V_3
Low	Low	V_4

COMMON MODE

Only Part2 can be selected to work in common mode (FCS pin = V_{DD}). These are the liquid crystal common drive outputs signal of driving pin in segment mode is the one of V_1 , V_2 , V_5 or V_6 . These selecting are following.

Data of latch	M	Output voltage
High	High	V_2
High	Low	V_1
Low	High	V_6
Low	Low	V_5

SHIFT DIRECTION SPECIFICATION

Part1

When Part1 shift direction control signal, SHL1, is set to V_{SS} .
Now the Part1 register shift direction is
DL1 → SC1 → SC2 → ... → SC19 → SC20
→ DR1
Otherwise, when SHL1 is set to V_{DD} . Its direction is
DL1 ← SC1 ← SC2 ← ... ← SC19 ← SC20
← DR1

Part2

When Part2 shift direction control signal, SHL2, is set to V_{SS} .
Now the Part2 register shift direction is
DL2 → SC21 → SC22 → ... → SC39 →
SC40 → DR2
Otherwise, when SHL2 is set to V_{DD} . Its direction is
DL2 ← SC21 ← SC22 ← ... ← SC39 ←
SC40 ← DR2

MAXIMUM ABSOLUTE LIMIT (Ta = 25 °C)

Characteristic	Symbol	Value	Unit
Operating Voltage	V_{DD}	-0.3 ~ +7.0	V
Driver Supply Voltage	V_{LCD}	$V_{DD}-13.5 \sim V_{DD}+0.3$	V
Input Voltage 1	V_{IN1}	-0.3 ~ $V_{DD}+0.3$	V
Input Voltage 2 ($V_1 \sim V_6$)	V_{IN2}	$V_{DD}+0.3 \sim V_{EE}-0.3$	V
Operating Temperature	T_{OPR}	-30 ~ +85	°C
Storage Temperature	T_{STG}	-55 ~ +125	°C

ELECTRICAL CHARACTERISTICSDC characteristics ($V_{DD} = 2.7 \sim 5.5V$, $0 \geq V_{EE} \geq V_{DD} - 10V$, $V_{SS} = 0V$, $T_a = -30 \sim +85^\circ C$)

Characteristic	Symbol	Test condition	Min	Max	Unit	Applicable pin
Operating Current*	I_{DD}	$f_{CL2} = 400KHz$	–	1	mA	–
Supply Current*	I_{EE}	$f_{CL1} = 1KHz$	–	10	μA	
Input High Voltage	V_{IH}	–	$0.7 V_{DD}$	V_{DD}	V	CL1, CL2, DR1, DR2, DR1, DR2, SHL1, SHL2, M, FCS
Input Low Voltage	V_{IL}		0	$0.2 V_{DD}$		
Input Leakage Current	I_{LKC}	$V_{IN} = 0 - V_{DD}$	-5	5	μA	
Output High Voltage	V_{OH}	$I_{OH} = -0.4mA$	$V_{DD} - 0.4$	–	V	DL1, DL2, DR1, DR2
Output Low Voltage	V_{OL}	$I_{OL} = +0.4mA$	–	0.4		
Voltage Descending	V_{D1}	$I_{ON} = 0.1mA$ for one of SC1 ~ SC40	–	1.1		$V (V_1 \sim V_6) -$ SC (SC1 ~ SC40)
	V_{D2}	$I_{ON} = 0.05mA$ for each SC1 ~ SC40	–	1.5		
Leakage Current	I_V	$V_{IN} = V_{DD} \sim V_{EE}$ (Output SC1 ~ SC40 : floating)	-10	10	μA	$V_1 \sim V_6$

AC characteristics ($V_{DD} = 2.7 \sim 5.5V$, $0 \geq V_{EE} \geq V_{DD} - 10V$, $V_{SS} = 0V$, $T_a = -30 \sim +85^\circ C$)

Characteristic	Symbol	Test condition	Min	Max	Unit	Applicable pin
Data shift Frequency	f_{CL}	–	–	400	KHz	CL2
Clock High Level Width	t_{WCKH}	–	800	–	ns	CL1,CL2
Clock Low Level Width	t_{WCKL}	–	800	–		CL2
Clock Set-up Time	t_{SL}	from CL2 to CL1	500	–		CL1,CL2
	t_{LS}	from CL1 to CL2	500	–		
Clock Rise / Fall Time	t_R / t_F	–	–	200		DL1,DL2,DR1,DR2,FLM
Data Set-up Time	t_{SU}	–	300	–		
Data Hold Time	t_{DH}	–	300	–		DL1,DL2,DR1,DR2
Data Delay Time	t_D	–	–	600		

TIMING CHARACTERISTICS

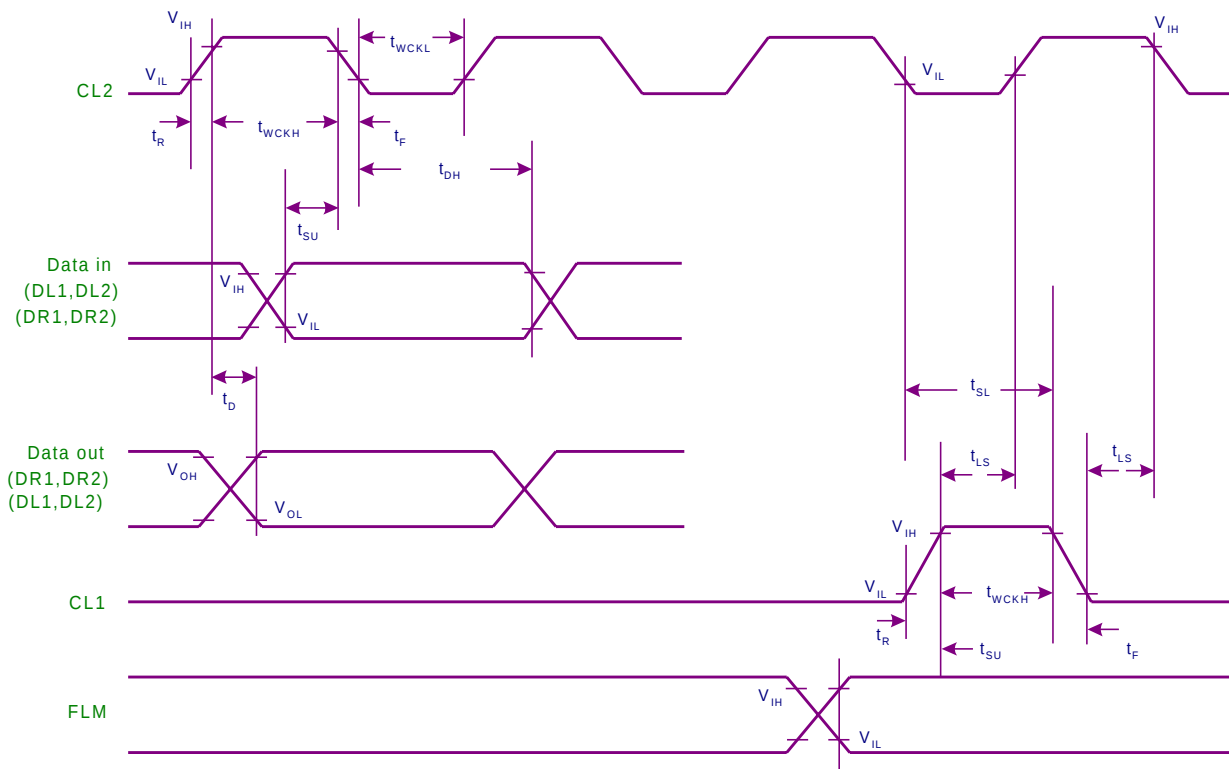
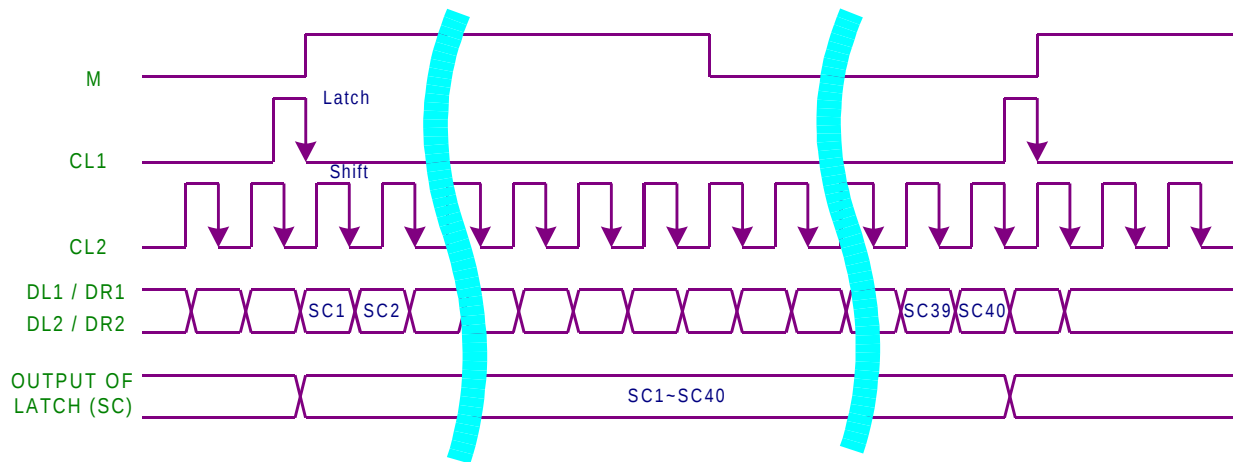


Figure 3. Timing diagram of signals

FUNCTIONAL DESCRIPTION

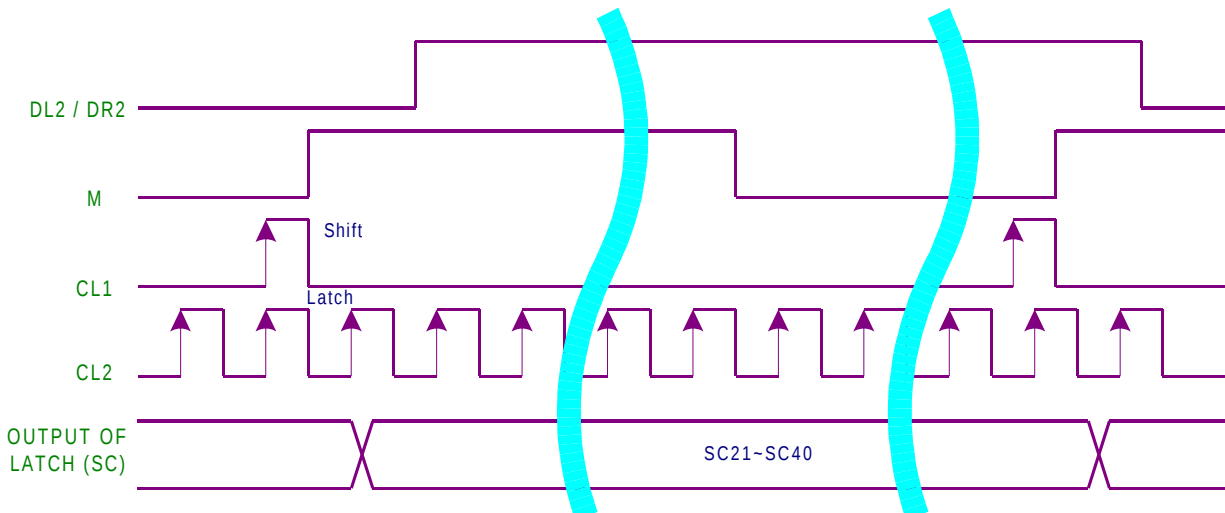
1) Segent mode



When the FCS is connected to V_{SS} , APU0065 (SC1 ~ SC40) is operated as segment driver.
(refer to figure 5)

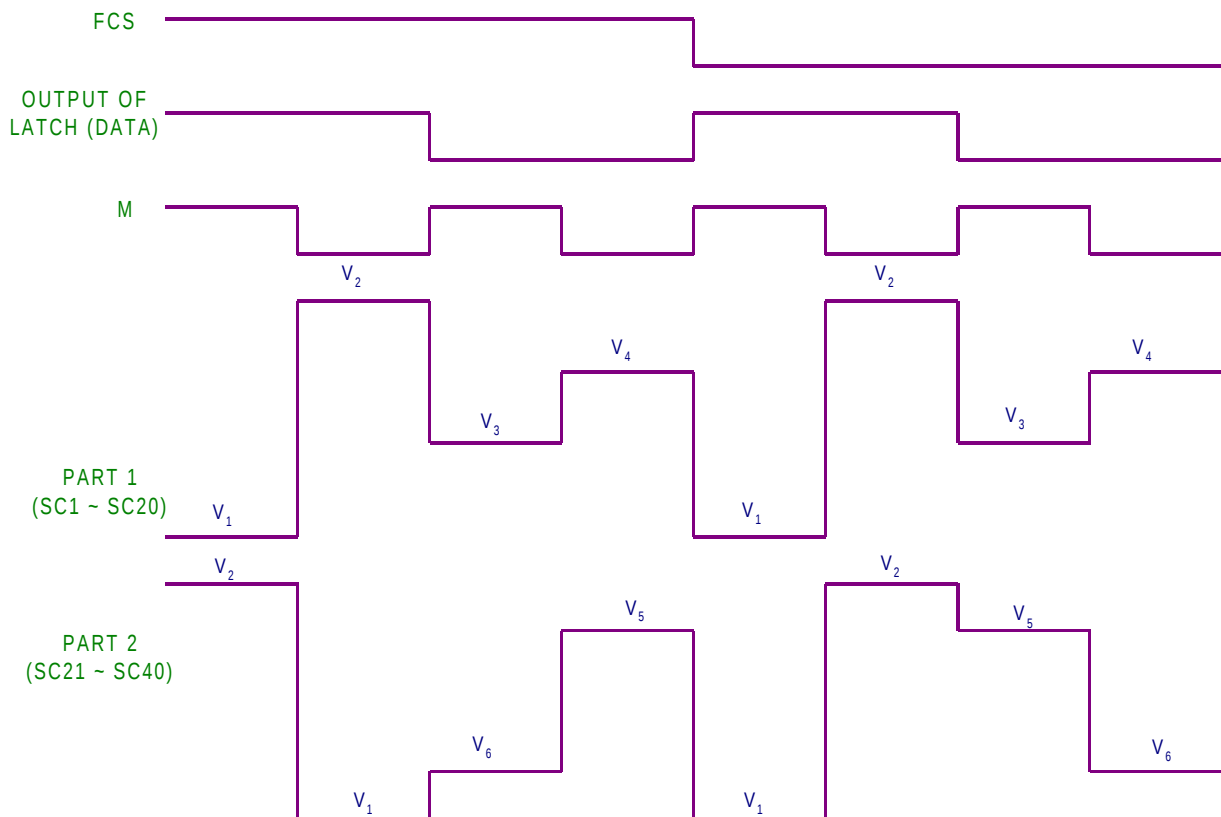
Figure 4. timing diagram of Segment mode

2) Common mode



When the FCS is connected to V_{DD} , only part2 (SC21 ~ SC40) of APU0065 is operated as common driver.
(refer to figure 6.)

Figure 5. timing diagram of Common mode



Note : When fcs equals to high voltage, PART 2 (SC21 ~ SC40) is operated as LCD Common driver.

PART 1 (SC1 ~ SC20) always be operated as LCD segment driver, no matter fcs equals to high or low

Figure 6. SC1 ~ SC40 output waveform

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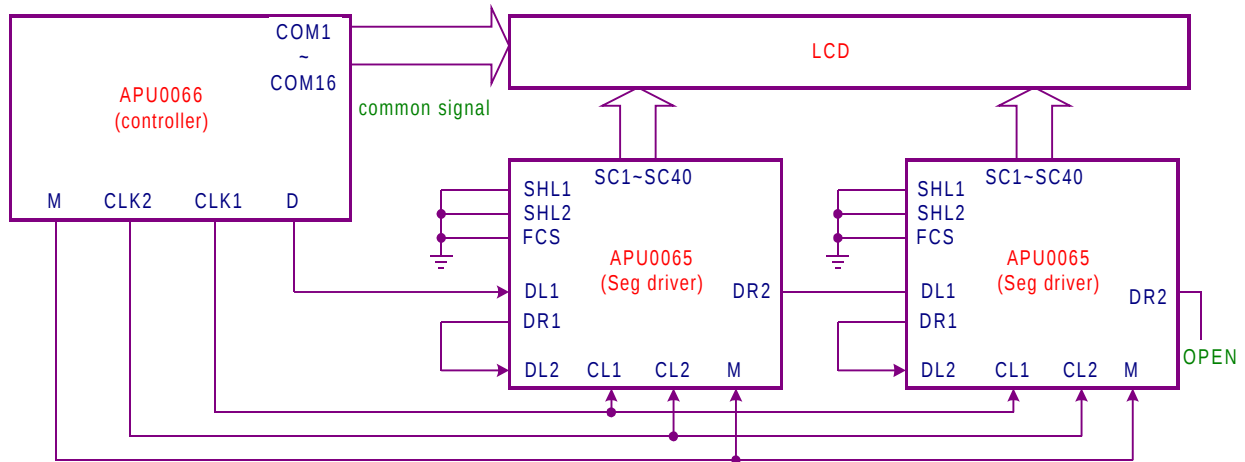
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APPLICATION CIRCUIT

1. Segment driver



2. Segment / Common driver

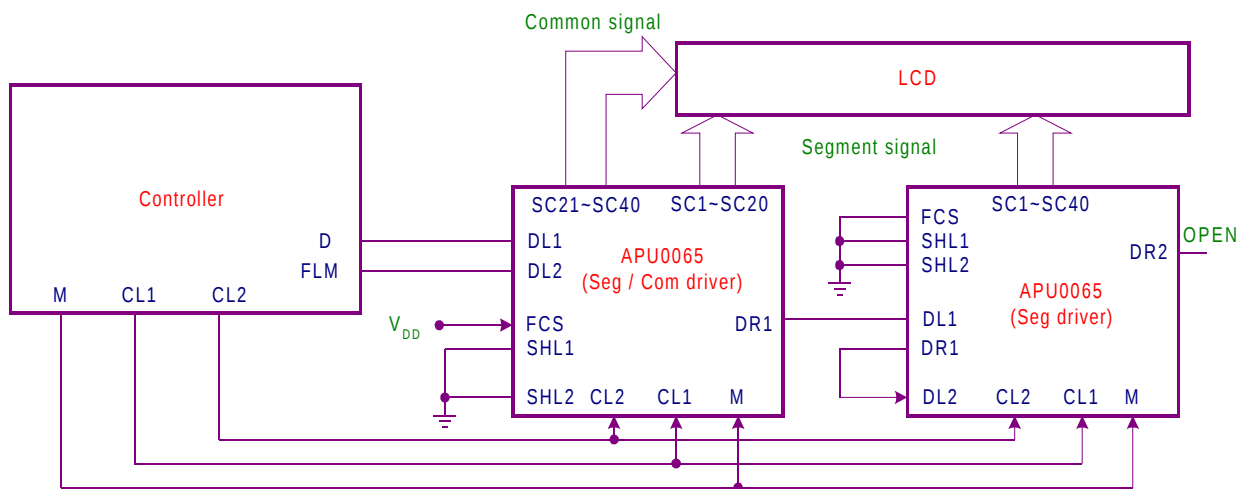


Figure 7. Connection between APU0065 and Controller

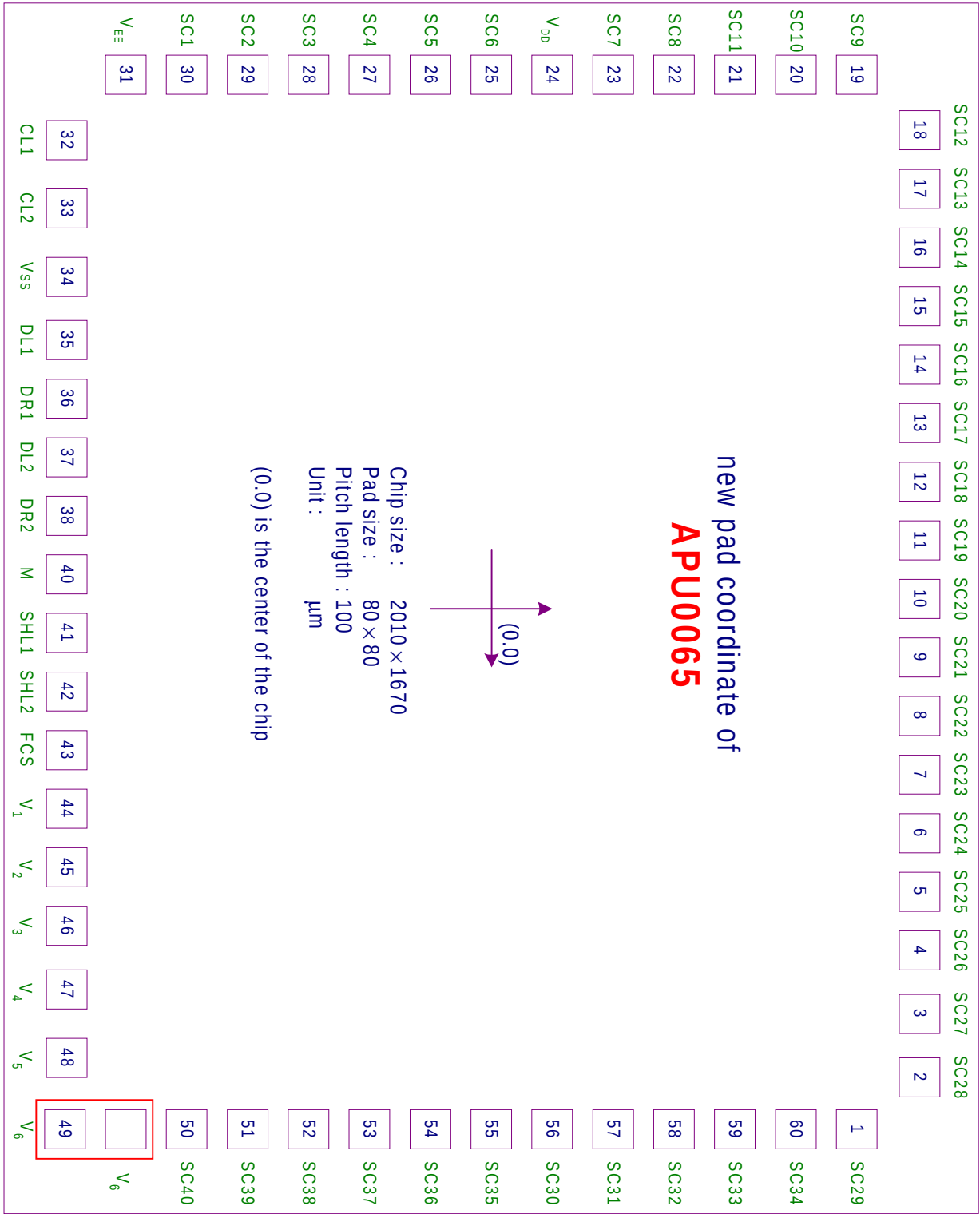


Figure 8. Chip pad arrangement

PAD LOCATION

PAD NUMBER	PAD NAME	COORDINATE		PAD NUMBER	PAD NAME	COORDINATE	
		X	Y			X	Y
1	SC29	902.5	630.0	31	VEE	-902.5	-630.0
2	SC28	850.0	732.5	32	CL1	-800.0	-722.5
3	SC27	725.0	732.5	33	CL2	-700.0	-732.5
4	SC26	600.0	732.5	34	V _{SS}	-600.0	-732.5
5	SC25	500.0	732.5	35	DL1	-500.0	-732.5
6	SC24	400.0	732.5	36	DR1	-400.0	-732.5
7	SC23	300.0	732.5	37	DL2	-300.0	-732.5
8	SC22	200.0	732.5	38	DR2	-200.0	-732.5
9	SC21	100.0	732.5	40	M	-100.0	-732.5
10	SC20	0.0	732.5	41	SHL1	0.0	-732.5
11	SC19	-100.0	732.5	42	SHL2	100.0	-732.5
12	SC18	-200.0	732.5	43	FCS	200.0	-732.5
13	SC17	-300.0	732.5	44	V ₁	315.0	-732.5
14	SC16	-400.0	732.5	45	V ₂	430.0	-732.5
15	SC15	-500.0	732.5	46	V ₃	545.0	-732.5
16	SC14	-600.0	732.5	47	V ₄	660.0	-732.5
17	SC13	-725.0	732.5	48	V ₅	775.0	-732.5
18	SC12	-850.0	732.5	49	V ₆	905.0	-632.5
19	SC9	-902.5	630.0	50	SC40	902.5	-525.0
20	SC10	-902.5	525.0	51	SC39	902.5	-420.0
21	SC11	-902.5	420.0	52	SC38	902.5	-315.0
22	SC8	-902.5	315.0	53	SC37	902.5	-210.0
23	SC7	-902.5	210.0	54	SC36	902.5	-105.0
24	V _{DD}	-902.5	105.0	55	SC35	902.5	0.0
25	SC6	-902.5	0.0	56	SC30	902.5	105.0
26	SC5	-902.5	-105.0	57	SC31	902.5	210.0
27	SC4	-902.5	-210.0	58	SC32	902.5	315.0
28	SC3	-902.5	-315.0	59	SC33	902.5	420.0
29	SC2	-902.5	-420.0	60	SC34	902.5	525.0
30	SC1	-902.5	-525.0				