

Multiple-Input Li-ion Battery Charger in QFN4x4 Package

General Description

The uP8003 is a highly integrated complete battery charger specifically designed for digital still camera where PCB area is specially concerned.

The uP8003 integrates a single-pole-triple-throw power multiplexer that automatically selects AC adaptor, Dock or USB inputs according to default priority. External ORing diode is not necessary in real application. The USB input power can be turned off by a USB_OFF control pin. The uP8003 features open-drain outputs for input power detection. A voltage monitoring pin is also available for USB input.

The uP8003 charges battery with a minimum current when the battery voltage is lower than 2.8V. The charger works at constant current mode when the battery voltage is between 2.8V and 4.2V, the charge current is programmable up to 1.5A by an external resistor. The charge works at constant voltage mode when the battery voltage is 4.2V. When the input voltage is removed, the uP8003 automatically enters a low quiescent current sleep mode, dropping the battery drain current to 1uA.

The uP8003 provides a programmable time-out function that initiates fault alarm if charge cycle is not complete within the time-out period. The uP8003 features open-drain status and fault outputs that indicate charge status and fault conditions respectively.

Other features include thermal foldback charge current, NTC thermistor interface and automatic recharge. The uP8003 is available in thermal-enhanced and space-saving VQFN4x4 - 24L package.

Ordering Information

Order Number	Package	Top Marking
uP8003AQAG	VQFN4x4 - 24L	uP8003AG

Note: uPI products are compatible with the current IPC/JEDEC J-STD-020 requirements. They are halogen-free, RoHS compliant and 100% matte tin (Sn) plating that are suitable for use in SnPb or Pb-free soldering processes.

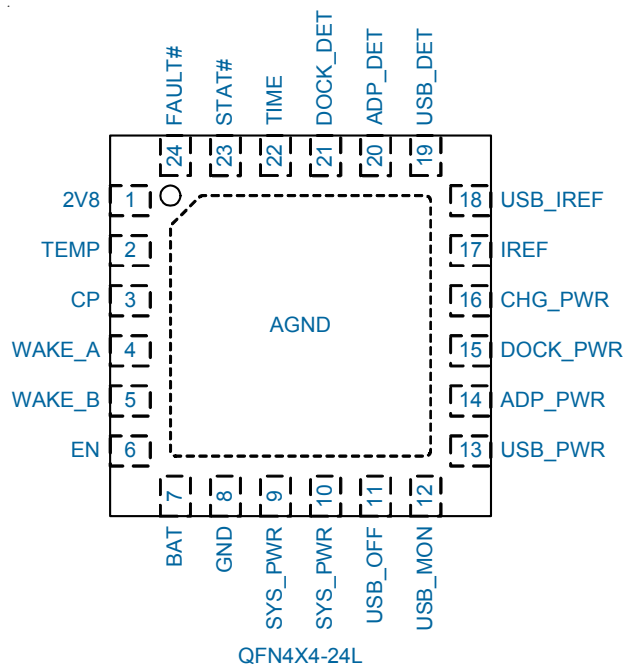
Applications

- ❑ Digital Still Camera
- ❑ Charging Docks and Cradles
- ❑ USB Powered Chargers

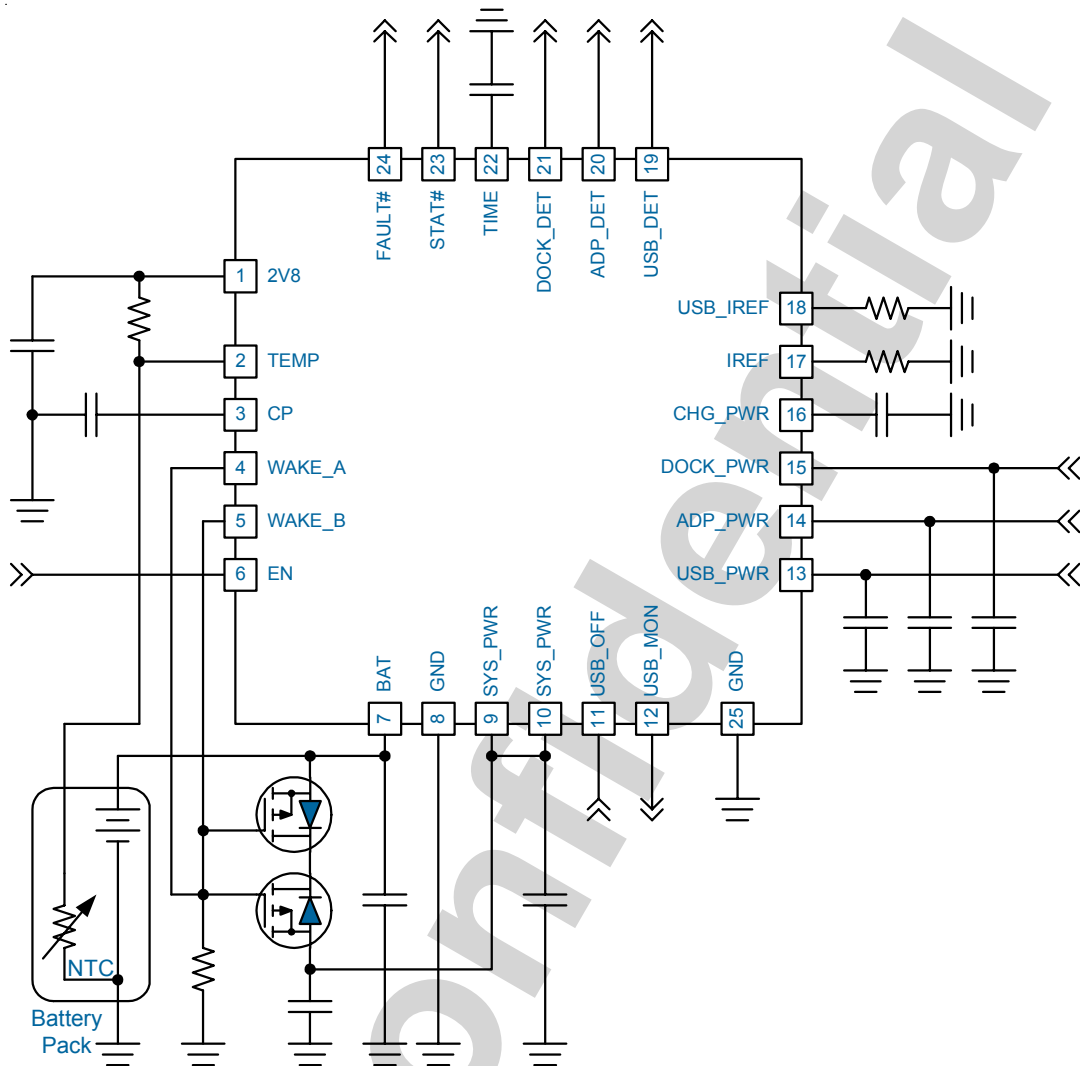
Features

- ❑ Complete Charger for 1-Cell Li-ion Batteries
- ❑ Integrated Single-Pole-Triple-Throw Power Multiplexer
- ❑ Three Power Input Indications
- ❑ USB Voltage Monitoring
- ❑ USB ON/OFF Control
- ❑ Integrated Pass Element and Current Sensor
- ❑ No External Blocking Diode Required
- ❑ 1% Voltage Accuracy
- ❑ Programmable Charge Current up to 1.5A
- ❑ NTC Interface for Battery Temperature Sensing
- ❑ Battery Insertion Detection
- ❑ 1uA Battery Drain Current when Input Voltage is Removed
- ❑ Automatic Trickle Charging of Low Voltage Cells
- ❑ Automatic Battery Recharge
- ❑ RoHS Compliant and Halogen Free

Pin Configuration



Typical Application Circuit



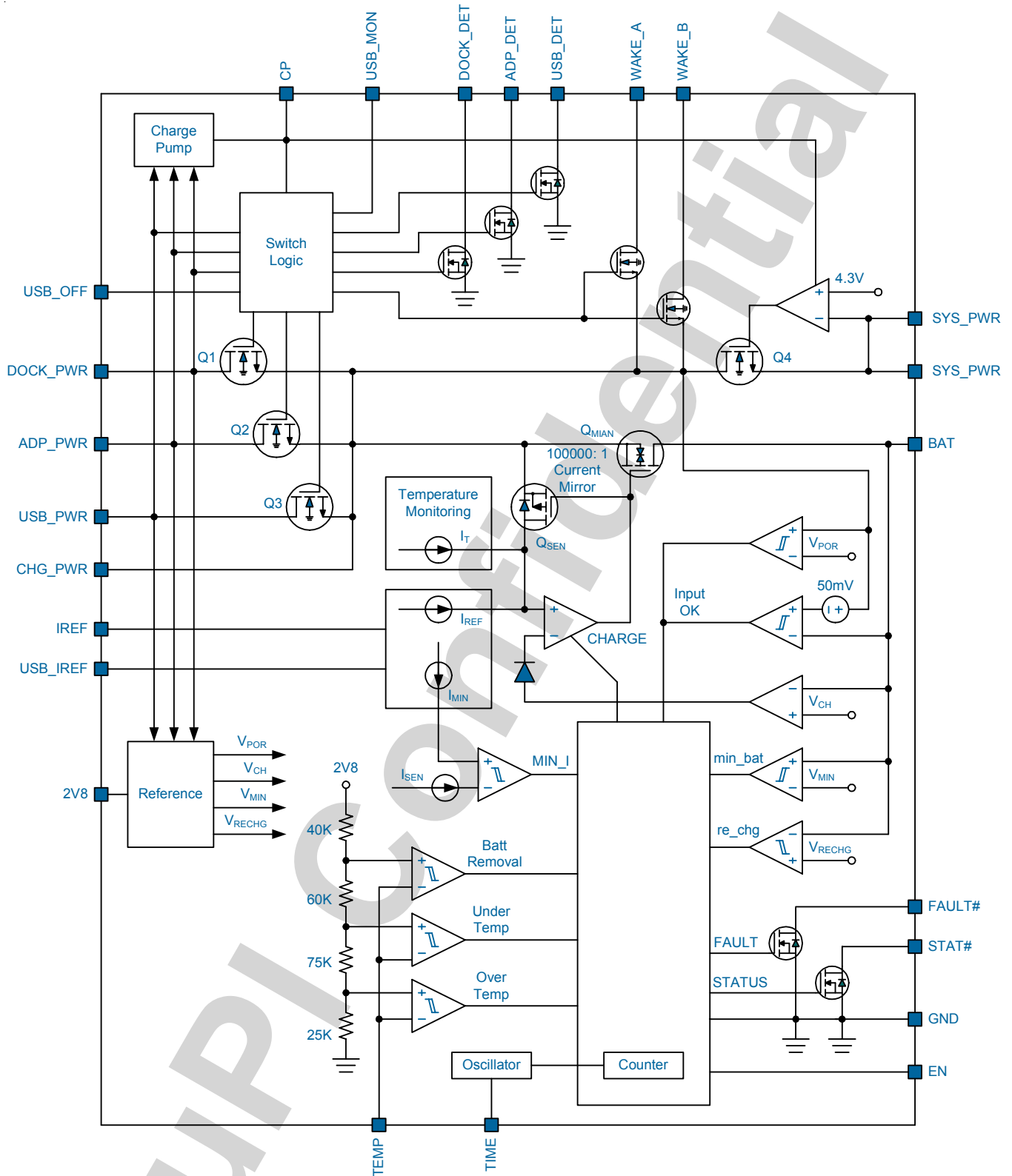
Functional Pin Description

Pin No.	Pin Name	Pin Function
1	2V8	2.8V Reference Output. This pin outputs a 2.8V voltage source when the CHG_PWR is above POR threshold level and the charger is enabled. This pin is capable of sourcing 2mA output current.
2	TEMP	Temperature and Battery Removal Detection Input. Connect this pin to the NTC thermal output of battery pack.
3	CP	Charge Pump Output. This pin is the output pin of internal charge pumper that provides charges for internal power multiplexer and LDO control. Bypass this pin with a 4.7nF ceramic capacitor.
4	WAKE_A	System Wake A. This is output A for system wake up. Connect this pin to gate of the PMOSFETs for system power input selection.
5	WAKE_B	System Wake B. This is output B for system wake up. Connect this pin to gate of the PMOSFETs for system power input selection.

Functional Pin Description

Pin No.	Pin Name	Pin Function
6	EN	Enable Input. Let this pin floating or pull this pin to GND to disable the charger. Pull this pin high to enable the charger.
7	BAT	Battery Output. Connect this pin to the positive terminal of battery pack. A minimum 1uF ceramic capacitor is required for stable operation of the charger.
8	GND	Ground. Connect this pin to system ground. All voltage is measured with respect to this pin.
9, 10	SYS_PWR	System Power Outputs. These pins are the output of internal 4.3V LDO. The LDO is turned on when CHG_PWR voltage is ready. The PMOSFET for system power input selection is turned off when the LDO is turned on.
11	USB_OFF	USB ON/OFF Control. Logic high turns off the USB input.
12	USB_MON	USB Voltage Monitoring. This pin outputs 1/2 of V_{USB} for USB voltage monitoring.
13	USB_PWR	Power Input for USB. Connect a minimum 1uF ceramic voltage physically near this pin for locally bypassing the supply input.
14	ADP_PWR	Power Input for AC Adaptor. Connect a minimum 1uF ceramic voltage physically near this pin for locally bypassing the supply input.
15	DOCK_PWR	Power Input for Dock. Connect a minimum 1uF ceramic voltage physically near this pin for locally bypassing the supply input.
16	CHG_PWR	Power Input for Charger and System Power LDO. This pin is the output of the internal single-pole-triple-throw power multiplexer. The CHG_PWR provides current for the charger and system power LDO.
17	IREF	Charging Current Programming for Adaptor and Dock Input. Connect a resistor between IREF and GND pins to program reference current I_{REF} for constant current charging mode.
18	USB_IREF	Charging Current Programming for USB Input. Connect a resistor between USB_IREF and GND pins to program reference current I_{USB_REF} for constant current charging mode.
19	USB_DET	USB Power Input Detection. This pin is an open-drain output that is pulled low when V_{USB} is higher than 4.4V and WAKE_A/B are pulled high.
20	ADP_DET	AC Adaptor Input Detection. This pin is an open-drain output that is pulled low when V_{ADP} is higher than 4.4V and WAKE_A/B are pulled high.
21	DOCK_DET	DOCK Input Detection. This pin is an open-drain output that is pulled low when V_{DOCK} is higher than 4.4V and WAKE_A/B are pulled high.
22	TIME	Oscillation Period. Connect a timing capacitor between TIME and GND pins to determine the oscillation period. This oscillation period provides a time reference for the charger.
23	STAT#	Charger Status Indication. This pin is an open-drain output indicating charging status. This pin is pulled to LOW when the charger is charging a battery.
24	FAULT#	Fault Indication. This pin is an open-drain output indicating fault status. This pin is pulled to LOW under any fault conditions.
25 Exposed Pad		Ground. The exposed pad is the main path for heat convection and should be well soldered to the PCB for best thermal performance.

Functional Block Diagram



Functional Description

The uP8003 is a highly integrated complete battery charger specifically designed digital still camera where PCB is specially concerned.

Supply Input Power for Charge Pump

The uP8003 integrates a charge pump that pumps ADP_PWR, DOCK_PWR, or USB_PWR, whichever is higher, to a 10V output voltage at CP pin for turning on the internal power multiplexer and 4.3V LDO. The ramp up time of the charge pump output voltage is highly dependent of the capacitor attached to the CP pin. A 4.7nF capacitor results in a typical 4.0ms ramp up time. The 4.3V LDO will not be enabled until the charge pump voltage is higher than 9V.

The charge pump is not designed to provide currents for external circuits.

Power Multiplexer

The uP8003 integrates a current-limited, break-before-make, single-pole-triple-throw power multiplexer that selects appropriate supply input according the availability of supply inputs and default priority. The power multiplexer consists of three body-diode-free NMOSFETs. The drains of the NMOSFETs are connected to ADP_PWR, DOCK_PWR and USB_PWR pins respectively. The sources of the NMOSFETs are connected to the CHG_PWR pin together.

The supply inputs are monitored for power on reset (POR). The CHG_PWR will not be enabled until at least one POR of the supply inputs is recognized. The POR threshold level is typically 4.4V at supply inputs rising. The input detection output ADP_DET, DOCK_DET or USB_DET is pulled low once its corresponding supply input is higher than the POR threshold level and the WAKE_A/B are connected to CHG_PWR.

The default priority for the single-pole-triple-throw power multiplexer is DOCK_PWR > ADP_PWR > USB_PWR. For example, DOCK_PWR is selected if both ADP_PWR and DOCK_PWR are both higher than their POR level.

The power multiplexer is break-before-make type. A typical 1us dead time is implemented when the multiplexer changes its position. This ensures the NMOSFETs will not conduct simultaneously.

The on-resistance of the ADP_PWR, DOCK_PWR and USB_PWR switches are 250mΩ typically.

USB Power Monitoring and Control

A 100kΩ + 100kΩ voltage divider from USB_PWR to GND is included for USB power monitoring. The USB_MON is the center of the voltage divider that makes $V_{MON} = V_{USB}/2$. Load effect of the USB_MON should be well considered

when interfacing to ASIC.

The USB_PWR can be turned off by pulling high the USB_OFF pin. The USB_DET pin is pulled low when V_{USB} is higher than its POR level and USB_OFF pin is pulled high, no matter if WAKE_A/B are ready.

System Power LDO

An LDO regulates SYS_PWR voltage at 4.3V for system power. The LDO will not be enabled until 1.) at least one POR of supply inputs is recognized; 2.) charge pump output V_{CP} is higher than 9V; 3.) CHG_PWR voltage V_{CHG} is higher than 4.3V. The system power LDO features internal soft start that minimizes the inrush current from supply inputs. The output voltage ramp-up slew rate is about 1V/ms.

The uP8003 integrates two redundant system wake-up pins for turning on/off the external PMOSFET pair as shown in the *typical application circuit*. The PMOSFETs are turned on by the pull-low resistor connected to the gates, connecting battery to system power bus. When supply inputs are available, the uP8003 switches the system power bus from battery to supply input by turning off the PMOSFETs and turning on the power multiplexer and LDO. The system wake-up pins WAKE_A and WAKE_B pull high the gates CHG_PWR and turn off the PMOSFETs. Route WAKE_A and WAKE_B traces in parallel in real application.

Battery Charger

The uP8003 charges battery with a minimum current when the battery voltage is lower than 2.8V. The charger works at constant current mode when the battery voltage is between 2.8V and 4.2V, the charge current is programmable up to 1.5A by an external resistor. The charger works at constant voltage mode when the battery voltage is 4.2V. When the input voltage is removed, the uP8003 automatically enters a low quiescent current sleep mode, dropping the battery drain current to 1uA.

Power On Reset at CHG_PWR pin

The charger power CHG_PWR is continuously monitored for power on reset. The uP8003 resets itself as the CHG_PWR voltage rises above the POR rising threshold, typically 3.9V. The device shuts down if the CHG_PWR voltage is under its POR falling threshold, typically 3.8V.

Chip Enable and 2.8V Bias Voltage

The EN pin is internally pulled low 100kΩ to GND for chip disable/enable. Pulling this pin to ground shuts down the uP8003 and disables the 2.8V bias voltage. When shut down, the charger draws typically less than 30uA current from the input power and less than 1uA from the battery.

Logic high of EN pin also enables the 2.8V bias voltage for

Functional Description

biasing the internal control and logic circuit. This voltage also provides current for external circuits such as NTC thermistor circuit. The maximum allowed external load for 2V8 is 2mA.

Charge Cycle

A charge cycle can be initiated by anyone of the following events:

- power on reset,
- the EN pin is toggled from low to high,
- a new battery is inserted (detected by TEMP pin),
- the battery voltage drops below a recharge threshold after completing a charge cycle,
- recovery from a battery over-temperature or under-temperature fault,

A charge cycle consists of three charge modes: trickle mode (TKM), constant current mode (CCM), and constant voltage mode (CVM) as shown in Figure 1.

Trickle Mode

A charge cycle always starts with the trickle mode where minimum charging current is used. T1 and T6 indicate the starting of charge cycle that are initiated by CHG_PWR POR and recharge threshold respectively. The uP8003 leaves TKM and enters CCM at T2 and T7 if the battery voltage stays above V_{MIN} (2.8V typical) for 15 consequently cycles of the internal oscillator. The uP8003 enters TKM and the 15-cycle counter is reset whenever the battery voltage drops below V_{MIN} .

Constant Current Mode

The uP8003 operates at CCM when the battery voltage is between 2.8V and V_{CH} (4.2V typical). The charger acts like a constant current regulator. The charge current I_{CHG} is programmed up to 1.5A by the IREF and USB_IREF pins, see the *Charge Current Programming* section for detail.

Constant Voltage Mode

The uP8003 operates at CVM when the battery voltage reaches the charge high voltage V_{CH} . The charger acts like a constant voltage regulator that regulates the battery terminal voltage at V_{CH} . The charge current is determined by the battery impedance and core voltage. The uP8003 asserts end-of-charge and sets STAT# high impedance at T4 and T8 when the charge current is less than 10% of I_{CHG} .

The charging cycle is actually not terminated until charge timeout is completed to bring the battery to its full capacity.

Recharge

After a charge cycle completes, charging is prohibited until the battery voltage drops to a recharge threshold, V_{RECHG} . Then a new charge cycle starts at point T6 and ends at point T9, as shown in Figure 1. The timeout counter is reset at T6.

Charge Current Setting

The voltage at IREF and USB_IREF pins are regulated to 0.8V reference voltage when they are left open. External resistors R_{IREF} and R_{USBREF} connecting between IREF and USB_IREF to ground programs reference current I_{REF} and

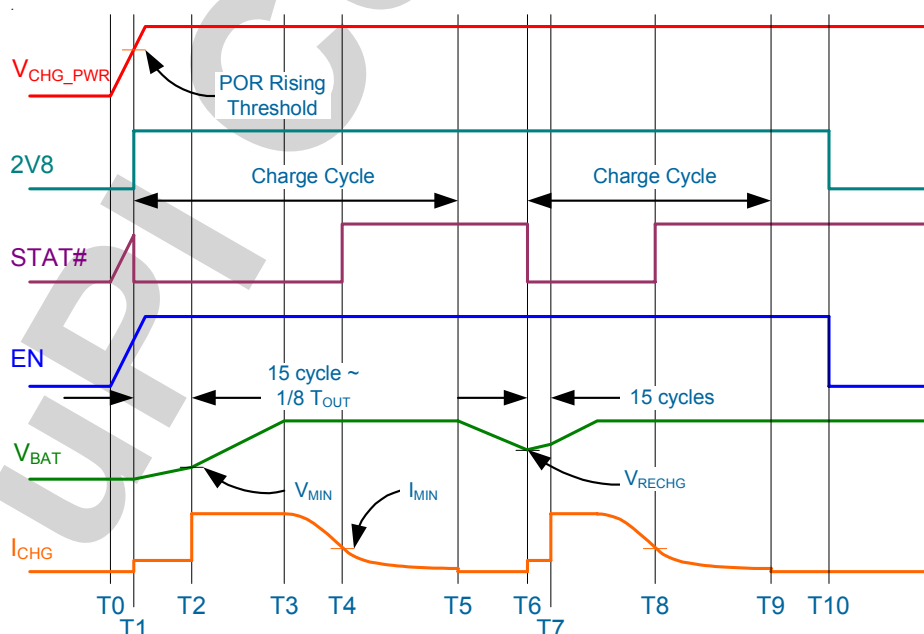


Figure 1. Typical Charge Cycles of uP8003.

Functional Description

I_{USBREF} respectively.

$$I_{REF} = \frac{V_{IREF}}{R_{IREF}} = \frac{0.8V}{R_{IREF}} \quad (A)$$

$$I_{USBREF} = \frac{V_{USBREF}}{R_{USBREF}} = \frac{0.8V}{R_{USBREF}} \quad (A)$$

I_{USBREF} is used for reference current when the battery is charged through USB_PWR; ($I_{USBREF} + I_{REF}$) is used when the battery is charged through DOCK_PWR or ADP_PWR. The charging current I_{CHG} at CCM is 100,000 times of the reference current. Take $R_{USBREF} = 160k\Omega$ and $R_{IREF} = 320k\Omega$ for example, the charging current I_{CHG} at CCM through adaptor is calculated as:

$$I_{CHG} = \left(\frac{0.8V}{160k\Omega} + \frac{0.8V}{320k\Omega} \right) \times 100,000 = 0.75A$$

The end-of-charge current I_{MIN} is set to 1/10 of I_{CHG} and cannot be changed externally.

Total Charge Time

An external timing capacitor C_{TIME} connecting between TIME pin and ground programs a timing reference. The uP8003 charges/discharges the C_{TIME} between 1.5V and 0.5V, both with 10uA current source. The oscillation period is described by the following equation:

$$T_{OSC} = 2 \times 10^5 \times C_{TIME} \quad (\text{second})$$

A 22-stage binary counter counts the timing oscillation and limits the total charge time T_{CHG} for the CCM and CVM. The T_{CHG} can be calculated as:

$$T_{OUT} = 2^{22} \times T_{OSC} = 8.39 \times 10^{11} \times C_{TIME} \quad (\text{second})$$

A 15nF C_{TIME} results in a 3.0ms oscillation period and 3.5 hours charge time. The charger MUST reach the end-of-charge status within T_{OUT} . Otherwise, a TIMEOUT fault is triggered and latches up the charger. Once latched by TIMEOUT fault, the charge can only be reset by CHG_PWR POR or toggling the EN pin.

The TKM also has a time limit of $1/8 T_{OUT}$. A TIMEOUT fault is triggered and latches up the charger if the battery voltage does not reach V_{MIN} within this limit. Therefore, the charge stays in trickle mode for at least $15 \times T_{OSC}$ and, at most $1/8$ of T_{OUT} as shown in Figure 1.

Charge Current Thermal Foldback

Thermal issue always deserved great attentions for a linear charger. The maximum power dissipation usually occurs at the beginning of constant current mode where the uP8003 charge the battery with maximum current and high dropout voltage.

The uP8003 integrated thermal shutdown function avoiding the charger from burning out. The thermal shutdown is triggered and latches up the charger when the junction temperature reaches 150°C typically. The uP8003 also integrates a thermal foldback function to ensure safe operation without triggering thermal shutdown when PCB space is limited for thermal dissipation as shown in Figure 2. The uP8003 automatically reduces the charge current when the junction temperature rises above +120°C to prevent further temperature rise.

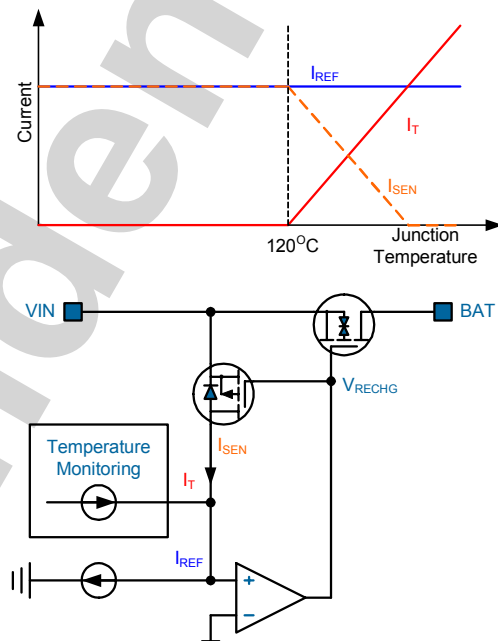


Figure 2. Charge Current Thermal Foldback.

I_{REF} is the current reference set by R_{IREF} connecting between IREF pin and ground. I_T is the current signal from Temperature Monitoring Block. I_T is kept zero and does not affect the charge current if the junction temperature is below +120°C. I_T rises at a rate of 1uA/°C and is added to the sensed current I_{SEN} when the junction temperature is over +120°C. This makes I_{SEN} decrease at a rate of -1uA/°C. The charge current decreases at a rate of -100mA/°C since it is 100,000 times mirrored of I_{SEN} . The charge current is reduced to zero when the junction temperature rises to +130°C for a charger with I_{REF} set to 1.0A. The actual charge current settles between +120°C and +130°C.

The uP8003 asserts end-of-charge only when the charge current is below I_{MIN} at constant voltage mode. If the charge current drops below I_{MIN} due to thermal foldback at constant current mode, the uP8003 will not assert end-of-charge.

Functional Description

NTC Thermistor

Use a NTC thermistor to form a voltage divider at TEMP pin for monitoring the battery pack as shown in Figure 3. CP2 and CP3 are Schmitt Triggers for upper and lower boundary, V_{TMAX} and V_{TMIN} , of temperature window comparator respectively. The uP8003 stops charging and set FAULT# pin low if the voltage at TEMP pin is out of the window. The uP8003 sets FAULT# pin high impedance and starts another charge cycle when the voltage TEMP is within the window again.

The temperature accuracy does not depend on the accuracy of 2.8V bias voltage since both reference voltages V_{TMIN} and V_{TMAX} and voltage at TEMP are percentages of the bias voltage. However, uP8003 provides a 2.8V with 2% high accuracy in case that the TEMP pin voltage is also monitored by other ASIC on the PCB for redundant thermal protection.

The lower temperature boundary is $V_{TMIN} = 1.4V$ that is 1/2 of the 2.8V bias voltage. This needs $R_U = (R_L + R_{TMIN})$ at low temperature limit, where R_U is the pull-high resistor, R_L is the pull-low resistor, and R_{TMIN} is the thermistor resistance at low temperature limit.

On the other hand, the voltage at TEMP pin at high temperature limit should be:

$$2.8V \times \frac{R_L + R_{TMAX}}{R_U + R_L + R_{TMAX}} = 0.35V$$

= 1/6 of the 2.8V bias voltage.

$$(R_L + R_{TMAX}) = (R_L + R_{TMIN}) / 7$$

where R_{TMAX} is the thermistor resistance at high temperature limit. The NTC thermistor must have a resistance ratio of 7:1 at least at the low and the high temperature limits.

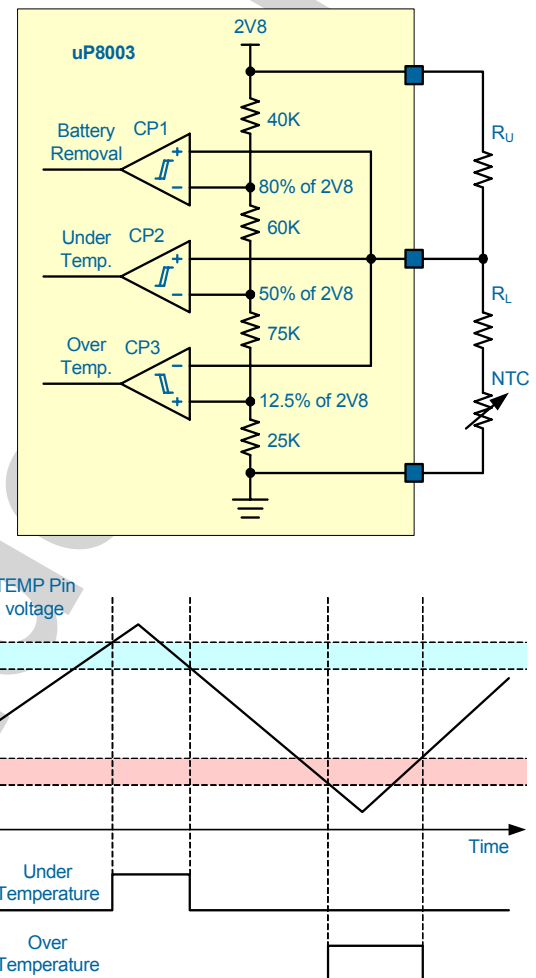


Figure 3. Battery Temperature Monitoring.

Battery Removal Detection

The uP8003 assumes that the NTC thermistor is co-packed with the battery and is removed together with the battery. The TEMP pin is pulled high to 2V8 if the NTC is removed. The uP8003 asserts the removal of battery, stops the charging cycle and sets FAULT# pin low if TEMP voltage is higher than 2.1V. A new charge cycle starts if a battery is inserted again.

For applications that do not support battery thermal detection, set TEMP voltage as 1/3 of 2V8 bias voltage by an external resistive voltage divider.

Indications

The uP8003 has three indications: the input presence, the charge status, and the fault indication. The input presence is indicated by the 2V8 pin while the other two indications are presented by the STAT# pin and FAULT# pin respectively. The 2V8 pin voltage is enabled and regulated typical 2.8V if

Functional Description

input voltage POR is granted and the chip is enabled. This pin is capable of sourcing 2mA output current and can be used as the power present indication. Figure 4 shows the 2V8 pin voltage vs. the input voltage.

The STAT# pin is an open-drain logic output that is pulled low when the charger is in charge states (from the beginning of a charge cycle to the end-of-charge condition is qualified.) The EOC condition is: the battery voltage is within VCH and VRECHG and the charge current falls belows a user programmable EOC current threshold. The STAT# pin is set to high impedance and latched once the EOC condition is granted. The latch is released at the beginning of another charge or recharge cycle.

The FAULT# pin is an open-drain logic output that is pulled when any fault conditions occur. The fault conditions include the external battery temperature fault, the battery removal , or a timeout fault. The STAT# pin is set to high impedance when the fault conditions are removed.

Absolute Maximum Rating

 Supply Input Voltage, V_{ADP} , V_{DOCK} , V_{USB} (Note 1)

DC	-0.3V to +6.5V
DC(No Oprating)	-0.3V to +7.0V
< 200ns	-0.3V to +8.0V

Output Pin Voltage, BAT -0.3V to +6.0V

Signal Input Voltage -0.3V to +3.3V

Signal Output Voltage -0.3V to +6.0V

Charge Current for VQFN 4x4 Package 1.5A

Storage Temperature -65°C to +150°C

Junction Temperature 150°C

Lead Temperature (Soldering, 10 sec) 260°C

ESD Rating (Note 2)

HBM (Human Body Mode) 2kV

MM (Machine Mode) 200V

Thermal Information

Package Thermal Resistance (Note 3)

 VQFN4x4 - 24L θ_{JA} 40°C/W

 VQFN4x4 - 24L θ_{JC} 4°C/W

 Power Dissipation, P_D @ $T_A = 70^\circ\text{C}$

VQFN4x4-24L 2.5W

Recommended Operation Conditions

Operating Junction Temperature Range (Note 4) -40°C to +125°C

Operating Ambient Temperature Range -40°C to +85°C

 Supply Input Voltage, (V_{ADP} , V_{DOCK} , V_{USB}) +4.6V to +5.50V

Electrical Characteristics

 (V_{ADP} , V_{DOCK} , $V_{USB} = 5\text{V}$, $T_A = 25^\circ\text{C}$, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Supply Input						
Supply Input Voltage		ADP_PWR, DOCK_PWR and USB_PWR	4.60	--	5.50	V
Supply Input POR Rising Threshold			4.3	4.4	4.5	V
Supply Input POR Hysteresis		ADP_PWR and DOCK_PWR	--	0.2	--	V
		USB_PWR	--	0.4	--	V
Supply Input Current		ADP_PWR, DOCK_PWR or USB_PWR = 5.5V. BAT, CHG_PWR, WAKE_A/B and SYS_PWR no load. EN = 0V.	--	--	5	mA
Supply Input Pull Low Resistance			--	10	--	k Ω

Electrical Characteristics

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Charge Pump						
Charge Pump Start Up Time	T_{CP}	from supply inputs POR to $V_{CP} = 9V$. $C_{CP} = 4.7nF$	--	4.0	--	ms
Charge Pump Output Voltage	V_{CP}	No Load.	9	10	11	V
Charge Pump Power OK Rising Threshold Level	V_{CP}		--	9.0	--	V
Power Multiplexer						
On Resistance of Q1	R_{Q1}	$V_{ADP} = 4.6V$, $I_{SYS} = 1A$.	--	250	--	$m\Omega$
On Resistance of Q2	R_{Q2}	$V_{DOCK} = 4.6V$, $I_{SYS} = 1A$.	--	250	--	$m\Omega$
On Resistance of Q3	R_{Q3}	$V_{SUB} = 4.6V$, $I_{SYS} = 1A$.	--	250	--	$m\Omega$
Turn On Delay	T_{DLYH}	from supply input POR to CHG_PWR ramps up.	--	1.0	--	ms
Turn Off Delay	T_{DLYL}		--	--	1.0	μs
Supply Input Detection						
Leakage Current	I_{DET}	$V_{ADP} = V_{DOCK} = V_{USB} = 0V$	--	0.1	1.0	μA
Supply Input Detection Output Capability	V_{DET}	$V_{ADP} = V_{DOCK} = V_{USB} = 4.6V$, $I_{DET} = 5mA$	--	--	0.25	V
System Power LDO						
Output Voltage	V_{SYS}	V_{ADP} , V_{DOCK} , or $V_{USB} = 4.6V \sim 5.50V$.	4.2	4.3	4.4	V
Output Voltage Slew Rate		$C_{SYS} = 150\mu F$	--	1.0	--	V/ms
Dropout Voltage	V_{DROP}	$V_{CHG} - V_{SYS}$, $I_{SYS} = 1A$, EN = Low.	--	250	--	mV
Current Limit	I_{LIM}	$V_{SYS} = 0V$	1.5	--	--	A
Current Threshold Level for System Wake Up	I_{LDO}	Current threshold level for WAKE_A and WAKE_B from low to high.	--	20	--	mA
Reverse Leakage Current	I_{LEAK}	$V_{SYS} = 4.2V$, CHG_PWR = Open.	-5	--	5	μA
System Wake Up						
Output Capability	V_{WAKE}	$V_{CHG} - V_{WAKE}$, $I_{WAKE} = 20mA$	--	40	--	mV
USB Monitoring						
USB Monitoring Accuracy	V_{MON}	% of CHG_PWR voltage, $V_{USB} = 4.6V \sim 5.50V$, $I_{MON} = 0mA$,	49	50	51	%
USB Monitoring Output Impedance	Z_{MON}	$V_{USB} = 4.6V \sim 5.50V$, $I_{MON} = 0mA$,	--	50	--	$k\Omega$
Charger Output						
Output Voltage	V_{BAT}		4.158	4.2	4.242	V
Dropout Voltage		$I_{OUT} = 500mA$	--	120	--	mV

Electrical Characteristics

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Charge Current						
Constant Charge Current from USB_PWR	I_{CHG}	$R_{USBREF} = 160k\Omega, V_{BAT} = 3.7V$	450	500	550	mA
Constant Charge Current from ADP_PWR or ADP_PWR	I_{CHG}	$R_{USBREF} = 160k\Omega, R_{IREF} = 160k\Omega, V_{BAT} = 3.7V$	900	1000	1100	mA
Trickle Charge Current from USB_PWR	I_{TRK}	$R_{USBREF} = 160k\Omega, V_{BAT} = 2.6V$	--	50	--	mA
Trickle Charge Current from ADP_PWR, DOCK_PWR	I_{TRK}	$R_{USBREF} = 160k\Omega, R_{IREF} = 160k\Omega, V_{BAT} = 2.6V$	--	100	--	mA
End-of-Charge Threshold from USB_PWR	I_{TER}	$R_{USBREF} = 160k\Omega$	43	50	57	mA
End-of-Charge Threshold from ADP_PWR, DOCK_PWR	I_{TER}	$R_{USBREF} = 160k\Omega, R_{IREF} = 160k\Omega$	85	100	115	mA
Threshold Voltage						
Recharge Voltage Threshold	V_{RCHG}		--	4.0	--	V
Trickle Charge Threshold Voltage	V_{MIN}		2.74	2.8	2.86	V
2V8						
2V8 Output Voltage	V_{2V8}		2.74	2.80	2.86	V
2V8 Soucing Current	I_{2V8}	Decrease to 98% of 2V8	2	--	--	mA
Oscillator						
Oscillation Period	T_{OSC}	$C_{TIME} = 15nF$	2.7	3.0	3.3	ms
Temperature Monitoring						
Low Temperature Threshold	V_{TMIN}	$V_{2V8} = 2.8V$	1.35	1.40	1.45	V
High Temperature Threshold	V_{TMAX}	$V_{2V8} = 2.8V$	332	350	368	mV
Battery Removal Threshold	V_{RMV}	$V_{2V8} = 2.8V$	--	2.24	--	V
Charge Current Foldback Threshold	T_{FOLD}		105	120	135	°C
Current Foldback Gain	G_{FOLD}		--	100	--	mA/°C
Over Temperature Protection			--	150	--	°C
Over Temperature Hysteresis		Hysteresis	--	10	--	°C
Logic Input and Output						
EN and USB_OFF Input High			2.0	--	--	V
EN and USB_OFF Input Low			--	--	0.8	V
STAT# and FAULT# Sink Current		$I_{sink} = 5mA$	--	--	0.25	V

Note 1. Stresses listed as the above "Absolute Maximum Ratings" may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.

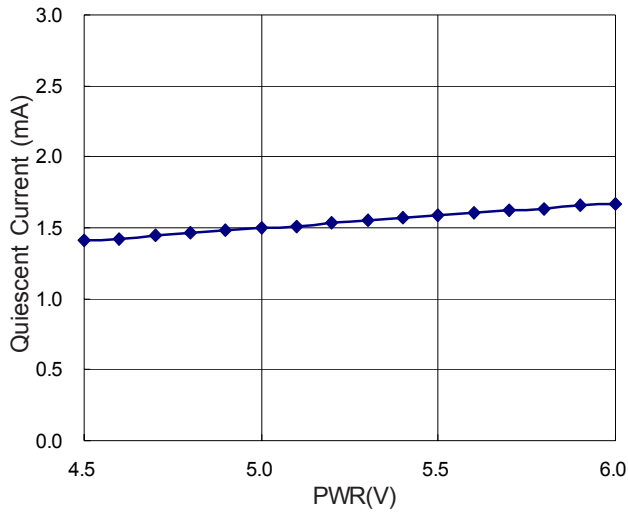
Note 2. Devices are ESD sensitive. Handling precaution recommended.

Note 3. θ_{JA} is measured in the natural convection at $T_A = 25^\circ C$ on a low effective thermal conductivity test board of JEDEC 51-3 thermal measurement standard.

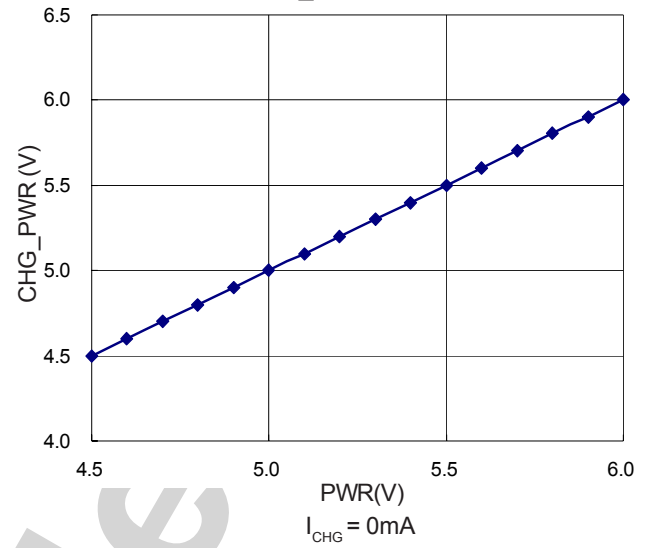
Note 4. The device is not guaranteed to function outside its operating conditions.

Typical Operation Characteristics

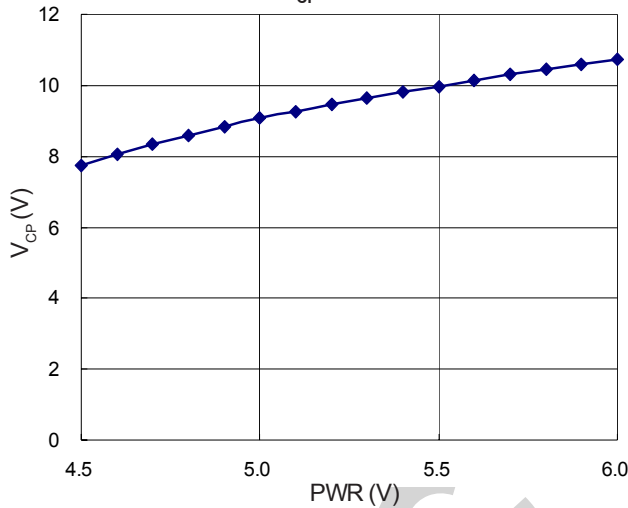
Quiescent Current vs. PWR



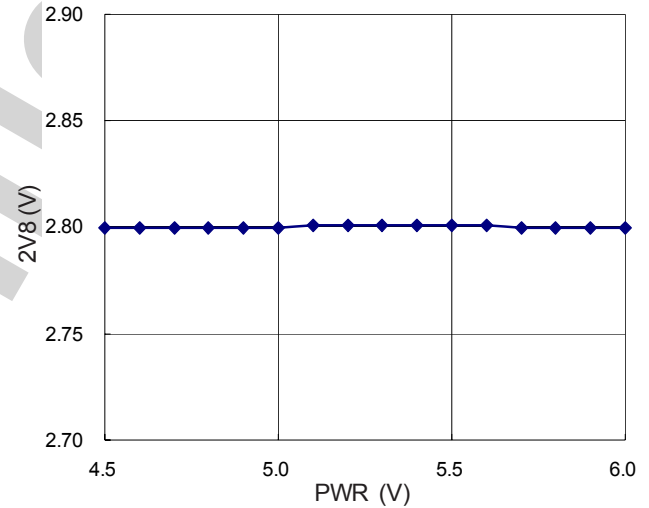
CHG_PWR vs. PWR



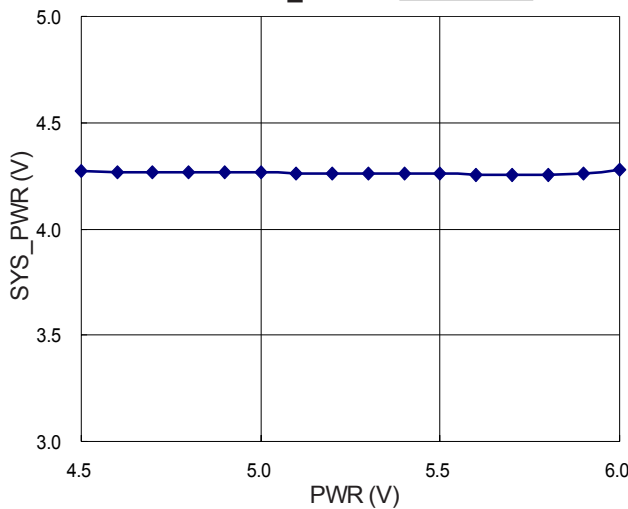
V_{CP} vs. PWR



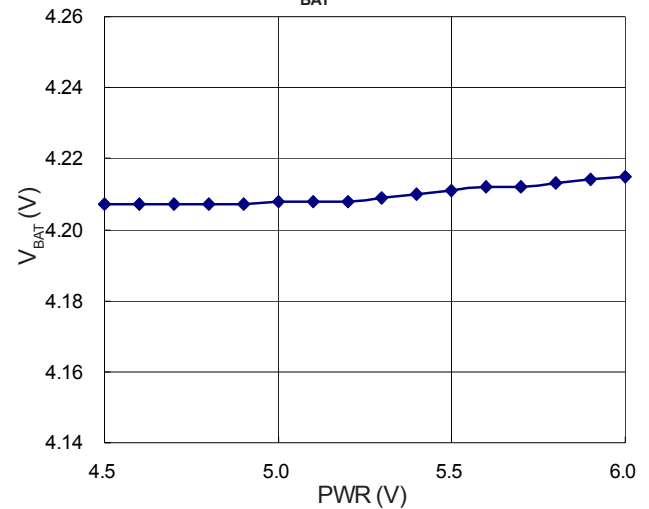
2V8 vs. PWR



SYS_PWR vs. PWR

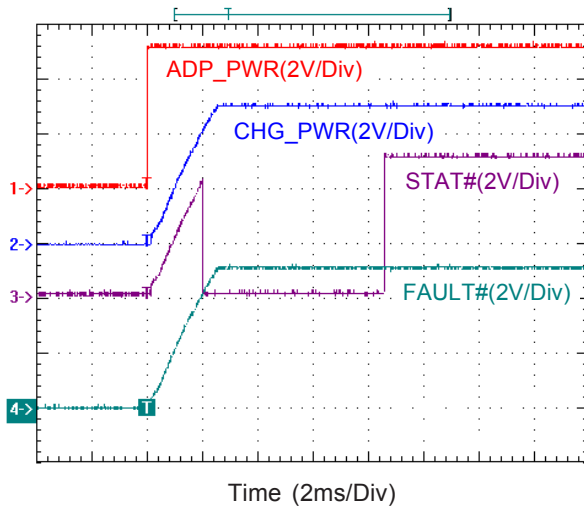


V_{BAT} vs. PWR

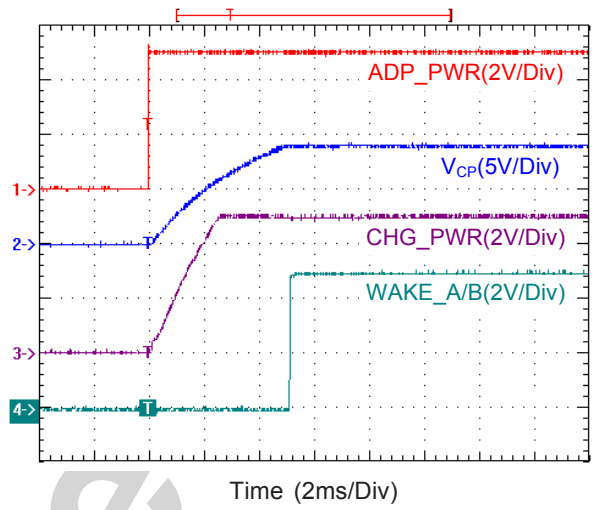


Typical Operation Characteristics

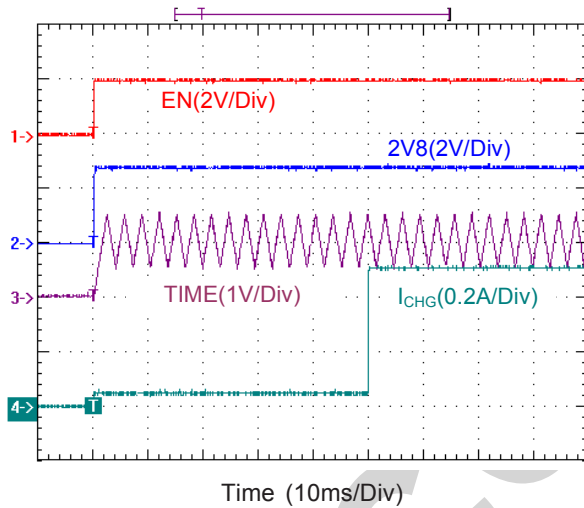
Power On Waveforms



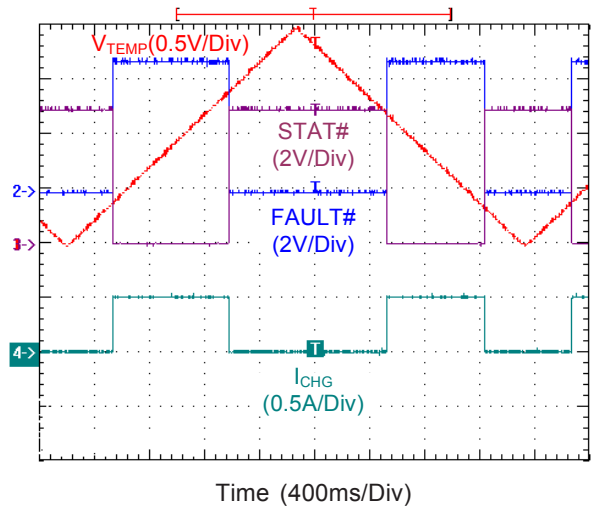
Power On Waveforms



Enable On Waveforms

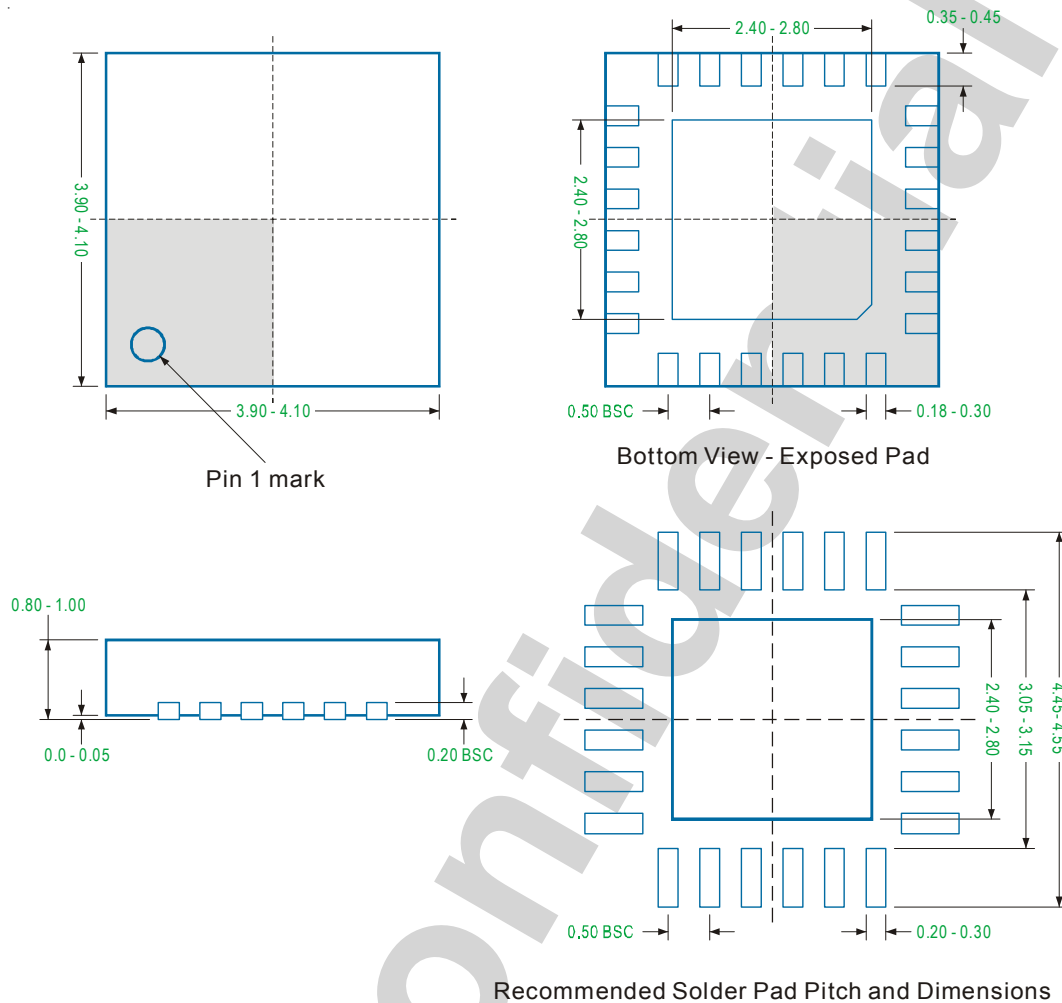


Temp. Waveforms



Package Information

VQFN4x4 - 24L



Note

1. Package Outline Unit Description:

BSC: Basic. Represents theoretical exact dimension or dimension target

MIN: Minimum dimension specified.

MAX: Maximum dimension specified.

REF: Reference. Represents dimension for reference use only. This value is not a device specification.

TYP: Typical. Provided as a general value. This value is not a device specification.

2. Dimensions in Millimeters.

3. Drawing not to scale.

4. These dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm.