Winbond Electronics Corp.

4-BIT MICROCONTROLLER

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1. GENERAL DESCRIPTION

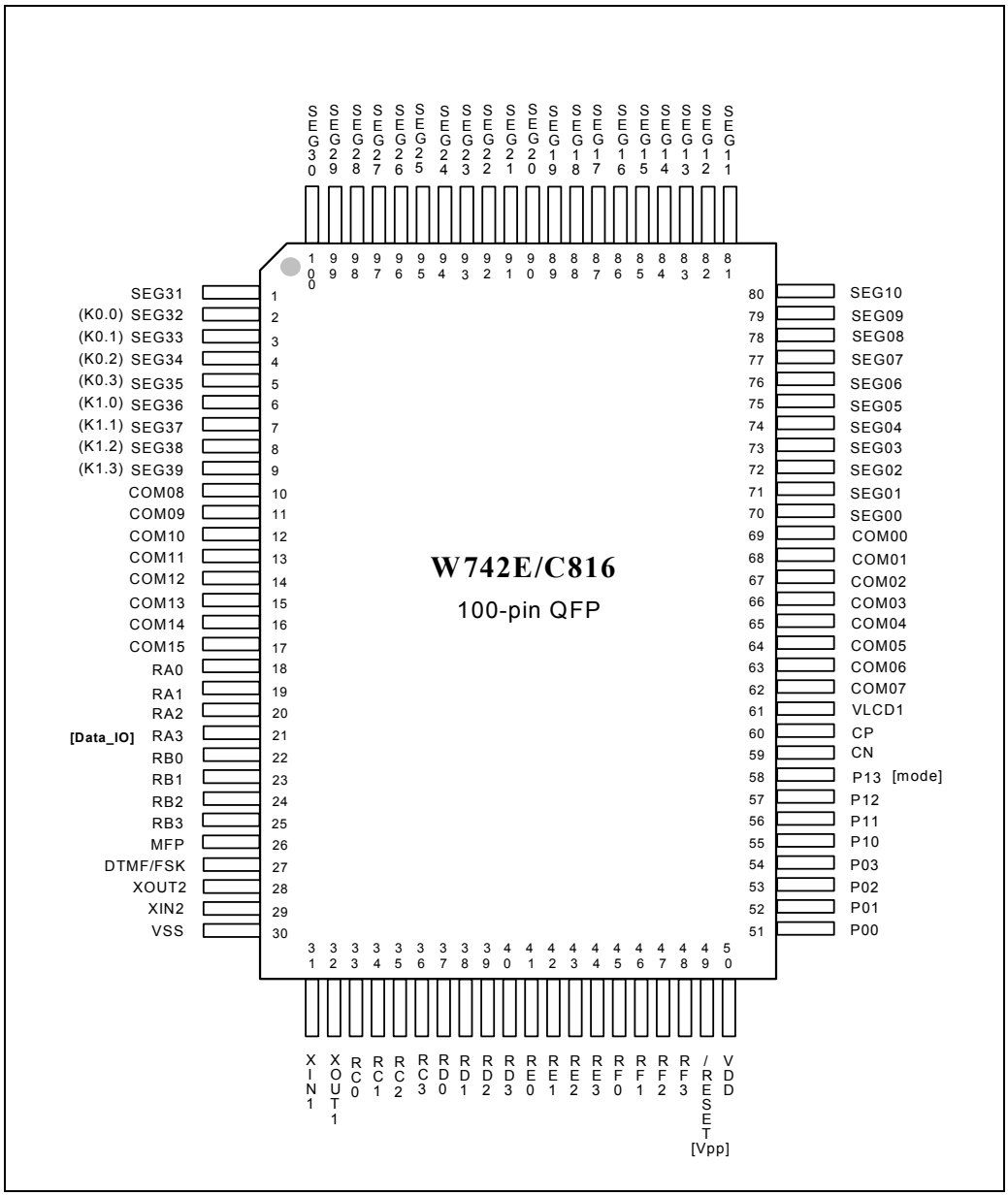
The W742E/C816 [W742E 816 is EEPROM type, W742C816 is mask type] is a high-performance 4-bit microcontroller (μC) that built in 640-dot LCD driver. The device contains a 4-bit ALU, two 8-bit timers, two dividers in dual-clock operation, a 40 × 16 LCD driver, ten 4-bit I/O ports (including 2 output port for LED driving), multiple frequency output, one channel DTMF generator and FSK modulator of CCITT V.23 or Bellcore 202. There are also eleven interrupt sources and 16-level stack buffer. The W742E/C816 operates on very low current and has three power reduction modes, hold mode, stop mode and slow mode, which help to minimize power dissipation.

2. FEATURES

- Operating voltage
  - 2.4V - 6.0V for mask type
  - 2.4V - 4.8V for EEPROM type
- Dual-clock operation
- Main oscillator
  - 3.58 MHz or 400 KHz can be selected by code option
  - Crystal or RC oscillator can be selected by code option
- Sub-oscillator
  - Connect to 32.768 KHz crystal only
- Memory
  - 32768(32K) x 16 bit program ROM (including 64K x 4 bit look-up table)
  - 5120(5K) x 4 bit data RAM (including 16 nibbles x 16 pages working registers)
  - 40 x 16 LCD data RAM
- 40 input/output pins
  - Port for input only: 3 ports/12 pins
  - Input/output ports: 3 ports/12 pins
  - High sink current output port for LED driving: 2 port /8 pins
  - DC output port: 2 ports/ 8 pins (selected by code option)
- Power-down mode
  - Hold mode: no operation (main oscillator and sub-oscillator still operate)
  - Stop mode: no operation (main oscillator and sub-oscillator are stopped)
  - Slow mode: main oscillator is stopped, system is operated by the sub-oscillator (32.768 KHz)

- Eleven interrupt sources
  - Four internal interrupts (Divider0, Divider1, Timer 0, Timer 1)
  - Seven external interrupts (RC.0 – 3, P1.2 ($\overline{INT0}$), Serial Port, P1.3 ($\overline{INT1}$))
- LCD driver output
  - 40 segments x 16 commons
  - 1/8 or 1/16 duty (selected by code option) 1/5 bias driving mode
  - Clock source should be the sub-oscillator clock in the dual-clock operation mode
  - 8 level software LCD contrast adjusting
  - LCD operating voltage source could come from V_{DD} or VLCD1 pin input
- MFP output pin
  - Output is software controlled to generate modulating or non-modulating frequency
  - Works as frequency output specified by Timer 1
  - Key tone generator
- DTMF output pin
  - Output is one channel Dual Tone Multi-Frequency signal for dialing
- FSK output
  - Output FSK signal of CCITT V.23 or Bellcore 202 by mask option
- 8-bit Serial I/O Interface
  - 8-bit transmit/receive mode by internal or external clock source
- Two built-in 14-bit frequency dividers
  - Divider0: the clock source is the main oscillator (F_{OSC})
  - Divider1: the clock source is the sub-oscillator (Fs)
- Two built-in 8-bit programmable countdown timers
  - Timer 0: one of two internal clock frequencies ($F_{OSC}/4$ or $F_{OSC}/1024$) can be selected
  - Timer 1: with auto-reload function and one of two internal clock frequencies (F_{OSC} or $F_{OSC}/64$ or Fs) can be selected (signal output through MFP pin)
- Built-in 18/14-bit watchdog timer selectable for system reset, enable/disable by code option
- 16-level stack buffer
- Packaged in 100-pin QFP

3. PIN CONFIGURATION



4. PIN DESCRIPTION

SYMBOL	I/O	FUNCTION
XIN2	I	Input pin for sub-oscillator. Connected to 32.768 KHz crystal only.
XOUT2	O	Output pin for sub-oscillator with internal oscillation capacitor. Connected to 32.768 KHz crystal only.
XIN1	I	Input pin for main-oscillator. Connected to 3.58 MHz crystal or resistor to generate system clock.
XOUT1	O	Output pin for main-oscillator. Connected to 3.58 MHz crystal or resistor to generate system clock.
RA0 – RA3 Data_IO	I/O	Input/Output port. Input/output mode specified by port mode 1 register (PM1). RA.3: Serial data input/output for EEPROM type
RB0 – RB3	I/O	Input/Output port. Input/output mode specified by port mode 2 register (PM2).
RC0 – RC3	I	Input port only. Each pin has an independent interrupt capability.
RD0 – RD3	I	Input port only. This port can release hold mode but can not occur interrupt service routine.
RE0 – RE3 RF0 – RF3	O	Output port only. CMOS type with high sink current capacity for the LED application.
P00 – P03	I/O	Input/Output port. Input/output mode specified by port mode 6 register (PM6). P0.0 and P0.1 can be a serial I/O interface selected by SIR register. P0.0 indicates serial clock, P0.1indicates serial data.
P10 – P13 Mode	I	Input port only. P1.2 & P1.3 indicates hardware interrupt ($\overline{INT0}$ & $\overline{INT1}$) P1.3: Mode select for EEPROM type
MFP	O	Output pin only, default in low state. This pin can output modulating or nonmodulating frequency, or Timer 1 clock output specified by mode register 1 (MR1).
DTMF/FSK	O	This pin can output dual-tone multi-frequency signal for dialing or FSK signal.
$\overline{RES}$ V_{PP}	I	System reset pin with internal pull-high resistor. V_{PP}: supply programming voltage, without internal pull-high resistor for EEPROM type for avoiding high voltage programming damage
SEG0 – SEG31	O	LCD segment output pins.

Pin Description, continued

SYMBOL	I/O	FUNCTION
COM0 – COM15	O	LCD common signal output pins. The LCD alternating frequency can be selected by code option.
SEG32 – SEG39 (K00 – K03, K10 – K13)	O	LCD segment output pins or DC N-MOS open drain output pins selected by code option.
CP, CN	I	Connection terminals for LCD voltage doubler capacitor (0.1 μF), tuning the capacitor value can reduce the LCD driving current.
VLCD1	I	LCD supply voltage input or connect capacitor (0.1μF) to ground when enable internal pump LCD voltage
VDD	I	Positive power supply (+).
VSS	I	Negative power supply (-).

5. FUNCTIONAL DESCRIPTION

5.1 Program Counter (PC)

Organized as an 15-bit binary counter (PC0 to PC14), the program counter generates the addresses of the 32768(32K) × 16 on-chip ROM containing the program instruction words. When the interrupt or initial reset conditions are to be executed, the corresponding address will be loaded into the program counter directly. From address 0000h to 0023h are reserved for reset and interrupt service routine. The format used is shown below.

Table 1 Vector address and interrupt priority

ITEM	ADDRESS	INTERRUPT PRIORITY
Initial Reset	0000H	-
INT 0 (Divider0)	0004H	1st
INT 1 (Timer 0)	0008H	2nd
INT 2 (Port RC)	000CH	3rd
INT 3 (Port 1.2 ($\overline{INT0}$))	0010H	4th
INT 4 (Divider1)	0014H	5th
INT 5 (Serial I/O or FSK baud rate)	0018H	6th
INT 6 (Port1.3 ($\overline{INT1}$))	001CH	7th
INT 7 (Timer 1)	0020H	8th
Code Start	0024H	-

5.2 Stack Register (STACK)

The stack register is organized as 53 bits x 16 levels (first-in, last-out). When either a call subroutine or an interrupt is executed, the program counter (PC), TAB0, TAB1, TAB2, TAB3, DBKRL, DBKRH, WRP, ROMPR, PAGE, ACC and CF will be pushed into the stack register automatically. At the end of a call subroutine or an interrupt service subroutine, the **RTN** (only restore the program counter) and **RTN #I** instruction could pop the contents of the stack register into the corresponding registers. It can restore part of contents of stack buffer. When the stack register is pushed over the 16th level, the contents of the first level will be overwritten. In the other words, the stack register is always 16 levels deep. The bit definition of #I is listed below.

I = 0000 0000	Pop PC from stack only
Bit0 = 1	Pop TAB0, TAB1, TAB2, TAB3 from stack
Bit1 = 1	Pop DBKRL, DBKRH from stack
Bit2 = 1	Pop WRP from stack
Bit3 = 1	Pop ROMPR from stack
Bit4 = 1	Pop PAGE from stack
Bit5 = 1	Pop ACC from stack
Bit6 = 1	Pop CF from stack

5.3 Program Memory (ROM)

The read-only memory (ROM) is used to store program codes or the look-up table that can be arranged up to 65536(64K) × 4 bits. The program ROM is divided into sixteen pages; the size of each page is 2048(2K) × 16 bits. So the total ROM size is 32768(32K) × 16 bits. Before the jump or subroutine call instructions are to be executed, the destination ROM page register (ROMPR) must be determined firstly. The ROM page can be selected by executing the **MOV ROMPR, #I** or **MOV ROMPR, RAM** instructions. But the branch decision instructions (e.g. JB0, SKB0, JZ, JC, ...) must jump into the same ROM page. **The look-up table area is allocated in lower half part of ROM (PC: 4000H to 7FFFH).** Each look-up table element is composed of 4 bits, so the look-up table can be addressed up to 65536(64K) elements. It uses instructions **MOV TAB0, R MOV TAB1, R MOV TAB2, R MOV TAB3, R** to determine the look-up table element address. The look-up table address is 4 times PC counter, and the offset value is 4000H. Instruction **MOVC R** is used to read the look-up table content and save data into the RAM. The organization of the program memory is shown in Figure 5-1.

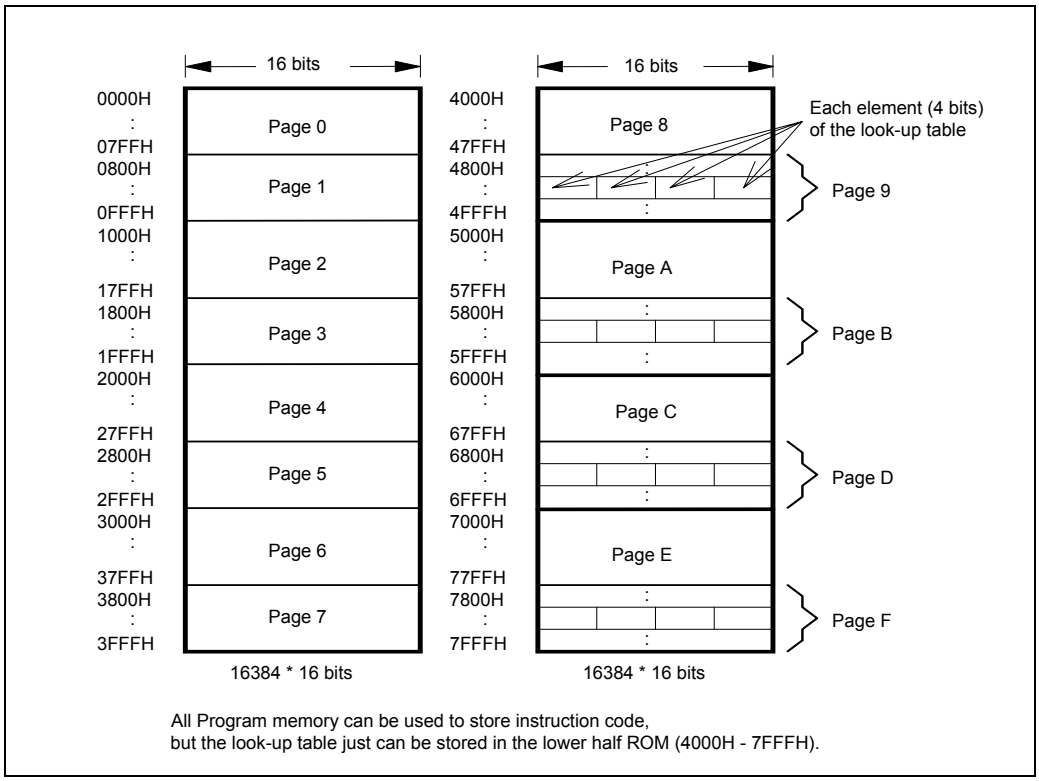


Figure 5-1 Program Memory Organization

5.3.1 ROM Page Register (ROMPR)

The ROM page register is organized as a 4-bit binary register. The bit descriptions are as follows:

	3	2	1	0
ROMPR	R/W	R/W	R/W	R/W

Note: W means write only.

Bit 3, Bit 2, Bit 1, Bit 0 ROM page bits:

0000 = ROM page 0 (0000H – 07FFH)
0001 = ROM page 1 (0800H – 0FFFH)
0010 = ROM page 2 (1000H – 17FFH)
0011 = ROM page 3 (1800H – 1FFFH)
0100 = ROM page 4 (2000H – 27FFH)
0101 = ROM page 5 (2800H – 2FFFH)
1000 = ROM page 8 (4000H – 47FFH)
1001 = ROM page 9 (4800H – 4FFFH)
1010 = ROM page A (5000H – 57FFH)
1011 = ROM page B (5800H – 5FFFH)
1100 = ROM page C (6000H – 67FFH)
1101 = ROM page D (6800H – 6FFFH)

0110 = ROM page 6 (3000H – 37FFH)
0111 = ROM page 7 (3800H – 3FFFH)
1110 = ROM page E (7000H – 77FFH)
1111 = ROM page F (7800H – 7FFFH)

5.3.2 ROM Addressing Mode

1. Direct Addressing

Bit 14-0	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PC	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0

2. Far Jump or Call

Bit 14-0	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PC	P3	P2	P1	P0	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0

P0-3 is ROM page register(ROMPR)

Example:

```
MOV   ROMPR, #I
JMP   Label_A
```

or

```
MOV   ROMPR, #I
CALL  SUB_A
```

3. Conditional JMP

Bit 14-0	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PC	0	0	0	0	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0

jmp into the same page

Example:

```
JB0     Lable_A0
JB1     Lable_A1
JB2     Lable_A2
JB3     Lable_A3
JZ      Label_Az
JNZ     Label_Anz
JC      Label_Ac
JNC     Label_Anc
```

4. Look-up Table

Bit 15-0	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
(PC-4000H)*4	TA33	TA32	TA31	TA30	TA23	TA22	TA21	TA20	TA13	TA12	TA11	TA10	TA03	TA02	TA01	TA00

Look-up table address = (PC address - 4000H) *4

Example:

```
TABLE     TAB_addr              ; Real_TAB_addr (PC value) = TAB_addr/4 + 4000H
00h, 01h, 02h, 0Ah, 0Ch, 0Dh, 0Eh, 0Fh
ENDT

MOV    TAB0, TAB_addr_B0_3 ; set Look-up table address
MOV    TAB1, TAB_addr_B4_7
MOV    TAB2, TAB_addr_B8_11
MOV    TAB3, TAB_addr_B12_15
MOVC   RAM                        ; get Look-up table value to RAM
```

5.4 Data Memory (RAM)

5.4.1 Architecture

The static data memory (RAM) used to store data is arranged up to 5120(5K) × 4 bits. The data RAM is divided into 40 banks; each bank has 128 × 4 bits. Executing the **MOV DBKRL, WR, MOV DBKRH, WR** or **MOV DBKRL, #I, MOV DBKRH, #I** instructions can determine which data bank is used. The data memory can be accessed directly or indirectly and the data bank register has to be confirmed firstly. In the indirect addressing mode, each data bank will be divided into eight pages. The RAM page register has to be setting when in the indirect accessing RAM. The instructions **MOV WRn, @WRq MOV @WRq, WRn** could Read or Write the whole memory in the indirect addressing mode. The RAM address of @WRq indicates to (DBKRH)*800H + (DBKRL)*80H + (RAM page)*10H + (WRq). The organization of the data memory is shown in Figure 5-2.

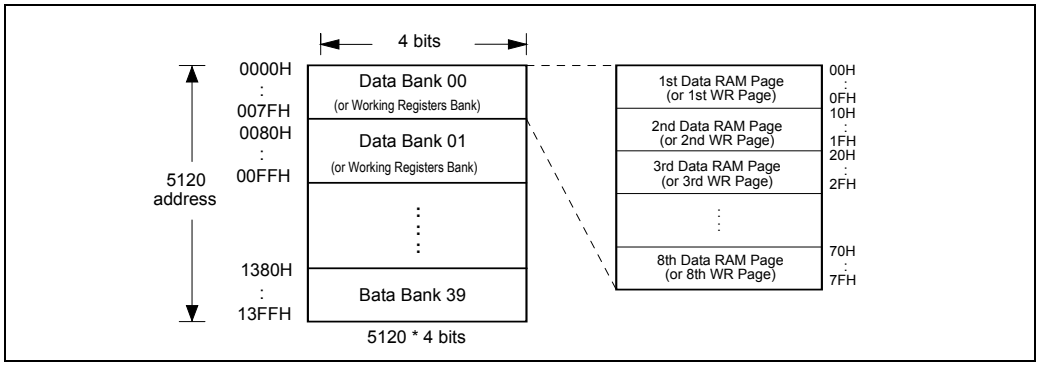


Figure 5-2 Data Memory Organization

The 1st and 2nd data bank (00H to 7FH & 80H to 0FFH) in the data memory can also be used as the working registers (WR). It is also divided into sixteen pages. Each page contains 16 working registers. When one page is used as Working Register, the others can be used as the normal data memory. The WR page register can be switched by executing the MOV WRP, R or MOV WRP, #I instructions. The data memory can not do the logical operation directly with the immediate data, it has to via the Working Register.

5.4.2 RAM Page Register (PAGE)

The page register is organized as a 4-bit binary register. The bit descriptions are as follows:

	3	2	1	0
PAGE	—	R/W	R/W	R/W

Note: R/W means read/write available.

Bit 3 is reserved.

Bit 2, Bit 1, Bit 0 RAM page bits:

000 = Page 0 (00H – 0FH)
001 = Page 1 (10H – 1FH)
010 = Page 2 (20H – 2FH)
011 = Page 3 (30H – 3FH)
100 = Page 4 (40H – 4FH)
101 = Page 5 (50H – 5FH)
110 = Page 6 (60H – 6FH)
111 = Page 7 (70H – 7FH)

5.4.3 WR Page Register (WRP)

The WR page register is organized as a 4-bit binary register. The bit descriptions are as follows:

	3	2	1	0
WRP	R/W	R/W	R/W	R/W

Note: R/W means read/write available.

Bit 3, Bit 2, Bit 1, Bit 0 Working registers page bits:

0000 = WR Page 0 (00H – 0FH)
0001 = WR Page 1 (10H – 1FH)
0010 = WR Page 2 (20H – 2FH)
0011 = WR Page 3 (30H – 3FH)
0100 = WR Page 4 (40H – 4FH)
0101 = WR Page 5 (50H – 5FH)
0110 = WR Page 6 (60H – 6FH)
0111 = WR Page 7 (70H – 7FH)
1000 = WR Page 8 (80H – 8FH)

1001 = WR Page 9 (90H – 9FH)
1010 = WR Page A (A0H – AFH)
1011 = WR Page B (B0H – BFH)
1100 = WR Page C (C0H – CFH)
1101 = WR Page D (D0H – DFH)
1110 = WR Page E (E0H – EFH)
1111 = WR Page F (F0H – FFH)

5.4.4 Data Bank Register (DBKRH, DBKRL)

The data bank register is organized as two 4-bit binary register. The bit descriptions are as follows:

	3	2	1	0
DBKRL	R/W	R/W	R/W	R/W

	3	2	1	0
DBKRH	—	—	R/W	R/W

Note: R/W means read/write available.

Bit5, Bit 4, Bit3, Bit 2, Bit 1, Bit 0 Data memory bank bits:

000000 = Data bank 0 (000H – 07FH)
000001 = Data bank 1 (080H – 0FFH)
000010 = Data bank 2 (100H – 17FH)
000011 = Data bank 3 (180H – 1FFH)
000100 = Data bank 4 (200H – 27FH)
000101 = Data bank 5 (280H – 2FFH)
000110 = Data bank 6 (300H – 37FH)
000111 = Data bank 7 (380H – 3FFH)
001000 = Data bank 8 (400H – 47FH)
001001 = Data bank 9 (480H – 4FFH)
001010 = Data bank 10 (500H – 57FH)
001011 = Data bank 11 (580H – 5FFH)
001100 = Data bank 12 (600H – 67FH)
001101 = Data bank 13 (680H – 6FFH)
001110 = Data bank 14 (700H – 77FH)
001111 = Data bank 15 (780H – 7FFH)
010000 = Data bank 16 (800H – 87FH)
010001 = Data bank 17 (880H – 8FFH)
010010 = Data bank 18 (900H – 97FH)

010011 = Data bank 19 (980H – 9FFH)
010100 = Data bank 20 (0A00H – 0A7FH)
010101 = Data bank 21 (0A80H – 0AFFH)
010110 = Data bank 22 (0B00H – 0B7FH)
010111 = Data bank 23 (0B80H – 0BFFH)
011000 = Data bank 24 (0C00H – 0C7FH)
011001 = Data bank 25 (0C80H – 0CFFH)
011010 = Data bank 26 (0D00H – 0D7FH)
011011 = Data bank 27 (0D80H – 0DFFH)
011100 = Data bank 28 (0E00H – 0E7FH)
011101 = Data bank 29 (0E80H – 0EFFH)
011110 = Data bank 30 (0F00H – 0F7FH)
011111 = Data bank 31 (0F80H – 0FFFH)
100000 = Data bank 32 (1000H – 107FH)
100001 = Data bank 33 (1080H – 10FFH)
100010 = Data bank 34 (1100H – 117FH)
100011 = Data bank 35 (1180H – 11FFH)
100100 = Data bank 36 (1200H – 127FH)
100101 = Data bank 37 (1280H – 12FFH)
100110 = Data bank 38 (1300H – 137FH)
100111 = Data bank 39 (1380H – 13FFH)

5.4.5 RAM Addressing Mode

1. Direct Addressing

Bit 12-0	12	11	10	9	8	7	6	5	4	3	2	1	0
RAM addr	BH1	BH0	BL3	BL2	BL1	BL0	RA6	RA5	RA4	RA3	RA2	RA1	RA0

RA0-6 is RAM address ; BL0-3 is DBKRL register ; BH0-1 is DBKRH register

Example:

```
MOV     DBKRL, #BL_value        ; set RAM bank
MOV     DBKRH, #BH_value
MOV     A, RAM                  ; get RAM data to ACC
```

2. Working Register Addressing

Bit 7-0	7	6	5	4	3	2	1	0
RAM addr	WP3	WP2	WP1	WP0	WA3	WA2	WA1	WA0

WA0-3 is Working register address ; WP0-3 is WR page register(WRP)

Example:

```
MOV     DBKRL, #BL_value      ; set RAM bank
MOV     DBKRH, #BH_value
MOV     WRP, #I               ; set WR page register
MOVA    WRn, RAM              ; mov RAM data to Working register and ACC
```

3. Indirect Addressing

Bit 12-0	12	11	10	9	8	7	6	5	4	3	2	1	0
RAM addr	BH1	BH0	BL3	BL2	BL1	BL0	DP2	DP1	DP0	(WA3	WA2	WA1	WA0)

(WA0-3) is Working register contents ; DP0-3 is RAM page register(PAGE)
BL0-3 is DBKRL register ; BH0-1 is DBKRH register

Example:

```
MOV     DBKRL, BL_value       ; set RAM bank
MOV     DBKRH, BH_value
MOV     PAGE, #Ip             ; set RAM page address, (0 – 07H)
MOV     WRq, #In              ; set WR pointer address; (0 – 0FH)
MOV     WRn, @WRq             ; get the contents of WRq pointing addr to WRn
```

5.5 Accumulator (ACC)

The accumulator (ACC) is a 4-bit register used to hold results from the ALU and transfer data between the memory, I/O ports, and registers.

5.6 Arithmetic and Logic Unit (ALU)

This is a circuit which performs arithmetic and logic operations. The ALU provides the following functions:

- Logic operations: ANL, XRL, ORL
- Branch decisions: JB0, JB1, JB2, JB3, JNZ, JZ, JC, JNC, DSKZ, DSKNZ, SKB0, SKB1, SKB2, SKB3
- Shift operations: SHRC, RRC, SHLC, RLC
- Binary additions/subtractions: ADC, SBC, ADD, SUB, ADU, DEC, INC

After any of the above instructions is executed, the status of the carry flag (CF) and zero flag (ZF) is stored in the internal registers. CF can be read out by executing MOV R, CF.

5.7 Main Oscillator

The W742E/C816 provides a crystal oscillation circuit to generate the system clock through external connections. The 3.58 MHz or 400 KHz crystal must be connected to XIN1 and XOUT1, and a capacitor must be connected to XIN1 and VSS if an accurate frequency is needed.

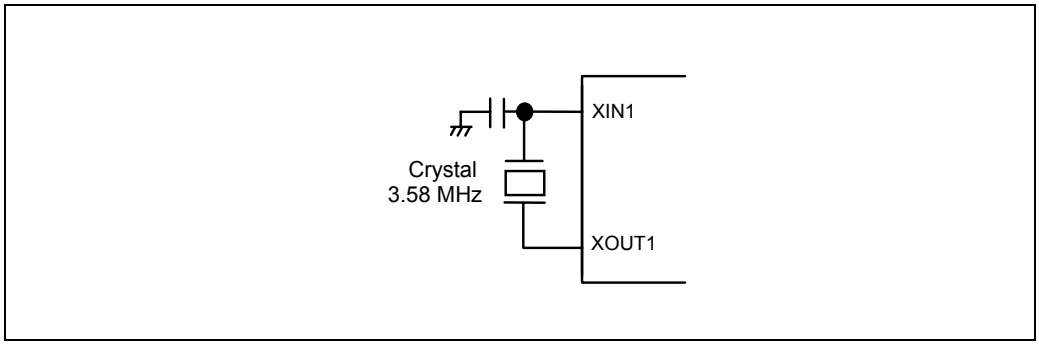


Figure 5-3. System Clock Oscillator Configuration

5.8 Sub-oscillator

The sub-oscillator is used in dual-clock operation mode. In the sub-oscillator application, just only the 32768 Hz crystal could be connected to XIN2 and XOUT2.

5.9 Dividers

Divider 0 is organized with a 14-bit binary up-counter that is designed to generate periodic interrupt. When the main clock starts action, the Divider0 is incremented by each clock (FOSC). The main clock can come from main oscillator or sub-oscillator by setting SCR register. When an overflow occurs, the Divider0 event flag is set to 1 (EVF.0 = 1). Then, if the Divider0 interrupt enable flag has been set (IEF.0 = 1), the interrupt is executed, while if the hold release enable flag has been set (HEF.0 = 1), the hold state is terminated. And the last 4-stage of the Divider0 can be reset by executing **CLR DIVR0** instruction. If the main clock is connected to the 32.768 KHz crystal, the EVF.0 will be set to 1 periodically at the period of 500 mS.

Divider 1 is orginized with 13/12 bits up-counter that only has sub-oscillator clock source. If the sub-oscillator starts action, the Divider1 is incremented by each clock (Fs). When an overflow occurs, the Divider1 event flag is set to 1 (EVF.4 = 1). Then, if the Divider1 interrupt enable flag has been set (IEF.4 = 1), the interrupt is executed, while if the hold release enable flag has been set (HEF.4 = 1), the hold state is terminated. And the last 4-stage of the Divider1 can be reset by executing CLR DIVR1 instruction. There are two period time (125 mS & 250 mS) that can be selected by setting the SCR.3 bit. When SCR.3 = 0 (default), the 250 mS period time is selected; SCR.3 = 1, the 125 mS period time is selected.

5.10 Dual-clock Operation

In this dual-clock mode, the normal operation is performed by generating the system clock from the main-oscillator clock (Fm). As required, the slow operation can be performed by generating the system clock from the sub-oscillator clock (Fs). The exchange of the normal operation and the slow operation is performed by setting the bit 0 of the System clock Control Register (SCR). If the SCR.0 is set to 0, the clock source of the system clock generator is main-oscillator clock; if the SCR.0 is set to 1, the clock source of the system clock generator is sub-oscillator clock. In the dual-clock mode, the main-oscillator can stop oscillating when the SCR.1 is set to 1. When the main clock switch, we must care the following cases:

1. X000B → X011B (FOSC = Fm→ FOSC = Fs): we should not exchange the FOSC from Fm into Fs and disable Fm simultaneously. We could first exchange the FOSC from Fm into Fs, then disable the main-oscillator. So it should be **X000B→X001B→X011B**.
2. X011B → X000B (FOSC = Fs→ FOSC = Fm): we should not enable Fm and exchange the FOSC from Fs into Fm simultaneously. We could first enable the main-oscillator; the 2nd step is calling a delay subroutine to wait the main-oscillator oscillating stabely; then exchange the FOSC from Fs into Fm is the last step. So it should be **X011B→X001B→delay the Fm oscillating stable time→X000B**.

We must remember that the X010B state is inhibitive, because it will induce the system shutdown.

The organization of the dual-clock operation mode is shown in Figure 5-4.

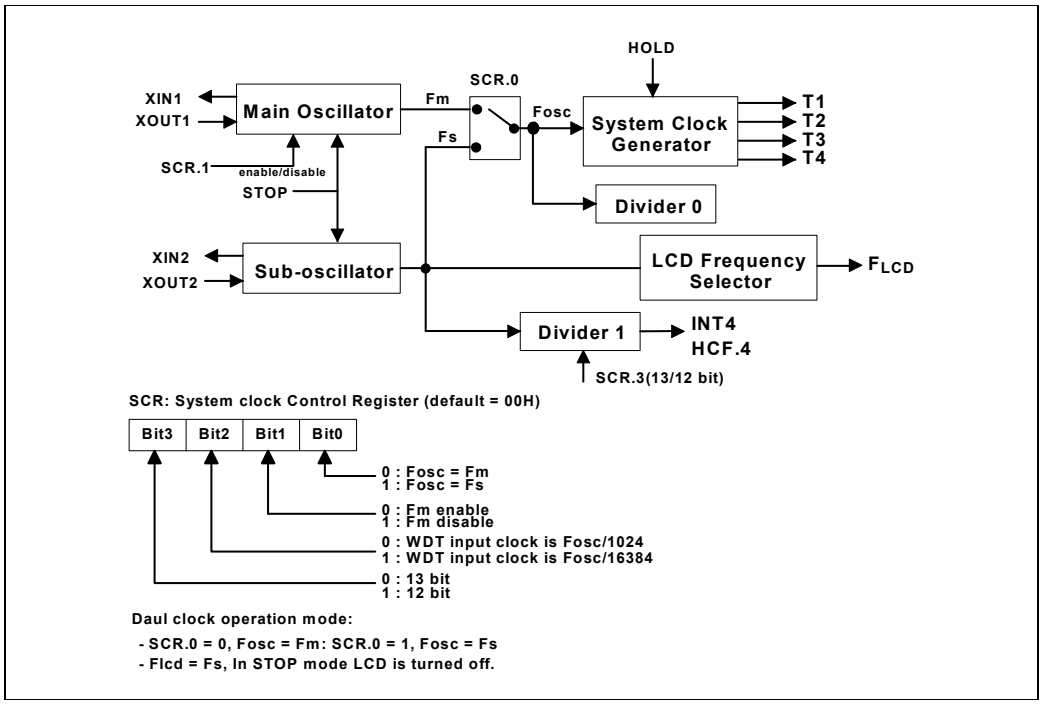


Figure 5-4. Organization of the dual-clock operation mode

5.11 Watchdog Timer (WDT)

The watchdog timer (WDT) is organized as a 4-bit up counter designed to prevent the program from unknown errors. The WDT can be enabled by mask option code. If the WDT overflows, the chip will be reset. At initial reset, the input clock of the WDT is FOSC/1024. The input clock of the WDT can be switched to FOSC/16384 by setting SCR.2 register. The contents of the WDT can be reset by the instruction CLR WDT. In normal operation, the application program must reset WDT before it overflows. A WDT overflow indicates that operation is not under control and the chip will be reset. The WDT overflow period is about 500 mS when the system clock (FOSC) is 32 KHz and WDT clock input is FOSC/1024. The organization of the Divider0 and watchdog timer is shown in Figure 5-5. The minimum WDT time interval is 1/(FOSC/16384 x 16) - 1/(FOSC/16384).

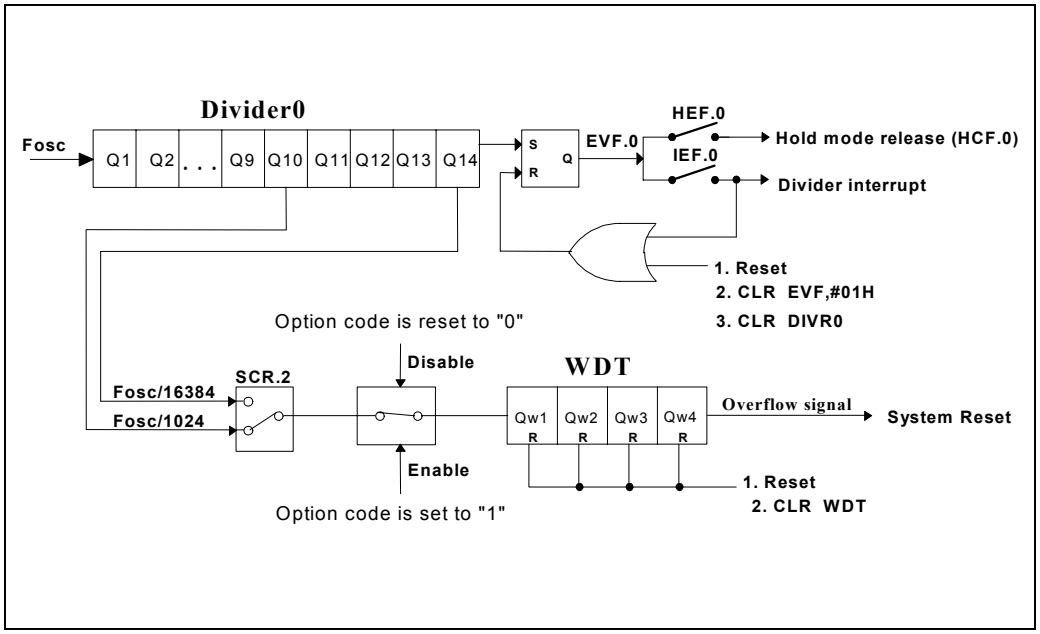


Figure 5-5. Organization of Divider0 and Watchdog Timer

5.12 Timer/Counter

5.12.1 Timer 0 (TM0)

Timer 0 (TM0) is a programmable 8-bit binary down-counter. The specified value can be loaded into TM0 by executing the **MOV TM0L(TM0H), R** instructions. When the MOV TM0L(TM0H), R instructions are executed, it will stop the TM0 down-counting (if the TM0 is down-counting) and reset the MR0.3 to 0, and the specified value can be loaded into TM0. Then we can set MR0.3 to 1, that will cause the event flag 1 (EVF.1) is reset and the TM0 starts to down count. When it decrements to FFH, Timer 0 stops operating and generates an underflow (EVF.1 = 1). Then, if the Timer 0 interrupt enable flag has been set (IEF.1 = 1), the interrupt is executed, while if the hold release enable flag 1 has been set (HEF.1 = 1), the hold state is terminated. The Timer 0 clock input can be set as FOSC/1024 or FOSC/4 by setting MR0 bit 0. The default timer value is FOSC/4. The organization of Timer 0 is shown in Figure 5-6.

If the Timer 0 clock input is FOSC/4:

Desired Timer 0 interval = (preset value +1) × 4 × 1/FOSC

If the Timer 0 clock input is FOSC/1024:

Desired Timer 0 interval = (preset value +1) × 1024 × 1/FOSC

Preset value: Decimal number of Timer 0 preset value

FOSC: Clock oscillation frequency

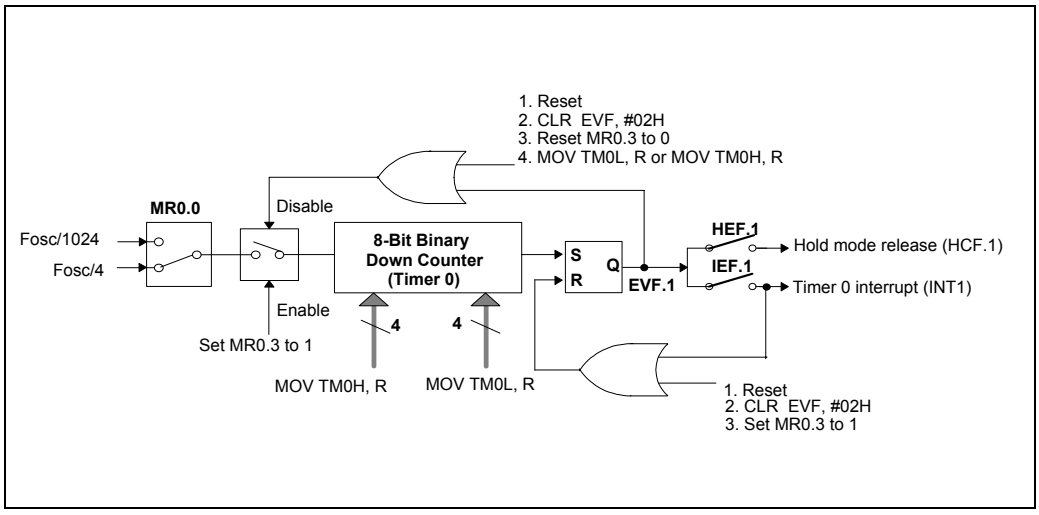


Figure 5-6 Organization of Timer 0

5.12.2 Timer 1 (TM1)

Timer 1 (TM1) is also a programmable 8-bit binary down counter, as shown in Figure 5-7. Timer 1 can output an arbitrary frequency to the MFP pin. The input clock of Timer 1 can be one of three sources: FOSC/64, FOSC or FS. The source can be selected by setting bit 0 and bit 1 of mode register 1 (MR1). At initial reset, the Timer 1 clock input is FOSC. When the **MOV TM1L, R** or **MOV TM1H, R** instruction is executed, the specified data are loaded into the auto-reload buffer and the TM1 down-counting will be disabled that is MR1.3 is reset to 0 at the same time. If the bit 3 of MR1 is set (MR1.3 = 1), the content of the auto-reload buffer will be loaded into the TM1 down counter, and Timer 1 starts to down count, and the event flag 7 is reset (EVF.7 = 0). When the timer decrements to 0FFH, it will generate an underflow (EVF.7 = 1) and be auto-reloaded with the specified data, after which it will continue to count down. Then, if interrupt enable flag 7 has been set to 1 (IEF.7 = 1), an interrupt is executed; if hold mode release enable flag 7 is set to 1 (HEF.7 = 1), the hold state is terminated. The specified frequency of Timer 1 can be delivered to the MFP output pin by programming bit 2 of MR1. Bit 3 of MR1 can be used to make Timer 1 stop or start counting.

In a case where Timer 1 clock input is FT:

Desired Timer 1 interval = (preset value +1) / FT

Desired frequency for MFP output pin = FT ÷ (preset value + 1) ÷ 2 (Hz)

Preset value: Decimal number of Timer 1 preset value

FOSC: Clock oscillation frequency

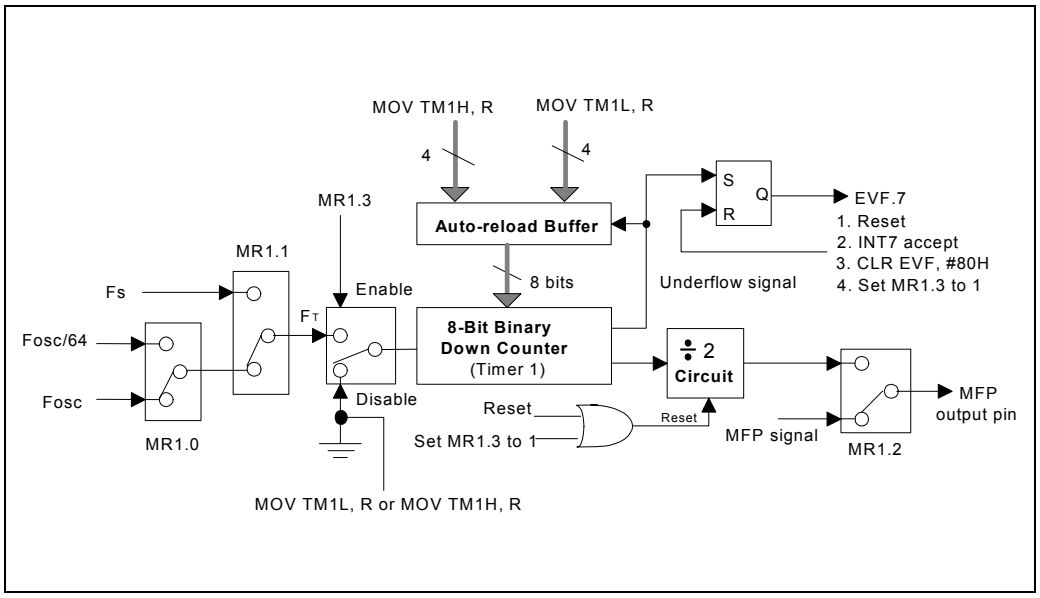


Figure 5-7. Organization of Timer 1

For example, when FT equals 32768 Hz, depending on the preset value of TM1, the MFP pin will output a single tone signal in the tone frequency range from 64 Hz to 16384 Hz. The relation between the tone frequency and the preset value of TM1 is shown in the table below.

Table 2 The relation between the tone frequency and the preset value of TM1

		3rd Octave			4th Octave			5th Octave		
		Tone Frequency	TM1 Preset Value & MFP	Frequency	Tone Frequency	TM1 Preset Value & MFP	Frequency	Tone Frequency	TM1 Preset Value & MFP	Frequency
TONE	C	130.81	7CH	131.07	261.63	3EH	260.06	523.25	1EH	528.51
	C#	138.59	75H	138.84	277.18	3AH	277.69	554.37	1CH	564.96
	D	146.83	6FH	146.28	293.66	37H	292.57	587.33	1BH	585.14
	D#	155.56	68H	156.03	311.13	34H	309.13	622.25	19H	630.15
	E	164.81	62H	165.49	329.63	31H	327.68	659.26	18H	655.36
	F	174.61	5DH	174.30	349.23	2EH	372.36	698.46	16H	712.34
	F#	185.00	58H	184.09	369.99	2BH	390.09	739.99	15H	744.72
	G	196.00	53H	195.04	392.00	29H	420.10	783.99	14H	780.19
	G#	207.65	4EH	207.39	415.30	26H	443.81	830.61	13H	819.20
	A	220.00	49H	221.40	440.00	24H	442.81	880.00	12H	862.84
	A#	233.08	45H	234.05	466.16	22H	468.11	932.23	11H	910.22
	B	246.94	41H	248.24	493.88	20H	496.48	987.77	10H	963.76

Note: Central tone is A4 (440 Hz).

5.12.3 Mode Register 0 (MR0)

Mode Register 0 is organized as a 4-bit binary register (MR0.0 to MR0.3). MR0 can be used to control the operation of Timer 0. The bit descriptions are as follows:

	3	2	1	0
MR0	W	—	—	W

Note: W means write only.

Bit 0 = 0 The fundamental frequency of Timer 0 is FOSC/4.
= 1 The fundamental frequency of Timer 0 is FOSC/1024.
Bit 1 & Bit 2 are reserved
Bit 3 = 0 Timer 0 stops down-counting.
= 1 Timer 0 starts down-counting.

5.12.4 Mode Register 1 (MR1)

Mode Register 1 is organized as a 4-bit binary register (MR1.0 to MR1.3). MR1 can be used to control the operation of Timer 1. The bit descriptions are as follows:

	3	2	1	0
MR1	W	W	W	W

Note: W means write only.

Bit 0 = 0 The internal fundamental frequency of Timer 1 is FOSC.
= 1 The internal fundamental frequency of Timer 1 is FOSC/64.
Bit 1 = 0 The fundamental frequency source of Timer1 is the internal clock.
= 0 The fundamental frequency source of Timer1 is the sub-oscillator frequency Fs (32.768 KHz).
Bit 2 = 0 The specified waveform of the MFP generator is delivered at the MFP output pin.
= 1 The specified frequency of Timer 1 is delivered at the MFP output pin.
Bit 3 = 0 Timer 1 stops down-counting.
= 1 Timer 1 starts down-counting.

5.13 Interrupts

The W742E/C816 provides four internal interrupt sources (Divider 0, Divider 1, Timer 0, Timer 1) and seven external interrupt source (port P1.2 ($\overline{INT0}$), RC.0-3, Serial port, P1.3 ($\overline{INT1}$)). Vector addresses for each of the interrupts are located in the range of program memory (ROM) addresses 004H to 023H. The flags IEF, PEF, and EVF are used to control the interrupts. When EVF is set to "1" by hardware and the corresponding bits of IEF and PEF have been set by software, an interrupt is generated. **When an interrupt occurs, the corresponding bit of EVF will be clear, and all of the interrupts will be inhibited until the EN INT or MOV IEF, #I instruction is invoked**. **Normally, the EN INT instruction will be asserted before the RTN instruction**. The interrupts can also be disabled by executing the DIS INT instruction. When an interrupt is generated in the hold mode, the hold mode will be released momentarily and interrupt service routine will be executed. After executing interrupt service routine, the μC will enter hold mode automatically. The operation flow chart is shown in Figure 5-9. The control diagram is shown Figure 5-8.

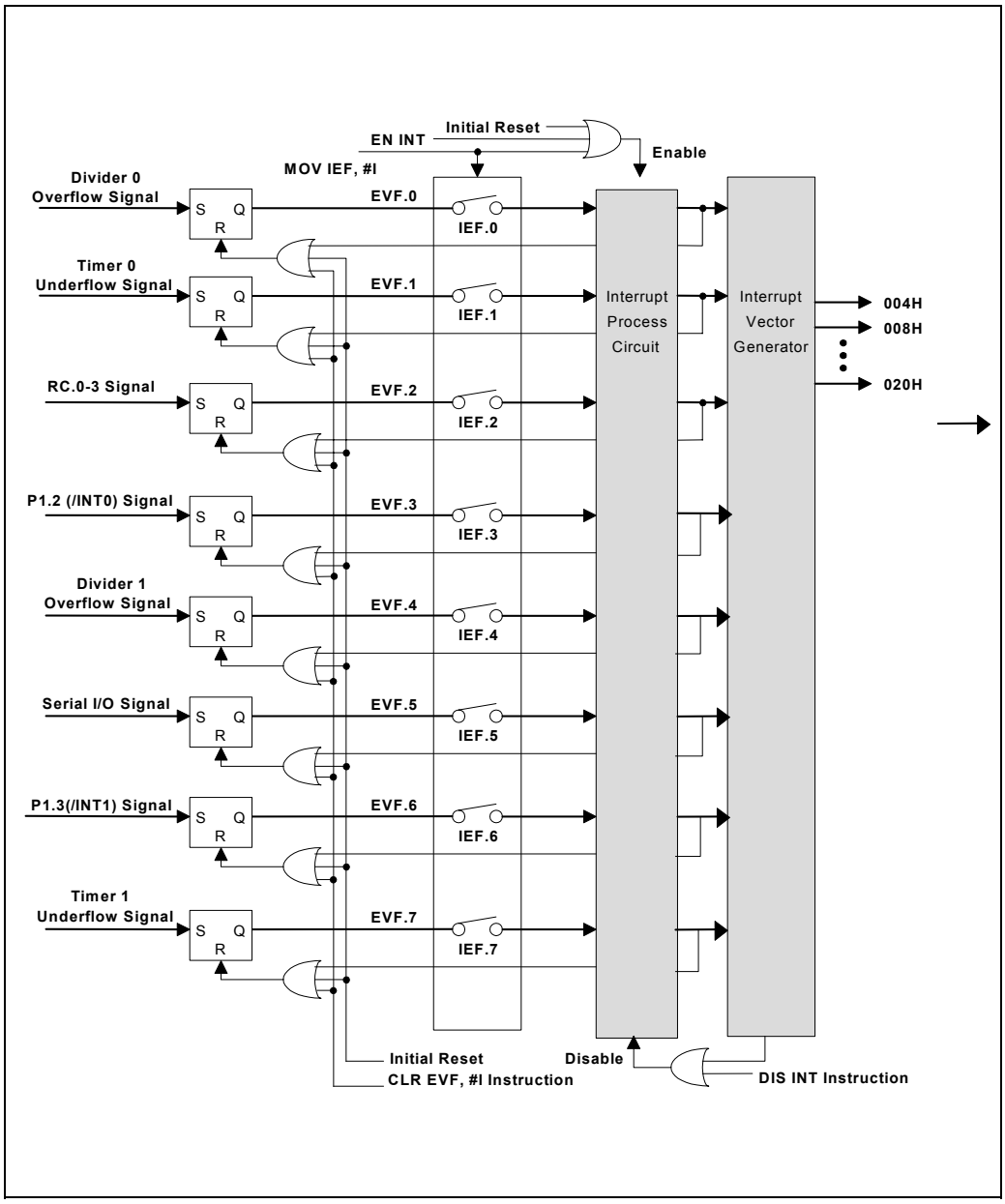


Figure 5-8. Interrupt event control diagram

5.14 Stop Mode Operation

In stop mode, all operations of the µC cease. The µC enters stop mode when the STOP instruction is executed and exits stop mode when an external trigger is activated (by a falling signal on the RC or RD port). When the designated signal is accepted, the µC awakens and executes the next instruction. In the dual-clock slow operation mode, the STOP instruction will disable both the main-oscillator and sub-oscillator oscillating; to avoid erroneous execution, the NOP instruction should follow the STOP command.

5.14.1 Stop Mode Wake-up Enable Flag for RC and RD Port (SEF)

The stop mode wake-up flag for port RC and RD is organized as an 8-bit binary register (SEF.0 to SEF.7). Before port RC and RD can be used to exit the stop mode, the content of the SEF must be set first. The SEF is controlled by the **MOV SEF, #I** instruction. The bit descriptions are as follows:

	7	6	5	4	3	2	1	0
SEF	w	w	w	w	w	w	w	w

Note: W means write only.

SEF.0 = 1 Device will exit stop mode when a falling edge signal is applied to pin RC.0
SEF.1 = 1 Device will exit stop mode when a falling edge signal is applied to pin RC.1
SEF.2 = 1 Device will exit stop mode when a falling edge signal is applied to pin RC.2
SEF.3 = 1 Device will exit stop mode when a falling edge signal is applied to pin RC.3
SEF.4 = 1 Device will exit stop mode when a falling edge signal is applied to pin RD.0
SEF.5 = 1 Device will exit stop mode when a falling edge signal is applied to pin RD.1
SEF.6 = 1 Device will exit stop mode when a falling edge signal is applied to pin RD.2
SEF.7 = 1 Device will exit stop mode when a falling edge signal is applied to pin RD.3

5.15 Hold Mode Operation

In hold mode, all operations of the µC cease, except for the operation of the oscillator, Timer, Divider, and LCD driver. The µC enters hold mode when the HOLD instruction is executed. The hold mode can be released in one of nine ways: by the action of timer 0, timer 1, divider 0, divider 1, RC port, P1.2 ($\overline{INT0}$), Serial I/O, P1.3 ($\overline{INT1}$) and RD port. Before the device enters the hold mode, the HEF, HEFD, PEF, and IEF flags must be set to control the hold mode release conditions. When any of the HCF bits is "1," the hold mode will be released. Regarding to RC and RD port, PSR0 and PSR1 registers indicate signal change on which pin of the port. The HCF and HCFD are set by hardware and clear by software. When EVF, EVFD and HEF, HEFD have been reset by the **CLR EVF, #I CLR EVFD** and **MOV HEF, #I CLR HEFD** instructions, the corresponding bit of HCF, HCFD is reset simultaneously. The HCF and HCFD should be clear every time before enter the hold mode. For more details, refer to the following flow chart.

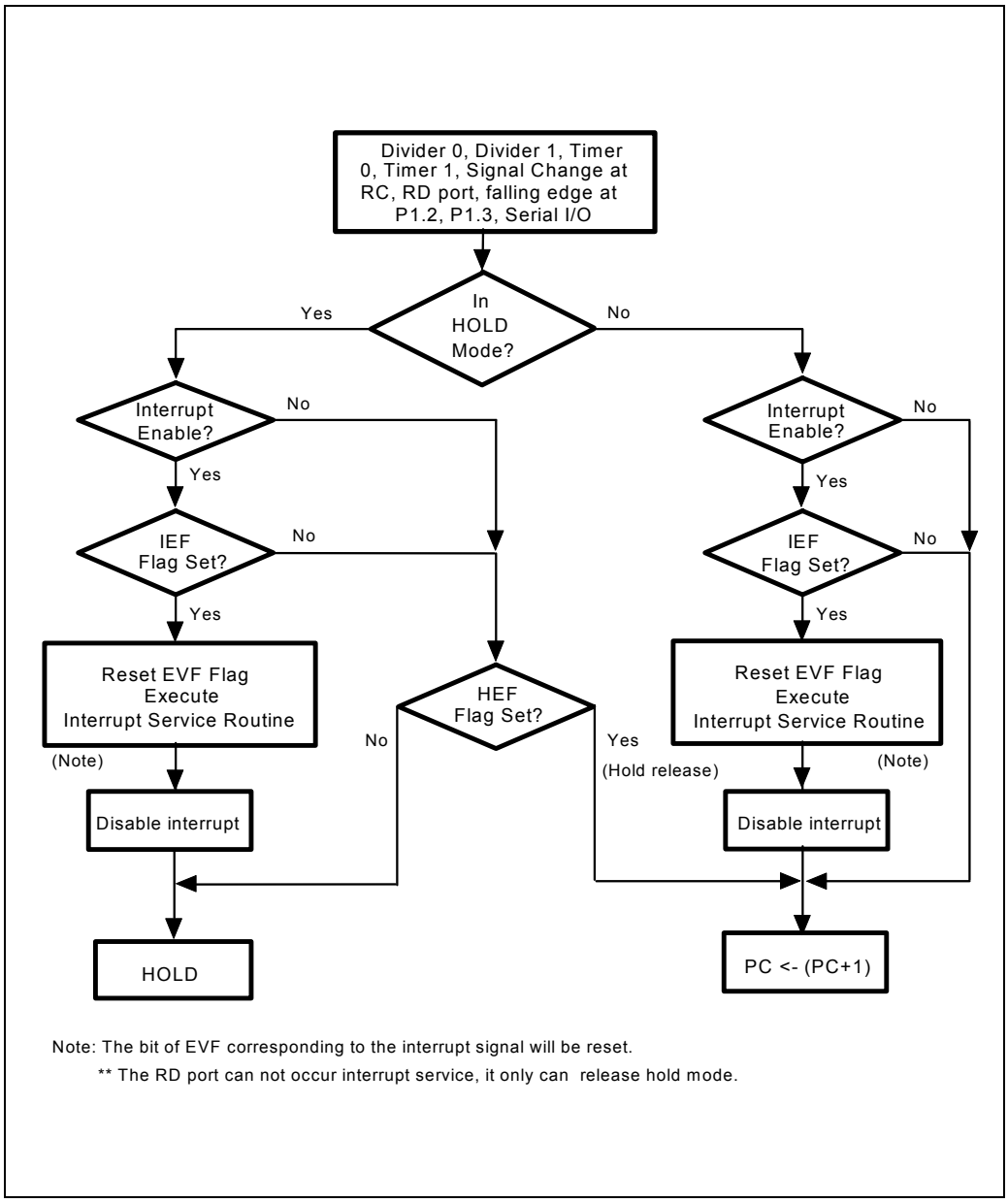


Figure 5-9. Hold Mode and Interrupt Operation Flow Chart

5.15.1 Hold Mode Release Enable Flag (HEF, HEFD)

The hold mode release enable flag is organized on an 8-bit binary register (HEF.0 to HEF.7) and a 1-bit register (HEFD). The HEF and HEFD are used to control the hold mode release conditions. It is controlled by the MOV HEF, #I, MOV HEFD, #I instructions. The bit descriptions are as follows:

	7	6	5	4	3	2	1	0
HEF	w	w	w	w	w	w	w	w

	0
HEFD	w

Note: W means write only.

HEF.0 = 1 Overflow from the Divider 0 causes Hold mode to be released.
HEF.1 = 1 Underflow from Timer 0 causes Hold mode to be released.
HEF.2 = 1 Signal change at port RC causes Hold mode to be released.
HEF.3 = 1 Falling edge signal at port P1.2 ($\overline{INT0}$) causes Hold mode to be released.
HEF.4 = 1 Overflow from the Divider 1 causes Hold mode to be released.
HEF.5 = 1 Serial I/O
HEF.6 = 1 Falling edge signal at port P1.3 ($\overline{INT1}$) causes Hold mode to be released.
HEF.7 = 1 Underflow from Timer 1 causes Hold mode to be released.
HEFD = 1 Signal change at port RD causes Hold mode to be released.

5.15.2 Interrupt Enable Flag (IEF)

The interrupt enable flag is organized as a 8-bit binary register (IEF.0 to IEF.7). These bits are used to control the interrupt conditions. It is controlled by the **MOV IEF, #I** instruction. When one of these interrupts is occurred, the corresponding event flag will be clear, but the other bits are unaffected. In interrupt subroutine, these interrupts will be disable till the instruction MOV IEF, #I **or EN INT** is executed again. However, these interrupts can be disable by executing **DIS INT** instruction. The bit descriptions are as follows:

	7	6	5	4	3	2	1	0
IEF	w	w	w	w	w	w	w	w

Note: W means write only.

IEF.0 = 1 Interrupt 0 is accepted by overflow from the Divider 0.
IEF.1 = 1 Interrupt 1 is accepted by underflow from the Timer 0.
IEF.2 = 1 Interrupt 2 is accepted by a signal change at port RC.
IEF.3 = 1 Interrupt 3 is accepted by a falling edge signal at port P1.2 ($\overline{INT0}$).
IEF.4 = 1 Interrupt 4 is accepted by overflow from the Divider 1.
IEF.5 = 1 Interrupt 5 is accepted by Serial I/O signal
IEF.6 = 1 Interrupt 6 is accepted by a falling edge signal at port P1.3 ($\overline{INT1}$).
IEF.7 = 1 Interrupt 7 is accepted by underflow from Timer 1.

5.15.3 Port Enable Flag (PEF, P1EF)

The port enable flag is organized as 8-bit binary register (PEF.0 to PEF.7) and 4-bit register (P1EF.2 and P1EF.3). Before port RC, RD may be used to release the hold mode, the content of the PEF must be set first. The PEF and P1EF are controlled by the **MOV PEF, #I MOV P1EF, #I** instructions. The bit descriptions are as follows. Besides release hold mode, the RC port can be bit controlled individually to perform interrupt function.

	7	6	5	4	3	2	1	0
PEF	w	w	w	w	w	w	w	w

	3	2	1	0
P1EF	w	w	-	-

Note: W means write only.

PEF.0: Enable/disable the signal change at pin RC.0 to release hold mode or perform interrupt.
PEF.1: Enable/disable the signal change at pin RC.1 to release hold mode or perform interrupt.
PEF.2: Enable/disable the signal change at pin RC.2 to release hold mode or perform interrupt.
PEF.3: Enable/disable the signal change at pin RC.3 to release hold mode or perform interrupt.
PEF.4: Enable/disable the signal change at pin RD.0 to release hold mode.
PEF.5: Enable/disable the signal change at pin RD.1 to release hold mode.
PEF.6: Enable/disable the signal change at pin RD.2 to release hold mode.
PEF.7: Enable/disable the signal change at pin RD.3 to release hold mode.
P1EF.2: Enable/disable the falling edge signal at P1.2 to release hold mode.
P1EF.3: Enable/disable the falling edge signal at P1.3 to release hold mode.

5.15.4 Hold Mode Release Condition Flag (HCF, HCFD)

The hold mode release condition flag is organized as 8-bit binary register (HCF.0 to HCF.7) and HCFD. It indicates which one releases the hold mode, and is set by hardware. The HCF can be read out by the **MOVA R, HCFL** and **MOVA R, HCFH** instructions. When any of the HCF bits is "1," the hold mode will be released. But the HCFD can not be read, it is only for internal flag. It records the port RD releasing the hold mode. The HCF and HCFD are set by hardware and clear by software. The HCF and HCFD should be clear every time before enter the hold mode. When EVF, EVFD and HEF, HEFD have been reset, the corresponding bit of HCF, HCFD is reset simultaneously. The bit descriptions are as follows:

	7	6	5	4	3	2	1	0
HCF	R	R	R	R	R	R	R	R

HCFD: internal flag, can not be read

Note: R means read only.

HCF.0 = 1 Hold mode was released by overflow from the divider 0.
HCF.1 = 1 Hold mode was released by underflow from the timer 0.
HCF.2 = 1 Hold mode was released by a signal change at port RC.
HCF.3 = 1 Hold mode was released by a signal change at port P1.2 ($\overline{INT0}$).
HCF.4 = 1 Hold mode was released by overflow from the divider 1.
HCF.5 = 1 Hold mode was released by Serial I/O signal.
HCF.6 = 1 Hold mode was released by a signal change at port P1.3 ($\overline{INT1}$).
HCF.7 = 1 Hold mode was released by underflow from the timer 1.
HCFD = 1 Hold mode was released by a signal change at port RD.

5.15.5 Event Flag (EVF, EVFD)

The event flag is organized as a 8-bit binary register (EVF.0 to EVF.7) and EVFD. It is set by hardware and reset by CLR EVF, #I CLR EVFD instructions or the interrupt occurrence. The bit descriptions are as follows:

	7	6	5	4	3	2	1	0
EVF	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
EVFD	R/W							

Note: R/W means read/write.

EVF.0 = 1 Overflow from divider 0 occurred.
EVF.1 = 1 Underflow from timer 0 occurred.
EVF.2 = 1 Signal change at port RC occurred.
EVF.3 = 1 Falling edge signal at port P1.2 ($\overline{INT0}$) occurred.
EVF.4 = 1 Overflow from divider 1 occurred.
EVF.5 = 1 Serial I/O occurred.
EVF.6 = 1 Falling edge signal at port P1.3 ($\overline{INT1}$) occurred.
EVF.7 = 1 Underflow from Timer 1 occurred.
EVFD = 1 Signal change at port RD occurred.

5.16 Reset Function

The W742E/C816 is reset either by a power-on reset or by using the external $\overline{RES}$ pin. The initial state of the W742E/C816 after the reset function is executed is described below.

Table 3 The initial state after the reset function is executed

Program Counter (PC)	000H
TM0, TM1	Reset
MR0, MR1, PAGE Registers	Reset
PSR0, PSR1, PSR2, SCR Registers	Reset
IEF, HEF, HEFD, HCF, PEF, P1EF, EVF, EVFD, SEF Flags	Reset
WRP, DBKR Register	Reset
Timer 0 Input Clock	FOSC/4
Timer 1 Input Clock	FOSC
MFP Output	Low
DTMF Output	Hi-Z
Input/Output Ports RA, RB, P0	Input Mode
Output Port RE & RF	High
RA, RB & P0 Ports Output Type	CMOS Type
RC, RD Ports Pull-high Resistors	Disable
Input Clock of the Watchdog Timer	FOSC/1024
LCD Display	OFF

5.17 Input/Output Ports RA, RB & P0

Port RA consists of pins RA.0 to RA.3. Port RB consists of pins RB.0 to RB.3. Port P0 consists of pins P0.0 to P0.3. At initial reset, input/output ports RA, RB and P0 are all in input mode. When RA and RB are used as output ports, CMOS or NMOS open drain output type can be selected by the PM0 register. But when P0 is used as output port, the output type is just fixed to be CMOS output type. Each pin of port RA, RB and P0 can be specified as input or output mode independently by the PM1, PM2 and PM6 registers. The **MOVA R, RA** or **MOVA R, RB** or **MOVA R, P0** instructions operate the input functions and the **MOV RA, R** or **MOV RB, R** or **MOV P0, R** operate the output functions. For more detail port structure, refer to the Figure 5-10 and Figure 5-10.

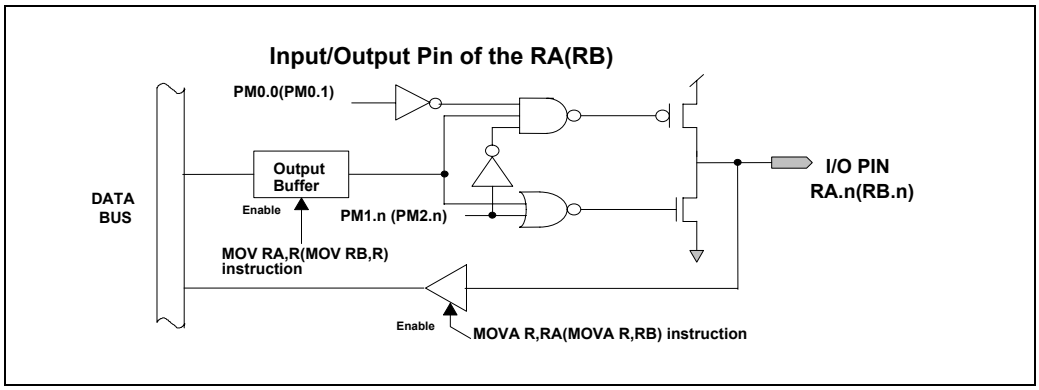


Figure 5-10. Architecture of RA (RB) Input/Output Pins

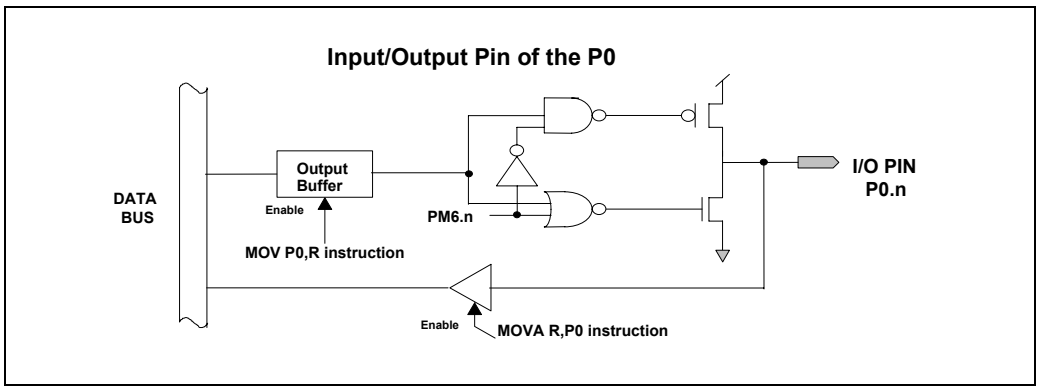


Figure 5-11. Architecture of P0 Input/Output Pins

5.17.1 Port Mode 0 Register (PM0)

The port mode 0 register is organized as 4-bit binary register (PM0.0 to PM0.3). PM0 can be used to determine the port structure; it is controlled by the **MOV PM0, #I** instruction. The bit description is as follows:

	3	2	1	0
PM0	w	w	w	w

Note: W means write only.

Bit 0 = 0 RA port is CMOS output type. Bit 0 = 1 RA port is NMOS open drain output type.
Bit 1 = 0 RB port is CMOS output type. Bit 1 = 1 RB port is NMOS open drain output type.
Bit 2 = 0 RC port pull-high resistor is disabled. Bit 2 = 1 RC port pull-high resistor is enabled.
Bit 3 = 0 RD port pull-high resistor is disabled. Bit 3 = 1 RD port pull-high resistor is enabled.

5.17.2 Port Mode 1 Register (PM1)

The port mode 1 register is organized as 4-bit binary register (PM1.0 to PM1.3). PM1 can be used to control the input/output mode of port RA. PM1 is controlled by the **MOV PM1, #I** instruction. The bit description is as follows:

	3	2	1	0
PM1	w	w	w	w

Note: W means write only.

Bit 0 = 0 RA.0 works as output pin; Bit 0 = 1 RA.0 works as input pin
Bit 1 = 0 RA.1 works as output pin; Bit 1 = 1 RA.1 works as input pin
Bit 2 = 0 RA.2 works as output pin; Bit 2 = 1 RA.2 works as input pin
Bit 3 = 0 RA.3 works as output pin; Bit 3 = 1 RA.3 works as input pin
At initial reset, port RA is input mode (PM1 = 1111B).

5.17.3 Port Mode 2 Register (PM2)

The port mode 2 register is organized as 4-bit binary register (PM2.0 to PM2.3). PM2 can be used to control the input/output mode of port RB. PM2 is controlled by the **MOV PM2, #I** instruction. The bit description is as follows:

	3	2	1	0
PM2	w	w	w	w

Note: W means write only.

Bit 0 = 0 RB.0 works as output pin; Bit 0 = 1 RB.0 works as input pin
Bit 1 = 0 RB.1 works as output pin; Bit 1 = 1 RB.1 works as input pin
Bit 2 = 0 RB.2 works as output pin; Bit 2 = 1 RB.2 works as input pin
Bit 3 = 0 RB.3 works as output pin; Bit 3 = 1 RB.3 works as input pin
At initial reset, the port RB is input mode (PM2 = 1111B).

5.17.4 Port Mode 6 Register (PM6)

The port mode 6 register is organized as 4-bit binary register (PM6.0 to PM6.3). PM6 can be used to control the input/output mode of port P0. PM6 is controlled by the **MOV PM6, #I** instruction. The bit description is as follows:

	3	2	1	0
PM6	w	w	w	w

Note: W means write only.

Bit 0 = 0 P0.0 works as output pin; Bit 0 = 1 P0.0 works as input pin

Bit 1 = 0 P0.1 works as output pin; Bit 1 = 1 P0.1 works as input pin

Bit 2 = 0 P0.2 works as output pin; Bit 2 = 1 P0.2 works as input pin

Bit 3 = 0 P0.3 works as output pin; Bit 3 = 1 P0.3 works as input pin

At initial reset, the port P0 is input mode (PM6 = 1111B).

5.18 Serial I/O interface

The bit 0 and bit 1 of port P0 can be used as a serial input/output port. P0.0 is the serial clock I/O pin and P0.1 is the serial data I/O pin. A 4-bit binary register, Serial Interface Control register (SIC), controls the serial port. SIC is controlled by the **MOV SIC, #I** instruction. The bit definition is as follow:

	3	2	1	0
SIC	w	w	w	w

Bit 0 = 0 P0.0 & P0.1 work as normal input/output pin;

Bit 0 = 1 P0.0 & P0.1 work as serial port function.

Bit 1 = 0 P0.0 works as serial clock input pin;

Bit 1 = 1 P0.0 works as serial clock output pin.

Bit 2 = 0 Serial data latched/changed at falling edge of clock;

Bit 2 = 1 Serial data latched/changed at rising edge of clock.

Bit 3 = 0 Serial clock output frequency is fosc/2;

Bit 3 = 1 Serial clock output frequency is fosc/256.

At initial reset, SIC = 0000B.

The serial I/O functions are controlled by the instructions **SOP R** and **SIP R**. The two instructions are described below:

(1) **When in the first time the SIP R instruction is executed, the data will be loaded to the ACC and RAM from the serial input buffer. But this data is not meaningful, it is used to enable serial port.** There are two methods to get the serial data, one is interrupt and the other is polling. When enable the serial input, the bit 1 of port status register 2(PRS2) will automatically be set to "1" (BUSYI = 1). Then the P0.0 pin will send out 8 clocks or accept 8 clcoks from external device and the data from the P0.1 pin will be loaded to SIB buffer at the rising or falling edge of the P0.0 pin. After the 8 clocks have been sent, BUSYI will be reset to "0" and EVF.5 will be set to "1." At this time, if IEF.5 has been set (IEF.5 = 1), an interrupt is executed then the SIP R instruction can get the correct data from the serial input buffer (SIB), **low nibble of SIB movs to ACC register and the high nibble moves to RAM**; if HEF.5 has been set (HEF.5 = 1), the hold state is terminated. The polling method is to check the status of PSR2.1 (BUSYI) to know whether the serial input process is completed or not. If a serial input process is not completed, but the SIP R instruction is executed again, the data will be lost. The timing is shown in Figure 5-12.

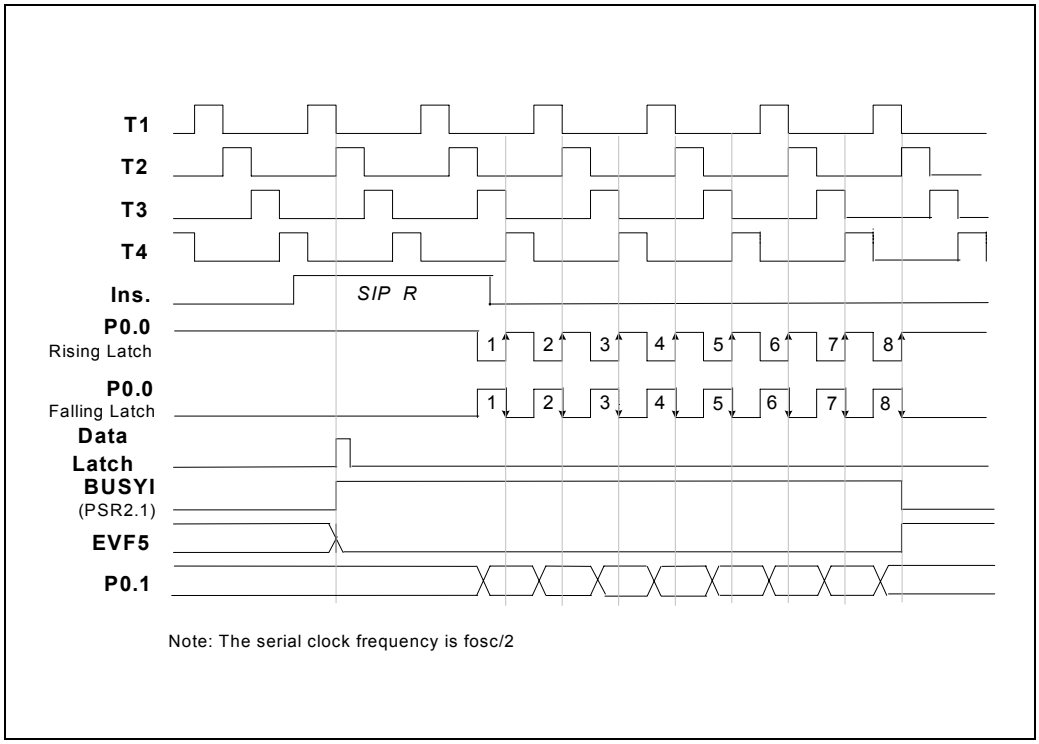


Figure 5-12. Timing of the Serial Input Function (SIP R)

(2) When the **SOP R** instruction is executed, the data will be loaded to the serial output buffer (SOB) from ACC and the RAM, the low nibble data of SOB is from ACC register and the high nibble data is from RAM, and bit 3 of port status register 2(PSR2) will be set to "1" (BUSYO = 1). Then the P0.0 pin will send out 8 clocks or accept 8 clocks from external device and the data in SOB will be sent out at the rising or falling edge of the P0.1 pin. After the 8 clocks have been sent, BUSYO will be reset to "0" and EVF.5 will be set to "1." At this time, if IEF.5 has been set (IEF.5 = 1), an interrupt is executed; if HEF.5 has been set (HEF.5 = 1), the hold state is terminated. Users can check the status of PSR2.3 (BUSYO) to know whether the serial output process is completed or not. If a serial output process is not completed, but the SOP R instruction is executed again, the data will be lost. The timing is shown in Figure 5-13.

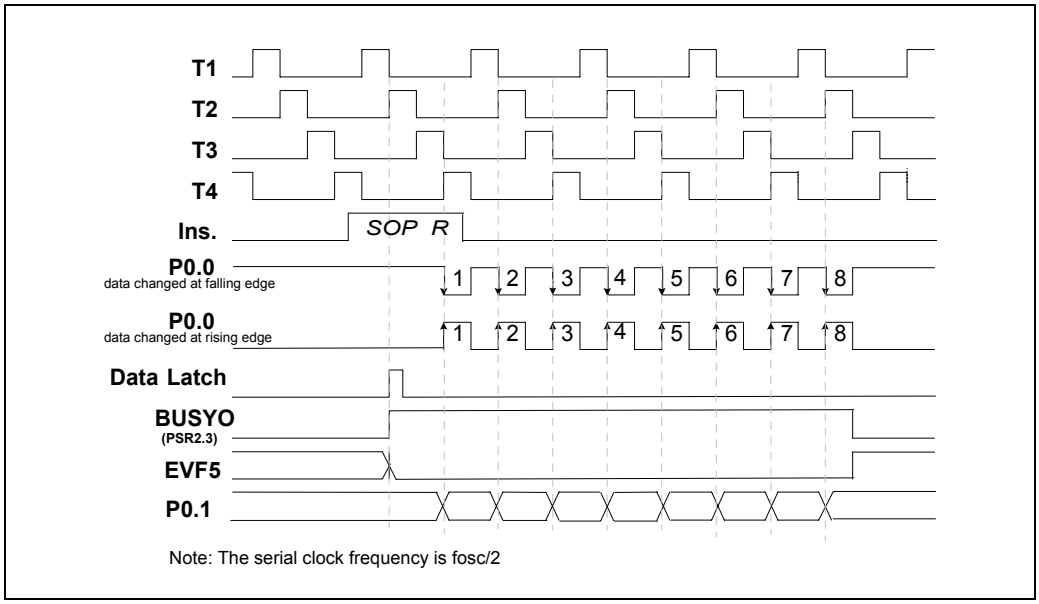


Figure 5-13 Timing of the Serial Output Function (SOP R)

Port Status Register 2 (PSR2)

Port status register 2 is organized as 4-bit binary register (PSR2.0 to PSR2.3). PSR2 is controlled by the MOVA R, PSR2, and CLR PSR2 instructions. The bit descriptions are as follows:

	3	2	1	0
PSR2	R	—	R	—

Note: R means read only.

Bit 0 is reserved.

Bit 1 (BUSYI): Serial port input busy flag.

Bit 2 is reserved.

Bit 3 (BUSYO): Serial port output busy flag.

5.19 Input Ports RC

Port RC consists of pins RC.0 to RC.3. Each pin of port RC can be connected to a pull-high resistor, which is controlled by the port mode 0 register (PM0). When the PEF, HEF, and IEF corresponding to the RC port are set, a signal change at the specified pins of port RC will execute the hold mode release or interrupt subroutine. Port status register 0 (PSR0) records the status of signal changes on the pins of port RC. PSR0 can be read out and cleared by the **MOVA R, PSR0**, and **CLR PSR0** instructions. In addition, the falling edge signal on the pin of port RC specified by the instruction **MOV SEF, #I** will cause the device to exit the stop mode. Refer to Figure 5-14 and the instruction table for more details.

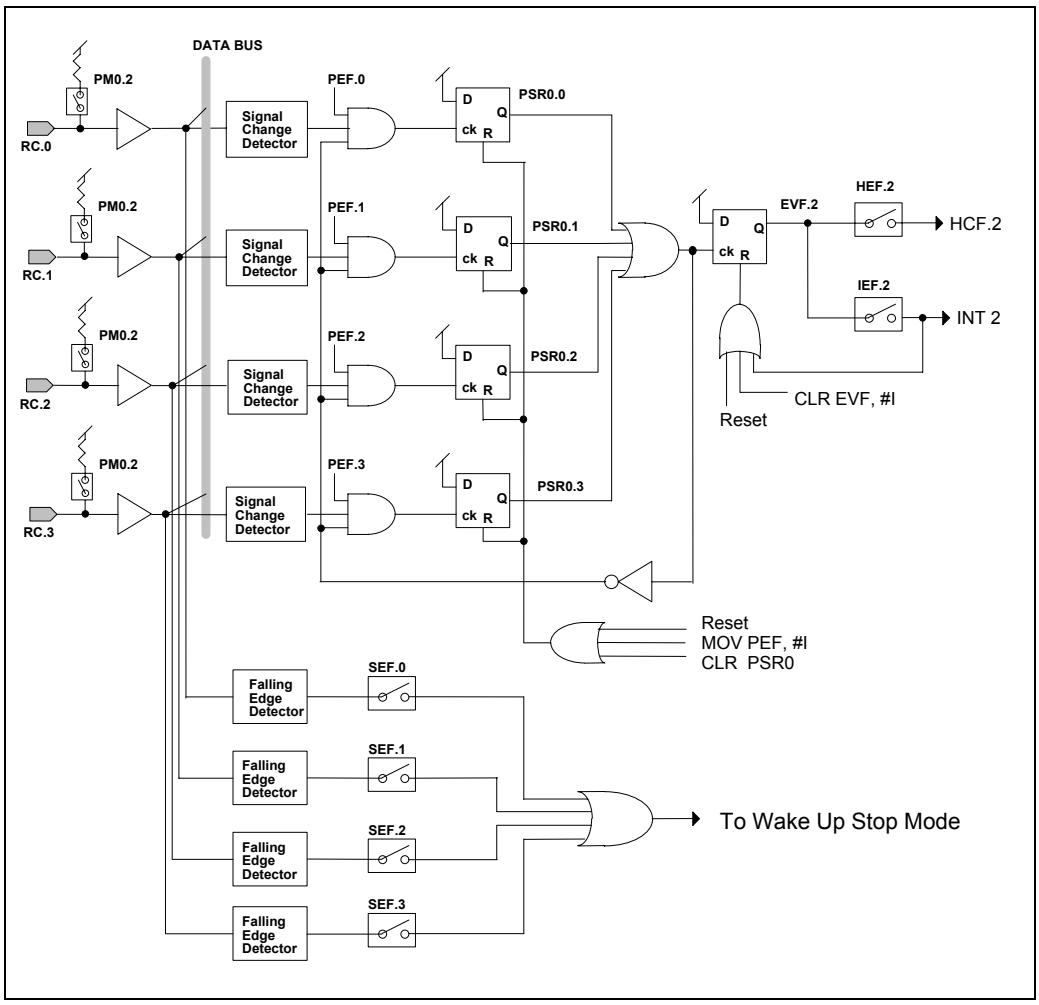


Figure 5-14. Architecture of Input Ports RC

5.19.1 Port Status Register 0 (PSR0)

Port status register 0 is organized as 4-bit binary register (PSR0.0 to PSR0.3). PSR0 can be read or cleared by the **MOVA R, PSR0**, and **CLR PSR0** instructions. The bit descriptions are as follows:

	3	2	1	0
PSR0	R	R	R	R

Note: R means read only.

Bit 0 = 1 Signal change at RC.0
Bit 1 = 1 Signal change at RC.1
Bit 2 = 1 Signal change at RC.2
Bit 3 = 1 Signal change at RC.3

5.20 Input Ports RD

Port RD consists of pins RD.0 to RD.3. Each pin of port RD can be connected to a pull-high resistor, which is controlled by the port mode 0 register (PM0). When the PEF and HEFD corresponding to the RD port are set, a signal change at the specified pins of port RD will execute the hold mode release. Port status register 1 (PSR1) records the status of signal changes on the pins of port RD. PSR1 can be read out and cleared by the **MOVA R, PSR1**, and **CLR PSR1** instructions. In addition, the falling edge signal on the pin of port RD specified by the instruction MOV SEF, #I will cause the device to exit the stop mode. Refer to Figure 5-15 and the instruction table for more details.

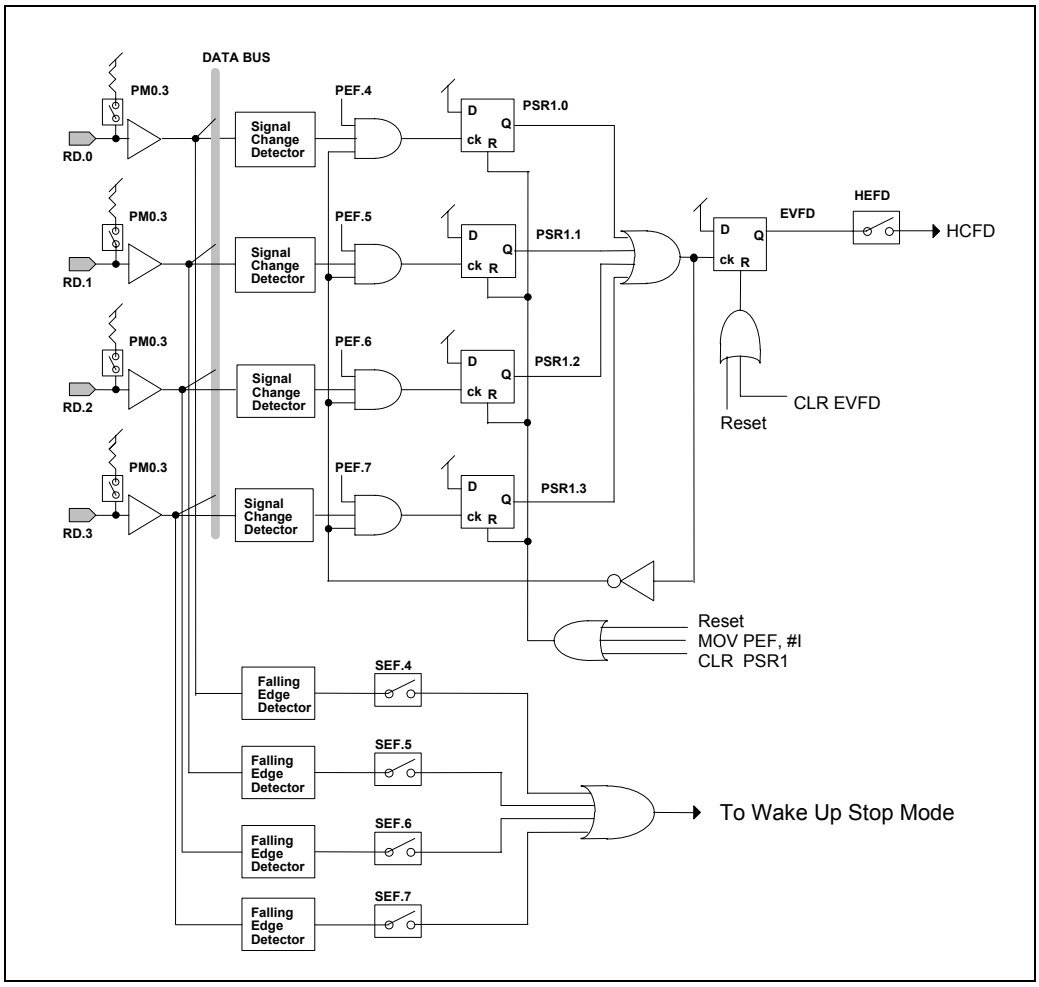


Figure 5-15. Architecture of Input Ports RD

5.20.1 Port Status Register 1 (PSR1)

Port status register 1 is organized as 4-bit binary register (PSR1.0 to PSR1.3). PSR1 can be read or cleared by the MOVA R, PSR1, and CLR PSR1 instructions. The bit descriptions are as follows:

	3	2	1	0
PSR1	R	R	R	R

Note: R means read only.

Bit 0 = 1 Signal change at RD.0
Bit 1 = 1 Signal change at RD.1
Bit 2 = 1 Signal change at RD.2
Bit 3 = 1 Signal change at RD.3

5.21 Output Port RE & RF

Output port RE and RF are used as output of the internal RT port. When the **MOV RE, R** or **MOV RF, R** instruction is executed, the data in the RAM will be output to port RT through port RE or RF. They provide high sink current to drive LED.

5.22 Input Port P1

Input port P1 is a multi-function input port. When the **MOVA R, P1** instruction is executed, the P1 data will be get to the RAM and A register. The P1.2 and P1.3 can be configurated as the external interrupt $\overline{INT0}$ and $\overline{INT1}$ by set P1EF.2 and P1EF.3.

5.23 DTMF Output Pin (DTMF)

W742E/C816 provides a DTMF generator which outputs the dual tone multi-frequency signal to the DTMF pin. The DTMF generator can work well at the operating frequency of 3.58 MHz. A DTMF register specify the desired low/high frequency. And the Dual Tone Control Register (DTCR) can control whether the dual tone will be output or not. The tones are divided into two groups (low group and high group). The relation between the DTMF signal and the corresponding touch tone keypad is shown in Figure 5-16.

	C1	C2	C3	C4
R1	1	2	3	A
R2	4	5	6	B
R3	7	8	9	C
R4	*	0	#	D

ROW/COL	FREQUENCY
R1	697 Hz
R2	770 Hz
R3	852 Hz
R4	941 Hz
C1	1209 Hz
C2	1336 Hz
C3	1477 Hz
C4	1633 Hz

Figure 5-16. The relation between the touch tone keypad and the frequency

5.23.1 DTMF Register

DTMF register is organized as 4-bit binary register. By controlling the DTMF register, one tone of the low/high group can be selected. The MOV DTMF, R instruction can specify the wanted tones. The bit descriptions are as follows:

	3	2	1	0
DTMF	W	W	W	W

Note: W means write only.

	B3	B2	B1	B0	SELECTED TONE
	X	X	0	0	1209 Hz
High	X	X	0	1	1336 Hz
Group	X	X	1	0	1477 Hz
	X	X	1	1	1633 Hz
	0	0	X	X	697 Hz
Low	0	1	X	X	770 Hz
Group	1	0	X	X	852 Hz
	1	1	X	X	941 Hz

Note: X means this bit do not care.

5.23.2 Dual Tone Control Register (DTCR)

Dual tone control register is organized as 4-bit binary register. The output of the dual or single tone will be controlled by this register. The **MOV DTCR, #I** instruction can specify the wanted status. The bit descriptions are as follows:

	3	2	1	0
DTCR	—	W	W	W

Note: W means write only.

Bit 0 = 1 Low group tone output is enabled.

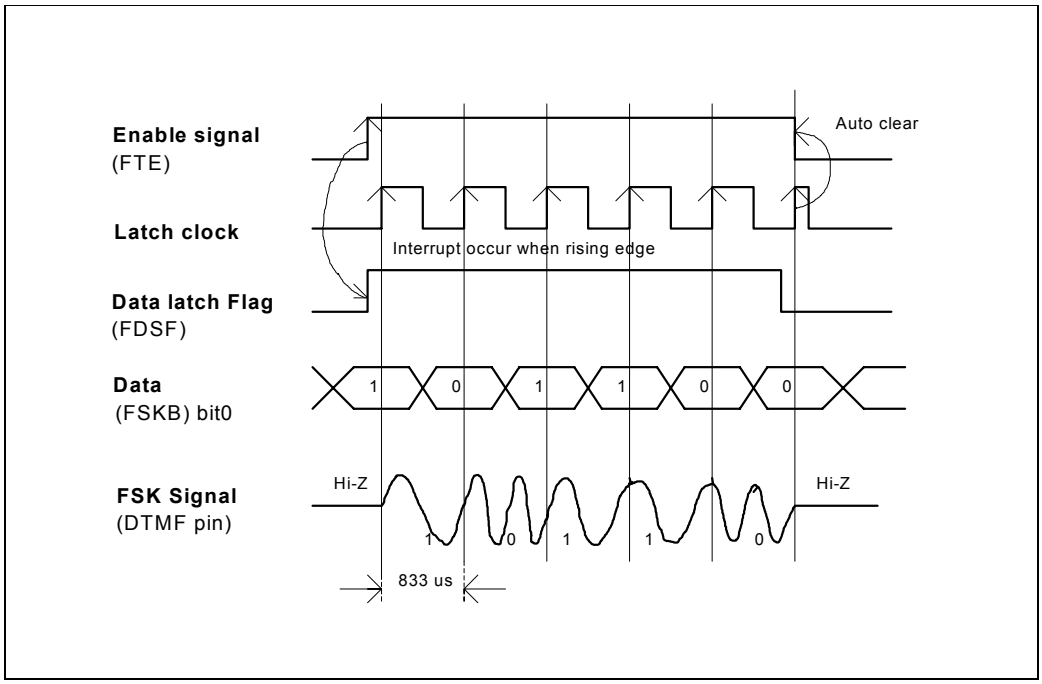
Bit 1 = 1 High group tone output is enabled.

Bit 2 = 1 DTMF output is enabled. When Bit 2 is reset to 0, the DTMF output pin will be Hi-Z state.

Bit 3 is reserved.

5.24 FSK Output

W742E/C816 provides a FSK generator which outputs the FSK signal to the DTMF pin. The FSK output share with DTMF output pin. It can out FSK signal with 1200 Hz baud rate of CCITT V.23 or Bellcore 202 signal by mask option. A FSK transmit data register (FSKB) specify the desired output data. And the FSK Transimit Control Register (FSKC) can control whether the FSK signal will be output or not. The relation timing is showed as following.



The relation timing diagram of FSK generator

When FTE enable will set the FDSF to high, while will enable the internal latch clock with 1200Hz.

Latch clock check FDSF in rising edge, if FDSF is high then FSKB bit0 will send out by modulate.

FDSF could be cleared by software to inform no more data want to be sent out. Meanwhile the data bit will send continually till next latch clock rising edge even the FDSF is low. If the FDSF is low then in next latch clock in rising will force FTE to disable and clear FDSF by hardware automatically.

The only way to stop FSK signal immediately is to Disable FTE.

Also a internal latch data in rising edge will set EVF.5 and occur an interrupt shared with Serial I/O Interrupt routine, If a serial I/O interrupt Enable.

5.24.1 FSK Transmit Control Register (FSKC)

FSK transmit control register is organized as 4-bit binary register. The output of the FSK signal status and signal level selection will be controlled by this register. The **MOV FSKC, R** instruction can specify the wanted status. And the **MOV R, FSKC** can read out the FDSF status. The bit descriptions are as follows:

Bit 3 = 1 FSK output Enable (FTE)

Bit 2 = 1 FDSF will set when FSK output is enable and clear by software or FTE is low.

Bit 0, 1 FSK output signal level selection

Transmit Level Option:

	Bit1	Bit0
150 mV	0	0
120 mV	0	1
95 mV	1	0
75 mV	1	1

5.24.2 FSK Transmit Data Buffer (FSKB)

FSK transmit data register is organized as 4-bit binary register. But only bit0 is defined.The output data of FSK signal need to put on bit0 before transmition. The **MOV FSKB, R** instruction can specify the wanted data. The bit descriptions are as follows:

	3	2	1	0
FSKB	—	—	—	W

Note: W means write only.

Bit 0 = data buffer, only this bit data will be send out.

Bit 1 is reserved

Bit 2 is reserved

Bit 3 is reserved.

5.25 MFP Output Pin (MFP)

The MFP output pin can select the output of the Timer 1 clock or the modulation frequency; the output of the pin is determined by mode register 1 (MR1). The organization of MR1 is shown in Figure 5-7. When bit 2 of MR1 is reset to "0," the MFP output can deliver a modulation output in any combination of one signal from among DC, 4096 Hz, 2048 Hz, and one or more signals from among 128 Hz, 64 Hz, 8 Hz, 4 Hz, 2 Hz, or 1 Hz (the clock source is from 32.768 KHz crystal). The **MOV MFP, #I** instruction is used to specify the modulation output combination. The data specified by the 8-bit operand and the MFP output pin are shown in next page.

Table 4 The relation between the MFP output frequncy and the data specified by 8-bit operand

(Fosc = 32.768 KHz)

R7 R6	R5	R4	R3	R2	R1	R0	FUNCTION
0 0	0	0	0	0	0	0	Low level
	0	0	0	0	0	1	128 Hz
	0	0	0	0	1	0	64 Hz
	0	0	0	1	0	0	8 Hz
	0	0	1	0	0	0	4 Hz
	0	1	0	0	0	0	2 Hz
	1	0	0	0	0	0	1 Hz
0 1	0	0	0	0	0	0	High level
	0	0	0	0	0	1	128 Hz
	0	0	0	0	1	0	64 Hz
	0	0	0	1	0	0	8 Hz
	0	0	1	0	0	0	4 Hz
	0	1	0	0	0	0	2 Hz
	1	0	0	0	0	0	1 Hz
1 0	0	0	0	0	0	0	2048 Hz
	0	0	0	0	0	1	2048 Hz * 128 Hz
	0	0	0	0	1	0	2048 Hz * 64 Hz
	0	0	0	1	0	0	2048 Hz * 8 Hz
	0	0	1	0	0	0	2048 Hz * 4 Hz
	0	1	0	0	0	0	2048 Hz * 2 Hz
	1	0	0	0	0	0	2048 Hz * 1 Hz
1 1	0	0	0	0	0	0	4096 Hz
	0	0	0	0	0	1	4096 Hz * 128 Hz
	0	0	0	0	1	0	4096 Hz * 64 Hz
	0	0	0	1	0	0	4096 Hz * 8 Hz
	0	0	1	0	0	0	4096 Hz * 4 Hz
	0	1	0	0	0	0	4096 Hz * 2 Hz
	1	0	0	0	0	0	4096 Hz * 1 Hz

5.26 LCD Controller/Driver

The W742E/C816 can directly drive an LCD with 40 segment output pins and 16 common output pins for a total of 40 × 16 dots. The LCD driving mode is 1/5 bias 1/8 or 1/16 duty. The alternating frequency of the LCD can be set as Fw/16, Fw/32, Fw/64, or Fw/128. The structure of the LCD alternating frequency (F_{LCD}) is shown in the Figure 5-17.

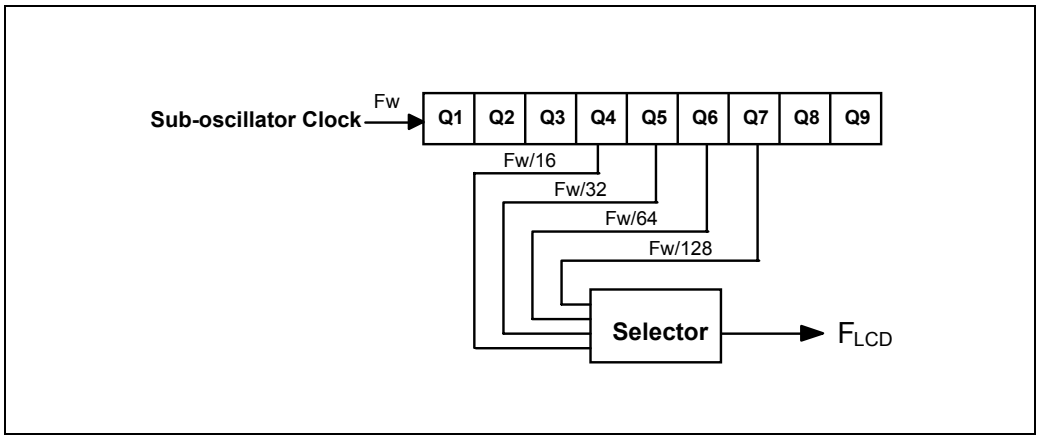


Figure 5-17 LCD alternating frequency (FLCD) circuit diagram

Fw = 32.768 KHz, the LCD frequency is as shown in the table below.

Table 5 The relartionship between the F_{LCD} and the duty cycle

LCD FREQUENCY	1/8 DUTY	1/16 DUTY
Fw/128 (256 Hz)	32	-
Fw/64 (512 Hz)	64	32
Fw/32 (1024 Hz)	128	64
Fw/16 (2048 Hz)	-	128

Corresponding to the 40 LCD drive output pins, there are 160 LCD data RAM segments. Instructions such as **MOV LPL, R, MOV LPH, R, MOV @LP, R,** and **MOV R, @LP** are used to control the LCD data RAM. The data in the LCD data RAM are transferred to the segment output pins automatically without program control. When the bit value of the LCD data RAM is "1," the LCD is turned on. When the bit value of the LCD data RAM is "0," LCD is turned off. The contents of the LCD data RAM (LCDR) are sent out through the segment0 to segment39 pins by a direct memory access. The relation between the LCD data RAM and segment/common pins is shown below.

Table 6 The reation between the LCDR and segment/common pins used as LCD drive output pins

OUTPUT PIN	LCD RAM	COM7 BIT3	COM6 BIT2	COM5 BIT1	COM4 BIT0	LCD RAM	COM3 BIT3	COM2 BIT2	COM1 BIT1	COM0 BIT0
SEG0	LCDR01	0/1	0/1	0/1	0/1	LCDR00	0/1	0/1	0/1	0/1
SEG1	LCDR03	0/1	0/1	0/1	0/1	LCDR02	0/1	0/1	0/1	0/1
: :	: :	: :	: :	: :	: :	: :	: :	: :	: :	: :
SEG38	LCDR4D	0/1	0/1	0/1	0/1	LCDR4C	0/1	0/1	0/1	0/1
SEG39	LCDR4F	0/1	0/1	0/1	0/1	LCDR4E	0/1	0/1	0/1	0/1
OUTPUT PIN	**LCD RAM**	**COM15 BIT3**	**COM14 BIT2**	**COM13 BIT1**	**COM12 BIT0**	**LCD RAM**	**COM11 BIT3**	**COM10 BIT2**	**COM9 BIT1**	**COM8 BIT0**
SEG0	LCDR81	0/1	0/1	0/1	0/1	LCDR80	0/1	0/1	0/1	0/1
SEG1	LCDR83	0/1	0/1	0/1	0/1	LCDR82	0/1	0/1	0/1	0/1
: :	: :	: :	: :	: :	: :	: :	: :	: :	: :	: :
SEG38	LCDRCD	0/1	0/1	0/1	0/1	LCDRCC	0/1	0/1	0/1	0/1
SEG39	LCDRCF	0/1	0/1	0/1	0/1	LCDRCE	0/1	0/1	0/1	0/1

The LCDON instruction turns the LCD display on (even in HOLD mode), and the LCDOFF instruction turns the LCD display off. At the initial reset state, the LCD display is turned off automatically. To turn on the LCD display, the instruction LCDON must be executed.

5.26.1 LCD RAM Addressing Method

There are 160 LCD RAMs (LCDR00H – LCDR4FH, LCDR80H - LCDR0CFH) that should be indirectly addressed. The LCD RAM pointer (LP) is used to point to the address of the wanted LCD RAM **but it is not readable**. The LP is organized as 8-bit binary register. The **MOV LPL, R** and **MOV LPH, R** instructions can load the LCD RAM address from RAM to the LP register. The **MOV @LP, R** and **MOV R, @LP** instructions can access the pointed LCD RAM content.

5.26.2 LCD Voltage and Contrast Adjusting

LCD power(VLCD2) has two source, one is directly from the VLCD1 pin, another is from internal pump circuit. The LCD power source is selected by mask option. The pump circuit doubles the μC input voltage(V_{DD}), the power consumption in internal pump mode is more than directly input from VLCD1. The LCD pump circuit only works in the V_{DD} range from 2.4V to 4.0V. If the operating voltage of V_{DD} is up 4.0V, the LCD power should come from the VLCD1 pin. The LCD contrast is adjustable by an

internal variable resistor (VR). VLCD voltage is controlled by setting bit2, bit1 and bit0 of LCD contrast control register (LCDCC). LCDCC is determined by executing MOV LCDCC, #I. The Figure 5-18 shows the LDC power control as below:

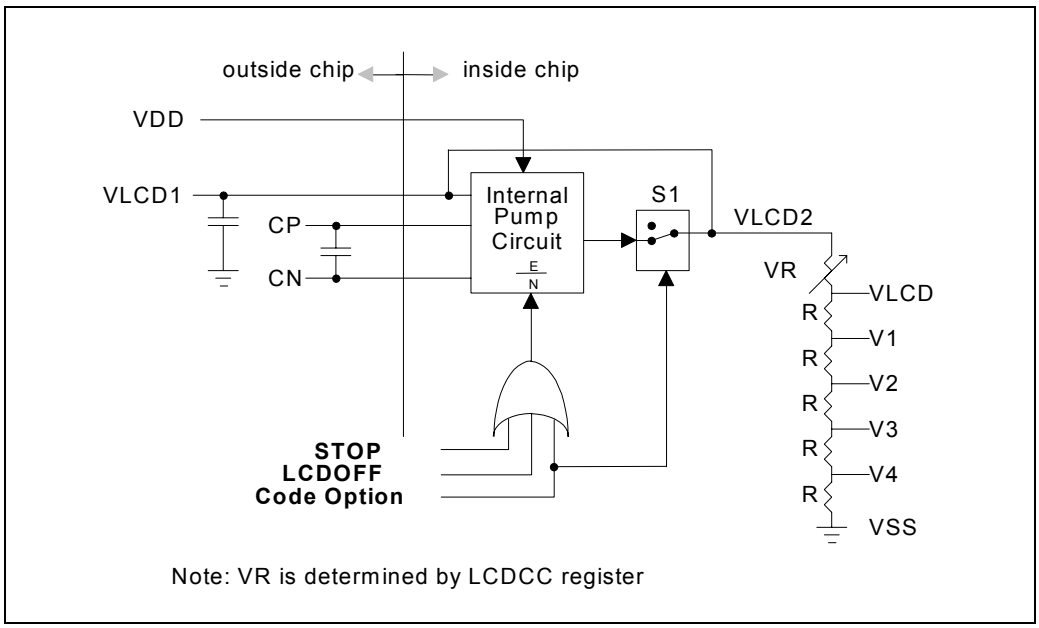


Figure 5-18. LCD power control circuit

	3	2	1	0
LCDCC	—	W	W	W

Note: W means write only.

LCDCC	VLCD/VLCD2
0000H	1.00
0001H	0.96
0010H	0.93
0011H	0.89
0100H	0.86
0101H	0.81
0110H	0.76
0111H	0.71

Bit 3 is reserved.

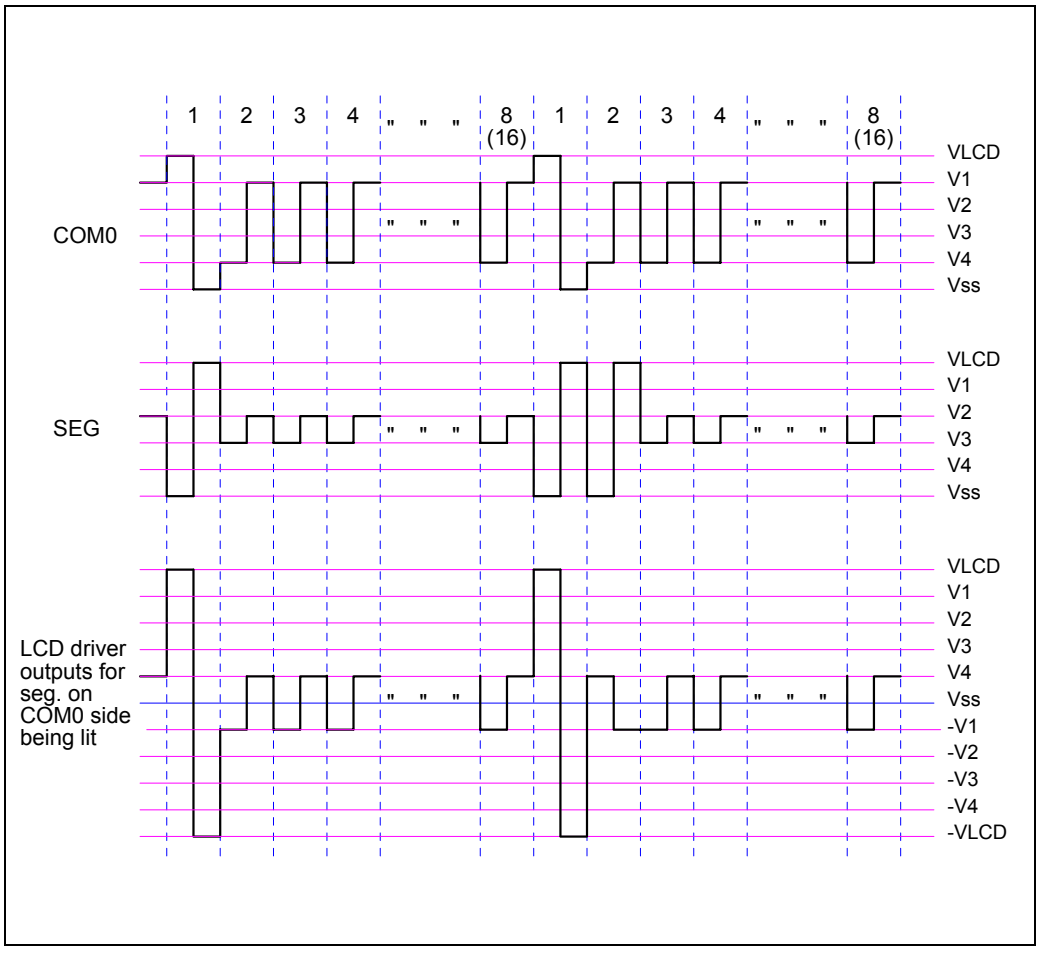
5.26.3 SEG32 – SEG39 Using as DC Output (NMOS Open Drain Type)

SEG32-SEG39 pins output type can be changed to DC output mode by code mask option. The correspoinding control resigters are LCD RAM address LCDR40 and LCDR41, these two parts are individually enabled by code mask option. LCDR40 controls the SEG32 – SEG35 pins and LCDR41 controls the SEG36 – SEG39 pins. When SEG32 – SEG39 are used as DC output, their output type is NMOS open drain type. The instruction **MOV @LP, R** outputs the ram data to SEG32 – 39, when SEG32 – 39 operate in DC output mode.

5.26.4 The Output Waveforms for the LCD Driving Mode

1/5 bias 1/8 (1/16) duty Lighting System (Example)

Normal Operating Mode



6. ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Supply Voltage to Ground Potential	-0.3 to +7.0	V
Applied Input/Output Voltage	-0.3 to +7.0	V
Power Dissipation	120	mW
Ambient Operating Temperature	0 to +70	°C
Storage Temperature	-55 to +150	°C

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device.

7. DC CHARACTERISTICS

(V_{DD} – V_{SS} = 3.0V, Fm = 3.58 MHz, Fs = 32.768 KHz, T_A = 25° C, LCD on, **INTERNAL PUMP DISABLE**; unless otherwise specified)

PARAMETER	SYM.	CONDITIONS	MIN.	TYP.	MAX.	UNIT
OP. Voltage (W742C816)	V_{DD}	-	2.4	-	6.0	V
Op. Voltage (W742E816)	V_{DD}	-	2.4	-	4.8	V
Op. Current (Crystal type)	I_{OP1}	No load (Ext-V) In dual-clock normal operation	-	0.5	1.0	mA
Op. Current (Crystal type)	I_{OP3}	No load (Ext-V) In dual-clock slow operation and Fm is stopped	-	30	50	µA
Hold Current (Crystal type)	I_{HM1}	Hold mode No load (Ext-V) In dual-clock normal operation	-	400	500	µA
Hold Current (Crystal type)	I_{HM3}	Hold mode No load (Ext-V) In dual-clock slow operation and Fm is stopped	-	30	50	µA
Hold Current (Crystal type)	I_{HM5}	Hold mode No load (Ext-V) V_{DD} = 5V; In dual-clock slow operation and Fm is stopped	-	50	80	µA
Stop Current	I_{SM1}	Stop mode No load (Ext-V) Fm and Fs are stopped	-	1	2	µA
Input Low Voltage	V_{IL}	-	V_{SS}	-	0.3 V_{DD}	V
Input High Voltage	V_{IH}	-	0.7 V_{DD}	-	V_{DD}	V

DC Characteristics, continued

PARAMETER	SYM.	CONDITIONS	MIN.	TYP.	MAX.	UNIT
MFP Output Low Voltage	V_{ML}	I_{OL} = 3.5 mA	-	-	0.4	V
MFP Output High Voltage	V_{MH}	I_{OH} = 3.5 mA	2.4	-	-	V
Port RA, RB, RD Output Low Voltage	V_{ABL}	I_{OL} = 2.0 mA	-	-	0.4	V
Port RA, RB, RD Output High Voltage	V_{ABH}	I_{OH} = 2.0 mA	2.4	-	-	V
LCD Supply Current	I_{LCD}	All Seg. ON	-	-	20	µA
SEG0 – SEG39 Sink Current (Used as LCD output)	I_{OL1}	V_{OL} = 0.4V V_{LCD} = 0.0V	90	-	-	µA
SEG0 – SEG39 Drive Current (Used as LCD output)	I_{OH1}	V_{OH} = 2.4V V_{LCD} = 3.0V	90	-	-	µA
Port RE, RF Sink Current	I_{EL}	V_{OL} = 0.9V	9	-	-	mA
Port RE, RF Source Current	I_{EH}	V_{OH} = 2.4V	0.4	1.2	-	mA
DTMF Output DC level	V_{TDC}	R_L = 5 KΩ, V_{DD} = 2.5 to 3.8V	1.1	-	2.8	V
DTMF Distortion	T_{HD}	R_L = 5 KΩ, V_{DD} = 2.5 to 3.8V	-	-30	-23	dB
DTMF Output Voltage	V_{TO}	Low group, R_L = 5 KΩ	130	150	170	mVrms
FSK Distortion	T_{FHD}	R_L = 5 KΩ, V_{DD} = 2.5 to 3.8V	-	-30	-25	dB
FSK Output Voltage	V_{FO}		130	150	170	mVrms
Pre-emphasis		Col/Row	1	2	3	dB
Pull-up Resistor	R_C	Port RC	100	350	1000	KΩ
RES Pull-up Resistor	R_{RES}	-	20	100	500	KΩ

8. AC CHARACTERISTICS

PARAMETER	SYM.	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Op. Frequency	F_{OSC}	RC type	-	2000	-	KHz
		Crystal type	-	3.58	-	MHz
Frequency Deviation by Voltage Drop for RC Oscillator	$\frac{\Delta f}{f}$	$\frac{f(3V) - f(2.4V)}{f(3V)}$	-	-	10	%
Instruction Cycle Time	T_I	One machine cycle	-	4/F_{OSC}	-	S
Reset Active Width	T_{RAW}	F_{OSC} = 32.768 KHz	1	-	-	µS
Interrupt Active Width	T_{IAW}	F_{OSC} = 32.768 KHz	1	-	-	µS

9. INSTRUCTION SET TABLE

Symbol Description

ACC:	Accumulator
ACC.n:	Accumulator Bit n
WR:	Working Register
WRP:	WR Page Register
PAGE:	Page Register
DBKRL:	Data Bank Register (Low nibble)
DBKRH:	Data Bank Register (High nibble)
ROMPR:	ROM Page Register
MR0:	Mode Register 0
MR1:	Mode Register 1
PM0:	Port Mode 0
PM1:	Port Mode 1
PM4:	Port Mode 4
PM5:	Port Mode 5
PM6:	Port Mode 6
PSR0:	Port Status Register 0
PSR1:	Port Status Register 1
PSR2:	Port Status Register 2
R:	Memory (RAM) of Address R
LP:	LCD Data RAM Pointer
LPL:	Low Nibble of the LCD Data RAM Pointer
LPH:	High Nibble of the LCD Data RAM Pointer
R.n:	Memory Bit n of Address R
I:	Constant Parameter
L:	Branch or Jump Address
CF:	Carry Flag
ZF:	Zero Flag
PC:	Program Counter

Symbol Description, continued

TM0L:	Low Nibble of the Timer 0 Counter
TM0H:	High Nibble of the Timer 0 Counter
TM1L:	Low Nibble of the Timer 1 Counter
TM1H:	High Nibble of the Timer 1 Counter
LCDCC	LCD Contrast Control Register
TAB0:	Look-up Table Address Buffer 0
TAB1:	Look-up Table Address Buffer 1
TAB2:	Look-up Table Address Buffer 2
TAB3:	Look-up Table Address Buffer 3
IEF.n:	Interrupt Enable Flag n
HCF.n:	HOLD Mode Release Condition Flag n
HEF.n:	HOLD Mode Release Enable Flag n
HEFD:	RD Port HOLD Mode Release Enable Flag
SEF.n:	STOP Mode Wake-up Enable Flag n
PEF.n:	Port Enable Flag n
P1EF.n:	P1 Port Enable Flag n
EVF.n:	Event Flag n
EVFD:	RD Port Event Flag n
! =:	Not Equal
&:	AND
^:	OR
EX:	Exclusive OR
←:	Transfer Direction, Result
[PAGE*10H+()]:	Contents of Address PAGE (bit2, bit1, bit0)*10H+()
[P()]:	Contents of Port P

Machine code	Mnemonic		Function	Flag affected	W/C
Arithmetic					
0001 1000 0xxx xxxx	ADD	R, ACC	ACC←(R) + (ACC)	ZF, CF	1/1
0001 1100 iiii nnnn	ADD	WRn, #I	ACC←(WRn) + I	ZF, CF	1/1
0001 1001 0xxx xxxx	ADDR	R, ACC	ACC, R←(R) + (ACC)	ZF, CF	1/1
0001 1101 iiii nnnn	ADDR	WRn, #I	ACC, WRn←(WRn) + I	ZF, CF	1/1
0000 1000 0xxx xxxx	ADC	R, ACC	ACC←(R) + (ACC) + (CF)	ZF, CF	1/1
0000 1100 iiii nnnn	ADC	WRn, #I	ACC←(WRn) + I + (CF)	ZF, CF	1/1
0000 1001 0xxx xxxx	ADCR	R, ACC	ACC, R←(R) + (ACC) + (CF)	ZF, CF	1/1
0000 1101 iiii nnnn	ADCR	WRn, #I	ACC, WRn←(WRn) + I + (CF)	ZF, CF	1/1
0010 1000 0xxx xxxx	ADU	R, ACC	ACC←(R) + (ACC)	ZF	1/1
0010 1100 iiii nnnn	ADU	WRn, #I	ACC←(WRn) + I	ZF	1/1
0010 1001 0xxx xxxx	ADUR	R, ACC	ACC, R←(R) + (ACC)	ZF	1/1
0010 1101 iiii nnnn	ADUR	WRn, #I	ACC, WRn←(WRn) + I	ZF	1/1
0001 1010 0xxx xxxx	SUB	R, ACC	ACC←(R) - (ACC)	ZF, CF	1/1
0001 1110 iiii nnnn	SUB	WRn, #I	ACC←(WRn) - I	ZF, CF	1/1
0001 1011 0xxx xxxx	SUBR	R, ACC	ACC, R←(R) - (ACC)	ZF, CF	1/1
0001 1111 iiii nnnn	SUBR	WRn, #I	ACC, WR←(WR) - I	ZF, CF	1/1
0000 1010 0xxx xxxx	SBC	R, ACC	ACC←(R) - (ACC) - (CF)	ZF, CF	1/1
0000 1110 iiii nnnn	SBC	WRn, #I	ACC←(WRn) - I - (CF)	ZF, CF	1/1
0000 1011 0xxxxxxx	SBCR	R, ACC	ACC, R←(R) - (ACC) - (CF)	ZF, CF	1/1
0000 1111 iiii nnnn	SBCR	WRn, #I	ACC, WRn←(WRn) - I - (CF)	ZF, CF	1/1
0100 1010 0xxx xxxx	INC	R	ACC, R←(R) + 1	ZF, CF	1/1
0100 1010 1xxx xxxx	DEC	R	ACC, R←(R) - 1	ZF, CF	1/1
Logic					
0010 1010 0xxx xxxx	ANL	R, ACC	ACC←(R) & (ACC)	ZF	1/1
0010 1110 iiii nnnn	ANL	WRn, #I	ACC←(WRn) & I	ZF	1/1
0010 1011 0xxx xxxx	ANLR	R, ACC	ACC, R←(R) & (ACC)	ZF	1/1
0010 1111 iiii nnnn	ANLR	WRn, #I	ACC, WRn←(WRn) & I	ZF	1/1
0011 1010 0xxx xxxx	ORL	R, ACC	ACC←(R) ∧ (ACC)	ZF	1/1
0011 1110 iiii nnnn	ORL	WRn, #I	ACC←(WRn) ∧ I	ZF	1/1
0011 1011 0xxx xxxx	ORLR	R, ACC	ACC, R←(R) ∧ (ACC)	ZF	1/1
0011 1111 iiii nnnn	ORLR	WRn, #I	ACC, WRn←(WRn) ∧ I	ZF	1/1
0011 1000 0xxx xxxx	XRL	R, ACC	ACC←(R) EX (ACC)	ZF	1/1
0011 1100 iiii nnnn	XRL	WRn, #I	ACC←(WRn) EX I	ZF	1/1
0011 1001 0xxx xxxx	XRLR	R, ACC	ACC, R←(R) EX (ACC)	ZF	1/1
0011 1101 iiii nnnn	XRLR	WRn, #I	ACC, WRn←(WRn) EX I	ZF	1/1

Instruction set, continued

Machine code	Mnemonic		Function	Flag affected	W/C
Branch					
0111 0aaa aaaa aaaa	JMP	L	PC13~PC0←(ROMPR) × 800H + L10~L0		1/1
1000 0aaa aaaa aaaa	JB0	L	PC10~PC0←L10~L0; if ACC.0 = "1"		1/1
1001 0aaa aaaa aaaa	JB1	L	PC10~PC0←L10~L0; if ACC.1 = "1"		1/1
1010 0aaa aaaa aaaa	JB2	L	PC10~PC0←L10~L0; if ACC.2 = "1"		1/1
1011 0aaa aaaa aaaa	JB3	L	PC10~PC0←L10~L0; if ACC.3 = "1"		1/1
1110 0aaa aaaa aaaa	JZ	L	PC10~PC0←L10~L0; if ACC = 0		1/1
1100 0aaa aaaa aaaa	JNZ	L	PC10~PC0←L10~L0; if ACC ! = 0		1/1
1111 0aaa aaaa aaaa	JC	L	PC10~PC0←L10~L0; if CF = "1"		1/1
1101 0aaa aaaa aaaa	JNC	L	PC10~PC0←L10~L0; if CF ! = "1"		1/1
0100 1000 0xxx xxxx	DSKZ	R	ACC, R←(R) - 1; PC ← (PC) + 2 if ACC = 0	ZF, CF	1/1
0100 1000 1xxx xxxx	DSKNZ	R	ACC, R←(R) - 1; PC ← (PC) + 2 if ACC ! = 0	ZF, CF	1/1
1010 1000 0xxx xxxx	SKB0	R	PC ← (PC) + 2 if R.0 = "1"		1/1
1010 1000 1xxx xxxx	SKB1	R	PC ← (PC) + 2 if R.1 = "1"		1/1
1010 1001 0xxx xxxx	SKB2	R	PC ← (PC) + 2 if R.2 = "1"		1/1
1010 1001 1xxx xxxx	SKB3	R	PC ← (PC) + 2 if R.3 = "1"		1/1
Subroutine					
0110 0aaa aaaa aaaa	CALL	L	STACK ← (PC)+1, TAB0, TAB1, TAB2, TAB3, DBKRL, DBKRH, WRP, ROMPR, PAGE, ACC, CF PC14 ~ PC0 ← (ROMPR) × 800H + L10 ~ L0		1/1
0000 0001 0000 0000	RTN		Pop PC		1/1
0000 0001 IIII IIII	RTN	# I	Pop PC; Pop other registers by I setting refer to below table		1/1

Bit Definition of I	
I = 0000 0000	Pop PC from stack only
Bit0 = 1	Pop **TAB0, TAB1, TAB2, TAB3** from stack
Bit1 = 1	Pop **DBKRL, DBKRH** from stack
Bit2 = 1	Pop **WRP** from stack
Bit3 = 1	Pop **ROMPR** from stack
Bit4 = 1	Pop **PAGE** from stack
Bit5 = 1	Pop **ACC** from stack
Bit6 = 1	Pop **CF** from stack

Instruction set, continued

Machine code	Mnemonic		Function	Flag affected	W/C
Data move					
1110 1nnn nxxx xxxx	MOV	WRn, R	WRn←(R)		1/1
1111 1nnn nxxx xxxx	MOV	R, WRn	R←(WRn)		1/1
0110 1nnn nxxx xxxx	MOVA	WRn, R	ACC, WRn←(R)	ZF	1/1
0111 1nnn nxxx xxxx	MOVA	R, WRn	ACC, R←(WRn)	ZF	1/1
0101 1001 1xxx xxxx	MOV	R, ACC	R←(ACC)		1/1
0100 1110 1xxx xxxx	MOV	ACC, R	ACC←(R)	ZF	1/1
1011 1 i i i i xxx xxxx	MOV	R, #I	R←I		1/1
1100 1nnn n000 qqqq	MOV	WRn, @WRq	WRn←[(DBKRH) x 800H + (DBKRL) × 80H + (PAGE) x 10H + (WRq)]		1/2
1101 1nnn n000 qqqq	MOV	@WRq, WRn	[(DBKRH) x 800H + (DBKRL) × 80H + (PAGE) x 10H + (WRq)]←WRn		1/2
1000 1100 0xxx xxxx	MOV	TAB0, R	TAB0←(R)		1/1
1000 1100 1xxx xxxx	MOV	TAB1, R	TAB1←(R)		1/1
1000 1110 0xxx xxxx	MOV	TAB2, R	TAB2←(R)		1/1
1000 1110 1xxx xxxx	MOV	TAB3, R	TAB3←(R)		1/1
1000 1101 0xxx xxxx	MOVC	R	R←[(TAB3) × 1000H + (TAB2) × 100H + (TAB1) x 10H + (TAB0)]/4		1/2
Input & Output					
0101 1011 0xxx xxxx	MOVA	R, RA	ACC, R←[RA]	ZF	1/1
0101 1011 1xxx xxxx	MOVA	R, RB	ACC, R←[RB]	ZF	1/1
0100 1011 0xxx xxxx	MOVA	R, RC	ACC, R←[RC]	ZF	1/1
0100 1011 1xxx xxxx	MOVA	R, RD	ACC, R←[RD]	ZF	1/1
0101 1100 0xxx xxxx	MOVA	R, P0	ACC, R←[P0]	ZF	1/1
0101 1100 0xxx xxxx	MOVA	R, P1	ACC, R←[P1]	ZF	1/1
0101 1010 0xxx xxxx	MOV	RA, R	[RA]←(R)		1/1
0101 1010 1xxx xxxx	MOV	RB, R	[RB]←(R)		1/1
1010 1100 0xxx xxxx	MOV	RC, R	[RC]←(R)		1/1
1010 1100 1xxx xxxx	MOV	RD, R	[RD]←(R)		1/1
0101 1110 0xxx xxxx	MOV	RE, R	[RE]←(R)		1/1
1010 1110 0xxx xxxx	MOV	RF, R	[RF]←(R)		1/1
1010 1101 0xxx xxxx	MOV	P0, R	[P0]←(R)		1/1
0001 0010 i i i i i i i i	MOV	MFP, #I	[MFP]← I		1/1

Instruction set, continued

Machine code	Mnemonic		Function	Flag affected	W/C
Flag & Register					
0101 1111 1xxx xxxx	MOVA	R, PAGE	ACC, R←PAGE (Page Register)	ZF	1/1
0101 1110 1xxx xxxx	MOV	PAGE, R	PAGE←(R)		1/1
0101 0110 1000 0iii	MOV	PAGE, #I	PAGE←I		1/1
1001 1101 1xxx xxxx	MOV	R, WRP	R←WRP		1/1
1001 1100 1xxx xxxx	MOV	WRP, R	WRP←(R)		1/1
0011 0101 1000 iiii	MOV	WRP, #I	WRP←I		1/1
0011 0101 0000 iiii	MOV	DBKRL, #I	DBKRL←I		1/1
0011 0101 0100 000i	MOV	DBKRH, #I	DBKRH←I		1/1
1001 1101 0000nnnn	MOV	WRn,DBKRL	WRn←DBKRL		1/1
1001 1101 0100nnnn	MOV	WRn,DBKRH	WRn←DBKRH		1/1
1001 1100 0000nnnn	MOV	DBKRL, WRn	DBKRL←WRn		1/1
1001 1100 0100nnnn	MOV	DBKRH, WRn	DBKRH←WRn		1/1
0011 0100 0000 iiii	MOV	ROMPR, #I	ROMPR←I		1/1
1000 1000 0xxx xxxx	MOV	ROMPR, R	ROMPR←(R)		1/1
1000 1001 0xxx xxxx	MOV	R, ROMPR	R←(ROMPR)		1/1
0001 0011 1000 i00i	MOV	MR0, #I	MR0←I		1/1
0001 0011 0000 iiii	MOV	MR1, #I	MR1←I		1/1
0101 1001 0xxx xxxx	MOVA	R, CF	ACC.0, R.0←CF	ZF	1/1
0101 1000 0xxx xxxx	MOV	CF, R	CF←(R.0)	CF	1/1
0100 1001 0xxx xxxx	MOVA	R, HCFL	ACC, R←HCF.0~HCF.3	ZF	1/1
0100 1001 1xxx xxxx	MOVA	R, HCFH	ACC, R←HCF.4~HCF.7	ZF	1/1
0101 0011 0000 iiii	MOV	PM0, #I	Port Mode 0← I		1/1
0101 0111 0000 iiii	MOV	PM1, #I	Port Mode 1← I		1/1
0101 0111 1000 iiii	MOV	PM2, #I	Port Mode 2← I		1/1
0011 0111 0000 iiii	MOV	PM4, #I	Port Mode 4← I		1/1
0011 0111 1000 iiii	MOV	PM5, #I	Port Mode 5← I		1/1
0101 0011 1000 iiii	MOV	PM6, #I	Port Mode 6← I		1/1
0100 0000 i00i iiii	CLR	EVF, #I	Clear Event Flag if In = 1		1/1
0011 0000 0000 0000	CLR	EVFD	Clear RD Event Flag if In = 1		1/1

Instruction set, continued

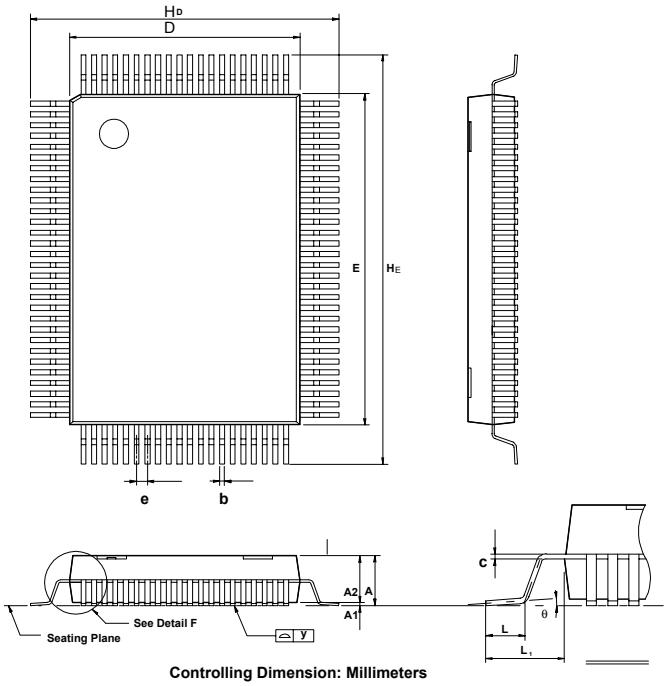
Machine code	Mnemonic		Function	Flag affected	W/C
Flag & Register					
0101 1101 0xxx xxxx	MOVA	R, EVFL	ACC, R← EVF.0 - EVF.3		1/1
0101 1101 1xxx xxxx	MOVA	R, EVFH	ACC, R← EVF.4 - EVF.7		1/1
0100 0001 iiii iiii	MOV	HEF, #I	Set/Reset HOLD mode release Enable Flag		1/1
0011 0001 0000 000 i	MOV	HEFD,#I	Set/Reset RD HOLD mode release Enable Flag		1/1
0101 0001 iiii iiii	MOV	IEF, #I	Set/Reset Interrupt Enable Flag		1/1
0100 0011 0000 iiii	MOV	PEF, #I	Set/Reset Port Enable Flag		1/1
0011 0011 0000 ii 00	MOV	P1EF, #I	Set/Reset P1 Port Enable Flag		1/1
0101 0010 iiiiiiii	MOV	SEF, #I	Set/Reset STOP mode wake-up Enable Flag for RC, RD port		1/1
0101 0100 0000 iiii	MOV	SCR, #I	SCR←I		1/1
0100 1111 0xxx xxxx	MOVA	R, PSR0	ACC, R←Port Status Register 0	ZF	1/1
0100 1111 1xxx xxxx	MOVA	R, PSR1	ACC, R←Port Status Register 1	ZF	1/1
0101 1111 0xxx xxxx	MOVA	R, PSR2	ACC, R←Port Status Register 2	ZF	1/1
0100 0010 0000 0000	CLR	PSR0	Clear Port Status Register 0		1/1
0100 0010 1000 0000	CLR	PSR1	Clear Port Status Register 1		1/1
0100 0010 1100 0000	CLR	PSR2	Clear Port Status Register 2		1/1
0101 0000 0100 0000	SET	CF	Set Carry Flag	CF	1/1
0101 0000 0000 0000	CLR	CF	Clear Carry Flag	CF	1/1
0001 0111 0000 0000	CLR	DIVR0	Clear the last 4-bit of the Divider 0		1/1
0101 0101 1000 0000	CLR	DIVR1	Clear the last 4-bit of the Divider 1		1/1
0001 0111 1000 0000	CLR	WDT	Clear WatchDog Timer		1/1
Shift & Rotate					
0100 1101 0xxx xxxx	SHRC	R	ACC.n, R.n←(R.n+1); ACC.3, R.3←0; CF←R.0	ZF, CF	1/1
0100 1101 1xxx xxxx	RRC	R	ACC.n, R.n←(R.n+1); ACC.3, R.3←CF; CF←R.0	ZF, CF	1/1
0100 1100 0xxx xxxx	SHLC	R	ACC.n, R.n←(R.n-1); ACC.0, R.0←0; CF←R.3	ZF, CF	1/1
0100 1100 1xxx xxxx	RLC	R	ACC.n, R.n←(R.n-1); ACC.0, R.0←CF; CF←R.3	ZF, CF	1/1

Instruction set, continued

Machine code	Mnemonic		Function	Flag affected	W/C
LCD					
1001 1000 0xxx xxxx	MOV	LPL, R	LPL←(R)		1/1
1001 1000 1xxx xxxx	MOV	LPH, R	LPH←(R)		1/1
1001 1010 0xxx xxxx	MOV	@LP, R	[(LPH) × 10H + (LPL)]←(R)		1/1
1001 1011 0xxx xxxx	MOV	R, @LP	R←[(LPH) × 10H + (LPL)]		1/1
0000 0010 0000 0000	LCDON		LCD ON		1/1
0000 0010 1000 0000	LCDOFF		LCD OFF		1/1
0000 0011 0000 0iii	MOV	LCDCC, #I	LCD contrast control		1/1
Serial I/O					
0011 0010 0000 iiii	MOV	SIC, #I	Serial Interface Control		1/1
1010 1111 0xxx xxxx	SOP	R	P0.1←R(high nibble), A(low nibble) Serially		1/1
1001 1111 0xxx xxxx	SIP	R	R(high nibble), A(low nibble)← P0.1 Serially	ZF	1/1
DTMF and FSK					
0011 0100 1000 iiii	MOV	DTCR, #I	DTMF Enable Control		1/1
1001 1110 1xxx xxxx	MOV	DTMF, R	Select DTMF frequency		1/1
1010 1111 1xxx xxxx	MOV	FSKC, R	FSKC←(R)		1/1
1001 1111 1xxx xxxx	MOVA	R, FSKC	ACC, R←FSKC		1/1
1001 1110 0xxx xxxx	MOV	FSKB, R	FSKB←(R)		1/1
Timer					
1010 1010 0xxx xxxx	MOV	TM0L, R	TM0L←(R)		1/1
1010 1010 1xxx xxxx	MOV	TM0H, R	TM0H←(R)		1/1
1010 1011 0xxx xxxx	MOV	TM1L, R	TM1L←(R)		1/1
1010 1011 1xxx xxxx	MOV	TM1H, R	TM1H←(R)		1/1
1000 1111 0xxx xxxx	MOV	R, TM0L	(R)←TM0L		1/1
1000 1111 1xxx xxxx	MOV	R, TM0H	(R)←TM0H		1/1
1001 1001 0xxx xxxx	MOV	R, TM1L	(R)←TM1L		1/1
1001 1001 1xxx xxxx	MOV	R, TM1H	(R)←TM1H		1/1
Other					
0000 0000 1000 0000	HOLD		Enter Hold mode		1/1
0000 0000 1100 0000	STOP		Enter Stop mode		1/1
0000 0000 0000 0000	NOP		No operation		1/1
0101 0000 1100 0000	EN	INT	Enable interrupt function		1/1
0101 0000 1000 0000	DIS	INT	Disable interrupt function		1/1

10. PACKAGE DIMENSIONS

100-lead QFP (14 x 20 x 2.75 mm footprint 4.8 mm)



Controlling Dimension: Millimeters

Symbol	Dimension in Inches			Dimension in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	—	—	—	—	—	—
A_1	0.010	0.014	0.018	0.25	0.35	0.45
A_2	0.101	0.107	0.113	2.57	2.72	2.87
b	0.008	0.012	0.016	0.20	0.30	0.40
c	0.004	0.006	0.008	0.10	0.15	0.20
D	0.547	0.551	0.555	13.90	14.00	14.10
E	0.783	0.787	0.791	19.90	20.00	20.10
e	0.020	0.026	0.032	0.498	0.65	0.802
H_D	0.746	0.740	0.756	18.40	18.80	19.20
H_E	0.960	0.976	0.992	24.40	24.80	25.20
L	0.039	0.047	0.055	1.00	1.20	1.40
L_1	—	0.064	—	—	2.40	—
y	—	—	0.003	—	—	0.08
θ	0°	—	7°	0°	—	7°

11. REVISION HISTORTY

VERSION	DATE	PAGE	REASONS FOR CHANGE
A1	December 17, 2001		-
A2	April 15, 2005	-	Add Important Notice

Important Notice

Winbond products are not designed, intended, authorized or warranted for use as components in systems or equipment intended for surgical implantation, atomic energy control instruments, airplane or spaceship instruments, transportation instruments, traffic signal instruments, combustion control instruments, or for other applications intended to support or sustain life. Further more, Winbond products are not intended for applications wherein failure of Winbond products could result or lead to a situation wherein personal injury, death or severe property or environmental damage could occur.

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