

NCP12600

Multi-Mode Controller for Offline Power Supplies

The NCP12600 is a peak-current controller operating at a 65-kHz or 100-kHz fixed frequency. In high power conditions, the part operates in continuous conduction mode (CCM). As the load current reduces, the converter enters the discontinuous conduction mode (DCM) of operation and synchronizes the turn-on event with the minimum of the drain voltage. The NCP12600 implements valley switching mode with a proprietary lockout scheme ensuring noise-free operations. As output power further reduces, the controller folds the switching frequency back and ensures stable valley switching operations down to the 32nd valley provided the ringing is of sufficient amplitude. The controller then enters a proprietary Quiet-Skip skip-mode at small peak currents which reduces acoustic noise and optimizes no-load standby power.

Adjustable over power protection ensures a flat output power level regardless of the operating input voltage. Slope compensation is ensured via the insertion of a resistor in series with the current sense pin and is thus user-adjustable. The device packs several useful features such as an extremely fast short circuit protection, a soft start in current and frequency plus a dedicated circuitry to avoid latch off in case of a line cycle dropout.

Over temperature protection (OTP) is implemented at the current sense pin and requires the connection of a simple NTC resistance to the auxiliary winding. Over voltage protection (OVP) is done by sampling the auxiliary plateau and exists at the V_{cc} pin level.

Features

- 65-kHz or 100-kHz Fixed-frequency Operation
- Valley Switching in Discontinuous Conduction Mode for Improved Efficiency
- Proprietary Valley Lockout for Controlled Operation in Quasi-resonant Operation and Foldback Modes
- Proprietary Quiet Skip Mode for Noiseless Operation in Light Load
- Adjustable Over Power Protection
- Single 64-ms Protection Timer or Dual OCP Protection in Option
- Frequency Foldback down to 25 kHz
- Auto-recovery or Latched Overload Protection
- True Output Short Circuit Protection with Pre-short Compatibility
- Line Cycle Dropout Recovery in Latched OCP Mode
- 5-ms Soft Start on Both Peak Current and Frequency for Lower Start-up Stress
- Frequency Jitter in All Operating Modes
- Over Voltage Protection with Precise Auxiliary Voltage Sampling Event



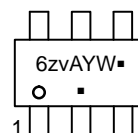
ON Semiconductor®

www.onsemi.com



TSOP-6
(SOT23-6)
SN SUFFIX
CASE 318G
STYLE 13

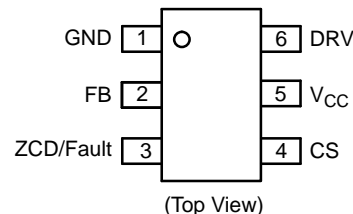
MARKING DIAGRAM



6zvAYW = Specific Device Code
z = A or 2 (frequency)
v = E, F, G or H
A = Assembly Location
Y = Year
W = Work Week
▪ = Pb-Free Package

(Note: Microdot may be in either location)

PIN CONNECTIONS



ORDERING INFORMATION

See detailed ordering, marking and shipping information on page 3 of this data sheet.

- Over Temperature Protection Combined on CS Pin
- Ultra-low Start-up Current Below 10 μ A up to 125°C T_j
- Proprietary Quick Latched-state Reset Scheme
- These are Pb-Free and RoHS-compliant Devices

Typical Applications

- Ac-dc Notebook Adapters, USB Adapters, Wall-mount Power Supplies, Set Top Boxes, etc.

NCP12600

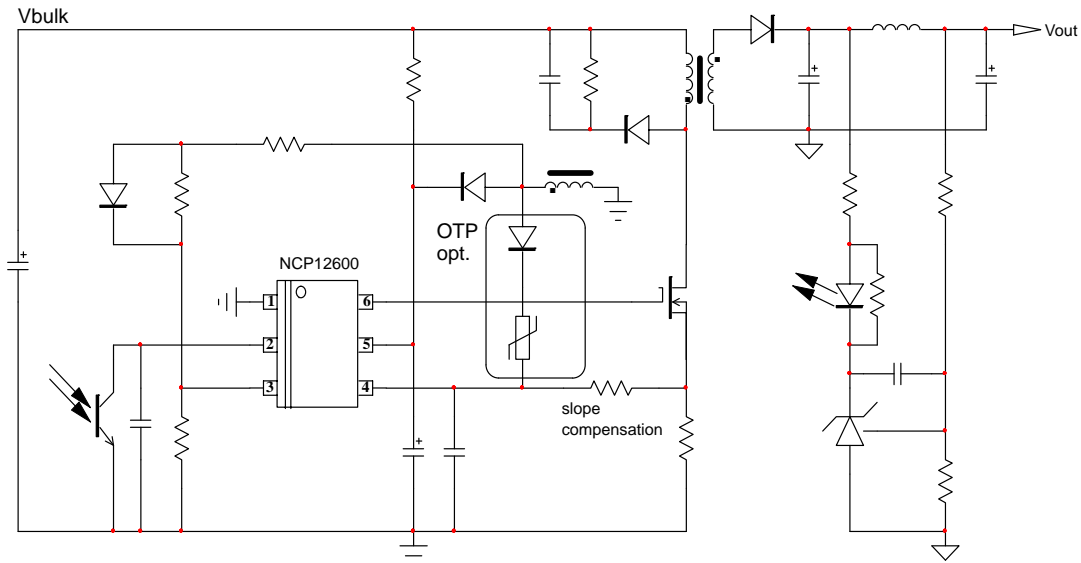


Figure 1. Typical Application Schematic

Table 1. PIN DESCRIPTION

Pin No	Pin Name	Function	Pin Description
1	GND	–	The controller ground.
2	FB	Feedback pin	Feedback input for the controller. Allows direct connection to an optocoupler.
3	ZCD/ OPP/ fault	Detects core reset in QR operation. Latches off the part in OVP. Adjusts OPP level.	A resistive bridge from this pin to the auxiliary winding adjusts the OPP level and lets the controller observe the core magnetic state. A precise OVP level can also be set via this pin.
4	CS	Current sense	This pin monitors the primary peak current but also offers a means to adjust the compensation ramp level. A NTC connected to the pin offers a simple over temperature protection.
5	V _{cc}	Supplies the controller	This pin is connected to an external auxiliary voltage and features an over voltage protection circuitry.
6	DRV	Driver output	The driver's output to an external MOSFET gate. It is clamped to a safe 12-V gate-source level.

Options

Forming the part-number:

NCP12600xyzSN65T1G – 65-kHz version with xyz picked up in the below list

NCP12600xyzSN100T1G – 100-kHz version with xyz picked up in the below list

The following code is adopted for the three letters x, y and z:

X implies the following choice:

A = single OCP

B = dual-level OCP level

Y is the protection scheme:

A = all protections are latched: OVP on demag, V_{cc} OVP, OTP on CS, overload (OCP) and short circuit (SCP)

B = overload (OCP) and short circuit (SCP) are in auto-recovery mode, all other protections (OVP on demag, V_{cc} OVP, OTP on CS) are latched

C = all protections are in auto-recovery: OVP on demag, V_{cc} OVP, OTP on CS, overload (OCP) and short circuit (SCP)

Z implies the following options:

A = quiet skip

B = normal skip mode

600	X	Y	Y
Part	OCP trip point	OCP Fault	Quiet Skip
	A – single, V _{CS} = 0.7 V (max I _p)	A – All latched	A – Yes
	B – dual, V _{CS} = 0.5 V (overload), V _{CS} = 0.7 V (max I _p)	B – SC/OCP autorecovery, rest is latched C – All autorecovery	B – No C to Z – reserved

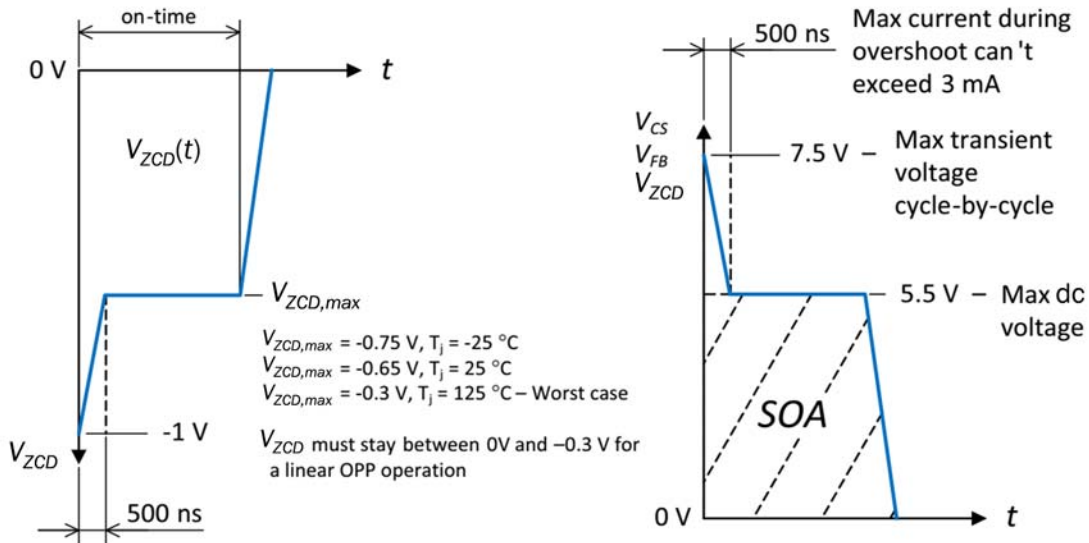
NCP12600

Table 2. MAXIMUM RATINGS TABLE

Symbol	Rating	Value	Unit
V_{CC}	Power Supply voltage, VCC pin, continuous voltage	-0.3 to 28	V
$V_{DRV(tran)}$	DRV pin voltage, transient voltage (Note 1)	-0.3 to $V_{CC} + 0.3$	V
V_{CS}, V_{FB}, V_{ZCD}	Maximum voltage on low power pins CS and FB	-0.3 to 5.5	V
$V_{ZCD(tran)}$	Maximum negative transient voltage on ZCD pin (Note 2)	-1	V
$V_{ZCD(tranp)}$	Maximum positive transient voltage on ZCD pin (2)	7	V
$I_{source,max}$	Maximum sourced current, pulse width < 800 ns	0.6	A
$I_{sink,max}$	Maximum sinked current, pulse width < 800 ns	1.0	A
I_{ZCD}	Maximum injected negative current into the ZCD pin (pin 1)	-2	mA
$R_{\theta J-A}$	Thermal Resistance Junction-to-Air	360	°C/W
$T_{J,max}$	Maximum Junction Temperature	150	°C
	Storage Temperature Range	-60 to +150	°C
HBM	Human Body Model ESD Capability per JEDEC JESD22-A114F (All pins)	7	kV

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. The transient voltage is a voltage spike injected to DRV pin being in high state. Maximum transient duration is 100 ns.
2. See below figure for detailed specification of transient voltage
3. This device contains latch-up protection and exceeds 100 mA per JEDEC Standard JESD78.



NCP12600

Table 3. ELECTRICAL CHARACTERISTICS

(For typical values $T_J = 25^\circ\text{C}$, for min/max values $T_J = -40^\circ\text{C}$ to $+125^\circ\text{C}$, Max $T_J = 150^\circ\text{C}$, $V_{CC} = 12\text{ V}$ unless otherwise noted)

Characteristics	Conditions	Symbol	Min	Typ	Max	Unit
SUPPLY SECTION AND V_{CC} MANAGEMENT						
V_{CC} level at which driving pulses are authorized	V_{CC} increasing	$V_{CC(on)}$	16	18	20	V
V_{CC} level at which driving pulses are stopped	V_{CC} decreasing	$V_{CC(min)}$	8.3	8.9	9.5	V
Start-up hysteresis	Hysteresis $V_{CC(on)} - V_{CC(min)}$	$V_{CC(hyst)}$	7.7			V
Latched-state reset voltage	–	$V_{CC(reset)}$		8.65		V
Hysteresis above $V_{CC(min)}$ for fast hiccup		$V_{CC(hiccup)}$		150		mV
Hysteresis below $V_{CC(min)}$ before reset	Hysteresis $V_{CC(min)} - V_{CC(reset)}$	$V_{CC(reset, hyst)}$	0.18	0.33	0.42	V
Start-up supply current, controller disabled or latched	$V_{CC} = V_{CC(on)} - 100\text{ mV}$	I_{CC1}	–	5	10	μA
Internal IC consumption, steady state	$F_{sw} = 65\text{ kHz}$, $C_{DRV} = 0\text{ nF}$, $V_{FB} = 3.2\text{ V}$ $F_{sw} = 100\text{ kHz}$, $C_{DRV} = 0\text{ nF}$, $V_{FB} = 3.2\text{ V}$	I_{CC2}	–	1 1.1		mA
Internal IC consumption, steady state	$F_{sw} = 65\text{ kHz}$, $C_{DRV} = 1\text{ nF}$, $V_{FB} = 3.2\text{ V}$ $F_{sw} = 100\text{ kHz}$, $C_{DRV} = 1\text{ nF}$, $V_{FB} = 3.2\text{ V}$	I_{CC3}	–	1.7 2.3		mA
Internal IC consumption, skip mode – non switching	Feedback voltage is below skip level	$I_{CC(no-load)}$		300		μA
Internal IC consumption in skip mode – switching in application, <u>for information only</u>	($V_{CC} = 12\text{ V}$, driving a typical 7-A/650-V MOSFET, includes optocoupler current)	$I_{CC(standby)}$		420		μA
Internal IC consumption from OVP acknowledgment to $V_{CC(off)}$ – Single-shot event	IC detects an OVP and quickly brings V_{CC} to $V_{CC(off)}$ for hiccup	$I_{CC(OVP)}$		1		mA
CURRENT SENSE COMPARATOR						
Maximum Current Sense Voltage Limit – no OPP	$V_{FB} = V_{FB(max)}$, V_{CS} increasing $V_{ZCD} < -60\text{ mV}$ (Notes 4, 5)	V_{LIM1}	0.65	0.7	0.75	V
Overload Current Sense Voltage Threshold – dual OCP option	$V_{FB} = V_{FB(max)}$, V_{CS} increasing	V_{LIM2}	0.46	0.5	0.53	V
Cycle by Cycle Leading Edge Blanking Duration		t_{LEB1}	230	280	340	ns
Cycle by Cycle Current Sense Propagation Delay	$V_{CS} > (V_{LIM1} + 100\text{ mV})$ to DRV turn-off	t_{LIM}	–	50	100	ns
Maximum Setpoint decrease for pin 3 biased to -290 mV (Note 6)	$V_{ZCD} = -290\text{ mV}$	$IOPP_M$		32.8		%
Voltage setpoint for pin 3 biased to -250 mV (Note 6)		$IOPP_{VET}$	0.46	0.51	0.56	V
Blanking delay before considering V_{ZCD} for OPP		$IOPP_{del}$		600		ns
Pin 4 voltage bias for 0% OPP	$V_{ZCD} = -60\text{ mV}$	$IOPP_0$		-60		mV
Frozen CS voltage in skip mode	$V_{FB} = 1\text{ V}$	V_{freeze}		200		mV
Soft start, time to meet $I_{p,max}$ at start up	Open feedback pin	t_{SS}		5		ms
OSCILLATOR						
Oscillator frequency – nominal (65 kHz version)	$2.4\text{ V} < V_{FB} < 3.8\text{ V}$	$f_{osc,nom}$	61	65	71	kHz
Oscillator frequency – nominal (100 kHz version)	$2.4\text{ V} < V_{FB} < 3.8\text{ V}$	$f_{osc,nom}$	90	100	110	kHz
Oscillator frequency – minimum	$V_{FB} < 1.3\text{ V}$	$f_{osc,min}$	23	26	31	kHz
Maximum duty ratio		D_{max}	76			%

4. OPP is not active as long as the negative voltage on the ZCD pin during t_{on} is less than -60 mV .

5. beyond 3.8 V, the peak current is clamped to V_{LIM} .

6. for proper linearity over negative bias voltage, we recommend keeping the level on pin 3 below -300 mV .

NCP12600

Table 3. ELECTRICAL CHARACTERISTICS

(For typical values $T_J = 25^\circ\text{C}$, for min/max values $T_J = -40^\circ\text{C}$ to $+125^\circ\text{C}$, Max $T_J = 150^\circ\text{C}$, $V_{CC} = 12\text{ V}$ unless otherwise noted)

Characteristics	Conditions	Symbol	Min	Typ	Max	Unit
OSCILLATOR						
Frequency jittering in percentage of f_{osc}	CCM-only operation	f_{jitter}		± 6		%
Frequency jitter in valley-switching mode	Internal offset to CS control	$f_{swingDCM}$		± 10		mV
Jitter modulation frequency in all modes	–	f_{swing}		1		kHz
Soft-start, time to meet nominal F_{sw} at start up	Open feedback pin	t_{SS}		5		ms
INTERNAL SLOPE COMPENSATION						
Artificial ramp level for slope compensation	Internal level at $T_J = 25^\circ\text{C}$	V_{ramp}	–	4.2	–	V
Internal ramp resistance to CS pin		R_{ramp}	–	20.4	–	k Ω
FEEDBACK SECTION						
Feedback Input Open Voltage	FB pin is unloaded	$V_{FB(open)}$		4		V
Internal Current Setpoint Division Ratio	–	K_{ratio}	–	5.4	–	–
Pull-up resistance	–	R_{FB}	–	40	–	k Ω
Equivalent resistance for the optocoupler	–	R_{eq}		29		k Ω
Frequency foldback threshold, $F_{sw} < 65\text{ kHz}$	–	V_{fold}	2.3	2.4	2.5	V
End of frequency foldback threshold	–	$V_{fold,end}$	1.8	1.9	2	V
Feedback voltage thresholds for skip mode	V_{FB} going down, $T_J = 25^\circ\text{C}$	$V_{skip(in)}$	0.9	1.0	1.1	V
Skip-cycle current in percentage of I_{LIM}	–	I_{skip}		26		%
Hysteresis on skip comparator	V_{FB} is going up	$I_{skip,hys}$		60		mV
QUIET SKIP ONLY						
Minimum number of pulses in burst		$n_{P,skip}$	3	–	–	–
Skip out delay		t_{skip}	–	–	38	μs
Quiet-Skip timer		t_{quiet}	1.0	1.25	1.5	ms
Quiet-Skip escape level (transient enhancer)	V_{FB} going up, $T_J = 25^\circ\text{C}$	$V_{skip(tran)}$	1.8	2	2.2	V
DEMAGNETIZATION SENSE						
V_{ZCD} threshold voltage	V_{ZCD} decreasing	$V_{ZCD(TH)}$	25	45	70	mV
V_{ZCD} hysteresis	V_{ZCD} increasing	$V_{ZCD(HYS)}$		30		mV
Threshold voltage for output short circuit or aux. winding short circuit detection (enter)	After t_{delay_ZCD} if $V_{ZCD} < V_{ZCD(short1)}$	$V_{ZCD(short1)}$	–	0.4	–	V
Threshold voltage for output short circuit or aux. winding short circuit detection (exit)	After t_{delay_ZCD} if $V_{ZCD} > V_{ZCD(short2)}$	$V_{ZCD(short2)}$		0.5		V
Propagation Delay from valley detection to DRV high	V_{ZCD} decreasing from 3 V to 0 V	T_{DEM}	–	–	150	ns
Internal delay after demagnetization detection		t_{delay}		100		ns
Timeout after last demagnetization transition (leakage ringing blanking)	–	$T_{timeout}$	4.5	5.5	6.5	μs
Input leakage current	$V_{CC} > V_{CC(on)}$ $V_{ZCD} = 3\text{ V}$, DRV is low	I_{ZCD}	–	–	0.1	μA
Low- V_{in} flag activation – latched OCP version only	Neg. bias present during the on-time	V_{BOin}	–22	–30	–38	mV
DRIVE OUTPUT						
Drive resistance DRV Sink DRV Source		R_{SNK} R_{SRC}	– –	16 22	– –	Ω

4. OPP is not active as long as the negative voltage on the ZCD pin during t_{on} is less than -60 mV .

5. beyond 3.8 V, the peak current is clamped to V_{LIM} .

6. for proper linearity over negative bias voltage, we recommend keeping the level on pin 3 below -300 mV .

NCP12600

Table 3. ELECTRICAL CHARACTERISTICS

(For typical values $T_J = 25^\circ\text{C}$, for min/max values $T_J = -40^\circ\text{C}$ to $+125^\circ\text{C}$, Max $T_J = 150^\circ\text{C}$, $V_{CC} = 12\text{ V}$ unless otherwise noted)

Characteristics	Conditions	Symbol	Min	Typ	Max	Unit
DRIVE OUTPUT						
Rise time	$C_{DRV} = 1\text{ nF}$, from 10% to 90%	t_r	–	40		ns
Fall time	$C_{DRV} = 1\text{ nF}$, from 90% to 10%	t_f	–	30		ns
DRV Low voltage	$V_{CC} = V_{CC(\text{off})} + 0.2\text{ V}$, $C_{DRV} = 220\text{ pF}$, $R_{DRV} = 33\text{ k}\Omega$	$V_{DRV(\text{low})}$	8	–	–	V
DRV High voltage	$V_{CC} = V_{CC(\text{OVP})} - 0.2\text{ V}$, $C_{DRV} = 220\text{ pF}$, $R_{DRV} = 33\text{ k}\Omega$	$V_{DRV(\text{high})}$	10	12	14	V
Source current	Peak source current $V_{GS} = 0\text{ V}$	I_{source}		300		mA
Sink current	Peak sink current $V_{GS} = 12\text{ V}$	I_{sink}		500		mA
PROTECTIONS						
Auto-recovery thermal shutdown	Device switching	T_{SHTDN}	–	150	–	$^\circ\text{C}$
Thermal Shutdown Hysteresis	Device switching	$T_{\text{SHTDN}(\text{HYS})}$	–	40	–	$^\circ\text{C}$
Fault level detection for OVP, demagnetization pin, t_{off} sensing	Internal sample V_{out} increasing	V_{OVP1}	2.85	3.15	3.35	V
Fault level detection on CS pin for OTP implementation – confirmation delay is T_{PP}	Internal sample V_{CS} increasing	V_{OTP}	0.97	1	1.03	V
Over Voltage Protection on the V_{CC} pin	–	V_{OVP2}	24	25.5	27	V
Sampling delay for OTP and OVP detection ($F_{\text{sw}} = 65\text{ kHz}$)	Sampling event on ZCD and CS pins	$T_{\text{delay_ZCD1}}$	1.2	1.5	1.8	μs
Sampling delay for OTP and OVP detection ($F_{\text{sw}} = 100\text{ kHz}$)	Sampling event on ZCD and CS pins	$T_{\text{delay_ZCD2}}$	0.8	1.1	1.3	μs
Number of drive cycles before latch confirmation on OVP1 and 2	$V_{\text{ZCD}} > V_{\text{OVP1}}$	$T_{\text{latch_count}}$	–	8	–	–
Timer Delay Before Fault Acknowledgment – Condition 1 – single OCP only	CS pin is $\geq 0.7\text{ V}$	T_{PP1}	55	64	75	ms
Timer Delay Before Fault Acknowledgment in Overload Condition – dual OCP only	CS pin $\geq 0.5\text{ V}$	T_{OCP}	200	256	300	ms
Timer Delay Before Fault Acknowledgment with dual OCP – dual OCP only	CS pin is $\geq 0.7\text{ V}$	T_{PP2}	55	64	75	ms
Timer Delay in Clock Cycles Before Fault Acknowledgment when in Output Short Circuit – Condition 2	$V_{\text{ZCD}} < 0.4\text{ V}$ Unit is clock cycles	T_{SCP}		8		

4. OPP is not active as long as the negative voltage on the ZCD pin during t_{on} is less than -60 mV .

5. beyond 3.8 V , the peak current is clamped to V_{ILIM} .

6. for proper linearity over negative bias voltage, we recommend keeping the level on pin 3 below -300 mV .

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

NOTE: Condition 1: V_{FB} is pushed to its maximum open-loop value. The demagnetization pin during the off-time is above 0.4 V .

Condition 2: V_{FB} is pushed to its maximum open-loop value. The demagnetization pin during the off-time is less than 0.4 V .

8 clock cycles are counted and the part latches off or goes into auto-recovery. This mechanism only activates once the 5-ms soft-start sequence is completed.

NCP12600

TYPICAL CHARACTERISTICS

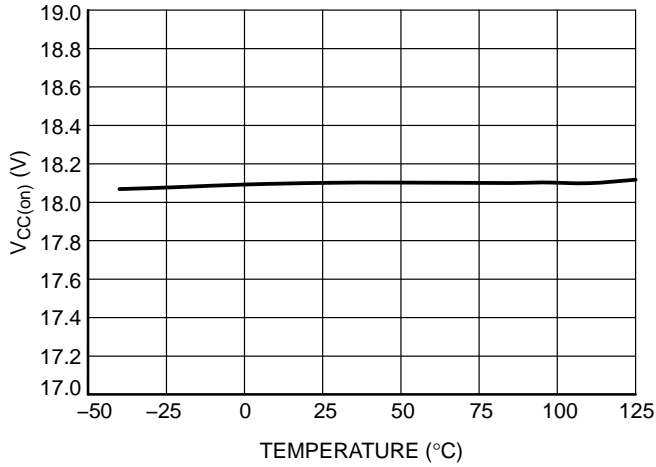


Figure 3.

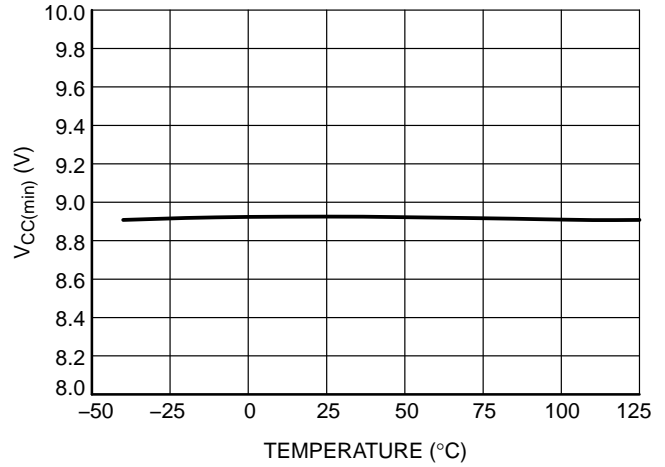


Figure 4.

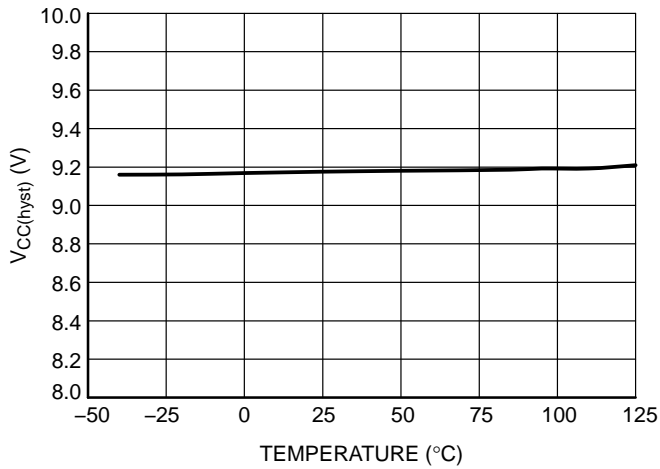


Figure 5.

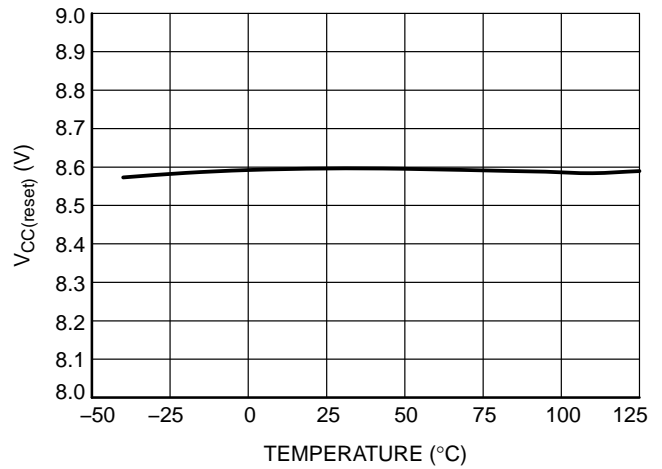


Figure 6.

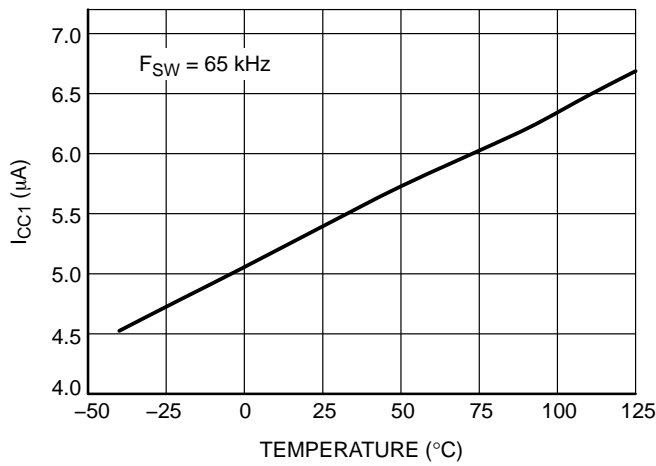


Figure 7.

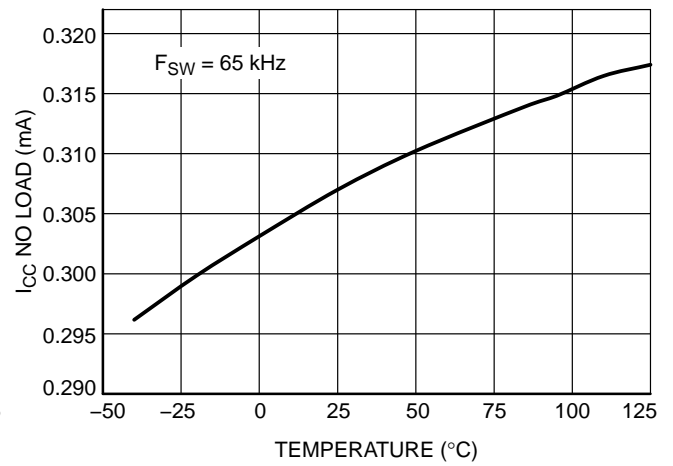


Figure 8.

NCP12600

TYPICAL CHARACTERISTICS

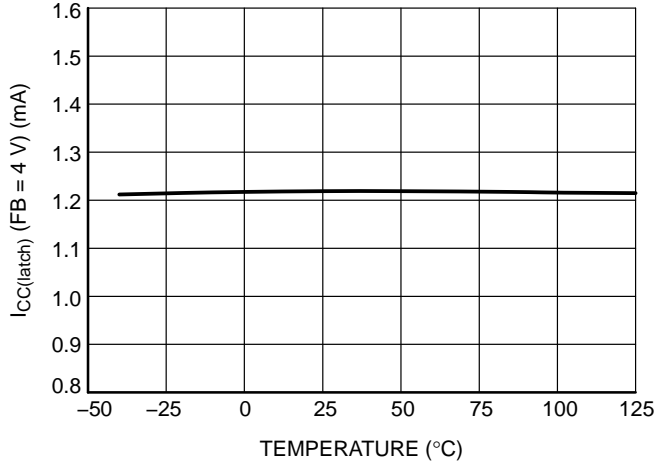


Figure 9.

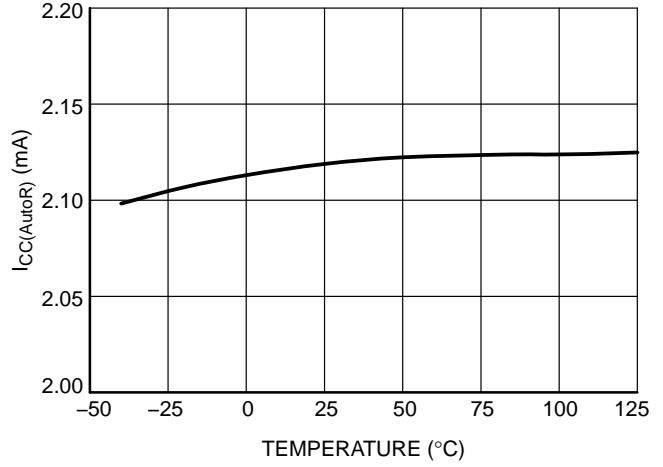


Figure 10.

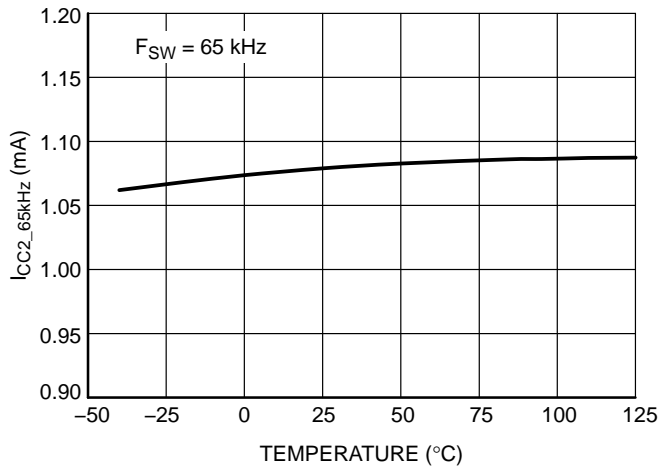


Figure 11.

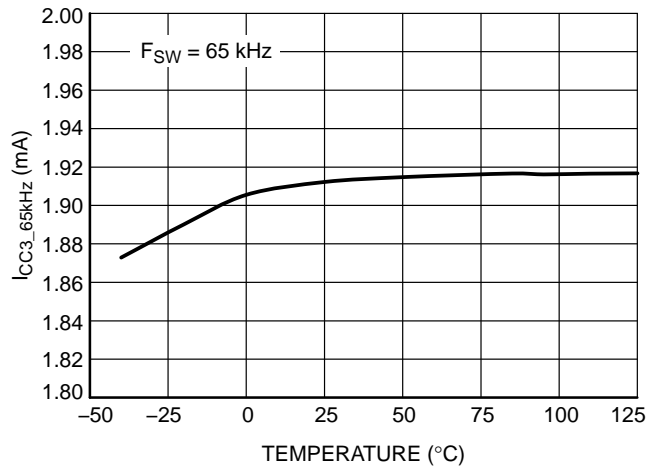


Figure 12.

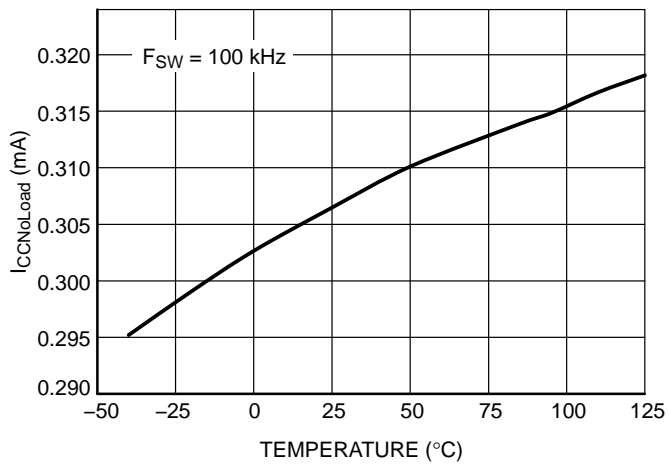


Figure 13.

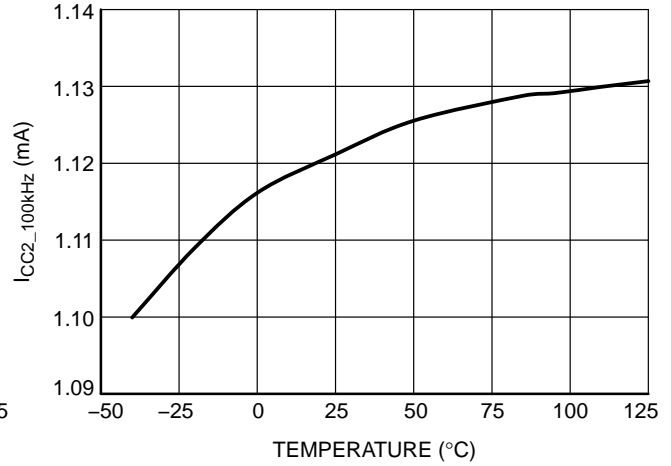


Figure 14.

NCP12600

TYPICAL CHARACTERISTICS

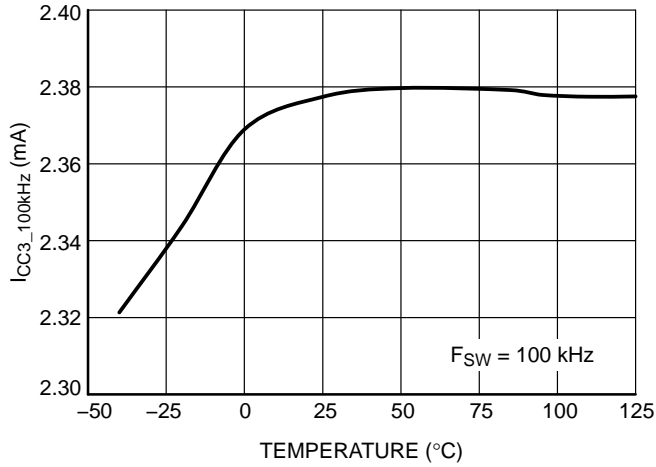


Figure 15.

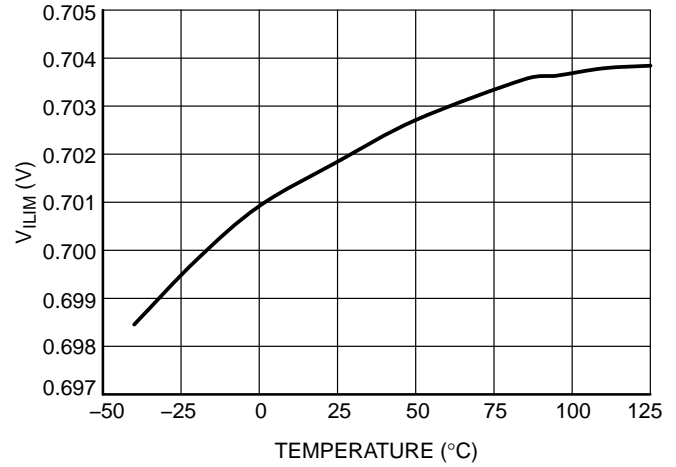


Figure 16.

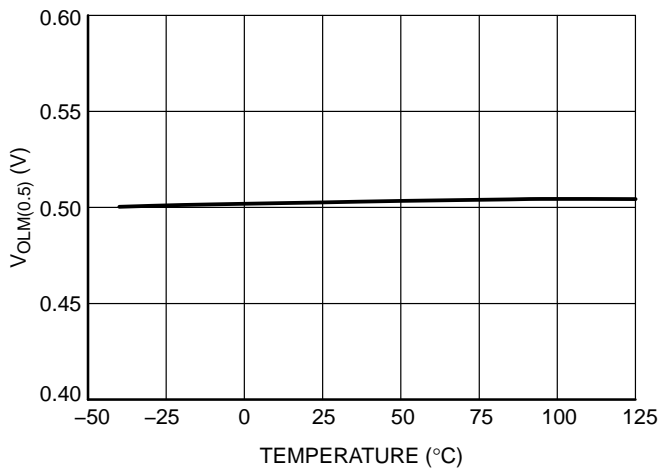


Figure 17.

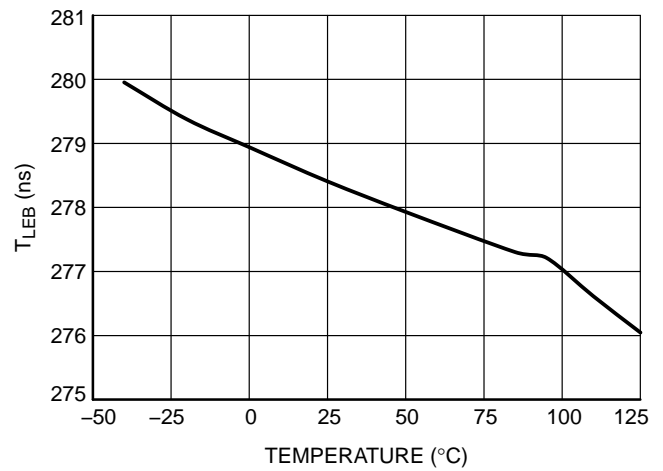


Figure 18.

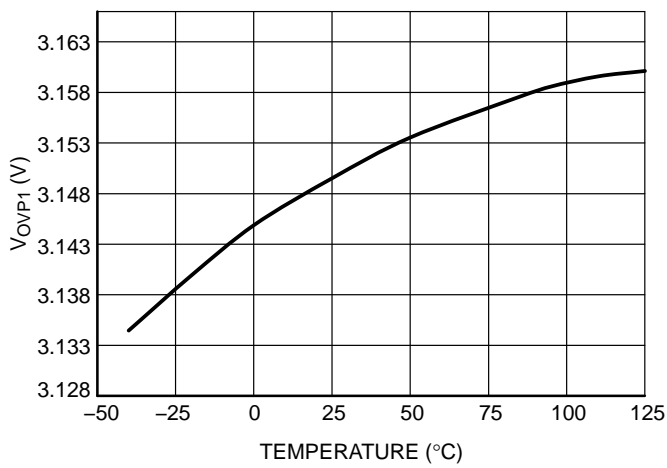


Figure 19.

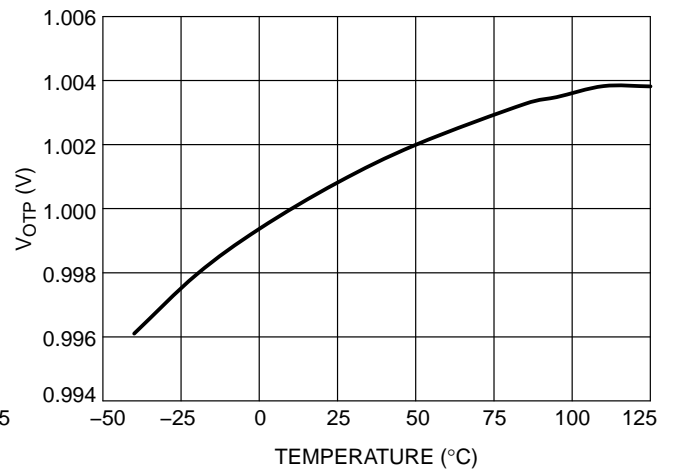


Figure 20.

NCP12600

TYPICAL CHARACTERISTICS

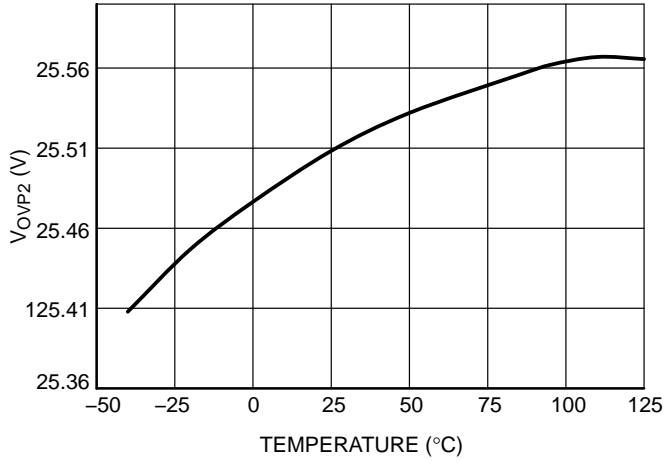


Figure 21.

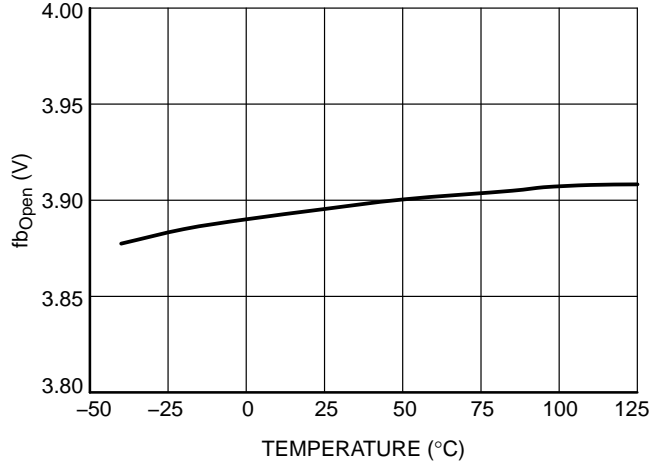


Figure 22.

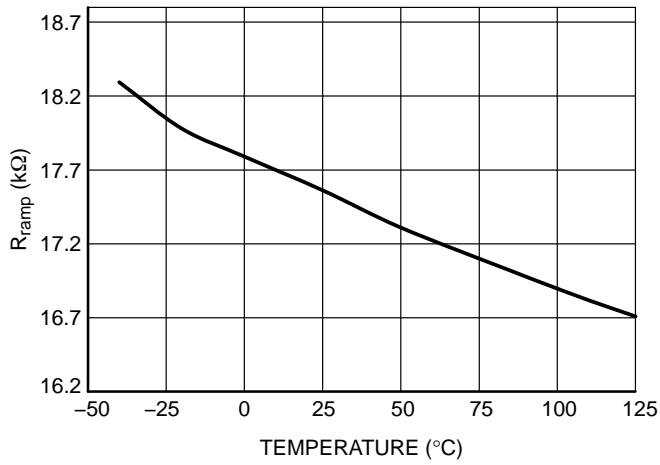


Figure 23.

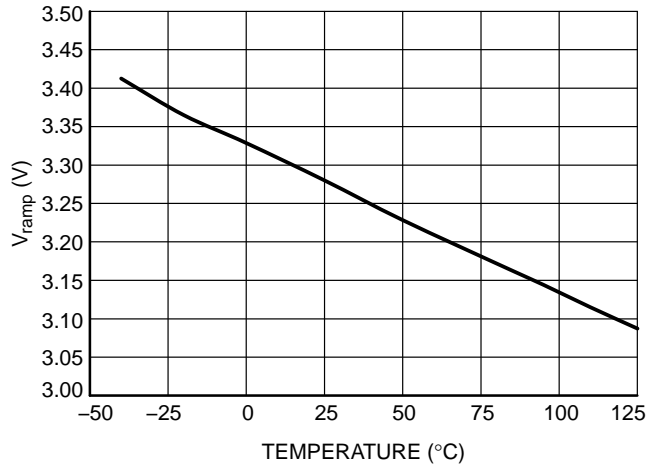


Figure 24.

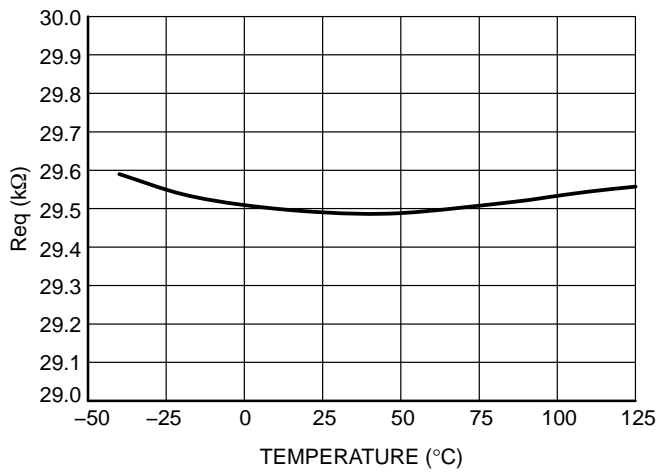


Figure 25.

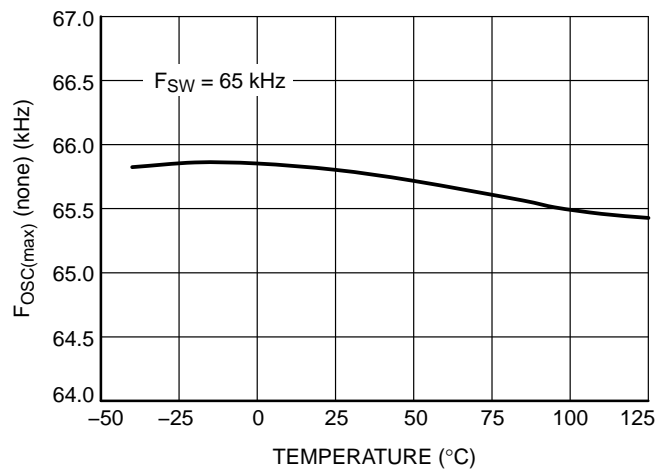


Figure 26.

NCP12600

TYPICAL CHARACTERISTICS

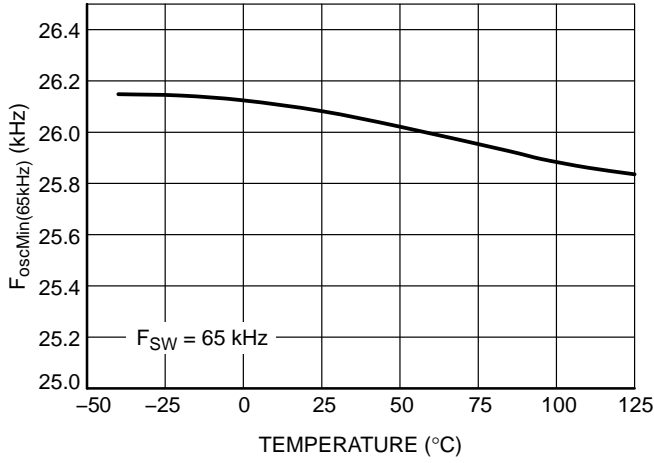


Figure 27.

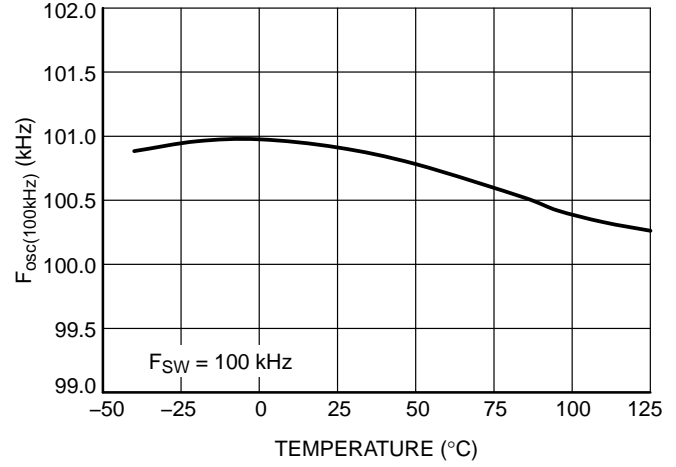


Figure 28.

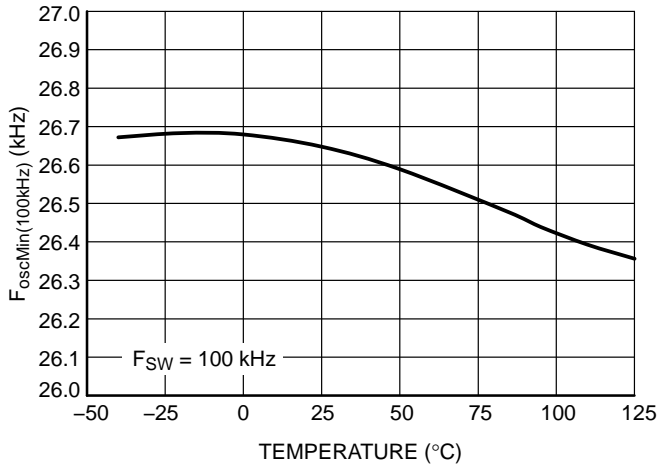


Figure 29.

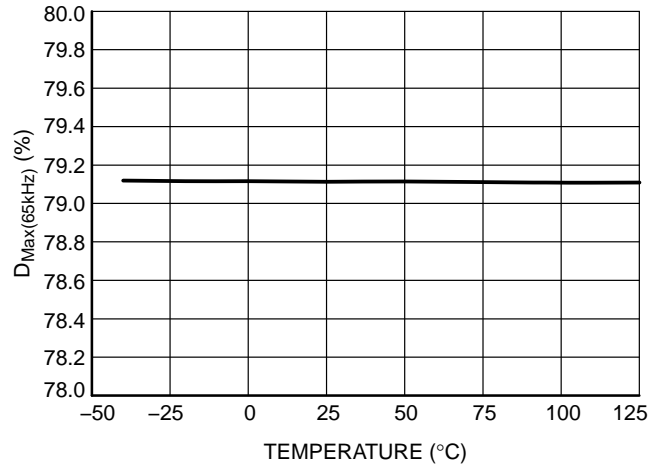


Figure 30.

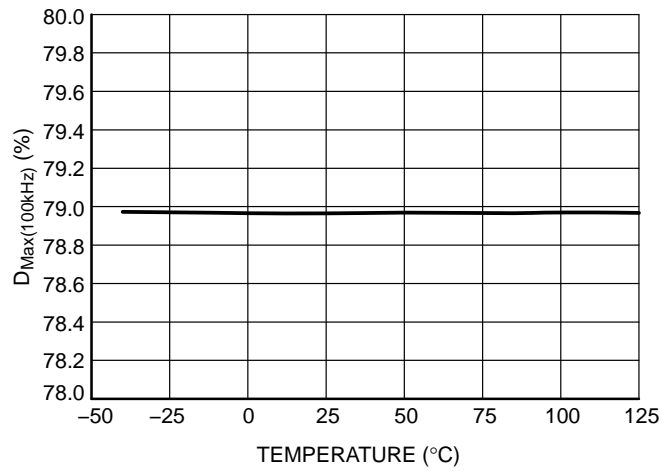


Figure 31.

Application Information

The NCP12600 includes a state-of-the-art multi-mode controller packed in a tiny 6-pin package for fixed-frequency current mode control flyback converters applications. Despite its limited amount of pins, the controller includes numerous proprietary functions which make it an ideal candidate for cost-sensitive applications.

- **Fixed-Frequency Operation:** Implementing peak current mode control, the NCP12600 drives a flyback converter at a 65-kHz or 100-kHz fixed switching frequency and can operate in discontinuous conduction mode (DCM) or continuous conduction mode (CCM).
- **When DCM operation occurs in fixed-frequency operation,** the converter locks in a valley and a specific mechanism paces valley jumps. When the output power reduces, the part enters frequency foldback and jumps into the valleys as the load further reduces. Going down to 32 valleys (if available), the part ensures the lowest turn-on losses and enables excellent overall efficiency. As output power further goes down, the Voltage-Controlled Oscillator (VCO) takes over and reduces frequency down to 25 kHz where the current freezes to 26% of the maximum peak value. Then the part enters normal skip cycle at lower power levels or in a no-load situation.
- **Quiet-Skip operation:** classical skip cycle occurring in light load is a known mechanism to improve the converter's efficiency when the load current becomes lighter. Quiet-Skip also reduces acoustic noise by preventing the skip mode burst period from entering the audible range. The part is also available with a normal skip option.
- **Temporary and peak power capability:** the part includes a 2-level OCP allowing the converter to permanently deliver a certain amount of power as long as V_{CS} is less than 0.5 V. When V_{CS} exceeds 0.5 V, a 256-ms timer is activated. If V_{FB} further increases, the switching frequency remains constant and the controller pushes V_{CS} to its maximum value, the 256-ms OCP timer is instantaneously divided by 4 and becomes a 64-ms timer. When it elapses, the part enters an auto-recovery or latched mode depending on the selected option. As such, the converter can be thermally designed for a 0.5-V V_{CS} and authorizes temporary excursions to a higher power level. Please note that the controller also exists in a single OCP level (0.7 V, 64 ms duration)..
- **Adjustable over power protection (OPP):** Switching power supplies are prone to output power runaway in high-line conditions. To keep the delivered power within control along the input voltage range, a circuit observes the negative voltage present on the demagnetization pin during the on-time and subtracts it from the maximum peak current limit.
- **Low start-up current:** A low start-up current is key to reducing the standby power in no- or light- load situations. With a 10- μ A max guaranteed up to 125°C, the NCP12600 lets you enjoy high-valued start-up resistors for the best standby power performance.
- **Over voltage protection:** By precisely sampling the auxiliary winding plateau voltage after the leakage inductance is damped, the circuit monitors the reflected output voltage with excellent precision. When the monitored voltage exceeds the internal threshold more than 8 successive clock cycles, the part definitively latches off.
- **Over current protection:** When the circuit senses that the feedback loop is lost, $V_{FB} > 3.8$ V, an internal 64-ms timer counts. If the fault disappears while countdown has started, the timer resets and the power converter keeps operating. If the timer elapses, all pulses are immediately stopped and the part enters an auto-recovery hiccup mode.
- **True short-circuit protection:** By observing the peak current setpoint and the off-time voltage on the demagnetization pin, the circuit can detect an output short circuit situation. When this conjunction of events is confirmed, the SCP timer keeps counting. If this situation is observed for more than 8 clock cycles, the circuit immediately stops pulses and enters auto-recovery or latched state. This circuit is active during a start-up sequence (after SS has completed) and in auto-recovery hiccup: if the demagnetization pin is less than 0.4 V after the soft-start period (peak current is maximum), then 8 cycles are counted and the part stops operations. This is extremely efficient to protect against board-level short circuits occurring at high line as the RCD circuit can fail to keep the V_{DS} within safe limits.
- **A general reset is implemented at too low an input voltage and avoids latch off in line dropout tests with OCP-latched versions of the NCP12600.** When V_{out} collapses within a line cycle dropout test, the part does not latch (in case the latched option has been selected) but nicely recovers when the mains is back to its normal level.
- **Quick reset scheme:** When latched on an OVP or an OCP situation, the part will enter a fast low-voltage hiccup mode slightly above the reset voltage. The reset time by input power cycling will be greatly reduced compared to existing solutions.
- **Frequency jitter:** An internal clock modulates the switching frequency and provides an efficient energy spread to ease the converter's EMI signature. Jitter

operates in fixed-frequency mode but also in QR and foldback modes when the VCO is active.

- Over temperature protection is implemented by forming a resistive divider on the CS pin. The auxiliary voltage appears during the off time and the CS level is only considered after the 1.5- μ s blanking time (1.1 μ s for the 100-kHz version). For a well-regulated output voltage, the precision favorably compares with a classical pull-down NTC on a dedicated pin.
- Temperature shutdown: the controller includes an internal thermal sensor which protects the circuit in case of thermal runaway.

Overall Description

The NCP12600 builds upon previous generations of fixed-switching frequency power supply controllers. The frequency is fixed in nominal power conditions but reduces as the load is getting lighter. The major improvement lies in the valley-switching operation: when DCM is entered whether it is in high-power mode or in foldback, the controller locks in the valley to ensure the best efficiency. When variable frequency mode is activated, the part locks in valleys and remains in this state. The peak current is free to move at all times.

CCM Operation

In fixed-frequency operation, the part switches at 65 kHz or 100 kHz in current-mode control and the feedback permanently adjusts the current setpoint. For a feedback voltage beyond 3.8 V, the peak current voltage setpoint is clamped to 0.7 V. The situation with this maximum current cannot last more than 64 ms (T_{PP}). However, if a true short circuit is detected in the output, the controller could potentially place the converter in a dangerous situation if it were pulsing while V_{out} is almost 0 V (heavy CCM can occur in the primary side with a RCD clamp voltage runaway). To avoid this stressful situation, the circuit senses the voltage on the demagnetization pin during t_{off} . If during t_{off} the demagnetization pin voltage is less than 0.4 V for more than 8 consecutive clock cycles, the controller stops all pulses and goes into latch or auto-recovery mode depending on the selected option. If during this mode and before the 8-cycle timer ends, the short circuit disappears and the demagnetization voltage goes above 0.5 V, the protection scheme is reset.

DCM Operation

In fixed-frequency operation, it is very likely that low- and high-line conditions lead to a different operating point for a given P_{out} : CCM in low line and DCM in high line. When the controller operates in CCM, the MOSFET is turned on at a pace imposed by the regular clock. When DCM is entered, the controller senses this mode and extends the off-time to exactly match the next available valley. The peak current is free to move while locked in the valley whether the part operates in fixed frequency mode or in foldback. Inside the controller, a low-frequency refresh

clock (LFC) initiates a valley acquisition and increases or decreases valley count during operations. When the next low-frequency clock occurs, a new valley acquisition is run to determine what valley number matches the upcoming 65-kHz (or 100 kHz) or VCO pulse. It is like a snapshot where you freeze the converter operating point for the upcoming period of time. For example, assume the 1st valley was selected, then the new acquisition may confirm the 3rd valley is the correct one and the part locks in valley 3. It remains there until the next acquisition occurs or a transient unlocks the control. That way, jumping between valleys occurs at a controlled recurrence and not in a completely random way, reducing the possibility to excite a mechanical resonance on the transformer.

Variable Frequency Mode

When the load gets lighter, the feedback voltage starts decreasing. When it reaches 2.4 V, the VCO takes over and frequency reduces. When VFB reaches 1.9 V, the frequency is clamped down to 25 kHz. Below this value, F_{sw} is fixed and down to the skip cycle point, the part operates in peak current mode control.

When the frequency reduces, the controller selects the valley next to the VCO clock and locks in until the next refresh signal comes from the LFC. By using a 5-bit counter, the controller goes down to the 32nd valley if necessary. When a transient is detected on the feedback voltage (load re- or disconnection), the LFC disappears and the part returns to a classical fixed-frequency operation for the best transient response.

Protections

There are several types of protection depending on loading conditions:

1. When the load imposes a peak current setpoint greater than 0.7 V, the 64-ms timer starts counting. When it elapses, the converter latches off or enters auto-recovery depending on the selected option.
2. A dual OCP version exists also for peak power capability: when the peak current setpoint reaches 0.5 V, the 256-ms timer starts counting. If the power further increases, V_{CS} also does and touches the 0.7-V limit. At this moment, the timer is divided by 4, authorizing a 64-ms duration in this mode. Afterwards, the controller latches off or enters an auto-recovery cycle.
3. In this maximum power mode, the converter observes the demagnetization voltage during t_{off} . If this voltage is lower than 0.4 V and if this situation lasts for more than 8 consecutive clock cycles, the controller immediately stops pulsing and enters auto-recovery or latches off depending on the selected options.
4. During start-up, the controller also observes the demagnetization pin during the off-time. If this voltage is less than 0.4 V once the soft-start sequence is over (peak current is max) while F_{sw} is

65 kHz (or 100 kHz), then the controller counts 8 clock cycles and terminates operation. V_{cc} goes down to UVLO and the IC restarts (hiccup mode) or remains latched (latched version).

5. At any moment when the 64–ms timer circuit is counting, the controller observes a brown–out (BO) flag raised if V_{ZCD} is less than V_{BOin} . If a condition arises during which the BO flag is raised AND any of the timer is counting, all pulses stop but the resulting counter effect (latch for instance) is ignored and V_{cc} is let go down to UVLO for a quick recovery. With this technique, when adapters featuring a latched OCP option are tested in line cycle dropouts, even if the converter would like to latch off because the mains has disappeared while it was heavily loaded, the circuit prevents this and forces the converter to auto recover when the mains is restored..
6. The part senses the plateau voltage on the demagnetization pin 1.5 μ s after the power switch has been turned off (1.1 μ s for the 100–kHz version). This helps ignore the leakage ringing and offers a clean plateau voltage to sense. When the voltage on the demagnetization pin exceeds 3.15 V for 8 consecutive clock cycles, the part latches off (or hiccups depending on the selected option). This is an easy and efficient way to protect the converter in an OVP situation.

7. A similar sampling occurs on the CS pin to check if an OTP event is detected. When the pin exceeds 1 V during the off time for more than 64 ms, the part latches off (or hiccups depending on the selected option).

Start–up Sequence

As illustrated in Figure 32, peak current and the switching frequency are gradually increased at start–up in a 5–ms soft–start (SS) sequence. Frequency starts from 25 kHz and hits 65 kHz (or 100 kHz) after 5 ms as feedback voltage is pushed to its maximum value. The 64–ms timer counts as V_{CS} is above 0.7 V. When the 5–ms SS sequence is over, the peak current is maximum. During this sequence (V_{FB} is still pushed to the max, V_{out} is not on target), if V_{cc} accidentally touches UVLO, the part featuring the pre–short option immediately latches off. On the contrary, if everything goes well – the loop closes (V_{out} is on target) before V_{cc} touches UVLO and the 64–ms timer is reset. If an UVLO event occurs after a normal start–up sequence, it auto–recovers as it should. This smooth start–up mode helps reduce the stress on the output diode or in the synchronous MOSFET when power up occurs on heavy load. As this mode is also activated in auto–recovery protection (for the selected option), it significantly reduces the stress on the various power components when the converter tries resuming operations. Figure 32 offers a typical drive waveform captured during the power–on sequence.

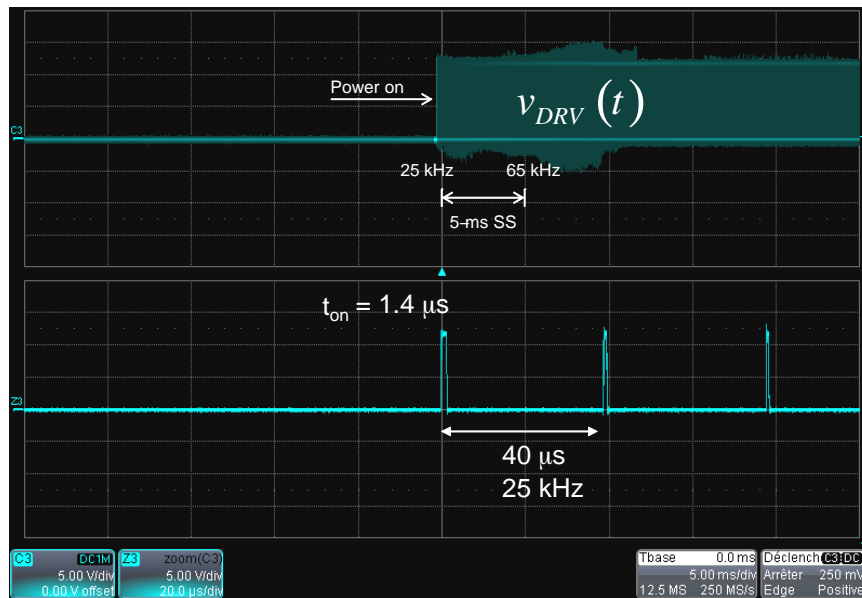


Figure 32. During the start–up sequence, both frequency and current setpoint are slowly raised for 5 ms

The NCP12600 start–up voltage is purposely made high to permit large energy storage in a small V_{cc} capacitor value. This helps operation with a small start–up current which, together with a small V_{cc} capacitor, will not hamper the start–up time. To further reduce the standby power, the

controller start–up current is purposely kept low, below 10 μ A and it is guaranteed up to a 125°C junction temperature. Start–up resistors can therefore be connected to the bulk capacitor or directly to the mains input voltage if desired to save a few more mW.

NCP12600

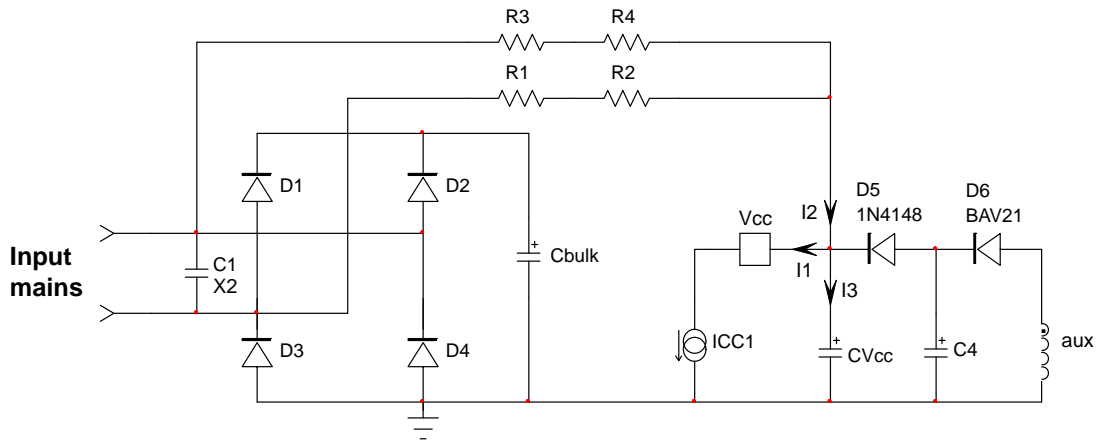


Figure 33. The startup resistor can be connected to the input mains for further power dissipation reduction

Figure 33 shows a typical recommended configuration where start-up resistors connect together to the mains input. This technique offers the benefit of freely discharging the X2 capacitor usually part of the EMI filter. The calculation of these resistors depends on several parameters. Assuming a 0.47- μF X2 capacitor, the safety standard recommends a time constant τ less than 1 s maximum when a resistor is connected in parallel to provide a discharge path. This sets the upper limit for the sum of discharge resistors connected to the controller V_{CC} :

$$R_{\text{startup}} < \frac{1}{0.47 \mu} < 2.1 \text{ M}\Omega \quad (\text{eq. 1})$$

The first step starts with the calculation of the needed V_{CC} capacitor which will supply the controller until the auxiliary winding takes over. Experience shows that this time t_1 can be between 5 and 20 ms depending on the loading conditions and the output capacitance. Considering that we need at least an energy reservoir for a t_1 time of 10 ms, the V_{CC} capacitor must be larger than:

$$C_{V_{CC}} \geq \frac{I_{CC} t_1}{V_{CC\text{on}} - V_{CC\text{min}}} \geq \frac{1.5 \text{ m} \times 10 \text{ m}}{9} \geq 1.6 \mu\text{F} \quad (\text{eq. 2})$$

Let us first select a 2.2- μF capacitor at first and experiments in the laboratory will let us know if we were too optimistic for t_1 . Testing across temperature range is important as capacitance and ESR of this V_{CC} capacitor can be affected. The V_{CC} capacitor being known, we can now evaluate the charging current we need to bring the V_{CC} voltage from 0 to the IC $V_{CC\text{on}}$ voltage, 18 V typical. This current has to be selected to ensure start-up at the lowest mains (85 V rms) to be less than 3 s (2.5 s for design margin) typically for an adapter:

$$I_{\text{charge}} \geq \frac{V_{CC\text{on}} C_{V_{CC}}}{2.5} \geq \frac{18 \times 2.2 \mu}{2.5} \geq 16 \mu\text{A} \quad (\text{eq. 3})$$

If we account for the 10- μA current that flows inside the controller (I_1 in Figure 33), then the total charging current delivered by the start-up resistor must be 26 μA , rounded to 30 μA . If we connect the start-up network to both mains

inputs (two half-wave connections then), half of the average current I_1 is defined by:

$$\frac{I_1}{2} = \frac{V_{ac,rms} \sqrt{2}}{\pi} - V_{CC\text{on}} \quad (\text{eq. 4})$$

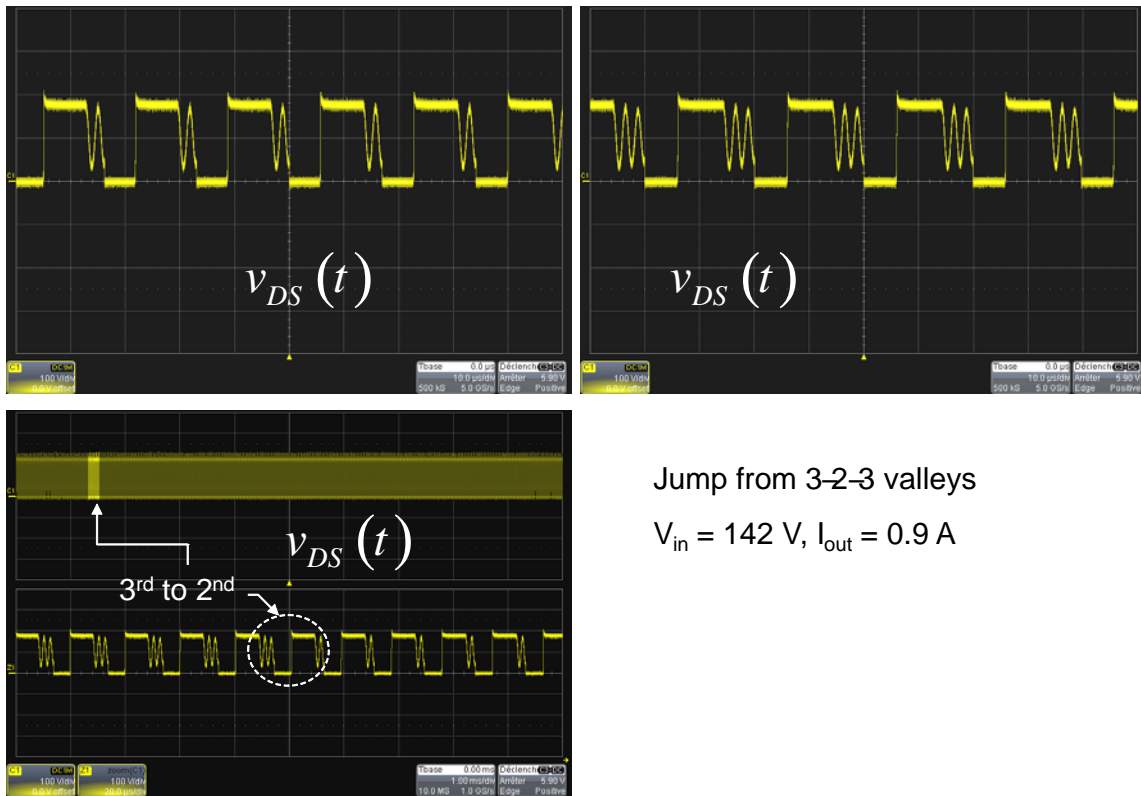
To make sure this current is always greater than 15 μA (half of the necessary 30- μA current), the minimum value for $R_{\text{start-up}}$ can be extracted:

$$R_{\text{start-up}} \leq \frac{V_{ac,rms} \sqrt{2}}{I_{CV_{CC},\text{min}}} - V_{CC\text{on}} \leq \frac{85 \times 1.414}{15 \mu} - 18 \quad (\text{eq. 5})$$

We could thus connect two resistors of 1.3 M Ω (total 2.6 M Ω) across the line to a) power the IC at start up b) ensure X2 discharge when the user unplugs the adapter. However, 2.6 M Ω conflicts with (1) and we will reduce the 1.3-M Ω resistor to a 1-M Ω value, totaling 2 M Ω , in agreement with (1).

Multi-mode Operation

The NCP12600 works as a classical fixed-switching frequency controller and can operate in CCM and DCM. When the load current is reducing, the converter eventually enters DCM. At this moment, NCP12600 implements a proprietary multimode engine which locks in the drain-source valley to improve efficiency. The frequency is now fixed but the peak current is free to move to maintain V_{out} in regulation. An internal refresh clock will start a new acquisition and valley jump occurs but at a controlled pace. This operation differs from other controllers in which the selected valley changes on the fly, resulting in a spectrally-distributed perturbation. This uncontrolled perturbation can possibly mechanically excite the transformer and generate acoustic noise. Here, because the refresh frequency is constant, it is less likely to excite the transformer across a variety of frequencies and acoustic noise is eliminated in this mode. In case a transient load occurs, the controller naturally returns to its normal operating mode until the feedback stabilizes again.



Jump from 3-2-3 valleys

$$V_{in} = 142 \text{ V}, I_{out} = 0.9 \text{ A}$$

Figure 34. The multimode engine paces the valley jump event at a controlled rate

Over Power and Over Voltage Protection

Over Power Protection (OPP) is a known means to limit the output power excursion at high mains. Several elements such as propagation delays and operating mode explain why a converter operated at high line delivers more power than at low line. NCP12600 implements a proprietary technique that senses the bulk input voltage via a resistive network connected to the auxiliary winding. However, as the pin used for OPP (pin 3) also combines other functions such as demagnetization detection and OVP, a specific network has to be designed as shown in Figure 35.

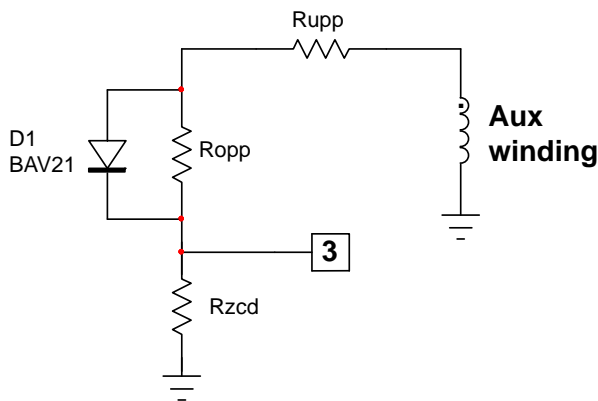


Figure 35. Over Power Protection is provided via the bulk voltage image present on Brown-Out pin

During t_{off} , the auxiliary winding jumps to the reflected output voltage scaled by the secondary-to-auxiliary transformer turns ratio. Diode D_1 is conducting and the network R_{upp}/R_{zcd} sets the OVP voltage. When the power MOSFET turns on, the auxiliary voltage jumps to a negative voltage representative of the input voltage. That negative voltage will be internally subtracted from the peak current setpoint. An internal 60-mV offset prevents compensation from taking place at low line.

The positive and negative auxiliary voltages depend on the transformer turns ratios. We can define them as follows:

$N_p:N_s = N_{pow}$, the primary to power winding turns ratio

$N_p:N_a = N_{aux}$, the primary to auxiliary winding turns ratio

During the off-time, the auxiliary winding jumps to the following plateau voltage:

$$V_{aux} = (V_{out} + V_{f1}) \frac{N_{aux}}{N_{pow}} \quad (\text{eq. 6})$$

in which V_{f1} is the power diode drop at nominal power. That voltage appears on pin 3 affected by the resistive divider R_{upp}/R_{zcd} and D_1 's forward drop V_{f2} :

$$V_{plat} = (V_{aux} + V_{f2}) \frac{R_{zcd}}{R_{zcd} + R_{upp}} \quad (\text{eq. 7})$$

During the on-time, D_1 is blocked and R_{opp} now appears in series with R_{upp} . The voltage on pin 3 is defined as

$$V_{pin3} = \frac{R_{zcd}}{R_{zcd} + R_{upp} + R_{opp}} N_{aux} V_{in} \quad (\text{eq. 8})$$

in which V_{in} is the bulk dc voltage. That voltage is the negative OPP voltage we need for our compensation. As pin3 internally includes a 60-mV offset, the negative voltage present on pin3 brings a final sense voltage reduction of

$$V_{sense} = 700 \text{ mV} + V_{pin3} + 60 \text{ m} \quad (\text{eq. 9})$$

Assume $V_{pin3} = -150 \text{ mV}$ during t_{on} , thus the effective sense reduction is

$$V_{sense} = 700 \text{ mV} - 150 \text{ m} + 60 \text{ m} = 610 \text{ mV} \quad (\text{eq. 10})$$

The peak current reduction is thus 12.8%. Combining the above equations lets us calculate the values for R_{upp} and R_{opp} based on design requirements:

$$R_{opp} = \frac{R_{zcd} \left(V_{f2} - \frac{N_{aux}(V_{f1} + V_{OVP})}{N_{pow}} \right)}{V_{OVP1}} - \frac{N_{aux} R_{zcd} V_{inHL}}{V_{opp}} \quad (\text{eq. 11})$$

$$R_{upp} = \frac{R_{zcd} \left(\frac{N_{aux}(V_{f1} + V_{OVP})}{N_{pow}} - V_{f2} \right)}{V_{OVP1}} - R_{zcd} \quad (\text{eq. 12})$$

In these expressions, we have:

R_{zcd} is the pull-down resistor arbitrarily selected. 1.8 k Ω could be a value to start with (we recommend to select a resistance below 2 k Ω for the best linearity in the OPP compensation)

V_{OVP} is the output voltage at which you want the plateau to reach the threshold voltage V_{OVP1} (3.15 V typical)

V_{inHL} is the high-line dc voltage measured across the input bulk capacitor

Assume the following data:

$V_{out} = 19 \text{ V}$, $N_{pow} = 0.250$, $N_{aux} = 0.184$, $V_{f1} = 0.8 \text{ V}$, $V_{f2} = 0.65 \text{ V}$, $V_{inHL} = 375 \text{ V}$, $R_{zcd} = 1.8 \text{ k}\Omega$

We want an OPP reduction of 12% and an output OVP set to 25 V. This leads to the following resistor values: $R_{upp} = 9.2 \text{ k}\Omega$ and $R_{opp} = 851 \text{ k}\Omega$.

Pin3 is also used for demagnetization detection. A small capacitance can be added in parallel with R_{zcd} to introduce a delay and to exactly turn-on in the drain-source valley. Experiments show that capacitances up to 150 pF provide adequate results. Please make sure the negative value during the on-time is not affected by too large a capacitance.

Pin3 protects the converter against short circuit to ground. Should you do this during safety tests, the part simply interprets the shortening to ground as an output short circuit and stops pulsing quickly. Please note that an Excel[®] spreadsheet is available from our product website and automates the calculation of the above resistances.

Slope Compensation

The NCP12600 includes an internal slope compensation signal. This is the buffered oscillator clock delivered during the on-time only. Its amplitude is around 4.2 V at the maximum duty ratio. Slope compensation is a known means used to eliminate sub-harmonic oscillations in CCM-operated current-mode converters. These oscillations take place at half the switching frequency and occur only during CCM with a duty ratio greater than 50%. To lower the current loop gain, one usually injects between 50 and 100% of the inductor downslope. Figure 36 depicts how internally the ramp is generated. Please note that the ramp signal will be disconnected from the CS pin, during the off time.

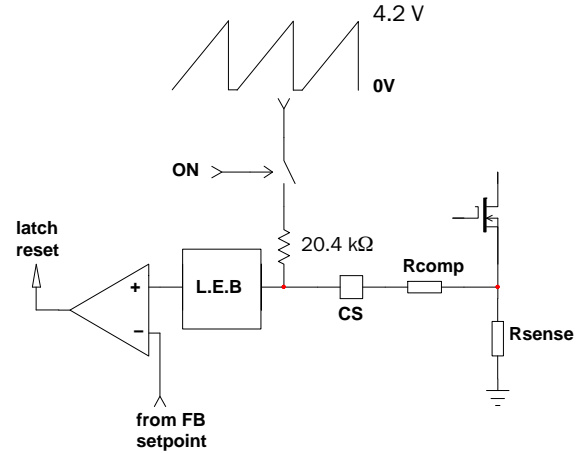


Figure 36. inserting a resistor in series with the current sense information brings ramp compensation and stabilizes the converter in CCM operation

NCP12600 oscillator ramp features a 4.2 V swing. If the clock operates at a 65-kHz frequency, then the available oscillator slope corresponds to:

$$S_{ramp} = \frac{V_{ramp,peak} D_{max}}{T_{sw}} = \frac{4.2 \cdot 0.8}{15.4 \mu} = 341 \text{ kV/s or } 341 \text{ mV}/\mu\text{s} \quad (\text{eq. 13})$$

In our flyback design, assume a primary inductance L_p of 550 μH . The converter delivers 19 V with a $N_p:N_s$ ratio of 1:0.25. The off-time primary current slope S_p is thus given by:

$$S_p = \frac{(V_{out} + V_{f1}) \frac{N_s}{N_p}}{L_p} = \frac{(19 + 0.8) \times 4}{550 \mu} = 144 \text{ kA/s} \quad (\text{eq. 14})$$

Considering a sense resistor of 330 m Ω , the above current ramp turns into a voltage ramp of the following amplitude:

$$S_{sense} = S_p R_{sense} = 144 \text{ k} \times 0.33 \approx 47 \text{ kV/s or } 47 \text{ mV}/\mu\text{s} \quad (\text{eq. 15})$$

If we select 50% of the downslope as the required amount of compensation, then we shall inject a ramp whose slope is

NCP12600

23 mV/μs. Our internal compensation being of 341 mV/μs, the divider ratio (*divratio*) between R_{comp} and the internal 20.4-kΩ resistor is:

$$\text{divratio} = \frac{23 \text{ m}}{341 \text{ m}} \approx 0.067 \quad (\text{eq. 16})$$

The series compensation resistor value is thus:

$$R_{comp} = R_{ramp} \text{divratio} = 20.4 \text{ k} \times 0.067 \approx 1.4 \text{ k}\Omega \quad (\text{eq. 17})$$

A resistor of the above value will then be inserted from the sense resistor to the current sense pin. We recommend adding a small capacitor of 100 pF, from the current sense pin to the controller ground for an improved immunity to the noise. Please make sure both components are located very close to the controller.

Feedback

The feedback is done by bringing the FB pin down with an optocoupler as shown in Figure 37. To maintain a low consumption current, the resistive network on the FB pin is higher than in other controllers. As a result, the optocoupler pole may be located at a lower position. Popular optocouplers like PC817 or SFH615 exhibit poles in the 3–4 kHz region. For that reason, a simple 100-pF capacitor connected between the circuit FB and GND pins (located close to the IC) will ensure local decoupling without interfering with crossover selection. In the secondary side, the figure shows a typical application for a 19.5-V output. This is a type 2 configuration and a single 0.1-μF capacitor will do the job typically for a fast and non-ringing transient response.

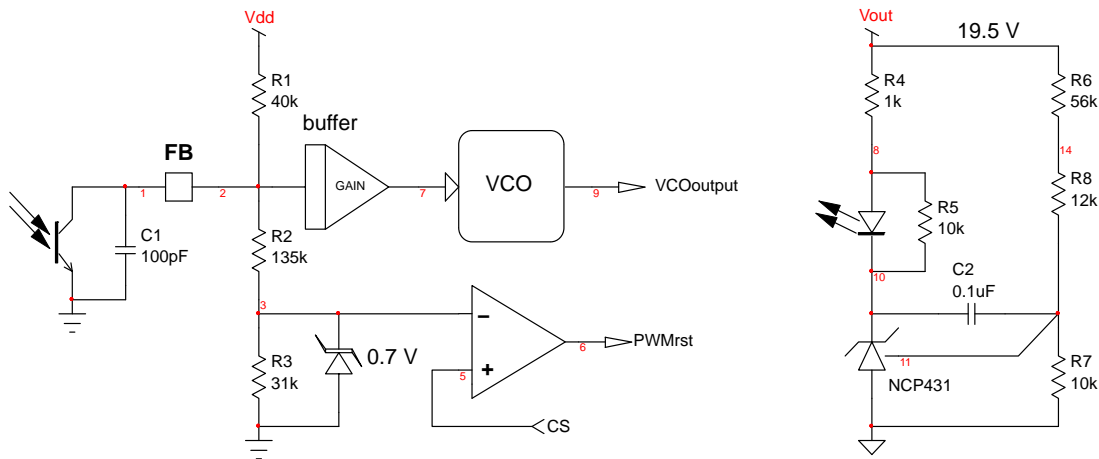


Figure 37. The optocoupler brings the FB pin down as the NCP431 injects more current into the LED

The NCP12600 is a multi-mode controller meaning that several operating modes are possible:

1. Continuous conduction mode (CCM) is available as with any PWM controller. Usually, CCM is entered at heavy load and low line.
2. As output power reduces, the converter leaves CCM and enters discontinuous conduction mode (DCM). The controller detects this mode and locks in the next available valley. The switching frequency is no longer fixed and is dictated by the valley jumps. The feedback voltage can be between its maximum value and 2.4 V in this quasi-resonant mode. Discrete frequency jumps occur but are controlled by NCP12600 internal logic.
3. If the load current continues to decrease, the feedback passes below the 2.4-V threshold and frequency foldback begins. The frequency is gradually reduced from 65 kHz (or 100 kHz) to

25 kHz. This low-frequency value is reached when V_{FB} reaches 1.9 V. When the voltage-controlled oscillator (VCO) operates, the controller also locks in the valley to ensure the best efficiency. Valley jumping is also likely to occur here but the controller sets the pace at which they occur. Of course, nothing prevents from finding a stable operating point between two hesitations, this is normal.

4. The load current is very small and the feedback voltage is below 1.9 V. Frequency is fixed to 25 kHz and classical peak current mode control operates. When the feedback voltage touches 1 V, classical or Quiet skip cycle takes place for the best standby power performance. See below for detailed operations.

The curve in Figure 38 describes the various operating stages as feedback varies.

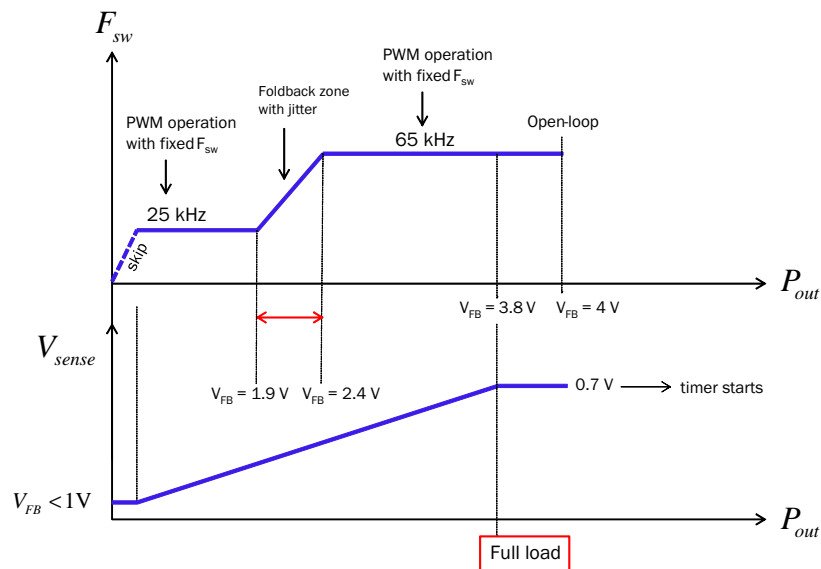


Figure 38. The frequency is folded back as output power demands reduces

Dual OCP – Option

Some applications require the possibility to deliver a peak power during a certain duration while the rest of the time, the average power is low. The converter is thus thermally sized to cope with a moderate average power ($V_{CS} < 0.5\text{ V}$) while allowing short-duration output power peaks when V_{CS} touches the 0.7-V limit. The NCP12600 can be configured in a so-called dual-OCP mode where a second level is inserted in the current sense circuitry. When the voltage on

the CS pin crosses this first 0.5-V threshold, a timer of duration t_1 starts. If the power keeps increasing and pushes the peak current to the next 0.7-V sense voltage limit, the charging current of the timer is multiplied by 4 making the new timer t_2 equal to $t_1/4$. For instance, a typical timer configuration of 256 ms/64 ms lets the converter deliver power for 256 ms when V_{CS} hits 0.5 V and this time is reduced to 64 ms if it directly jumps to 0.7 V during an overload condition.

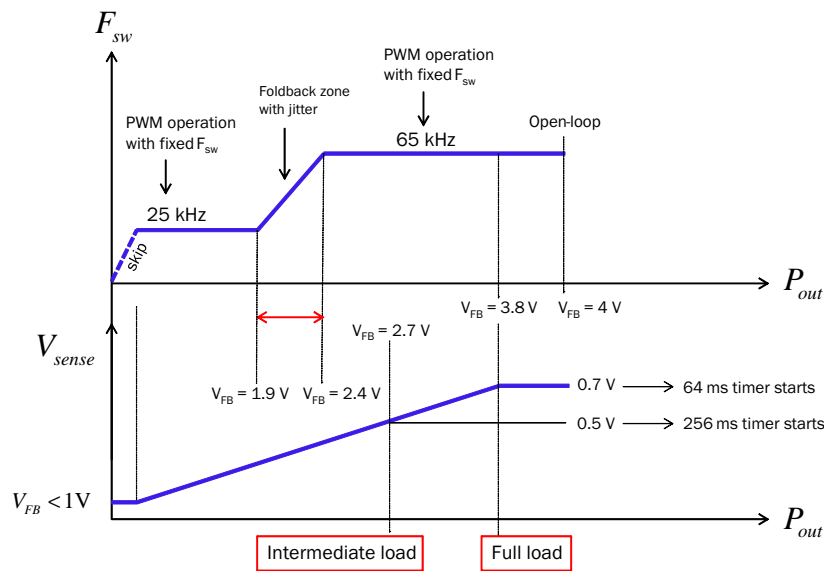


Figure 39. The dual-OCP option sets two timers depending on the amount of delivered current

Quiet-Skip – Option

To further avoid acoustic noise, the circuit prevents the burst frequency during skip mode from entering the audible range by limiting it to a maximum of 800 Hz. This is achieved via a timer t_{quiet} that is activated during Quiet-Skip. The start of the next burst cycle is prevented

until this timer has expired. As the output power decreases, the switching frequency decreases. Once it hits minimum switching frequency $f_{OSC(min)}$, the skip-in threshold is reached and burst mode is entered – switching stops as soon as the current drive pulses ends – it does not stop immediately.

Once switching stops, FB will rise. As soon as FB crosses the skip–exit threshold, drive pulses will resume but the controller remains in burst mode. At this point, a 1250 μs (typ) timer t_{quiet} is started together with a count to $n_{P,skip}$ pulses counter. This $n_{P,skip}$ pulses counter ensures the minimum number of DRV signal pulses in burst. The next time the FB voltage drops below the skip–in threshold, DRV pulses stop at the end of the current pulse as long as $n_{P,skip}$ drive pulses have been counted (if not, they do not stop until the end of the $n_{P,skip}$ –th pulse). They are not allowed to start again until the timer expires, even if the skip–exit threshold is reached first. It is important to note that the timer will not force the next cycle to begin – i.e. if the natural skip frequency is such that skip–exit is reached after the timer

expires, the drive pulses will wait for the skip–exit threshold.

This means that during no–load, there will be a minimum of $n_{P,skip}$ drive pulses, and the burst–cycle period will likely be much longer than 1250 μs. This operation helps to improve efficiency at no–load conditions.

In order to exit burst mode, the FB voltage must rise higher than $V_{skip(tran)}$ level. If this occurs before t_{quiet} expires, the drive pulses will resume immediately – i.e. the controller won’t wait for the timer to expire. Figure 40 provides an example of how Quiet–Skip works, while Figure 41 shows the immediate escape from Quiet–Skip if V_{FB} crosses the transient level $V_{skip(tran)}$.

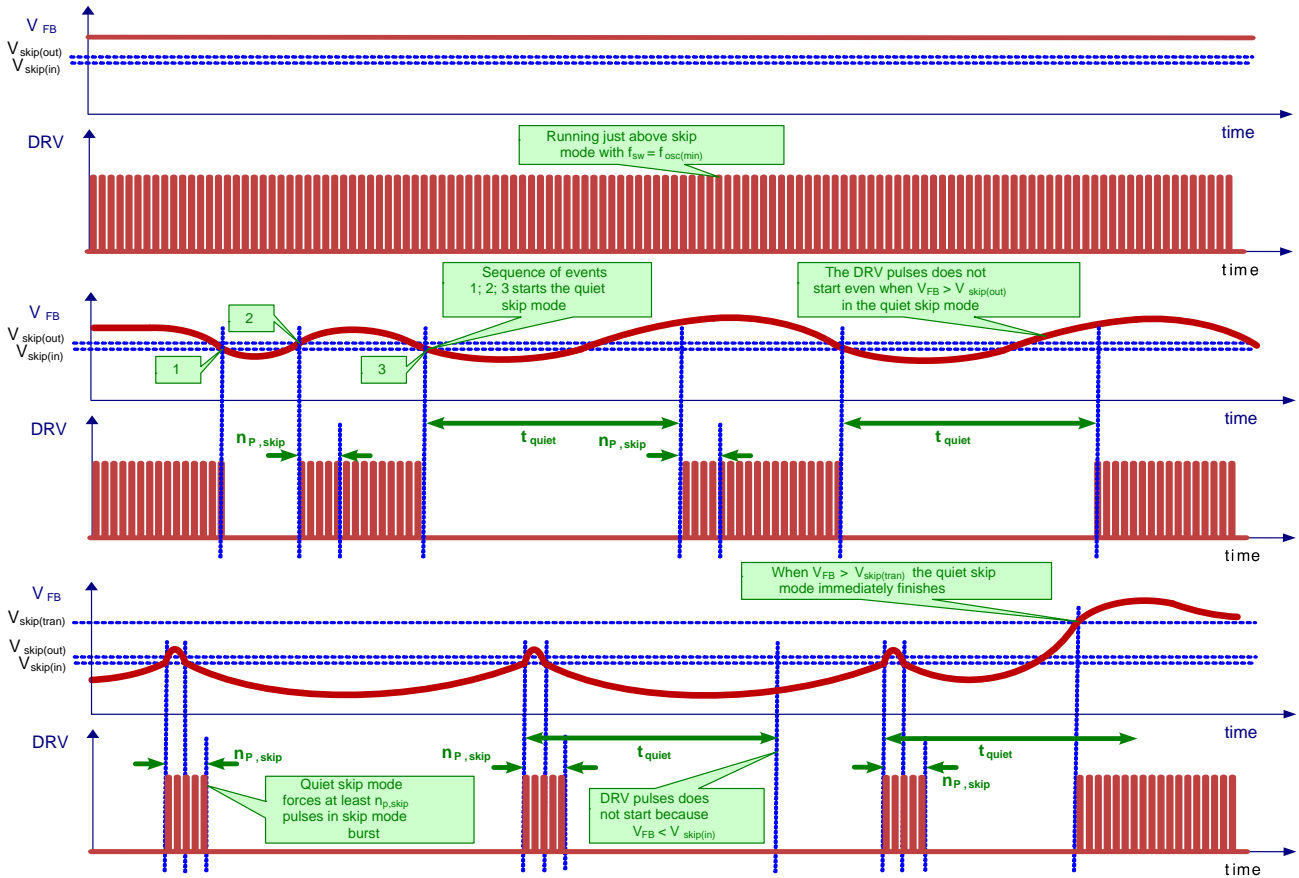


Figure 40. Leaving the Quiet–Skip Mode during Load Transient

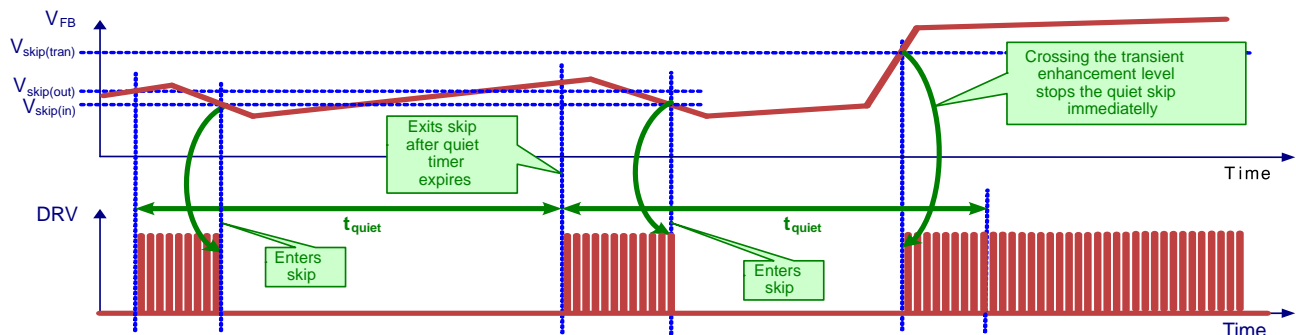


Figure 41. Quiet–skip Timing Diagram

Over Temperature Protection

It is possible to trip a second protection via the CS pin. If you connect a NTC resistor from the auxiliary winding through a fast diode and a series resistance, it is possible to latch off the part (or make it auto-recover depending on the selected option) at the desired temperature. Figure 42 shows the adopted principle. The auxiliary winding jumps to the output voltage reflected to the primary side during t_{off} and described by (6). If the loop is well designed, i.e. with sufficient loop gain in dc, the precision of this available voltage can be very good. As this voltage is available during the off-time, we can use it to build a temperature-dependent voltage on the CS pin and compare the value to an internal precise 1-V reference. According to Figure 42 labels, the voltage at the CS pin during t_{off} equals

$$V_{CS} = (V_{aux} - V_{f2}) \frac{R_{ramp}}{R_{ramp} + R_{NTC} + R_{OTP}} \quad (\text{eq. 18})$$

The ramp resistor R_{ramp} is selected depending on the operating mode at low line while R_{OTP} must be calculated as

$$R_{OTP} = \frac{R_{ramp}(V_{aux} - V_{f2})}{V_{OTP}} - R_{ramp} - R_{NTC} \quad (\text{eq. 19})$$

A very popular NTC model is the TT3 series. Assume we have selected a device exhibiting a 470-k Ω resistance at 25°C. When the temperature reaches 110°C, this resistance drops to 8.8 k Ω typically. Statistical analysis show that a good precision can be obtained as long as the ramp resistance is of moderate value. Here, experiments show that a 1-k Ω resistance is a good fit to the application and leads to the following R_{OTP} calculation:

$$R_{OTP} = \frac{1 \text{ k}(14 - 0.35)}{1} - 1 \text{ k} - 8.8 \text{ k} = 4.1 \text{ k}\Omega \quad (\text{eq. 20})$$

The NCP12600 reference voltage V_{OTP} is guaranteed at $\pm 3\%$ across the entire temperature range while all resistors are $\pm 1\%$. The auxiliary plateau is estimated to a $\pm 5\%$ precision. The V_f of the series diode can be calibrated at the trip point to refine calculations but if the auxiliary winding is of large amplitude, its contribution to the final error remains small.

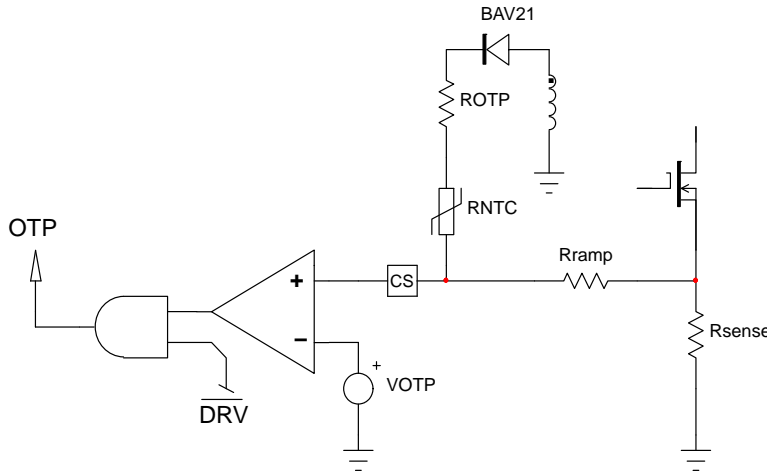


Figure 42. The NTC lifts the CS pin voltage during the off-time. If the voltage exceeds 1 V, all pulses stop

We can estimate what the final spread will be in the temperature trip point by assigning uniform distributions to each of the parameters. The resulting curve shown in Figure 43 indicates that an NTC resistance varying between 7.6 k Ω and 10 k Ω will trip the controller in OTP.

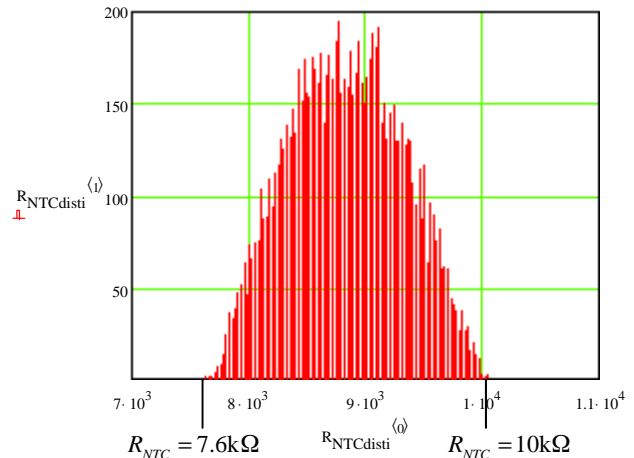


Figure 43. By assigning precision to the various components, it is possible to calculate the OTP trip point dispersion

If we now look at the corresponding temperatures the NTC resistance varying between these two limits correspond to, we obtain a range between 116 and 104°C. Centered at 110°C, it gives a theoretical precision of ±5.4°C.

It is possible to improve the precision by removing the R_{OTP} resistor. That element is inserted because the ramp resistance is imposed before the OTP calculation. Now assume that you remove R_{OTP} and calculate R_{ramp} to match the 1-V trip point when $R_{NTC} = 8.8\text{ k}\Omega$. In our example, R_{ramp} would be 680 Ω . Considering a 2-element divider versus 3 as originally selected, then the dispersion would narrow down to 8 k Ω – 9.6 k Ω , leading to a temperature trip point of 110°C ± 4.5°C. Something worth considering if the

converter requires less slope compensation (light CCM operation) or works exclusively in DCM.

Latched Mode

When the part latches off in OVP or OTP (or even in an OCP condition if the option is selected), the part immediately stops pulsing and activates an internal 1-mA current source. This source brings V_{CC} quickly to the UVLO level +100 mV and a fast hiccup around UVLO starts. That way, if the user cycles the input source, reset occurs at a quicker pace. Figure 44 shows a typical waveform inherent to this proprietary techniques.

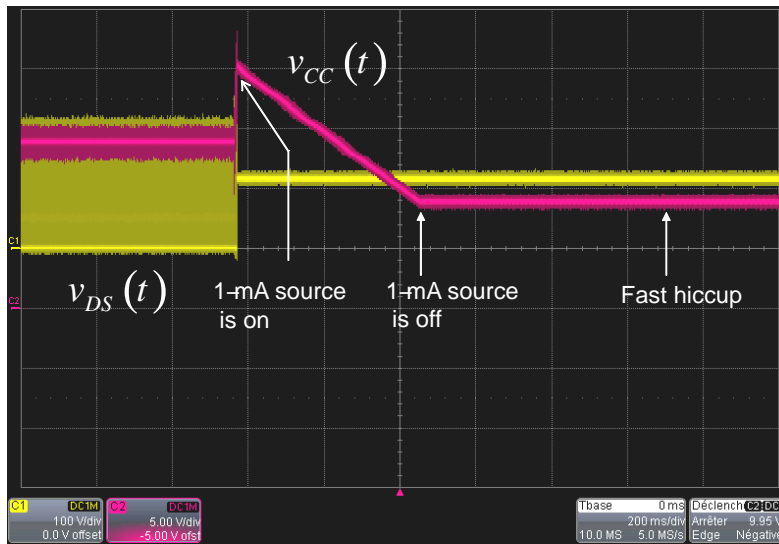


Figure 44. when the controller latches off, the V_{CC} is quickly discharged to the fast hiccup level, authorizing a fast reset

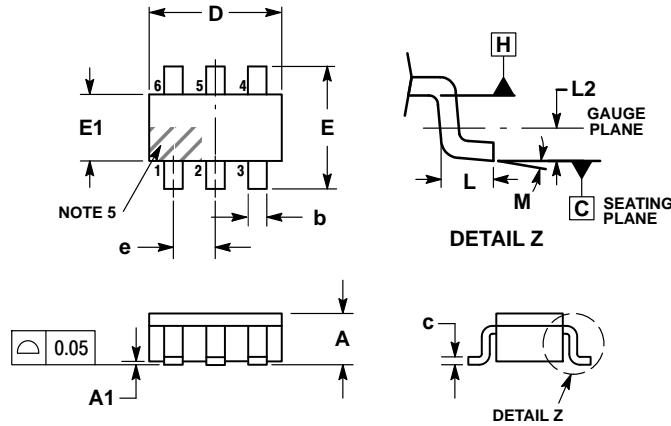
Please note that another OVP is installed on the V_{CC} pin and monitors the dc value permanently biasing the pin. If that voltage exceeds V_{OVP2} typically set at 25 V the part

latches off or auto-recovers depending on the selected option.

NCP12600

PACKAGE DIMENSIONS

TSOP-6 CASE 318G-02 ISSUE V



NOTES:

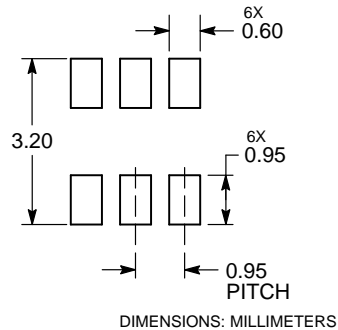
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE. DIMENSIONS D AND E1 ARE DETERMINED AT DATUM H.
5. PIN ONE INDICATOR MUST BE LOCATED IN THE INDICATED ZONE.

DIM	MILLIMETERS		
	MIN	NOM	MAX
A	0.90	1.00	1.10
A1	0.01	0.06	0.10
b	0.25	0.38	0.50
c	0.10	0.18	0.26
D	2.90	3.00	3.10
E	2.50	2.75	3.00
E1	1.30	1.50	1.70
e	0.85	0.95	1.05
L	0.20	0.40	0.60
L2	0.25 BSC		
M	0°	-	10°

STYLE 13:

- PIN 1. GATE 1
 2. SOURCE 2
 3. GATE 2
 4. DRAIN 2
 5. SOURCE 1
 6. DRAIN 1

RECOMMENDED SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERM/D.

ON Semiconductor and are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of ON Semiconductor's product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marketing.pdf. ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using ON Semiconductor products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by ON Semiconductor. "Typical" parameters which may be provided in ON Semiconductor data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. ON Semiconductor does not convey any license under its patent rights nor the rights of others. ON Semiconductor products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use ON Semiconductor products for any such unintended or unauthorized application, Buyer shall indemnify and hold ON Semiconductor and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that ON Semiconductor was negligent regarding the design or manufacture of the part. ON Semiconductor is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:

Literature Distribution Center for ON Semiconductor
 19521 E. 32nd Pkwy, Aurora, Colorado 80011 USA
 Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada
 Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada
 Email: orderlit@onsemi.com

N. American Technical Support: 800-282-9855 Toll Free
 USA/Canada
Europe, Middle East and Africa Technical Support:
 Phone: 421 33 790 2910

ON Semiconductor Website: www.onsemi.com

Order Literature: <http://www.onsemi.com/orderlit>

For additional information, please contact your local Sales Representative