AM42-0041

GaAs MMIC VSAT Power Amplifier, 0.5 W
14.0 - 14.5 GHz

Rev. V4

Features

- High Linear Gain: 28 dB Typ.
- High Saturated Output Power: +28 dBm Typ.
- High Power Added Efficiency: 22% Typ.
- 50 Ω Input/Output Broadband Matched
- Lead-Free Ceramic Bolt Down Package
- RoHS* Compliant and 260°C Reflow Compatible

Description

M/A-COM's AM42-0041 is a four-stage MMIC linear power amplifier in a lead-free, ceramic bolt down style hermetic package. The AM42-0041 employs a fully matched chip with internally decoupled Gate and Drain bias networks. The AM42-0041 is designed to be operated from a constant current Drain supply. By varying the Gate bias voltage, the saturated output power performance of this device can be tailored for various applications.

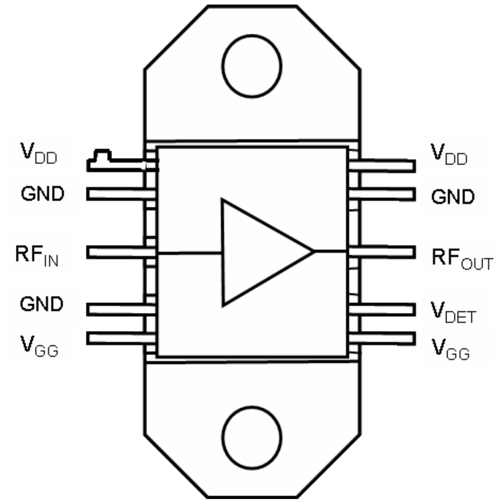
The AM42-0041 is ideally suited for use as an output stage or driver, in applications for VSAT systems. This design is fully monolithic and requires a minimum of external components.

M/A-COM's AM42-0041 is fabricated using a mature 0.5 micron GaAs MESFET process. The process features full passivation for increased performance and reliability. This product is 100% RF tested to ensure compliance to performance specifications.

Ordering Information

Part Number	Package
AM42-0041	Ceramic Bolt Down Package

Functional Schematic



Pin Configuration

Pin No.	Pin Name	Description
1	V_{DD}	Drain Supply
2	GND	DC and RF Ground
3	RF In	RF Input
4	GND	DC and RF Ground
5	V_{GG}	Gate Supply
6	V_{GG}	Gate Supply
7	V_{DET}	Detector
8	RF Out	RF Output
9	GND	DC and RF Ground
10	V_{DD}	Drain Supply

* Restrictions on Hazardous Substances, European Union Directive 2002/95/EC.

Electrical Specifications: T_A = 25°C, V_{DD} = +8 V, V_{GG} adjusted for I_{DS} = 500 mA, Z_0 = 50 Ω

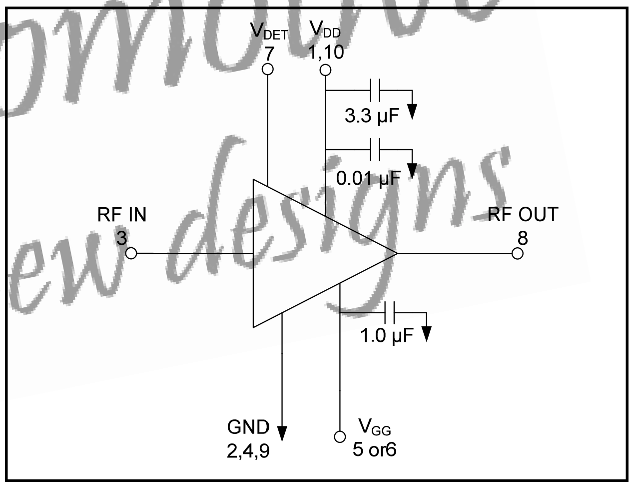
Parameter	Test Conditions	Units	Min.	Typ.	Max.
Linear Gain	P_{IN} ≤ -10 dBm	dB	27	28	—
Input VSWR	P_{IN} ≤ -10 dBm	Ratio	—	2.5:1	2.7:1
Output VSWR	P_{IN} ≤ -10 dBm	Ratio	—	2.5:1	—
Saturated Output Power	P_{IN} = +3 dBm, I_{DD} = 500 mA Typ.	dBm	27	28	29
Output Power Flatness vs. Frequency	P_{IN} = +3 dBm, I_{DD} = 500 mA Typ.	dB	—	1.0	1.5
Output Power vs. Temperature (with respect to T_A = +25°C)	P_{IN} = +3 dBm, I_{DD} = 500 mA Typ. T_A = -40°C to +70°C	dB	—	±0.4	—
Noise Figure	P_{IN} ≤ -10 dBm, I_{DD} = 500 mA Typ.	dB	—	7	—
Drain Bias Current	P_{IN} = +3 dBm	mA	400	500	600
Gate Bias Voltage	P_{IN} = +3 dBm, I_{Ds} = 500 mA Typ.	V	-2.4	-1.0	-0.4
Gate Bias Current	P_{IN} = +3 dBm, I_{Ds} = 500 mA Typ.	mA	—	5	15
Thermal Resistance	25°C Heat Sink	°C/W	—	9.5	—
Power Added Efficiency	P_{IN} = +3 dBm, I_{Ds} = 500 mA Typ.	%	—	22	—
V_{DET}	P_{IN} = +3 I_{DS} 500 mA	V	1	—	—

Absolute Maximum Ratings [1,2,3]

Parameter	Absolute Maximum
Input Power	+23 dBm
V_{DD}	+12 Volts
V_{GG}	-3 Volts
V_{DD} - V_{GG}	12 Volts
I_{ds}	1000 mA
Channel Temperature	-40°C to +85°C
Storage Temperature	-65°C to 150°C

1. Exceeding any one or combination of these limits may cause permanent damage to this device.
2. M/A-COM does not recommend sustained operation near these survivability limits.
3. Case Temperature (TC) = +85°C

Application Schematic [4,5,6,7,8]

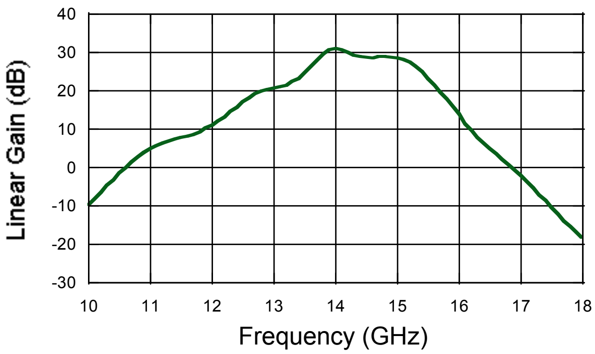


4. Nominal bias is obtained by first connecting -2.4 volts to pin 5 or pin 6 (VGG), followed by connecting +8 volts to pin 1 or pin 10 (VDD). Note sequence. Adjust VGG for a drain current of 500 mA typical.
5. RF ground and thermal interface is the flange (case bottom). Adequate heat sinking is required.
6. No DC bias voltage appears at the RF ports.
7. No DC resistance at the input and output ports is a short circuit. No voltage is allowed on these ports.
8. For optimum IP3 performance, the VDD bypass capacitors should be placed within 0.5 inches of the V_{DD} leads.

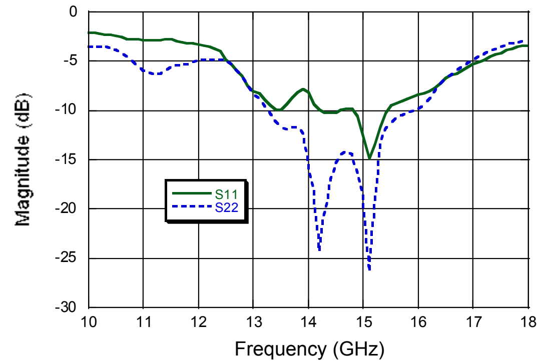
• **North America** Tel: 800.366.2266 / Fax: 978.366.2266
• **Europe** Tel: 44.1908.574.200 / Fax: 44.1908.574.300
• **Asia/Pacific** Tel: 81.44.844.8296 / Fax: 81.44.844.8298
Visit www.macomtech.com for additional data sheets and product information.

Typical Performance Curves @ +25°C

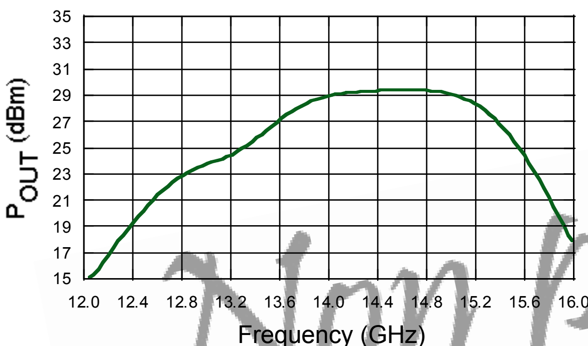
Linear Gain vs. Frequency



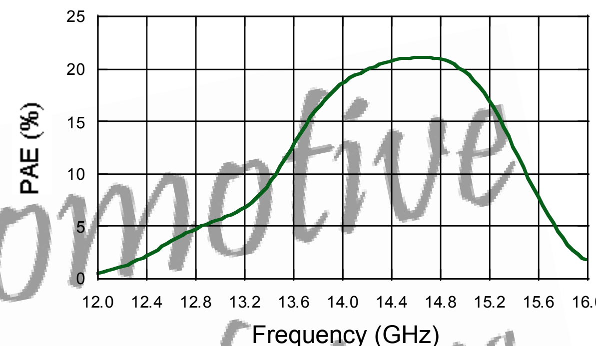
Input and Output Return Loss vs. Frequency



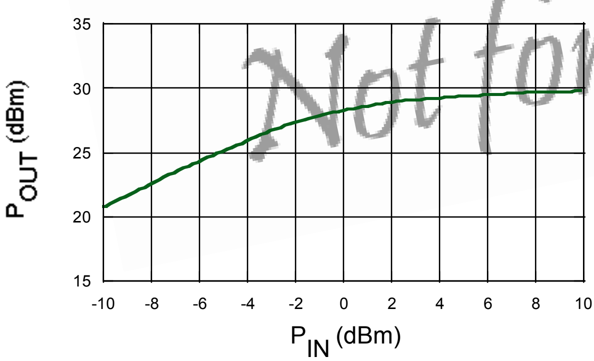
Output Power vs. Frequency @ P_{IN} = +3 dBm



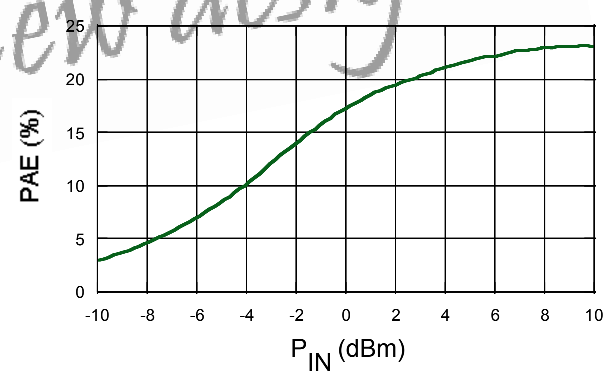
PAE vs. Frequency @ P_{IN} = +3 dBm



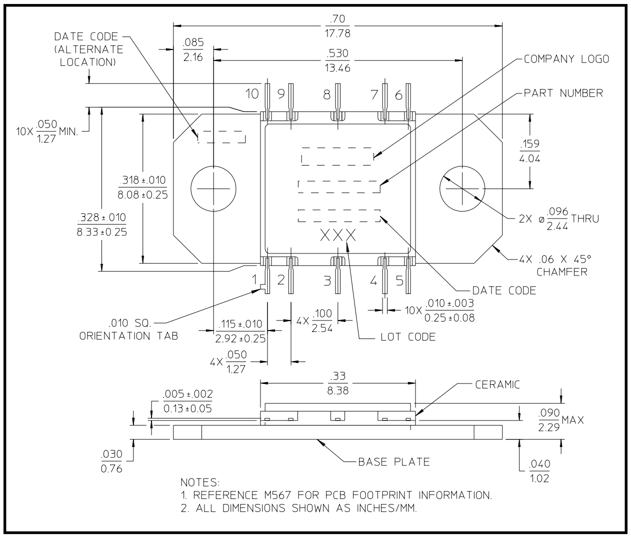
Output Power vs. Input Power @ 14.25 GHz



PAE vs. Input Power @ 14.25 GHz



Lead-Free CR-15†



† Reference Application Note M538 for lead-free solder reflow recommendations.
Meets JEDEC moisture sensitivity level 1 requirements.

Handling Procedures

Please observe the following precautions to avoid damage:

Static Sensitivity

Gallium Arsenide Integrated Circuits are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. Proper ESD control techniques should be used when handling these devices.

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