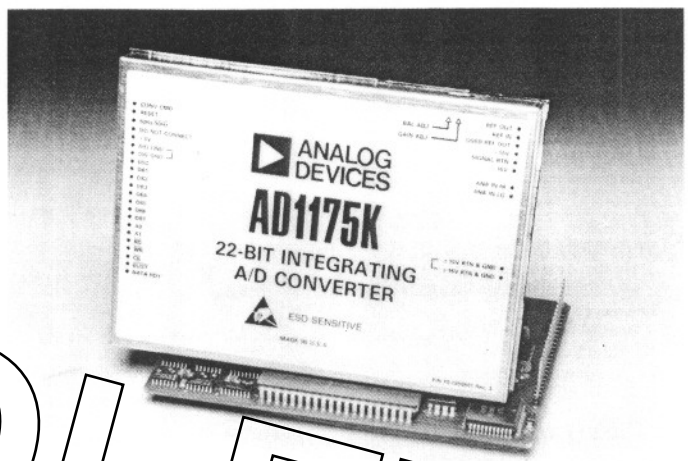
High Accuracy, 22-Bit Integrating A/D Converter

AD1175K

FEATURES
- High Resolution: 22 Bits
- Wide Dynamic Range: 133dB
- Low Nonlinearity:
  - Integral: ±0.5ppm max
  - Differential: ±0.5LSB max
- High Stability:
  - Gain: ±1ppm/°C max
  - Zero: ±0.5μV/°C max
  - INL: ±0.01ppm/°C
  - DNL: ±0.0025ppm/°C
- High Throughput Rate: 20 Conversions/Second
- Microprocessor Compatible Interface
- Compact Modular Package

APPLICATIONS
- Data Acquisition Systems
- Scientific Instruments
- Medical Instruments
- Weighing Systems
- Automatic Test Equipment
- Test and Measurement Equipment



GENERAL DESCRIPTION

The AD1175 is a very high resolution integrating A/D converter intended for applications that require the highest possible accuracy without sacrificing conversion speed, board space or modest pricing. This converter provides the performance of large benchtop or rack mount instruments in a compact, modular package.

The AD1175 utilizes an auto-zeroed, multislope, integrating principle that features 22-bit resolution with extremely low nonlinearity (Integral: ±0.5ppm max and Differential: ±0.5LSB max). Temperature stability is specified at ±0.5ppm/°C maximum for gain (exclusive of reference), ±0.5μV/°C maximum for zero, ±0.01ppm/°C for integral nonlinearity, and ±0.0025ppm/°C for differential nonlinearity.

The integration time is user selectable for maximum, line frequency noise rejection at either 60Hz or 50Hz. The conversion rate is 20 or 16 per second respectively, which is many times faster than benchtop instruments of similar performance.

The nominal full-scale input range is ±5V; however, rated accuracy is specified for inputs up to 10% over nominal, yielding a total dynamic range of greater than 4.6 million to 1. The analog input is a high impedance, high CMRR, true differential input pair. The input low operates within ±100mV of analog ground and is used to sense signal low (at the source) to minimize ground loop problems.

The output of the AD1175 consists of four addressable 8-bit bytes (STATUS and 3 DATA) presented at an 8-bit tri-stated port with standard chip select.

Several modes of operation are available and allow writing to one of several addressable locations to program gain and offset, or to initiate a conversion.

The AD1175 requires no external components and operates from ±15V dc and +5V dc power. All digital inputs and outputs are LSTTL compatible. The 3.7″ × 5.2″ × 0.53″ metal case package provides excellent electrostatic and electromagnetic shielding.

PRODUCT HIGHLIGHTS

1. The unparalleled dynamic range, accuracy, linearity and stability of the AD1175 represent a breakthrough for an A/D converter offering small size and modest cost. Only large, expensive benchtop meters offer similar performance.
2. The AD1175 converts approximately ten times as fast as digital meters with like performance.
3. The microprocessor interface of the AD1175 provides for straightforward operation, but with the features required for optimum system performance. Simple commands control offset adjust, gain adjust, external offset null and initiate conversions. The output bytes indicate input polarity, off-scale condition and a variety of additional status information.
4. The AD1175 is a complete A/D converter including a precision internal reference, clock and integration capacitor. Offset and coarse gain adjust are bus controlled, while user accessible trim potentiometers allow fine gain adjust and ±full-scale balance adjust.
5. Conversions may be made using either the offset and coarse gain settings stored in internal nonvolatile memory, or new settings made via the bus. The nonvolatile memory may be updated on command with the new settings.

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Telex: 924491 **Cables: ANALOG NORWOODMASS**

SPECIFICATIONS (typical @ +25°C, V_S = ±15V, V_D = +5V unless otherwise specified)

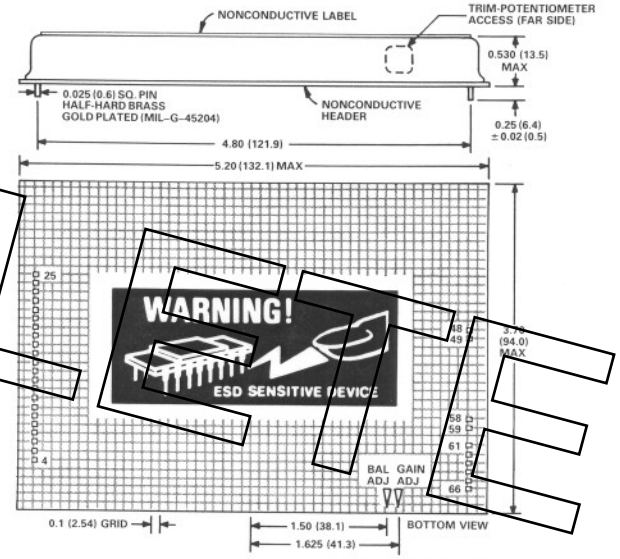
Model	AD1175K
RESOLUTION	22-bits + 10% Overrange (4,600,000 Counts) min
DYNAMIC RANGE	133dB
ACCURACY	
Integral Nonlinearity[1]	±0.5ppm F.S.R.[2], max
Differential Nonlinearity (@ 22 Bits)	±0.5LSB, max
Total Noise (Ref to Input, 95% Confidence)	5μV p-p max
STABILITY	
Gain T.C. (Excluding Reference)	±1ppm RDG/°C, max
Zero T.C.	±0.5μV/°C, max
Integral Nonlinearity T.C.	±0.01ppm F.S.R.[2]/°C
Differential Nonlinearity T.C.	±0.0025ppm F.S.R.[2]/°C
POWER SUPPLY REJECTION RATIO (±15V)	±5ppm F.S.R.[2]/V
WARMUP TIME	
Relative Accuracy (for Rated Performance)	15 Minutes
Full Rated Performance	45 Minutes
REFERENCE	
External Reference In	
For Rated Performance	+6.95V ±2%[3]
Maximum Input (Operating Only)	+9.6V
Reference Output	
Voltage	+6.95 ±2%
Output Resistance	250Ω
Temperature Coefficient	±0.4ppm/°C (±0.8ppm/°C, max)
Drift with Time[4]	
1st 15 Days Operating	±1ppm/Day
After 15 Days Operation	±25ppm/$\sqrt{1000}$hrs., max
Noise, 0.01 to 10Hz (95% Confidence)	1ppm p-p, max
User Reference Output	
Gain (Referred to Reference In)	1.000 to 1.012[5]
Current	±2mA, max
Stability: Temperature Coefficient	±1μV/°C, max
THROUGHPUT RATE[6]	
@ Integrate Time of 1/30 sec (60Hz)	20 conversions/sec
@ Integrate Time of 1/25 sec (50Hz)	16 conversions/sec
ANALOG INPUT CHARACTERISTICS	
Voltage Range[7,8]	±5V Bipolar
Max V_{IN}H (at Input Hi, Without Damage)	±12V
Max V_{IN}L (at Input Lo, Without Damage)	±3V
Max V_{IN}LR (Input Lo, for Rated Performance)	±100mV
Input Resistance (Input Hi, or Input Lo)	1000MΩ
Input Bias Current, Input Hi or Input Lo (+10°C to +50°C)	±10nA, typ; ±40nA, max
Input Bandwidth[9]	
Small Signal	2.0MHz
Large Signal	150kHz
CMRR at dc to 60Hz	80dB, min
ADJUSTMENTS	
Offset (Programmable)	
Range	±75mV
Resolution	1LSB Steps
Gain-Coarse (Programmable)[8]	
Range	<4.7V to >5.6V
Resolution	0.009% Steps
Gain-Fine Range[5,8]	±0.006% F.S.
Gain-Balance (±Full Scale) Range[5]	±0.005% F.S.
DIGITAL LEVELS	
Inputs	
Low	0.8V max
High	2.0V min
Outputs	
Low (@ 4mA)	0.45V max
High (@ 100μA)	2.4V min
POWER REQUIREMENTS	
Supply Voltages (for Rated Accuracy)	
$\pm V_S$	±15V (±0.3V each)
$+V_D$	+5V (−0.2V to +0.4V)
Supply Current Drain	
@ ±15V	
After Warm-Up	+55mA, −70mA
During Warm-Up	150mA
@ +5V	175mA
ENVIRONMENTAL	
Rated Performance	10°C to +50°C, 70% RH
Operating	0 to +70°C
Storage	−25°C to +70°C
MECHANICAL	
Size	3.7" × 5.2" × 0.53" max
Shielding	Electrostatic, 6 Sides Electromagnetic, 5 Sides
Weight	170 grams

NOTES
[1]Integral Nonlinearity is specified over the entire input span (NOMINAL FULL-SCALE + 10% Overrange). It is specified using the "End Point" definition, where the error is measured after removing the offset error and the gain errors at plus and minus full scale.
[2]FSR means Full Scale Range which = 10 volts.
[3]Single ended, ground referred.
[4]Average trend line.
[5]Adjustment is performed via user accessible 10-turn trim potentiometer.
[6]Integration Time is selectable to either 1/30 sec for 60Hz rejection, or 1/25 sec for 50Hz rejection.
[7]The Nominal Analog Input Voltage Range is ±5V, but the AD1175 may be calibrated for input voltages from ±4.7V to ±5.6V and maintain specified accuracy over the entire range, including a 10% on-scale overrange. Therefore, input voltages of up to ±6.16V will be accurately converted when calibrated for ±5.6V Nominal input.
[8]Converter section GAIN is digitally adjustable, via the data bus, in steps of 0.009% from <4.7 to >5.6V FS. A user accessible 10-turn trim potentiometer is also provided for fine GAIN adjust (±0.006% range). All units are factory calibrated for ±5V Nominal Full Scale to within ±50μV.
[9]Input Bandwidth specifications are for true integration without clipping.

Specifications subject to change without notice.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



NOTE: SEE PAGE 8 FOR RECOMMENDED SOCKET.

ASSEMBLY INSTRUCTIONS

CAUTION: This module is not an embedded assembly and is not hermetically sealed. Do not subject to a solvent or water-wash process that would allow direct contact with free liquids or vapors. Entrapment of contaminants may occur, causing performance degradation and permanent damage. Install after any clean/wash process and then only spot clean by hand.

PIN DESCRIPTIONS

PIN	SIGNAL	DESCRIPTION
4	CONV CMD	External Convert Command
5	RESET	Reset Internal Microcomputer Following Power-Up
6	60Hz/$\overline{50Hz}$	When Set Low, Integration Time is 1/25 sec When Set High, Integration Time is 1/30 sec
7	DO NOT CONNECT	Used Only for Factory Test
8	+5V	Digital Power Supply
9, 10	DIG GND	Digital Ground (Both Pins are Tied Together Internally)
11-18	DB0-DB7	Bidirectional Data Bus (LSB-MSB)
19	A0	Address, Bit Zero
20	A1	Address, Bit One
21	$\overline{RD}$	READ
22	$\overline{WR}$	WRITE
23	$\overline{CS}$	CHIP SELECT
24	$\overline{BUSY}$	BUSY, Responding to a Bus Command
25	DATA RDY	DATA READY
48, 49	±15V RTN & GND	Analog Power Ground and Case (Tied Together Internally)
58	ANA IN LO	Analog Input, Low
59	ANA IN HI	Analog Input, High
61	−15V	Negative Analog Power Supply
62	SIGNAL RTN	Signal Return (Non-Current Carrying Ground)
63	+15V	Positive Analog Power Supply
64	USER REF OUT	Buffered Output of Reference at REF IN
65	REF IN	Reference Input, Normally Connected to REF OUT
66	REF OUT	Internal +6.95V Reference Output, Unbuffered

ARCHITECTURAL OVERVIEW

The AD1175 is a complete, precision analog-to-digital converter. It consists of three major elements: a linearized, auto-zeroed integrator, a single-chip microcomputer, and a custom CMOS controller/bus interface chip. (See Figure 1 AD1175 Functional Block Diagram.)

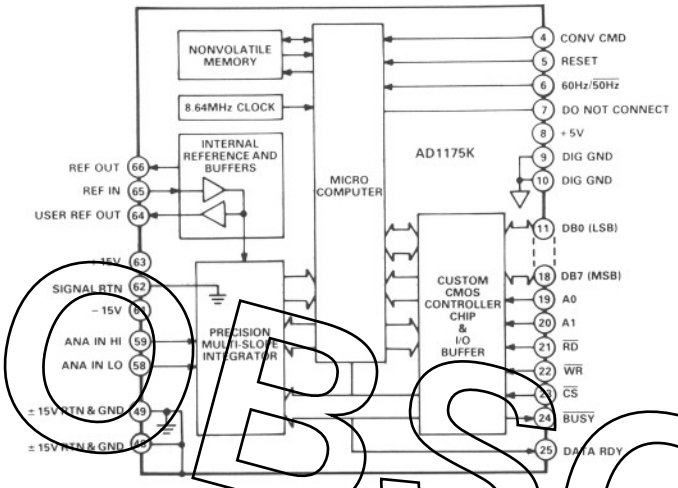


Figure 1. AD1175 Functional Block Diagram

The conversion process is similar to the classic dual-slope technique, where the input signal is integrated during a whole number of line cycles (for line noise rejection) and then a digital measurement is made of the time required for a known reference voltage to drive the integrator output back to zero (i.e., to zero charge). Since the process begins with zero charge in the integrator, and also ends there, we can express this function as follows:

$$\text{CHARGE IN} = \text{CHARGE OUT}$$

$$\text{WHERE CHARGE} = \int_0^t I\,dt = \frac{1}{R}\int_0^t V\,dt$$

$$\text{OR} \ldots \frac{1}{R_{INT}}\int_0^{T_{SIG}} V_{SIG}\,dt = \frac{1}{R_{INT}}\int_0^{T_{REF}} V_{REF}\,dt$$

$$\text{OR} \ldots \int_0^{T_{SIG}} V_{SIG}\,dt = V_{REF} \times T_{REF} \text{ (SINCE } V_{REF} = \text{CONSTANT)}$$

$$\text{OR} \ldots \frac{\int_0^{T_{SIG}} V_{SIG}\,dt}{T_{SIG}} = \text{AVG. } [V_{SIG}] = \frac{V_{REF} \times T_{REF}}{T_{SIG}}$$

$$\text{HENCE} \ldots \frac{\text{AVG. } [V_{SIG}]}{V_{REF}} = \frac{T_{REF}}{T_{SIG}} \quad \begin{cases} \text{WHERE } T_{REF} \text{ IS MEASURED AND} \\ V_{REF} \text{ \& } T_{SIG} \text{ ARE CONSTANT} \end{cases}$$

Principle of Dual-Slope Conversion

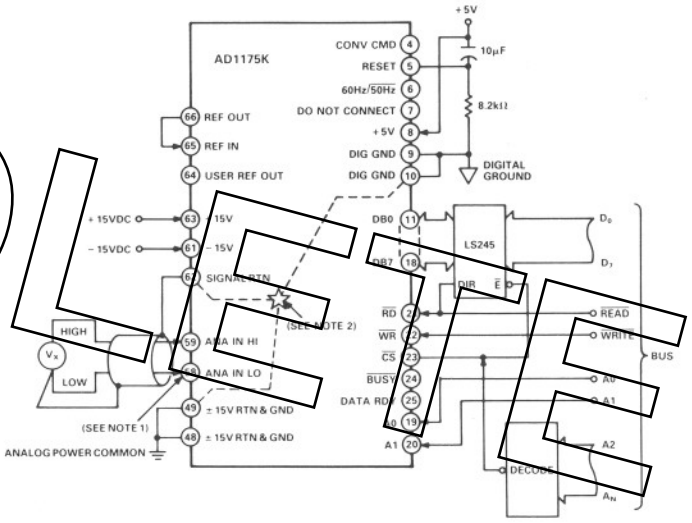
Therefore, the ratio of the signal measured (its average value) to the reference voltage, is equal to the ratio of the *measured time* (to force the integrator back to zero charge) to the signal integration time (which is held constant).

The AD1175 repeats the above sequence ten times during the first 33-1/3 milliseconds of each conversion for a 60Hz integrate selection (40 milliseconds for a 50Hz integrate selection). The 10 individual readings together with the result of a final, slow (about 6ms) vernier reference integration are summed. The numeric result is then placed in the addressable output latches and DATA is indicated as AVAILABLE. During the next ten milliseconds, the integrator is reset and AUTO-ZERO nulls out offset errors in preparation for the next conversion.

The device status is indicated by the addressable STATUS byte (busy, converting, data available, etc.). DATA READY and $\overline{\text{BUSY}}$ are also indicated by logic levels at Pins 25 and 24 respectively.

SIGNAL INPUT CONNECTIONS

The ANA IN HI and ANA IN LO pins comprise a true, high-impedance, high CMRR, differential input pair. ANA IN LO must be within ±100mV of SIGNAL RTN (Pin 62). The ANA IN LO pin is used to remote sense the source low (ground) to minimize system ground current related errors. Both *HI* AND *LO* SIGNALS MUST HAVE A BIAS CURRENT PATH BACK TO *SIGNAL RTN*. Figure 2 details the proper connections.



NOTES
1. BOTH HIGH AND LOW SIGNALS MUST HAVE A BIAS CURRENT PATH BACK TO GROUND AT THE AD1175. "ANA IN LO" SHOULD REFERENCE TO GROUND (SIGNAL RTN) AT THE SIGNAL SOURCE, VIA A MINIMUM OF RESISTANCE.
2. "DIG GND" AND "± 15V RTN & GND" ARE STAR CONNECTED WITHIN THE CONVERTER, AND INTENDED TO BE SEPARATE OUTSIDE OF THE CONVERTER. HOWEVER, IF ± 15V AND + 5V POWER SHARE A SINGLE COMMON RETURN, THEN THAT COMMON MUST BE CONNECTED TO THE "± 15V RTN & GND" PIN WHICH MUST BE CONNECTED VIA HEAVY COPPER TO THE "DIG GND" PIN. "SIGNAL RTN" (PIN 62) IS THE "NON-CURRENT CARRYING" GROUND, ONLY TO BE USED AS SHOWN AND AS GROUND REFERENCE FOR AN EXTERNALLY SUPPLIED REFERENCE SOURCE.

Figure 2. AD1175 Bus Driven Interface

Printed circuit board layout should insure that both analog inputs (Pins 58 and 59) are guarded by copper which is tied to SIGNAL RTN (Pin 62) on the front *and* back of the board.

Note that an offset error of up to one LSB per 120Ω of source impedance can occur, due to input bias current, which may approach 20nA at elevated temperatures.

REFERENCE CONNECTIONS

A very stable 6.95V ±2% internal reference is filtered and brought out to REF OUT (Pin 66) of the converter. This output should be tied to REF IN (Pin 65) to accomplish the specifications for initial absolute accuracy. REF OUT is a high impedance output and should not be loaded in any way other than by REF IN (Pin 65). A buffered version of the reference applied to REF IN, and that which is used by the converter, is available at USER REF OUT (Pin 64).

When making ratiometric measurements, where the source excitation is derived from the converter reference, use the reference signal present at USER REF OUT (Pin 64). The load applied to Pin 64 should not exceed two milliamps. If an external reference source is to be used, it should be applied to REF IN (Pin 65).

POWER SUPPLIES AND GROUNDS

The power supply pins are all well bypassed internally to their respective common or ground pins. The converter is very tolerant of dc and low frequency noise (≤100s of Hz) on any of the supplies, as evidenced in the power supply rejection specifications. High frequency noise (≥1MHz) in excess of 10mV on the ±15V supplies could, however, degrade the converter's performance.

To avoid large, digital-rate, circulating ground currents, the system's analog supply common and that of the digital supply should be kept separate and then tied together at the converter by a heavy track (to supplement that which is internal to the converter) from ±15V RTN & GND (Pins 48 and 49) to DIG GND (Pins 9 & 10).

If the logic supply and analog supply share a single common, then that common should be brought to ±15V RTN & GND (Pins 48 and 49) and then from these pins a heavy track should be run to DIG GND (Pins 9 & 10).

RESET (Pin 5; Input)

After power-up and before access may be made to the converter, a reset of the internal microcomputer must be accomplished. The RESET (Pin 5) may be driven from an external source, such as may exist in most computer-based systems, or it may be connected to a simple RC circuit which will automatically generate a reset sequence upon power-up. See Figure 2 for the recommended circuit.

When driven from an external source, RESET must be held high for a minimum of 3 microseconds, but must not terminate before the +5V logic supply and the ±15V analog supply have been stable (> +4.7V, and > ±11V) for 300 microseconds.

60Hz/$\overline{50Hz}$ (Pin 6; Input)

Pin 6 of the module selects either 33-1/3 milliseconds or 40 milliseconds for the signal integration time. This input is internally pulled up to 5V via 10kΩ and may be left open for 60Hz normal-mode rejection. The pin should be connected to Digital Ground for operation in a 50Hz line frequency environment.

CONV CMD (Pin 4; Input)

A negative logic transition on this input causes a MODCON conversion to occur (see CALIBRATION section). A minimum hold time of 1.5μs is required at both the High and the Low states, to operate properly. The $\overline{BUSY}$ output (Pin 24) will not respond, and BUSY (bit 0) of the STATUS word will *not* be indicated, but all other bits of the STATUS word will be active. DATA RDY (Pin 25) will occur per Figure 8.

This input is provided to allow externally triggered conversions which will use the temporarily programmed gain and offset values (or the start-up defaults if no changes have been made).

DATA RDY (Pin 25; Output)

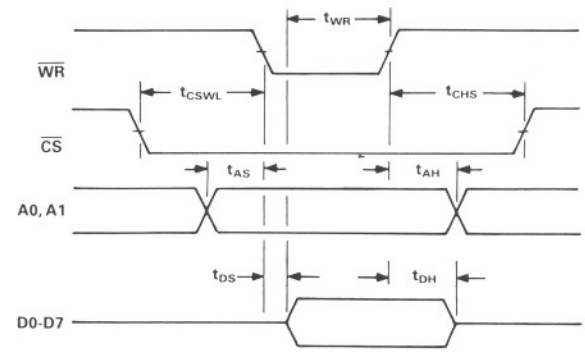
This signal will go to logic "1" when any conversion's new data has become stable in the output latches. It will remain high for the duration of the auto-zero phase (about 10 milliseconds) and go low at the end of that phase (at the end of BUSY).

$\overline{BUSY}$ (Pin 24; Output)

When a COMMAND byte is written to the microprocessor compatible port, this line is set low and remains low for the duration of the converter's response to that command. It is the opposite state of the BUSY bit within the STATUS byte.

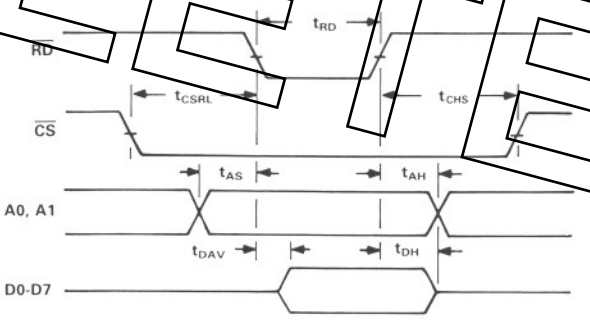
THE BUS INTERFACE

The AD1175's 8-bit microprocessor compatible interface consists of an 8-bit, latched ,tri-stated, bi-directional port and its associated control lines: Chip Select ($\overline{CS}$), READ ($\overline{RD}$), WRITE ($\overline{WR}$) and two address bits (A1 and A0). Timing requirements for the bus interface are shown in Figure 3, and the operation of the interface is shown in Figure 4.



WRITE CYCLE TIMING REQUIREMENTS

PARAMETER	DESCRIPTION	MIN	MAX	UNITS
t_{WR}	$\overline{WR}$ Pulse Width	0.1	20	μs
t_{CSWL}	Chip Select to $\overline{WR}$ Low	0		ns
t_{CHS}	Chip Select Hold Time	0		ns
t_{AS}	Address Setup time	10		ns
t_{AH}	Address Hold Time	0		ns
t_{DS}	Data Setup Time	$-\infty$	5	μs
t_{DH}	Data Hold Time	20		ns



READ CYCLE TIMING REQUIREMENTS

PARAMETER	DESCRIPTION	MIN	MAX	UNITS
t_{RD}	$\overline{RD}$ Pulse Width	150		ns
t_{CSRL}	Chip Select to $\overline{RD}$ Low	0		ns
t_{CHS}	Chip Select Hold Time	0		ns
t_{AS}	Address Setup Time	10		ns
t_{AH}	Address Hold Time	0		ns
t_{DAV}	Data Valid Time		100	ns
t_{DH}	Data Hold Time		80	ns

Figure 3. Interface Timing Requirements

	$\overline{CS}$	$\overline{RD}$	$\overline{WR}$	A1	A0	FUNCTION
READ	L	L	H	H	H	High CONV Data Byte READ
	L	L	H	H	L	Mid CONV Data Byte READ
	L	L	H	L	H	Low CONV Data Byte READ
	L	L	H	L	L	STATUS READ
WRITE	L	H	L	H	H	Unused
	L	H	L	H	L	Unused
	L	H	L	L	H	PARAMETER WRITE
	L	H	L	L	L	COMMAND WRITE
	X	H	H	X	X	DEVICE NOT SELECTED
	H	X	X	X	X	

NOTE THAT X = DON'T CARE

Figure 4. Bus Control Functions

	BIT # MSB 23	22	21	20	19	18	17	16	15	14	13		5	4	3	2	1	LSB 0	HEX
POS. OVERLOAD	1	1	1	1	1	1	1	1	1	1	1		1	1	1	1	1	1	FF,FF,FF
+1.25 × FULL SCALE	0	1	1	0	1	0	0	0	0	0	0		0	0	0	0	0	0	68,00,00
+FULL SCALE	0	1	1	0	0	0	0	0	0	0	0		0	0	0	0	0	0	60,00,00
+1/2 SCALE	0	1	0	1	0	0	0	0	0	0	0		0	0	0	0	0	0	50,00,00
ZERO	0	1	0	0	0	0	0	0	0	0	0		0	0	0	0	0	0	40,00,00
−1/2 SCALE	0	0	1	1	0	0	0	0	0	0	0		0	0	0	0	0	0	30,00,00
−FULL SCALE	0	0	1	0	0	0	0	0	0	0	0		0	0	0	0	0	0	20,00,00
−1.25 × FULL SCALE	0	0	0	1	1	0	0	0	0	0	0		0	0	0	0	0	0	18,00,00
NEG. OVERLOAD	1	1	1	1	1	1	1	1	1	1	1		1	1	1	1	1	1	FF,FF,FF

Figure 5. Data Format

OUTPUT DATA FORMAT

The result of a conversion is made available in three 8-bit bytes (addressed as shown in Figure 4). The numeric result is presented as an offset binary number, where the offset value is equal to 2e22 (40,00,00 Hex), i.e., zero volts input yields this numerical output. Therefore the nominal plus and minus full scale are 2e22 ±2e21, or 60,00,00 Hex and 20,00,00 Hex respectively. For inputs greater than approximately 1.3× nominal full scale, the converter will indicate an overload error (Bit 5 of the STATUS byte) and will also flag the occurrence by forcing all "1"s in the conversion result, i.e., FF,FF,FF Hex. Bit 23 (MSB) cannot be a "1" for any legitimate conversion result, so that bit is used to flag an overload. The data format is depicted in Figure 5.

COMMAND BYTE

The COMMAND BYTE allows eight different instructions to be given. Five of these will require that a parameter be loaded into the PARAMETER* register prior to writing the command register. The commands are written at address 00 (ADDRESS lines A1 and A0, Pins 20 and 19 respectively) while a parameter is written to address 01. See Figure 4 for Bus Control Functions. Figure 8 details command timing requirements.

The commands are described below, preceded by an opcode name and the digital code (in hex). Figure 6 summarizes each command and its execution time.

DEFCON [00]
DEFault CONversion initiates a conversion, using the gain and offset values which are stored in the nonvolatile memory (power-up defaults).

MODCON [01]
MODified CONversion initiates a conversion using the gain and offset values which have been modified (since power-up) as in commands 02 through 07 below.

NEWOS [02]
NEW OffSet subtracts the result of the last conversion from all subsequent MODCON conversions, i.e., *acquire a new system offset*. The maximum range of this offset is 65,536 codes (= ±75mV). Attempts to acquire an offset outside of this range will be ignored and BIT 5 and BIT 6 (Overload and command byte ERRor) will be set in the STATUS byte.

INCROS [03]
INCRease OffSet alters the offset (in LSBs) used by MODCON in the *positive* direction by a number between zero and 255 (decimal), which has already been written to PARAMETER*.

*The PARAMETER register retains the last word written to it. Any subsequent commands will repeatedly use that PARAMETER until it is updated.

This may be performed repeatedly until a maximum offset of +75mV has been reached, as indicated by an Overload/BIT5 response in the STATUS byte.

DECROS [04]
DECRease OffSet alters the offset (in LSBs) used by MODCON in the negative direction by a number between zero and 255 (decimal), which has already been written to PARAMETER*. This may be performed repeatedly until a maximum offset of −75mV has been reached, as indicated by an Overload/BIT 5 response in the STATUS byte.

INCGAN [05]
INCrease GAiN by $N \times 0.01\%$, where N (a decimal number between 0 and 255) has already been written to PARAMETER*. This may be performed repeatedly until a maximum gain (<4.7V full scale) has been reached, as indicated by an Overload/BIT 5 response in the STATUS byte. Further INCGAN commands will have no other effect.

DECGAN [06]
DECrease GAiN by $N \times 0.01\%$, where N (a decimal number between 0 and 255) has already been written to PARAMETER*. This may be performed repeatedly until a minimum gain (>5.6V full scale) has been reached, as indicated by an Overload/BIT 5 response in the STATUS byte. Further DECGAN commands will have no other effect.

UPDATE [07]
Takes the current modified gain and offset values and writes them to nonvolatile memory as the new start-up defaults. To enable this function, decimal 165 (A5 in hex) must first be loaded into PARAMETER* – failure to do so will result in an ERRor (BIT6) response in the STATUS byte.

Note: Codes other than 00 through 07 will do nothing, except cause an ERRor (BIT 6) response in the STATUS byte.

MNEMONIC	FUNCTIONAL DESCRIPTION	EXECUTION TIME (APPROXIMATE)
DEFCON	Initiate a Conversion Using the Power-Up Default Offset and Gain	50ms
MODCON	Initiate a Conversion Using the Modified Offset and Gain Values	50ms
NEWOS	Subtract System Offset (Last Conv. Result) from All MODCON Conversions	120µs
INCROS	Increase the Offset Used by MODCON Conversions	110µs
DECROS	Decrease the Offset Used by MODCON Conversions	110µs
INCGAN	Increase the Gain Used by MODCON Conversions	135µs
DECGAN	Decrease the Gain Used by MODCON Conversions	135µs
UPDATE	Write Most Recent Modified Offset & Gain Values to Nonvolatile Memory	48ms

Figure 6. Synopsis of Commands

THE STATUS BYTE

The STATUS byte contains eight bits of information about the current status of the AD1175. This byte may be examined by the host processor at any time. The individual bits in the status byte are assigned the following functions:

BIT 0 The BUSY bit is always set when the COMMAND BYTE is written, and cleared when the initiated routine has terminated. BUSY is also indicated at $\overline{\text{BUSY}}$ (Pin 24) of the module.

BIT 1 The CONVerting bit is set when the converter is in the active process of converting and computation. It is initiated by writing DEFCON or MODCON to the COMMAND-BYTE, or by a negative transition at CONV CMD (Pin 4).

BIT 2 The Data AVailable bit indicates that a new conversion is complete and the result is in the output latches. This bit sets to "1" at the conclusion of the converting process and remains "1" for the remainder of the minimum AUTO-ZERO time (about 10 milliseconds). It is reset to "0" at the end of BUSY.

BIT 3 The MODified bit, when set to "1", means that modified gain and offset values are being used for the current conversion; i.e., a conversion initiated by MODCON or an external signal at CONV CMD (Pin 4).

BIT 4 The VALue bit responds to COMMANDS 02 through 07 by setting to "1" at the end of BUSY, and remains until the next write to the COMMAND byte. This bit signals that a gain or offset value used by MODCON has been altered, or that the current MODCON gain and offset values have been loaded to nonvolatile memory as the new power-up defaults.

BIT 5 The Overload bit will be set following any conversion where the integrator has been exposed to an overload voltage. Following commands 03 through 06, it indicates that a parameter (gain or offset) has been incremented to its maximum or minimum possible value (note that further attempts to increment that parameter will not cause an overflow or underflow). Also, following NEWOS (02) command, this bit implies that an attempt was made, and ignored, to acquire an offset outside of the allowable range of ±75mV.

BIT 6 The ERRor bit indicates one of the following: *1.* A COMMAND-BYTE was written which was not within the allowable range of 00 to 07. *2.* An update (07) command was attempted without the KEY number (165 decimal) having first been written to PARAMETER at ADDRESS 01. *3.* A NEWOS (02) command was attempted for a value outside the permissible range of ±32,768 codes (>75mV) from zero.

BIT 7 The WaRMUP bit flags the three second time-out taken by the converter following RESET, to allow the reference and auto-zero circuits to settle. The converter will *not* convert during this time.

B7	B6	B5	B4	B3	B2	B1	B0
WRMUP	ERR	OL	VAL	MOD	DAV	CONV	BUSY

Figure 7. The Status Byte

CALIBRATION

The AD1175 is factory calibrated for plus and minus full scale (2e21) to be within ±50μV of five volts, absolute. Since the converter will operate within specifications for inputs up to ten percent over nominal full scale, those inputs between ±5.5V will be converted accurately. (See Figure 9 for typical linearity vs. input voltage.)

To correct for system offset voltage (particularly larger offset voltages – up to ±75mV) the NEWOS (03) command subtracts the result of the last conversion from all subsequent MODCON conversions. If source noise is a concern when making the offset adjustment, follow a single NEWOS command with multiple MODCON conversions, average the results and adjust offset incrementally using the INCROS (03) or DECROS (04) commands.

The INCGAN 05 and DECGAN 06 commands are the *coarse gain* increment and decrement controls respectively. The minimum gain attainable will require greater than 5.6V to achieve a full-scale output. At maximum gain, less than 4.7V will be required to yield a full-scale indication. The user accessible GAIN ADJ potentiometer is the vernier, or *fine gain* trim (10 turns, with a total adjustment range of about ±0.006% FS).

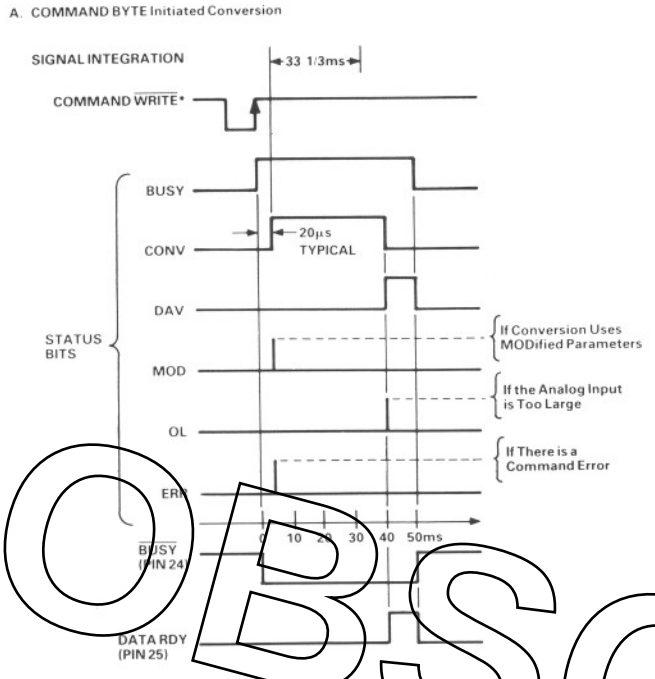
The modified offset and gain resulting from commands 02, 03, 04, 05 and 06 are used only when conversions are initiated by MODCON (command 01), or conversions triggered by a negative logic transition at the CONV CMD (Pin 4 of the converter). This pin requires a minimum hold time of 1.5μs at both the High and the Low states, in order to operate properly.

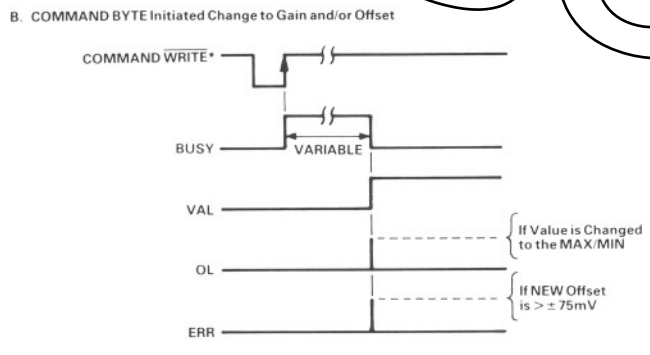
The GAIN ADJ potentiometer changes the overall gain for both positive and negative inputs. The BAL ADJ potentiometer changes the gain for positive inputs only and allows setting of plus and minus full-scale tracking to within ±1ppm.

To Calibrate the AD1175:

1. Attach a calibration source and set its output to zero volts.
2. Perform MODCON conversions and null out any observed offset (via external computation, or by executing one or more of the AD1175's offset controlling commands: INCROS, DECROS and NEWOS).
3. Set the GAIN ADJ potentiometer fully clockwise (10 turns, i.e., maximum gain).
4. Apply a negative full-scale calibration voltage (−4.7V to −5.6V).
5. Using the INCGAN or DECGAN command, coarse adjust the gain such that a subsequent MODCON conversion yields a result just larger than minus full scale. In other words, a subsequent DECGAN by 01 would just yield a result that is less than or equal to minus full scale.
6. Adjust the GAIN ADJ potentiometer to yield the precise value desired by turning counterclockwise and observing conversion results. When the correct gain is reached, rotate the potentiometer about 3 degrees in the opposite direction to remove the tension from its wiper.
7. Switch the polarity of the calibration source to positive.
8. Adjust the BAL ADJ potentiometer to yield the same gain as that achieved in Step 6 above.
9. Save the new offset value and coarse gain value, if you want them to become the power-up defaults, by performing UPDATE (Command 07).

Note: See the COMMAND BYTE section for details of command operation.





*NOTE: COMMAND WRITE Always Causes Rewrite of the Entire STATUS Byte. For Example: If the Overload Bit (OL) is Set as the Result of a Conversion, It Will Remain Set in the STATUS Byte Until the Next COMMAND WRITE.

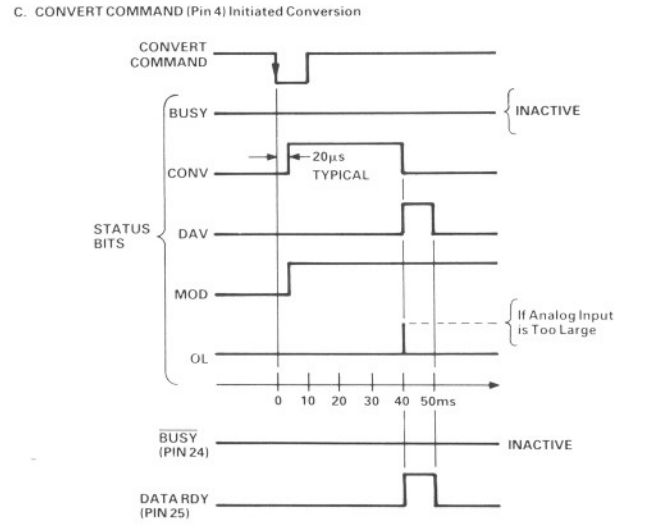
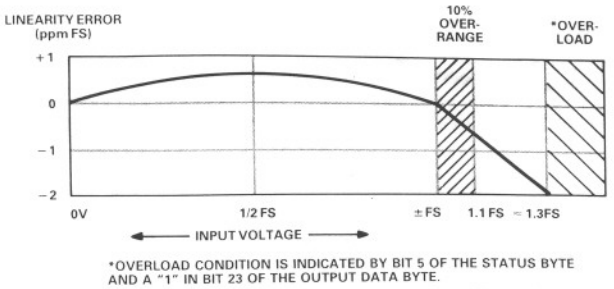


Figure 8. Command Timing Requirements



*OVERLOAD CONDITION IS INDICATED BY BIT 5 OF THE STATUS BYTE AND A "1" IN BIT 23 OF THE OUTPUT DATA BYTE.

Figure 9. Typical Linearity Transfer Function

FACTORY TESTING

Each AD1175 converter is factory calibrated via test apparatus designed and constructed by Analog Devices. The heart of the test system is a digitally programmable voltage reference capable of sub-ppm accuracy and stability. Calibration of the test system is verified daily using the highest precision instruments commercially available, e.g., FLUKE* model 720A Kelvin Varley voltage divider (accurate to within ±0.1ppm[1]) and model 732A dc secondary voltage standard (accurate to within ±1.5ppm of the international volt[1]).

IBM PC INTERFACE

Figure 10 is an example of an AD1175/IBM interface suitable for the IBM PC, XT or AT** personal computers. In this case, the AD1175 is interfaced in the I/O space; a DIP switch controls the specific location of the AD1175 within the available address space.

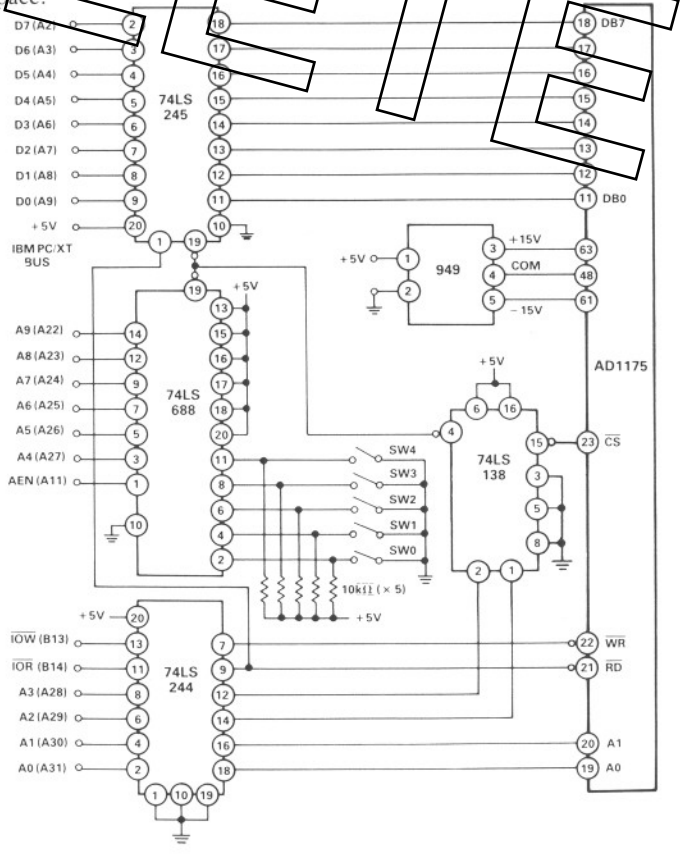


Figure 10. AD1175 to IBM PC/XT/AT Interface

*FLUKE is a registered tradedmark of John Fluke Manufacturing Company, Inc.

**IBM PC/XT/AT is a trademark of International Business Machines Corp.

[1]Traceable to the NATIONAL BUREAU OF STANDARDS.

INTERFACING TO AN 8051 MICROCONTROLLER

Figure 11 shows how the AD1175 may be interfaced to an 8051 microcontroller using a technique commonly called "byte banging", where the control lines and data bus of a device are manipulated under firmware control. This "byte banging" technique can be adapted to most microprocessors and is useful in situations where a conventional bus structure is either nonexistent or unavailable for use.[1]

The AD1175's data bus is connected to the 8051 using I/O lines P2.0 through P2.7. The address lines A0 and A1 are connected to I/O lines P1.0 and P1.1 respectively. The RD/ and WR/ lines are connected to P1.2 and P1.3. The CS/ line of the AD1175 is grounded when it is the only device connected to the 8051, but multiple AD1175s could easily be connected in the same way if each CS/ line were separately controlled.

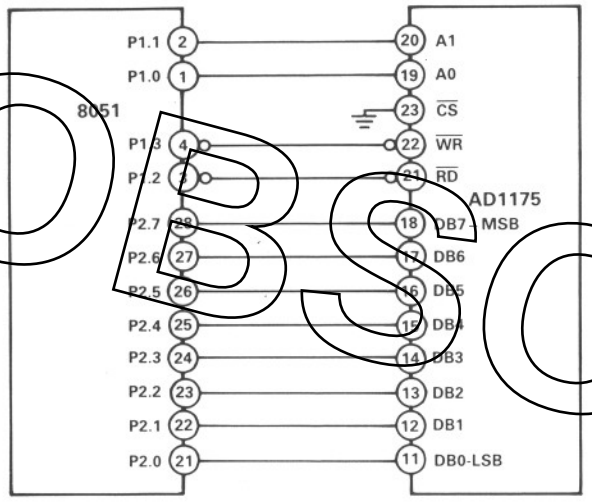


Figure 11. Simple AD1175 to 8051 Interface

To initialize the interface, first write "1"s to the port pins connected to the data bus and the RD/ and WR/ control lines. This puts the 8051 I/O lines into a lightly "pulled up" state, simulating a tri-stated condition on the bus to insure that neither RD/ nor WR/ are selected:

```
INIT:   SETB  P1.2        ;DISABLE RD/
        SETB  P1.3        ;AND WR/
                          ;
        MOV   P2, #OFFH   ;SET P2 TO ALL ONES
```

To write a command to the AD1175, first set the state of the P1.1 and P1.0 lines for the address corresponding to the byte to be written to (00 = COMMAND BYTE, 01 = PARAMETER). Set the P2 port to the command data, then strobe the WR/ line by first clearing the P1.3 line and then setting it:

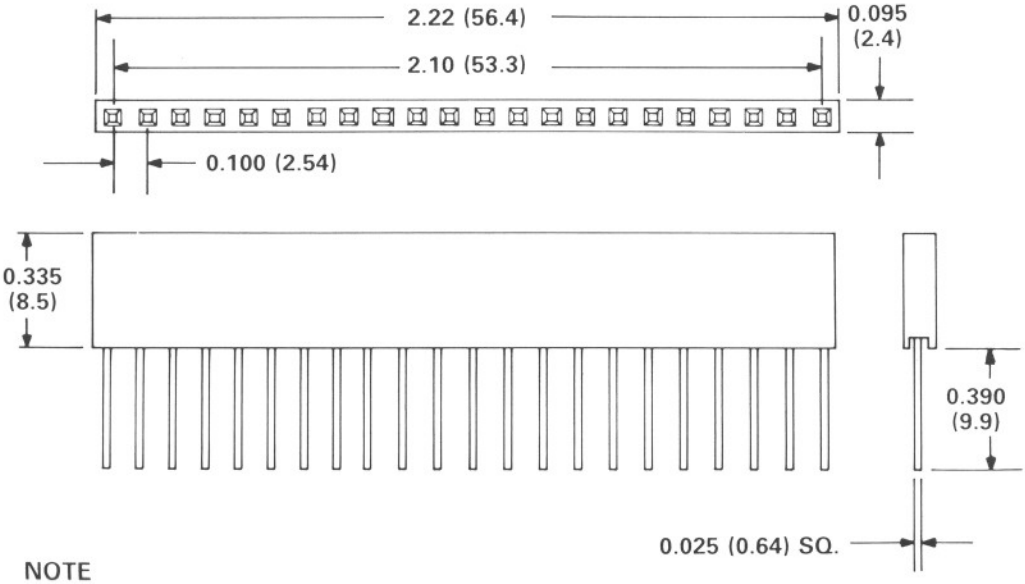
```
WRCMD:  CLR   P1.0        ;FIRST CLEAR A0 AND A1
        CLR   P1.1        ;TO POINT TO CMD BYTE
                          ;
        MOV   P2, #00     ;00 IS THE OPCODE FOR
                          ;A DEFAULT MODE
                          ; CONVERSION
                          ;
        CLR   P1.3        ;STROBE THE WR/ LINE
        SETB  P1.3        ;ONE TIME
                          ;
        MOV   P2, #OFFH   ;SET DATA BUS TO
                          ;ALL ONES
```

To read a byte from the AD1175, first set the P1.0 and P1.1 lines to point to the address of the byte desired. Bring the RD/ line low, reading the contents of P2. Return the RD/ line high:

```
RDSTAT: CLR   P1.0        ;POINT TO STATUS BYTE
        CLR   P1.1        ;
                          ;
        CLR   P1.2        ;BRING RD/ LINE LOW
        MOV   A,P2        ;READ CONTENTS OF BUS
        SETB  P1.2        ;RESTORE RD/ LINE HIGH
```

[1]Note that the 8051 microcontroller *does* contain a conventional bus structure; the "byte banging" interface shown here is presented as an example of an alternative technique.

SAMTEC Part Number SSQ-122-03-G-S (2 Each Required Per AD1175)
Available direct from the manufacturer or through distributors.



NOTE
0.025" (0.64) SQUARE SOCKET STRIP, 22-PIN POSITIONS
GOLD PLATED CONTACTS AND PINS, BODY IS MOLDED
DUPONT RYNITE PET POLYESTER.