GENERAL DESCRIPTION

The XRA1206 is an 8-bit GPIO expander with an I^2C/SMBus interface. After power-up, the XRA1206 has internal 100K ohm pull-up resistors on each I/O pin that can be individually enabled.

In addition, the GPIOs on the XRA1206 can individually be controlled and configured. As outputs, the GPIOs can be outputs that are high, low or in three-state mode. The three-state mode feature is useful for applications where the power is removed from the remote devices, but they may still be connected to the GPIO expander.

As inputs, the internal pull-up resistors can be enabled or disabled and the input polarity can be inverted. The interrupt can be programmed for different behaviors. The interrupts can be programmed to generate an interrupt on the rising edge, falling edge or on both edges. The interrupt can be cleared if the input changes back to its original state or by reading the current state of the inputs.

The XRA1206 is an enhanced version of the TCA6408. The XRA1206 is pin and software compatible with the TCA6408.

The XRA1206 is available in 16-pin QFN and 16-pin TSSOP packages.

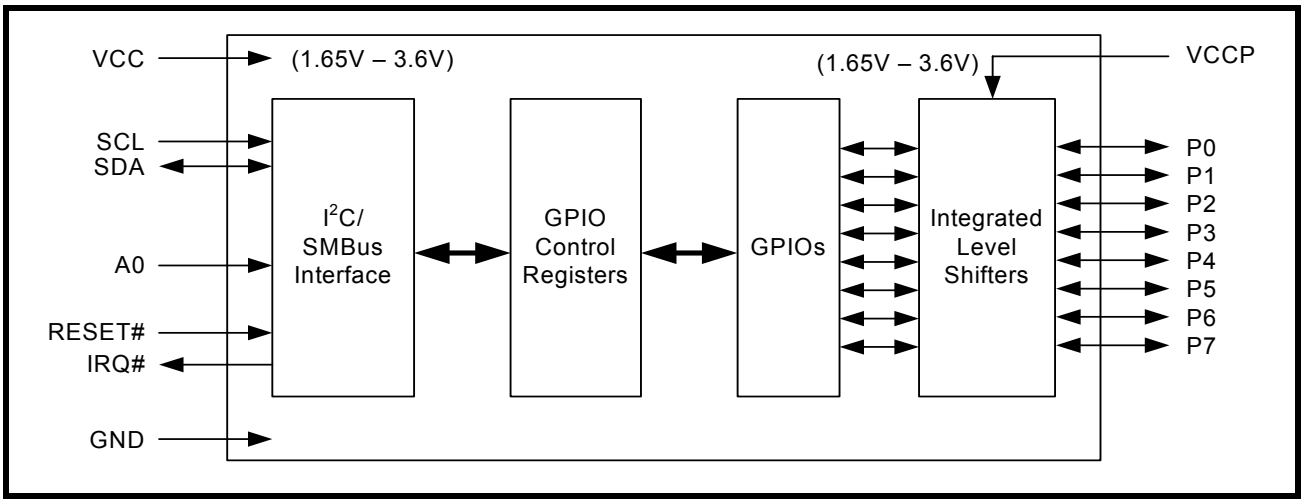
FEATURES

- 1.65V to 3.6V operating voltage
- Integrated level shifters
- 8 General Purpose I/Os (GPIOs)
- 5V tolerant inputs
- Maximum stand-by current of 1uA at +1.8V
- I^2C/SMBus bus interface
  - I^2C clock frequency up to 400kHz
  - Noise filter on SDA and SCL inputs
  - Up to 4 I^2C Slave Addresses
- Individually programmable inputs
  - Internal pull-up resistors
  - Polarity inversion
  - Individual interrupt enable
  - Rising edge and/or Falling edge interrupt
  - Input filter
- Individually programmable outputs
  - Output Level Control
  - Output Three-State Control
- Open-drain active low interrupt output
- Active-low reset input
- Pin and software compatible with TCA6408
- 3kV HBM ESD protection per JESD22-A114F
- 200mA latch-up performance per JESD78B

APPLICATIONS

- Personal Digital Assistants (PDA)
- Cellular Phones/Data Devices
- Battery-Operated Devices
- Global Positioning System (GPS)
- Bluetooth

FIGURE 1. XRA1206 BLOCK DIAGRAM

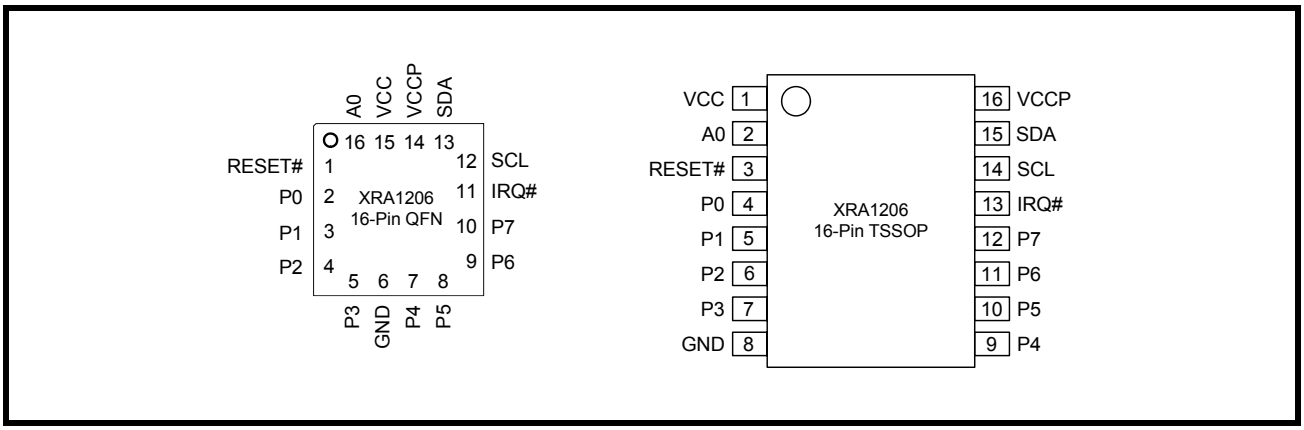


ORDERING INFORMATION

PART NUMBER	PACKAGE	NUMBER OF GPIOS	OPERATING TEMPERATURE RANGE	DEVICE STATUS
XRA1206IL16-F	QFN-16	8	-40°C to +85°C	Active
XRA1206IL16TR-F	QFN-16	8	-40°C to +85°C	Active
XRA1206IG16-F	TSSOP-16	8	-40°C to +85°C	Active
XRA1206IG16TR-F	TSSOP-16	8	-40°C to +85°C	Active

NOTE: **TR = Tape and Reel, F = Green / RoHS**

FIGURE 2. PIN OUT ASSIGNMENTS



PIN DESCRIPTIONS

Pin Description

NAME	QFN-16 PIN#	TSSOP-16 PIN#	TYPE	DESCRIPTION
I²C INTERFACE				
SDA	13	15	I/O	I²C-bus data input/output (open-drain).
SCL	12	14	I	I²C-bus serial input clock.
IRQ#	11	13	OD	Interrupt output (open-drain, active LOW).
A0	16	2	I	This pin selects the I²C slave address. See **Table 1**.
RESET#	1	3	I	Reset (active LOW) - A longer than 40 ns LOW pulse on this pin will reset the internal registers and all GPIOs will be configured as inputs.
GPIOs				
P0	2	4	I/O	General purpose I/Os P0-P7. All GPIOs are configured as inputs upon power-up or after a reset.
P1	3	5	I/O	
P2	4	6	I/O	
P3	5	7	I/O	
P4	7	9	I/O	
P5	8	10	I/O	
P6	9	11	I/O	
P7	10	12	I/O	
ANCILLARY SIGNALS				
VCCP	14	16	Pwr	1.65V to 3.6V VCC supply voltage for GPIOs.
VCC	15	1	Pwr	1.65V to 3.6V VCC supply voltage for I²C-bus interface.
GND	6	8	Pwr	Power supply common, ground.
GND	Center Pad	-	Pwr	The exposed pad at the bottom surface of the package is designed for thermal performance. Use of a center pad on the PCB is strongly recommended for thermal conductivity as well as to provide mechanical stability of the package on the PCB. The center pad is recommended to be solder masked defined with opening size less than or equal to the exposed thermal pad on the package bottom to prevent solder bridging to the outer leads of the device. Thermal vias must be connected to GND plane as the thermal pad of package is at GND potential.

Pin type: I=Input, O=Output, I/O= Input/output, OD=Output Open Drain.

1.0 FUNCTIONAL DESCRIPTIONS

1.1 I²C-bus Interface

The I²C-bus interface is compliant with the Standard-mode and Fast-mode I²C-bus specifications. The I²C-bus interface consists of two lines: serial data (SDA) and serial clock (SCL). In the Standard-mode, the serial clock and serial data can go up to 100 kbps and in the Fast-mode, the serial clock and serial data can go up to 400 kbps.

The first byte sent by an I²C-bus master contains a start bit (SDA transition from HIGH to LOW when SCL is HIGH), 7-bit slave address and whether it is a read or write transaction. The next byte is the sub-address that contains the address of the register to access. The XRA1206 responds to each write with an acknowledge (SDA driven LOW by XRA1206 for one clock cycle when SCL is HIGH). The last byte sent by an I²C-bus master contains a stop bit (SDA transition from LOW to HIGH when SCL is HIGH). See **Figures 3 - 5** below. For complete details, see the I²C-bus specifications.

FIGURE 3. I²C START AND STOP CONDITIONS

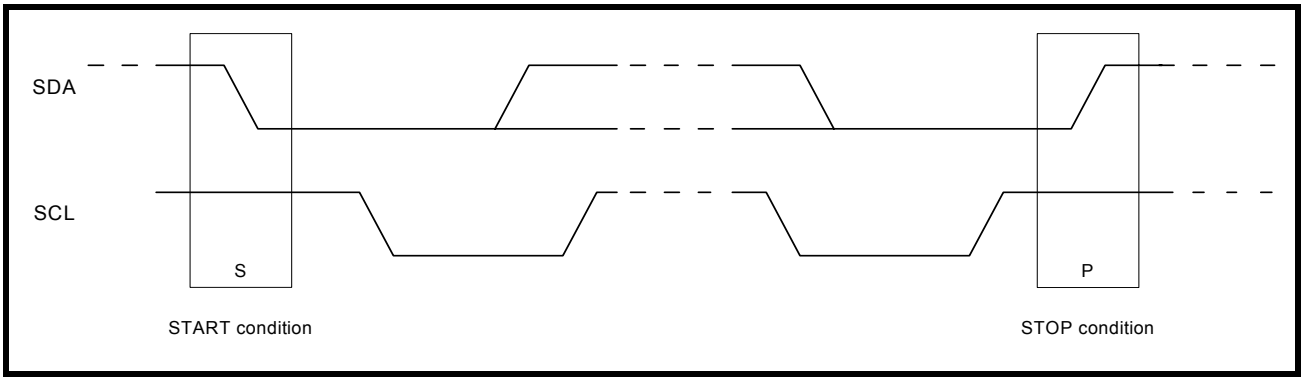


FIGURE 4. MASTER WRITES TO SLAVE

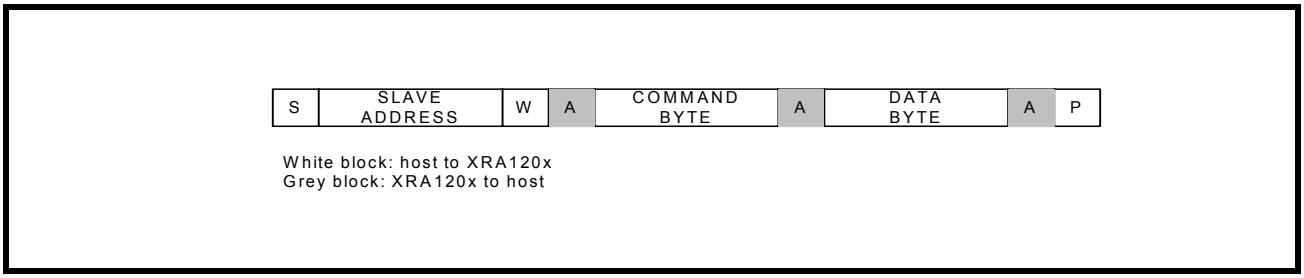
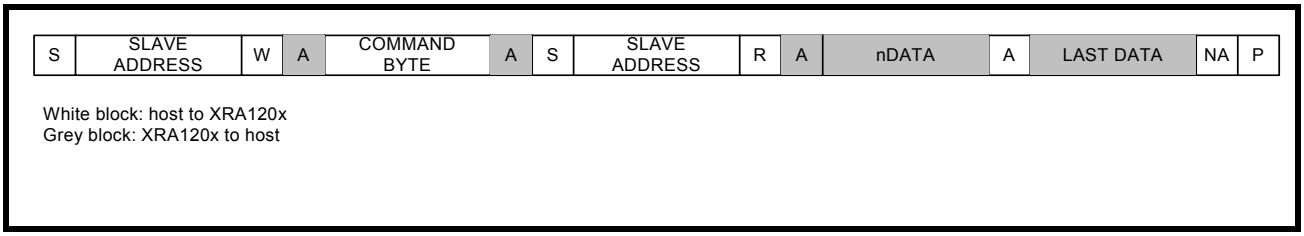


FIGURE 5. MASTER READS FROM SLAVE



1.1.1 I²C-bus Addressing

There could be many devices on the I²C-bus. To distinguish itself from the other devices on the I²C-bus, the XRA1206 has up to 4 I²C slave addresses using the A0 address line. Table 1 below shows the different addresses that can be selected.

TABLE 1: I²C ADDRESS MAP

A0	I²C ADDRESS
GND	0x40 (0100 000X)
VCC	0x42 (0100 001X)
SCL	0x50 (0101 000X)
SDA	0x52 (0101 001X)

1.1.2 I²C Read and Write

A read or write transaction is determined by bit-0 of the slave address. If bit-0 is '0', then it is a write transaction. If bit-0 is '1', then it is a read transaction.

1.1.3 I²C Command Byte

An I²C command byte is sent by the I²C master following the slave address. The command byte indicates the address offset of the register that will be accessed. Table 2 below lists the command bytes for each register.

TABLE 2: I²C COMMAND BYTE (REGISTER ADDRESS)

COMMAND BYTE	REGISTER NAME DESCRIPTION	READ/WRITE	DEFAULT VALUES
0x00	GSR - GPIO State	Read-Only	0xXX
0x01	OCR - Output Control	Read/Write	0xFF
0x02	PIR - Input Polarity Inversion	Read/Write	0x00
0x03	GCR - GPIO Configuration	Read/Write	0xFF
0x04	PUR - Input Internal Pull-up Resistor Enable/Disable	Read/Write	0x00
0x05	IER - Input Interrupt Enable	Read/Write	0x00
0x06	TSCR - Output Three-State Control	Read/Write	0x00
0x07	ISR - Input Interrupt Status	Read	0x00
0x08	REIR - Input Rising Edge Interrupt Enable	Read/Write	0x00
0x09	FEIR - Input Falling Edge Interrupt Enable	Read/Write	0x00
0x0A	IFR - Input Filter Enable/Disable	Read/Write	0xFF

1.2 Interrupts

The table below summarizes the interrupt behavior of the different register settings for the XRA1206.

TABLE 3: INTERRUPT GENERATION AND CLEARING

GCR BIT	IER BIT	REIR BIT	FEIR BIT	IFR BIT	INTERRUPT GENERATED BY:	INTERRUPT CLEARED BY:
1	0	X	X	X	No interrupts enabled (default)	N/A
1	1	0	0	0	A rising or falling edge on the input	Reading the GSR register or if the input changes back to its previous state (state of input during last read to GSR)
				1	A rising or falling edge on the input and remains in the new state for more than 1075ns	
1	1	1	0	0	A rising edge on the input	Reading the GSR register
				1	A rising edge on the input and remains high for more than 1075ns	
1	1	0	1	0	A falling edge on the input	Reading the GSR register
				1	A falling edge on the input and remains low for more than 1075ns	
1	1	1	1	0	A rising or falling edge on the input	Reading the GSR register
				1	A rising or falling edge on the input and remains in the new state for more than 1075ns	
0	x	x	x	x	No interrupts in output mode	N/A

2.0 REGISTER DESCRIPTION

2.1 GPIO State Register (GSR) - Read-Only

The status of P7 - P0 can be read via this register. A read will show the current state of these pins (or the inverted state of these pins if enabled via the PIR Register). Reading this register will clear an input interrupt (see **Table 3** for complete details). Reading this register will also return the last value written to the OCR register for any pins that are configured as outputs (ie. this is not the same as the state of the actual output pin since the output pin can be in three-state mode). A write to this register has no effect. The MSB of this register corresponds with P7 and the LSB of this register corresponds with P0.

2.2 Output Control Register (OCR) - Read/Write

When P7 - P0 are defined as outputs, they can be controlled by writing to this register. Reading this register will return the last value written to it, however, this value may not be the actual state of the output pin since these pins can be in three-state mode. The MSB of this register corresponds with P7 and the LSB of this register corresponds with P0.

2.3 Input Polarity Inversion Register (PIR) - Read/Write

When P7 - P0 are defined as inputs, this register inverts the polarity of the input value read from the Input Port Register. If the corresponding bit in this register is set to '1', the value of this bit in the GSR Register will be the inverted value of the input pin. If the corresponding bit in this register is set to '0', the value of this bit in the GSR Register will be the actual value of the input pin. The MSB of this register corresponds with P7 and the LSB of this register corresponds with P0.

2.4 GPIO Configuration Register (GCR) - Read/Write

This register configures the GPIOs as inputs or outputs. After power-up and reset, the GPIOs are inputs. Setting these bits to '0' will enable the GPIOs as outputs. Setting these bits to '1' will enable the GPIOs as inputs. The MSB of this register corresponds with P7 and the LSB of this register corresponds with P0.

2.5 Input Internal Pull-up Enable/Disable Register (PUR) - Read/Write

This register enables/disables the internal pull-up resistors for an input. After power-up and reset, the internal pull-up resistors are disabled for the XRA1206. Writing a '1' to these bits will enable the internal pull-up resistors. Writing a '0' to these bits will disable the internal pull-up resistors. The MSB of this register corresponds with P7 and the LSB of this register corresponds with P0.

2.6 Input Interrupt Enable Register (IER) - Read/Write

This register enables/disables the interrupts for an input. After power-up and reset, the interrupts are disabled. Writing a '1' to these bits will enable the interrupt for the corresponding input pins. See **Table 3** for complete details of the interrupt behavior for various register settings. No interrupts are generated for outputs when GCR bit is 0. The MSB of this register corresponds with P7 and the LSB of this register corresponds with P0.

2.7 Output Three-State Control Register (TSCR) - Read/Write

This register can enable/disable the three-state mode of an output. Writing a '1' to these bits will enable the three-state mode for the corresponding output pins. The MSB of this register corresponds with P7 and the LSB of this register corresponds with P0.

2.8 Input Interrupt Status Register (ISR) - Read-Only

This register reports the input pins that have generated an interrupt. See **Table 3** for complete details of the interrupt behavior for various register settings. The MSB of this register corresponds with P7 and the LSB of this register corresponds with P0.

2.9 Input Rising Edge Interrupt Enable Register (REIR) - Read/Write

Writing a '1' to these bits will enable the corresponding input to generate an interrupt on the rising edge. See **Table 3** for complete details of the interrupt behavior for various register settings. The MSB of this register corresponds with P7 and the LSB of this register corresponds with P0.

2.10 Input Falling Edge Interrupt Enable Register (FEIR) - Read/Write

Writing a '1' to these bits will enable the corresponding input to generate an interrupt on the falling edge. Writing a '1' to these bits will make that input generate an interrupt on the rising edge only. See **Table 3** for complete details of the interrupt behavior for various register settings. The MSB of this register corresponds with P7 and the LSB of this register corresponds with P0.

2.11 Input Filter Enable Register (IFR) - Read/Write

By default, the input filters are enabled (IFR = 0xFF). When the input filters are enabled, any pulse that is greater than 1075ns will generate an interrupt (if enabled). Pulses that are less than 225ns will be filtered and will not generate an interrupt. Pulses in between this range may or may not generate an interrupt. Writing a '0' to these bits will disable the input filter for the corresponding inputs. With the input filters disabled, any change on the inputs will generate an interrupt (if enabled). See **Table 3** for complete details of the interrupt behavior for various register settings. The MSB of this register corresponds with P7 and the LSB of this register corresponds with P0.

ABSOLUTE MAXIMUM RATINGS

Power supply voltage	3.6 Volts
Supply current	160 mA
Ground current	200 mA
External current limit of each GPIO	25 mA
Total current limit for GPIO[7:0]	100 mA
Total supply current sourced by all GPIOs	160 mA
Operating Temperature	-40^{o} to +85^{o}C
Storage Temperature	-65^{o} to +150^{o}C
Power Dissipation	200 mW

TYPICAL PACKAGE THERMAL RESISTANCE DATA (MARGIN OF ERROR: ± 15%)

Thermal Resistance (16-QFN)	theta-ja = 40^{o}C/W, theta-jc = 26^{o}C/W
Thermal Resistance (16-TSSOP)	theta-ja = 105^{o}C/W, theta-jc = 20^{o}C/W

ELECTRICAL CHARACTERISTICS

DC ELECTRICAL CHARACTERISTICS

UNLESS OTHERWISE NOTED: TA = -40^{O} TO +85^{O}C, VCC IS 1.65V TO 3.6V

SYMBOL	PARAMETER	LIMITS 1.8V ± 10% MIN	LIMITS 1.8V ± 10% MAX	LIMITS 2.5V ± 10% MIN	LIMITS 2.5V ± 10% MAX	LIMITS 3.3V ± 10% MIN	LIMITS 3.3V ± 10% MAX	UNITS	CONDITIONS
V_{IL}	Input Low Voltage	-0.3	0.3VCC	-0.3	0.3VCC	-0.3	0.3VCC	V	Note 1
V_{IL}	Input Low Voltage	-0.3	0.2	-0.3	0.5	-0.3	0.8	V	Note 2
V_{IH}	Input High Voltage	1.3	VCC	1.8	VCC	2.3	VCC	V	Note 1
V_{IH}	Input High Voltage	1.4	5.5	1.8	5.5	2.0	5.5	V	Note 2
V_{OL}	Output Low Voltage		0.4		0.4		0.4	V V V	I_{OL} = 3 mA I_{OL} = 3 mA I_{OL} = 3 mA Note 3
V_{OL}	Output Low Voltage		0.5		0.5		0.5	V	I_{OL} = 8 mA Note 4
V_{OL}	Output Low Voltage		0.4		0.4		0.4	V V V	I_{OL} = 6 mA I_{OL} = 4 mA I_{OL} = 1.5 mA Note 5
V_{OH}	Output High Voltage	1.2		1.8		2.6		V V V	I_{OH} = -8 mA I_{OH} = -8 mA I_{OH} = -8 mA Note 4
I_{IL}	Input Low Leakage Current		±10		±10		±10	uA	
I_{IH}	Input High Leakage Current		±10		±10		±10	uA	
I_{CC}	Power Supply Current		50		100		200	uA	Test 1
I_{CC}	Power Supply Current		150		250		500	uA	Test 2
I_{CCS}	Standby Current		1		2		5	uA	Test 3
C_{IN}	Input Pin Capacitance		5		5		5	pF	
R_{GPIO}	GPIO pull-up resistance	60	140	60	140	60	140	kΩ	100kΩ ± 40%
$R_{RESET\#}$	Reset# pull-up resistance	35	85	35	85	35	85	kΩ	60kΩ ± 40%

NOTE: *The Vcc comes from VCCP pin for the GPIOs and the VCC pin for the other signals;*

NOTES:

1. *For I^2C input signals (SDA, SCL);*
2. *For GPIOs, A0, A1 and A2 signals;*
3. *For I^2C output signal SDA;*
4. *For GPIOs;*

5. For IRQ# signal;

Test 1: SCL frequency is 400 KHz with internal pull-ups disabled. All GPIOs are configured as inputs. All inputs are steady at VCC or GND. Outputs are floating or in the tri-state mode.

Test 2: SCL frequency is 400 KHz with internal pull-ups enabled. All GPIOs are configured as inputs. All inputs are steady at VCC or GND. Outputs are floating or in the tri-state mode.

Test 3: All inputs are steady at VCC or GND to minimize standby current. If internal pull-up is enabled, input voltage level should be the same as VCC. All GPIOs are configured as inputs. SCL and SDA are at VCC. Outputs are left floating or in tri-state mode.

AC ELECTRICAL CHARACTERISTICS

Unless otherwise noted: TA=-40^{o} to +85^{o}C, Vcc=1.65V - 3.6V

SYMBOL	PARAMETER	STANDARD MODE I²C-BUS		FAST MODE I²C-BUS		UNIT
		MIN	MAX	MIN	MAX	
f_{SCL}	Operating frequency	0	100	0	400	kHz
T_{BUF}	Bus free time between STOP and START	4.7		1.3		µs
$T_{HD;STA}$	START condition hold time	4.0		0.6		µs
$T_{SU;STA}$	START condition setup time	4.7		0.6		µs
$T_{HD;DAT}$	Data hold time	0		0		ns
$T_{VD;ACK}$	Data valid acknowledge		0.6		0.6	µs
$T_{VD;DAT}$	SCL LOW to data out valid		0.6		0.6	ns
$T_{SU;DAT}$	Data setup time	250		150		ns
T_{LOW}	Clock LOW period	4.7		1.3		µs
T_{HIGH}	Clock HIGH period	4.0		0.6		µs
T_{F}	Clock/data fall time		300		300	ns
T_{R}	Clock/data rise time		1000		300	ns
T_{SP}	Pulse width of spikes tolerance	50		50		ns
T_{D1}	I²C-bus GPIO output valid		0.2		0.2	µs
T_{D4}	I²C input pin interrupt valid		4		4	µs
T_{D5}	I²C input pin interrupt clear		4		4	µs
T_{D15}	SCL delay after reset	3		3		µs

FIGURE 6. I²C-BUS TIMING DIAGRAM

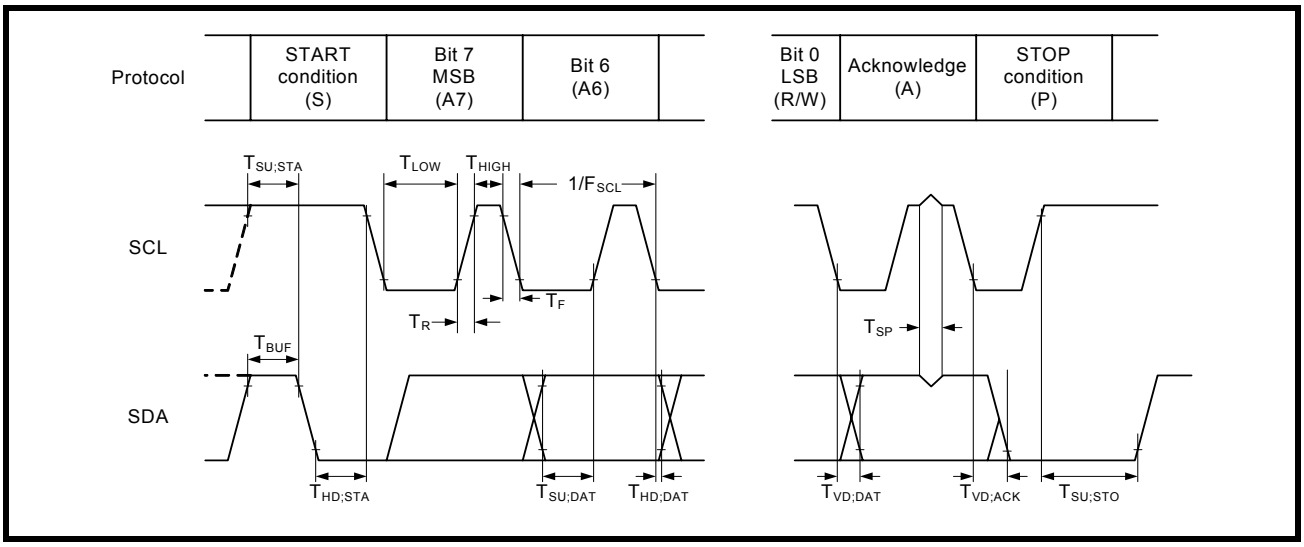


FIGURE 7. WRITE TO OUTPUT

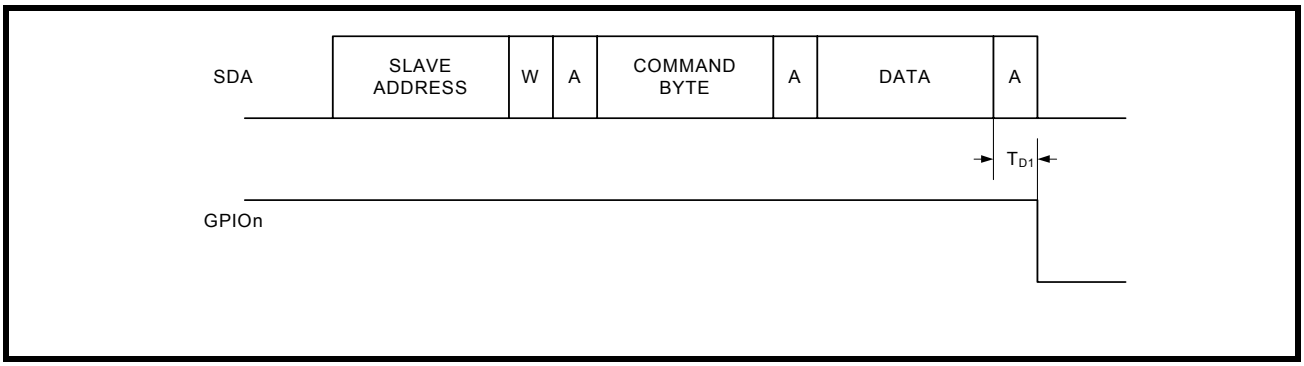
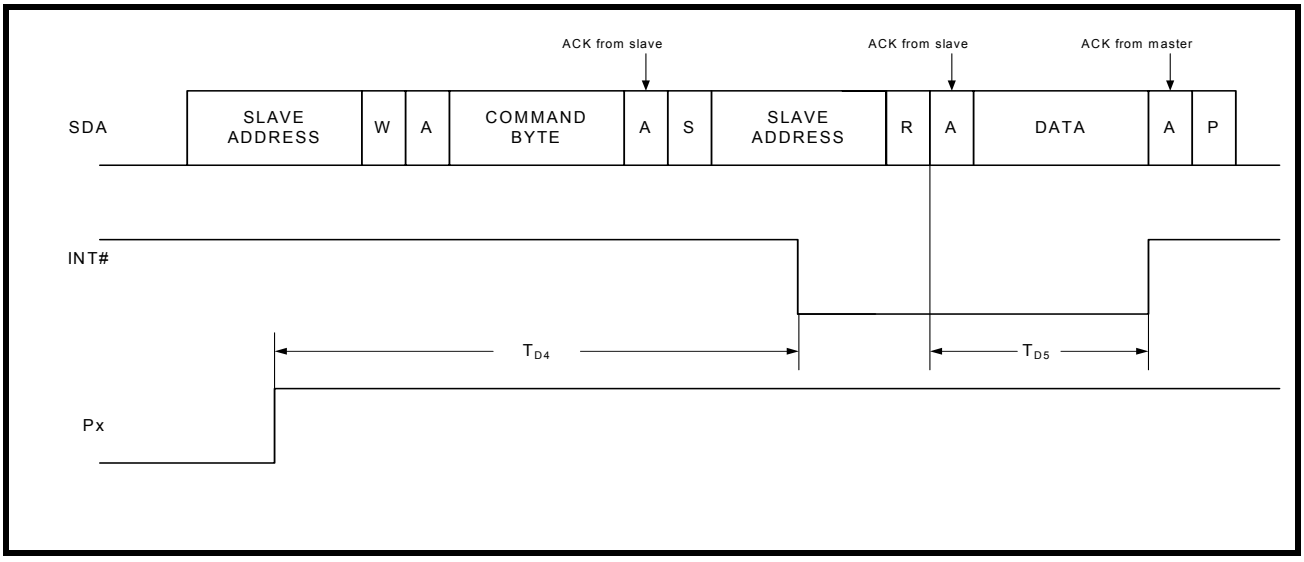
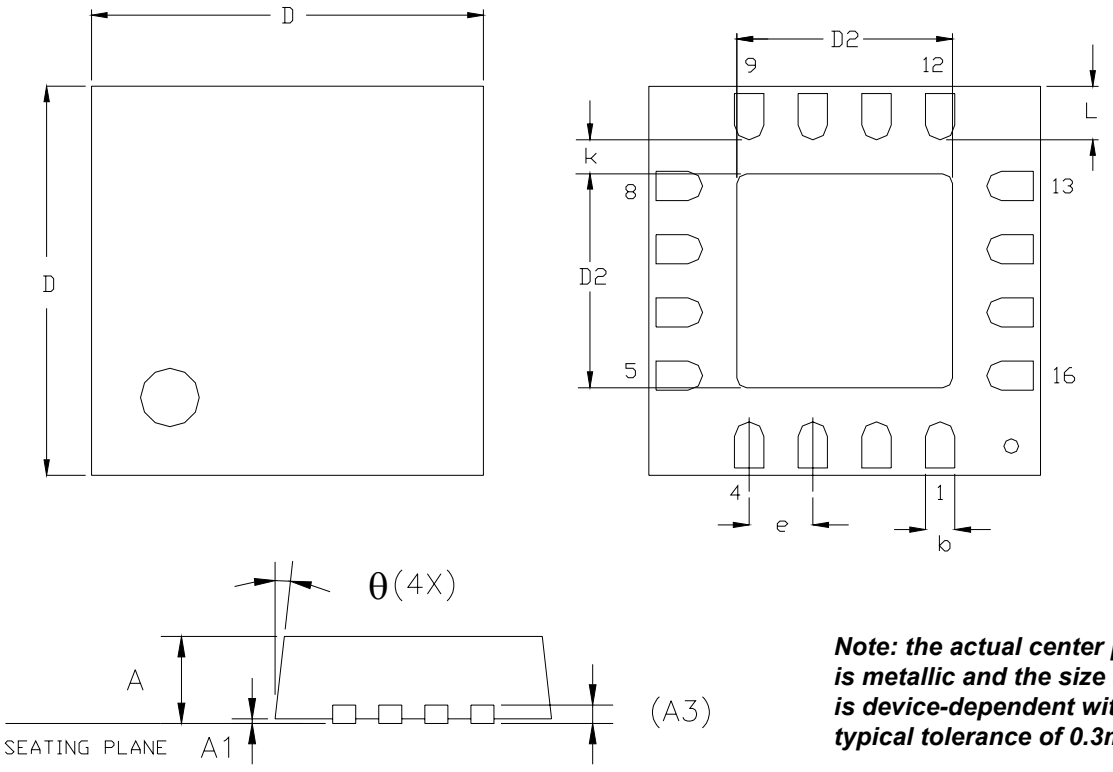


FIGURE 8. GPIO PIN INTERRUPT



PACKAGE DIMENSIONS (16 PIN QFN - 3 X 3 X 0.9 mm, 0.50 PITCH)

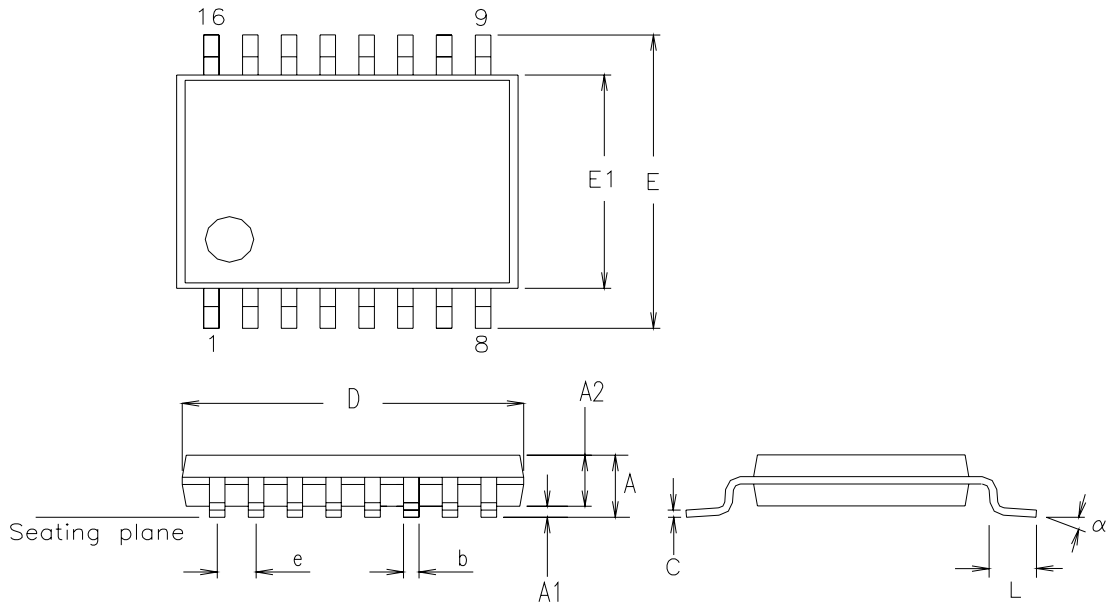


Note: the actual center pad is metallic and the size (D2) is device-dependent with a typical tolerance of 0.3mm

Note: The control dimension is in millimeter.

SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.031	0.039	0.80	1.00
A1	0.000	0.002	0.00	0.05
A3	0.000	0.008	0.00	0.20
D	0.118 BSC		3.00 BSC	
D2	0.063	0.071	1.60	1.80
b	0.010	0.014	0.25	0.35
e	0.020 BSC		0.50 BSC	
L	0.012	0.020	0.30	0.50
θ	0	14°	0	14°
k	0.008	-	0.20	-

PACKAGE DIMENSIONS (16 PIN TSSOP - 4.4 mm)



Note: The control dimension is in millimeter.

SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.031	0.047	0.80	1.20
A1	0.002	0.006	0.05	0.15
A2	0.031	0.037	0.80	0.95
b	0.007	0.012	0.19	0.30
C	0.004	0.008	0.09	0.2
D	0.193	0.201	4.90	5.10
E	0.240	0.264	6.30	6.60
E1	0.169	0.177	4.30	4.50
e	0.0256 BSC		0.65 BSC	
L	0.018	0.030	0.45	0.75
α	0°	8°	0°	8°

REVISION HISTORY

DATE	REVISION	DESCRIPTION
September 2011	1.0.0	Final Datasheet.

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