HMC900LP5E

50 MHz DUAL PROGRAMMABLE LOW PASS FILTER with DRIVER

Typical Applications

The HMC900LP5E is ideal for various modulation systems:

- Baseband filtering before A/D or after D/A converters for point-to-point fixed wireless or base station transceivers (GSM/GPRS, WCDMA & TD-SCDMA)
- Integrated direct conversion receiver (DCR) when mated with mixer and VGA
- Software defined radio applications
- Anti-aliasing and reconstruction filters
- Test and measurement equipment

Features

Low Noise Figure: 12 dB

High linearity: Output IP3 +30 dBm

Pre-programmed and/or Programmable Bandwidth: 3.5 MHz to 50 MHz. (Please see "HMC900LP5E Ordering Information")

Integrated ADC Driver Amplifier

Exceptional 3 dB Bandwidth Accuracy: ±2.5%

6th order Butterworth Magnitude & Phase Response

Automatic Filter Calibration

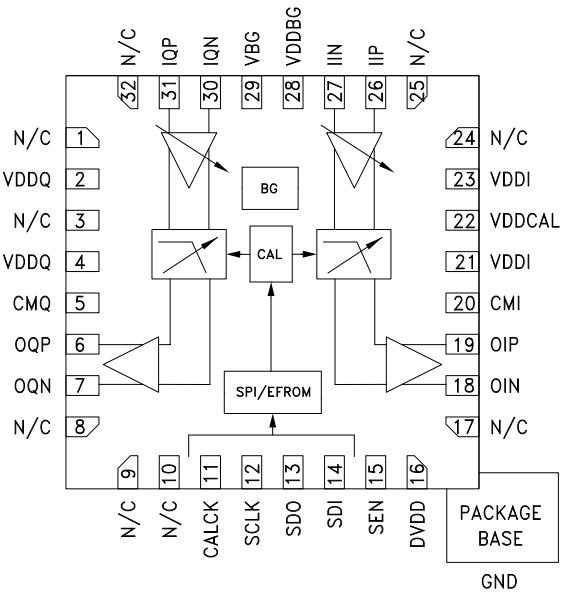
Externally Controlled Common Mode Output Level Simplifies Interface

Filter Bypass Option: 100 MHz Bandwidth

Read/Write Serial Port Interface (SPI)

32 Lead 5x5 mm SMT Package 25 mm^2

Functional Diagram



General Description

The HMC900LP5E is a 6th order, programmable bandwidth, fully calibrated, dual low pass filter. It features 0 or 10 dB input gain setting and supports arbitrary bandwidths from 3.5 MHz to 50 MHz, and when calibrated, is accurate to +/-2.5% of the desired bandwidth. It includes a 100 MHz bandwidth filter bypass option while retaining gain setting and common mode control.

Housed in a compact 5x5 mm SMT QFN package, the HMC900LP5E requires minimal external components and provides a low cost alternative to more complicated switched discrete filter architectures. The integrated ADC driver and externally controlled common mode output level further simplify system implementations.

Filter calibration for the HMC900LP5E is accomplished with any reference clock rate from 20 to 80 MHz. One time programmable (OTP) memory offers unsurpassed flexibility allowing the user "set and forget" parameters like gain and bandwidth setting.

Matched filter paths provide excellent quadrature balance, making the HMC900LP5E ideal for I/Q communications applications.

The 6th order Butterworth transfer function delivers superior stop band rejection while maintaining both a flat passband and minimal group delay variation.

For price, delivery, and to place orders, please contact Hittite Microwave Corporation:
2 Elizabeth Drive, Chelmsford, MA 01824 Phone: 978-250-3343 Fax: 978-250-3373
Order On-line at www.hittite.com

Table 1. Electrical Specifications

T_A = +25°C, VDDI, VDDQ, VDDCAL, VDDBG, DVDD = 5V +/-5%, GND = 0V, 400 Ω load unless otherwise stated.

Parameter	Conditions	Min.	Typ.	Max.	Units
Analog Performance					
Passband Gain [1]	min gain setting max gain setting		0 10		dB dB
3dB corner frequency (fc) Programmable to any frequency in this range	[1]	3.5		50	MHz
	Bypass mode	75	100		MHz
3dB corner frequency variation	uncalibrated			± 20	%
	calibrated		±2.5	± 3.5	%
3dB corner frequency variation vs temperature	over -40°C to +85°C			±0.03	% / °C
Max passband gain error[2]	vs ideal 6th order LPF H(s)			±0.5	dB
Max passband group delay variation (group delay * 3dB frequency fc) e.g. for 1.0 dB BW of 40 MHz (fc ~ 44.9 MHz): max group delay variation = 0.400/ 44.9 MHz = 8.9 ns	at 0.1dB BW (~0.73 fc)			0.250	
	at 0.5dB BW (~0.83 fc)			0.350	
	at 1.0dB BW (~ 0.89 fc)			0.400	
	at 3.0dB BW (at fc)			0.400	
Output Noise (f = 1 MHz)	min gain, fc = 3.5 MHz		22		nV/rtHz
	min gain, fc = 28 MHz		22		nV/rtHz
	max gain fc = 3.5 MHz		25		nV/rtHz
	max gain, fc = 28 MHz		25		nV/rtHz
Output noise (f > 10*fc)	min gain, fc = 3.5 MHz		8		nV/rtHz
	max gain, fc = 3.5 MHz		8		nV/rtHz
	min gain fc = 28 MHz		8		nV/rtHz
	max gain, fc = 28 MHz		8		nV/rtHz
Noise Figure (100 Ω source)	min gain		25		dB
	max gain		17		dB
Noise Figure (1 kΩ source)	min gain		19		dB
	max gain		12		dB
Input referred Passband IM3	half scale tones at 0.8fc and 0.6fc fc = 20 MHz fc = 50 MHz[2]		 -60 -50		 dBc dBc
Input referred Out of Band IM3	half scale tones at 1.2fc and 1.6fc. IM3 product at 0.8fc fc = 20 MHz fc = 50 MHz [2]		 -60 -50		 dBc dBc
Input referred Out of Band IM3	half scale tones at 2fc and 3fc. IM3 product at 0.5fc fc = 20 MHz fc = 50 MHz [2]		 -50 -45		 dBc dBc
Output IP3 (inband)	half scale tones at 0.8fc and 0.6fc fc = 20 MHz fc = 50 MHz	 25 17	 30 20		 dBm dBm
Output IP3 (out of band)	half scale tones at 1.2fc and 1.6fc. IM3 product at 0.8fc fc = 20 MHz fc = 50 MHz [2]	 25 17	 30 20		 dBm dBm
Output IP3 (out of band)	half scale tones at 2fc and 3fc. IM3 product at fc fc = 20 MHz fc = 50 MHz[2]	 25 17	 30 20		 dBm dBm
Output IP2 (inband)	half scale tones at 0.8fc and 0.6fc IM2 product at 0.2fc fc = 20 MHz fc = 50 MHz [2]	 55 55	 60 60		 dBm dBm

Table 1. Electrical Specifications, TA = +25°C (Continued)

Parameter	Conditions	Min.	Typ.	Max.	Units
Output IP2 (out of band)[2]	half scale tones at 1.2fc and 1.6fc. IM2 product at 0.4fc	60	65		dBm
Sideband Suppression (Uncalibrated)	complex signal measured at 0.8fc vs -0.8fc	40	45		dB
I/Q Channel Balance magnitude phase			 0.04 0.5		 dB o
I/Q Channel Isolation		60	80		dB
Analog I/O					
Differential Input Impedance			1000		Ω
Full Scale Differential Input (400 Ω Differential Load)	min gain			2	Vppd
	max gain			0.613	Vppd
Full Scale Differential Input (100 Ω Differential Load)	min gain			0.5	Vppd
	max gain			0.156	Vppd
Input Common Mode Voltage Range		1		4	V
Full Scale Differential Output	400 Ω Differential Load			2	Vppd
Full Scale Differential Output	100 Ω Differential Load			0.5	Vppd
Output Voltage Range		0.5		Vdd-0.5	V
Output Common Mode Voltage Range		Vdd/2-1	Vdd/2	Vdd/2+1	V
Digital I/O					
CALCK Frequency	Use doubler mode for clocks between 20 MHz and 40 MHz	20	40	80	MHz
CALCK Duty Cycle		40	50	60	%
SCLK Frequency			20	30	MHz
Digital Input Low Level (VIL)				0.4	V
Digital Input High Level (VIH)		1.5			V
Digital Output Low Level (VOL)				0.4	V
Digital Output High Level (VOH)		Vdd - 0.4			
Power Supply	Analog & Digital Supplies	4.75	5	5.25	V
Supply Current			130		mA
Power on Reset			250		us

[1] The attenuation of the filter transfer function can be calculated directly at any frequency f as: attenuation = $10*\log_{10}(1+(f/f_0)^{\wedge(2*6)})$, where f_0 is the 3dB bandwidth or corner frequency for the filter. Similarly, for a given maximum attenuation and 3dB bandwidth, f_0, the frequency at which the attenuation is achieved can be calculated as: $f=(10^{\wedge(\text{attenuation}/10)}-1)^{\wedge(1/(2*6))} * f_0$. Note that for a 6th order Butterworth filter the 1dB bandwidth is at ~89% of the filter bandwidth and 0.5dB bandwidth is at 84% of the filter bandwidth.

[2] Specified distortion is measured with in "high linearity" mode with opamp_bias[1:2]=2 and drvr_bias[1:0] = 2. See Reg 02h.

Table 2. Test Conditions

Unless otherwise specified, the following test conditions were used

Parameter	Condition
Temperature	+25 °C
Filter Bandwidth Setting	20 MHz
Gain Setting	0 dB
bias settings (opamp_bias[1:0]/ drvr_bias[1:0])	01/10
Input Signal Level	2 Vppd
Input/Output Common Mode Level	2.5V
Output Load	200Ω / Output
Supply	Analog: +5V, Digital +5V

Figure 1. Filter Attenuation (all Bandwidths)

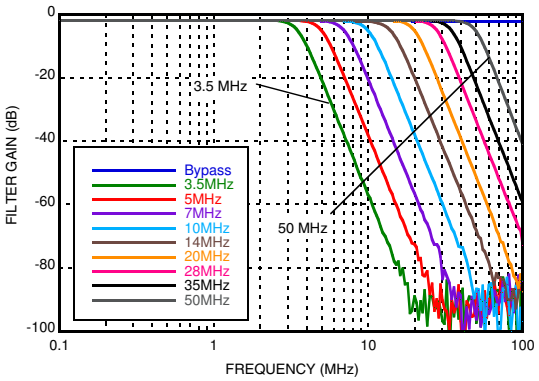


Figure 2. Filter Noise Figure vs Bandwidth[1]

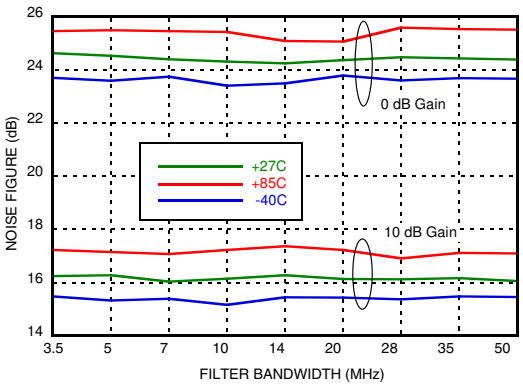


Figure 3. Filter Passband Gain Response

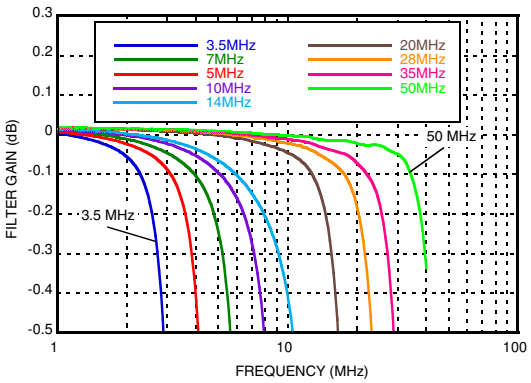


Figure 4. Filter Output Noise

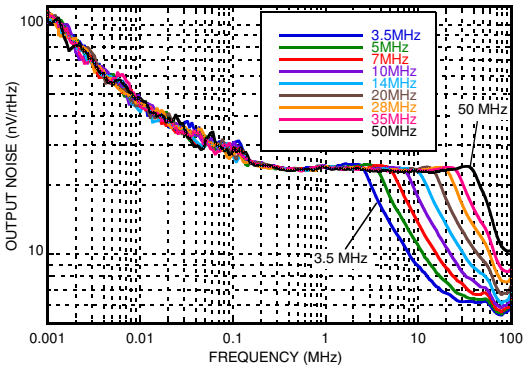


Figure 5. Filter 3 dB Cutoff vs Temperature, 10 MHz Bandwidth

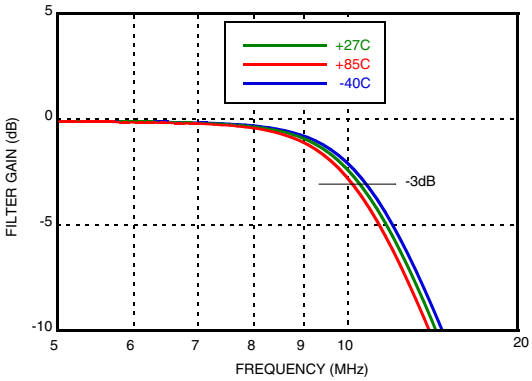
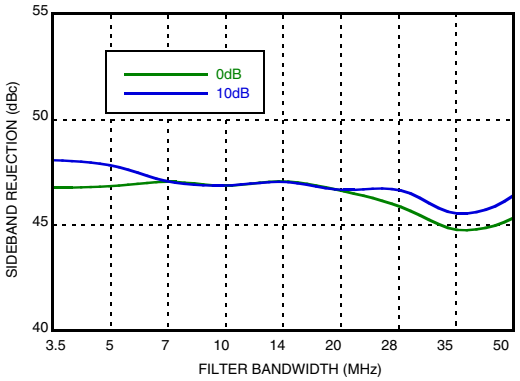


Figure 6. Filter Side Band Rejection vs Bandwidth



[1] Measured with 100 Ω source impedance

Figure 7. In-band OIP3 [1] & OIP2 [1] vs Temperature, 0 dB Gain (standard bias)

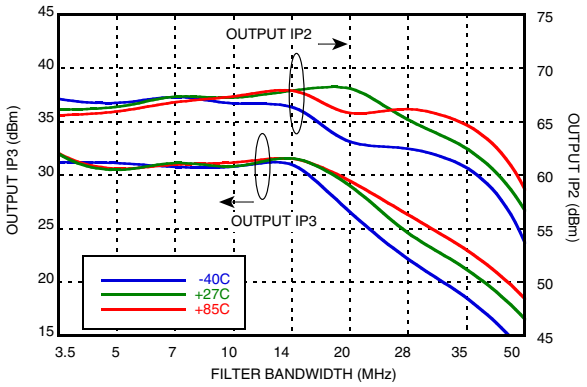


Figure 8. In-band OIP3 [1] and OIP2 [1] vs Temperature, 0 dB Gain (high linearity)

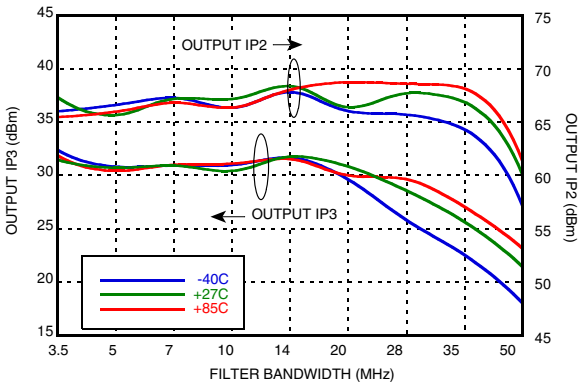


Figure 9. In-band OIP3 [1] and OIP2 [1] vs Bandwidth (standard bias)

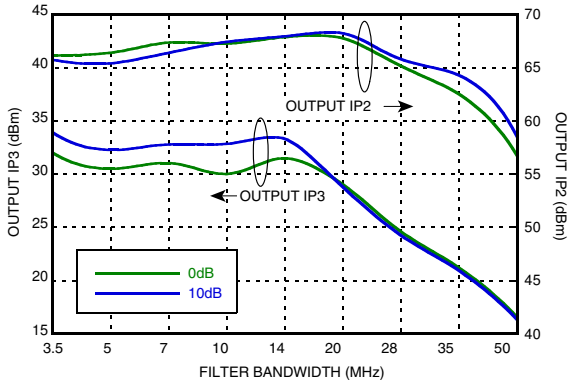


Figure 10. In-band OIP3 [1] and OIP2 [1] vs Bandwidth (high linearity)

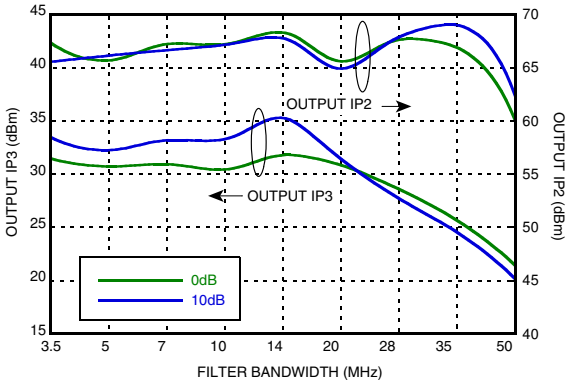


Figure 11. Out-of-band OIP3 [1] and OIP2 [1] vs Bandwidth (standard bias)

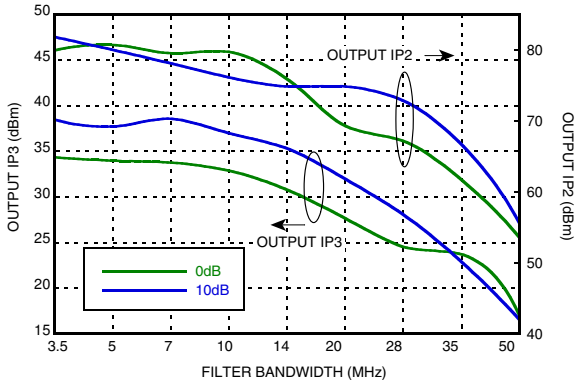
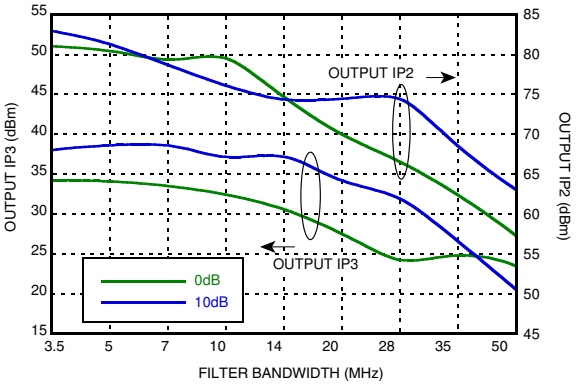


Figure 12. Out-of-band OIP3 [1] and OIP2 [1] vs Bandwidth (high linearity)



[1] OIP3 and OIP2 measured into 400 Ω differential load. OIP3 and OIP2 can be translated from dBm into dBVrms as follows:
IPx [dBVrms] = IPx [dBm] -4 dB

Figure 13. 3.5 MHz Filter Magnitude and Group Delay

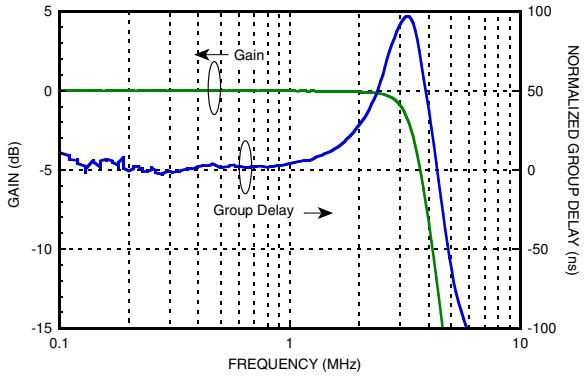


Figure 14. 50 MHz Filter Magnitude and Group Delay

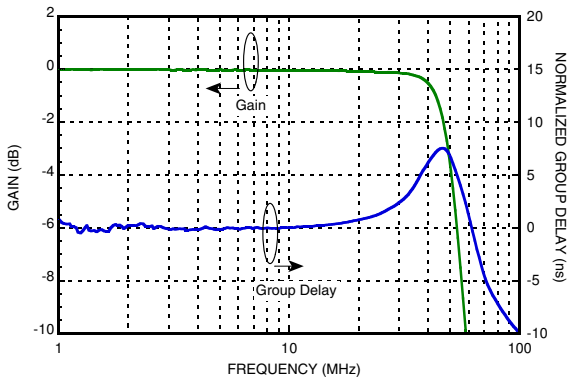


Figure 15. HMC900LP5E OIP2 at 10 MHz & 10.1 MHz [1]

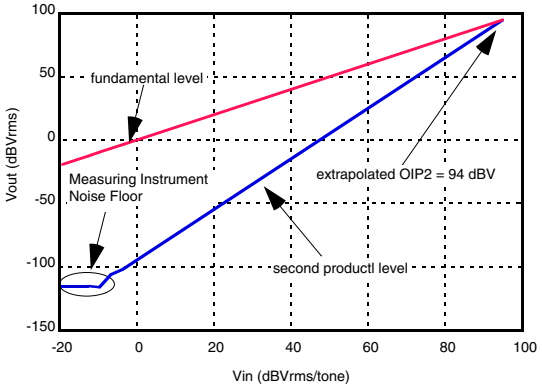


Figure 16. HMC900LP5E OIP3 at 10 MHz & 10.1 MHz [1]

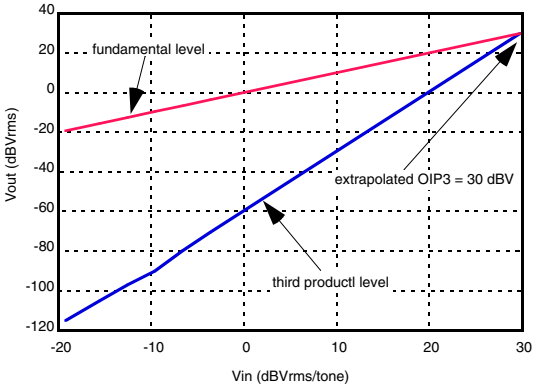
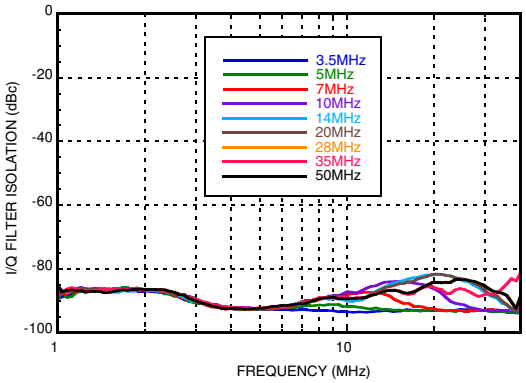


Figure 17. Filter I/Q Channel Isolation



[1] 14 MHz Coarse BW, Op-Amp bias 01

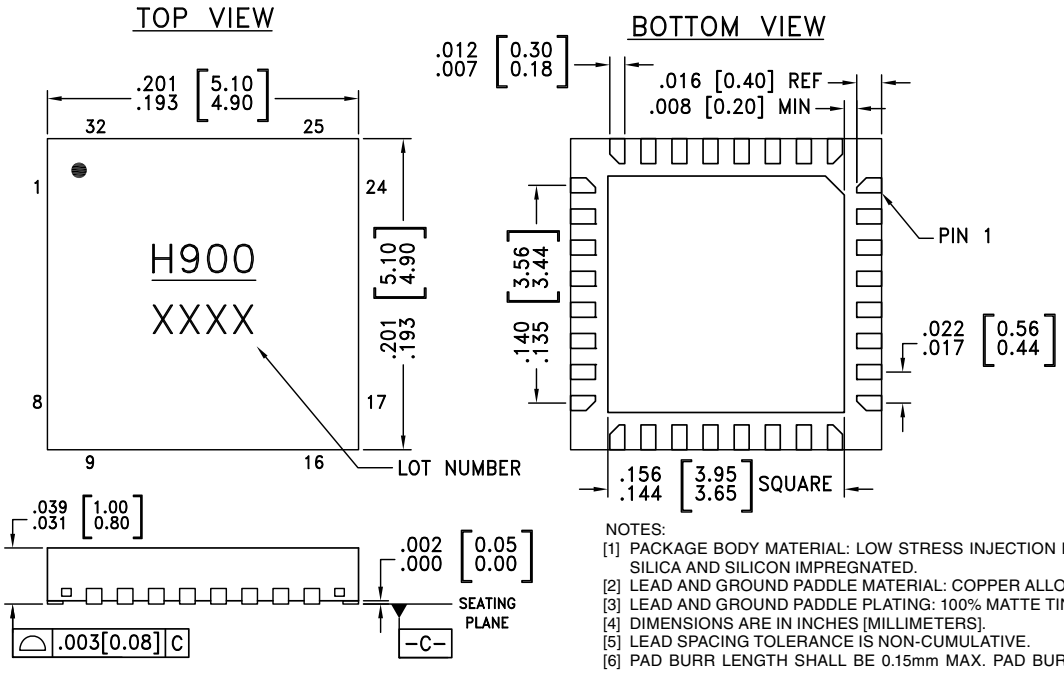
Table 3. Absolute Maximum Ratings

Nominal 5V Supply to GND VDDCAL, VDDI, VDDQ, VDDBG, DVDD	-0.3 to 5.5V
Common Mode Inputs Pins (CMI, CMQ)	-0.3 to 5.5V
Input and Output Pins IIP, IIN, IQP, IQN, OIP, OIN, OQP, OQN	-0.3 to 5.5V
Digital Pins SEN, SDI, SCK, SDO, CALCK SDO min load impedance	-0.3 to 5.5V 1kΩ
Operating Temperature Range	-40 to +85 °C
Storage Temperature	-65 to +125 °C
Maximum Junction Temperature	125 °C
Thermal Resistance (R_{TH}) (junction to ground paddle)	10 °C/W
Reflow Soldering Peak Temperature Time at Peak Temperature	260 °C 40 µs
ESD Sensitivity (HBM)	1kV Class 1C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTROSTATIC SENSITIVE DEVICE
OBSERVE HANDLING PRECAUTIONS

Outline Drawing



NOTES:
[1] PACKAGE BODY MATERIAL: LOW STRESS INJECTION MOLDED PLASTIC SILICA AND SILICON IMPREGNATED.
[2] LEAD AND GROUND PADDLE MATERIAL: COPPER ALLOY.
[3] LEAD AND GROUND PADDLE PLATING: 100% MATTE TIN.
[4] DIMENSIONS ARE IN INCHES [MILLIMETERS].
[5] LEAD SPACING TOLERANCE IS NON-CUMULATIVE.
[6] PAD BURR LENGTH SHALL BE 0.15mm MAX. PAD BURR HEIGHT SHALL BE 0.25m MAX.
[7] PACKAGE WARP SHALL NOT EXCEED 0.05mm
[8] ALL GROUND LEADS AND GROUND PADDLE MUST BE SOLDERED TO PCB RF GOUND.
[9] REFER TO HITTITE APPLICATION NOTE FOR SUGGESTED PCB LAND PATTERN.

Table 4. Package Information

Part Number	Package Body Material	Lead Finish	MSL Rating [1]	Package Marking [2]
HMC900LP5E	RoHS-compliant Low Stress Injection Molded Plastic	100% matte Sn	MSL1	H900 XXXX

[1] Max peak reflow temperature of 260 °C
[2] 4-Digit lot number XXXX

Table 5. Pin Descriptions

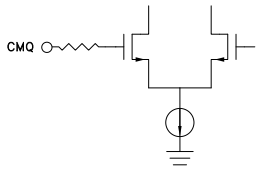
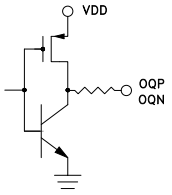
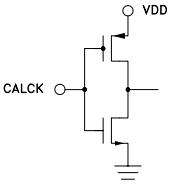
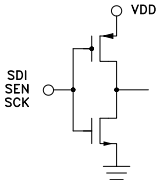
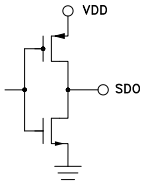
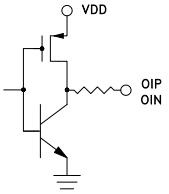
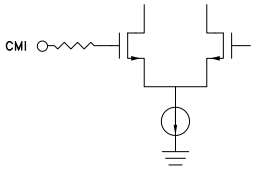
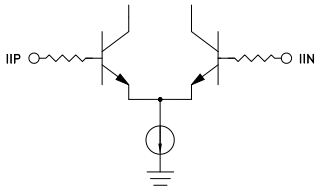
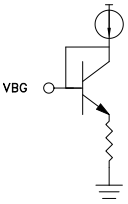
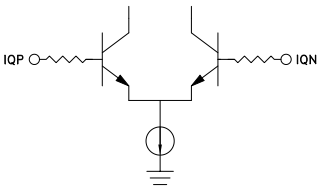
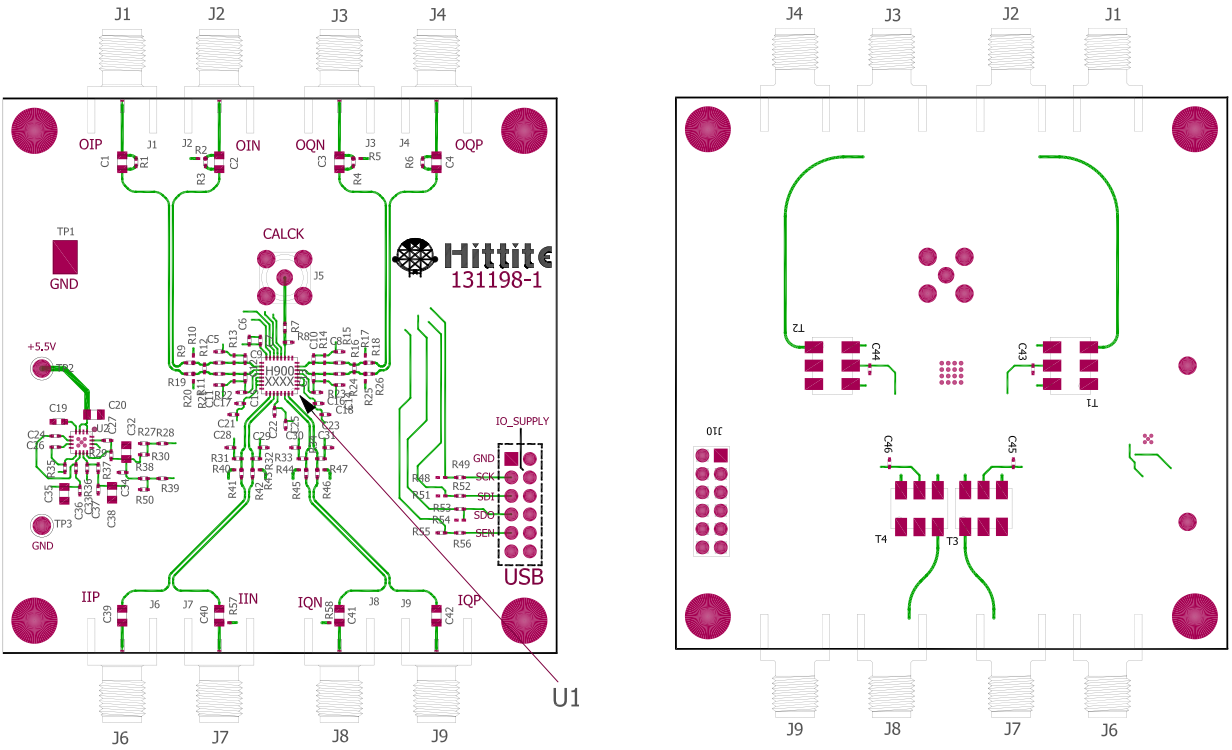
Pin Number	Function	Description	Interface Schematic
1, 3, 8 - 10, 17, 24, 25, 32	N/C	The pins are not connected internally; however, all data shown herein was measured with these pins connected to RF/DC ground externally.	
2, 4	VDDQ	Quadrature (Q) Channel 5V Supply. Must be locally decoupled to GND	
5	CMQ	Quadrature (Q) channel output common mode level	
6, 7	OQP, OQN	Quadrature (Q) channel positive and negative differential outputs	
11	CALCK	Calibration clock input	
12, 14, 15	SCLK, SDI, SEN	SPI Data clock, data input and enable respectively.	
13	SDO	SPI Data Output	
16	DVDD	Digital 5V Supply. Must be locally decoupled to GND.	
18, 19	OIN, OIP	Inphase (I) channel negative and positive differential outputs respectively	

Table 5. Pin Descriptions *(Continued)*

Pin Number	Function	Description	Interface Schematic
20	CMI	Inphase (I) channel output common mode level	
21, 23	VDDi	Inphase (I) Channel 5V Supply. Must be locally decoupled to GND	
22	VDDCAL	Calibration 5V Supply. Must be locally decoupled to GND	
26, 27	IIP, IIN	Inphase (I) channel positive and negative differential inputs respectively	
28	VDDBG	Bias 5V Supply. Must be locally decoupled to GND.	
29	VBG	1.2V Bandgap output (testing only)	
30, 31	IQN, IQP	Quadrature (Q) channel negative and positive differential inputs respectively	

Evaluation PCB



The circuit board used in the application should use RF circuit design techniques. Signal lines should have 50 Ohms impedance while the package ground leads and exposed paddle should be connected directly to the ground plane similar to that shown. A sufficient number of via holes should be used to connect the top and bottom ground planes. The evaluation circuit board shown is available from Hittite upon request.

Table 6. Evaluation Order Information

Item	Contents	Part Number
Evaluation PCB Only	HMC900LP5E Evaluation PCB	131200-HMC900LP5E
Evaluation Kit	HMC900LP5E Evaluation PCB USB Interface Board 6' USB A Male to USB B Female Cable CD ROM (Contains User Manual, Evaluation PCB Schematic, Evaluation Software)	130521-HMC900LP5E

Evaluation PCB Schematic

To view Evaluation PCB Schematic please visit www.hittite.com and choose HMC900LP5E from the "Search by Part Number" pull down menu to view the product splash page.

Evaluation Setup

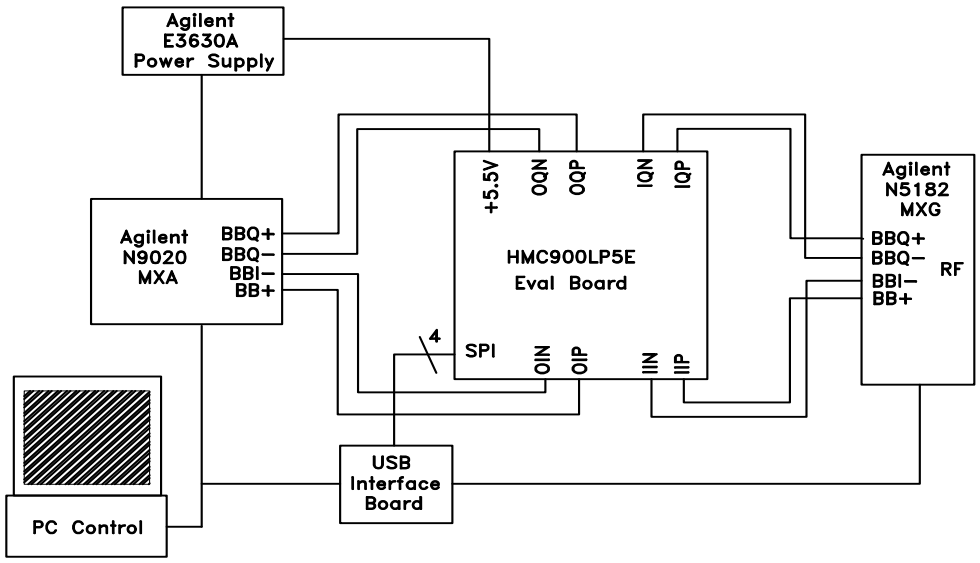


Figure 18. Characterization Setup Block Diagram

HMC900LP5E Usage Information

The HMC900LP5E addresses different filter applications such as fixed frequency or variable bandwidth implementations dependent on the part selected (see "HMC900LP5E Ordering Information") and the control provided to the HMC900LP5E. These modes provide the user with different filter options depending on the system implementation.

An overview of these trade-offs are shown below.

Table 7. HMC900LP5E Modes of Operation

Function	Unprogrammed HMC900LP5E-00000	Pre-programmed HMC900LP5E-BBBGL	SPI Req'd	CALCK Req'd	Comments
Fixed Bandwidth Filter	Yes	Yes	No	No	
Default Bandwidth and Gain setting after Power On Reset (POR)	Default Bandwidth and Gain as defined by register defaults. (3.5 MHz /0dB gain)	Bandwidth and Gain as defined by pre-programming at factory.			Pre-programmed gain and bandwidth are defined when ordering the part. See "HMC900LP5E Ordering Information".
Typical Corner Frequency Accuracy at Default Bandwidth	+/- 20 %	+/- 2.5 %			Accuracy is with respect to bandwidth after POR.
Variable Bandwidth Filter	Yes	Yes	Yes	No	Full control over HMC900LP5E requires access via the digital serial port (SPI).
Default Bandwidth and Gain setting after Power On Reset (POR)	Default Bandwidth and Gain as defined by register defaults. (3.5 MHz /0dB gain)	Bandwidth and Gain as defined by pre-programming at factory.			Pre-programmed gain and bandwidth are defined when ordering the part. See "HMC900LP5E Ordering Information".
Typical Corner Frequency Accuracy at Default Bandwidth	+/- 20 %	+/- 2.5 %			Accuracy is with respect to bandwidth after POR.
Typical Corner Frequency Accuracy at all other Bandwidths	+/- 20 %	+/- 5.0 %			Accuracy is with respect to the desired bandwidth. See "Filter Bandwidth Setting" for information regarding changing the bandwidth after when calibration is not possible.
Variable Bandwidth Filter (with ability to execute User Calibration to calibrate filter bandwidth)	Yes	Yes	Yes	Yes	Full control over HMC900LP5E requires access via the digital serial port (SPI). Filter calibration requires valid calibration clock (via CALCK pin). See "RC Calibration Circuit"
Default Bandwidth and Gain setting after Power On Reset (POR)	Default Bandwidth and Gain as defined by register defaults. (3.5 MHz /0dB gain)	Bandwidth and Gain as defined by pre-programming at factory.			Pre-programmed gain and bandwidth are defined when ordering the part. See "HMC900LP5E Ordering Information".
Typical Corner Frequency Accuracy after POR (before User Calibration)	+/- 20 %	+/- 2.5 %			Accuracy is with respect to bandwidth after POR.
Typical Corner Frequency Accuracy after User Calibration at **calibrated** bandwidth	+/- 2.5 %	+/- 2.5 %			Accuracy is with respect to calibrated bandwidth. User Calibration requires access to the HMC900LP5E via the digital serial port (SPI) and requires a valid calibration clock (via CALCK pin).
Typical Corner Frequency Accuracy after User Calibration at **non calibrated** bandwidths	+/- 5.0 %	+/- 5.0 %			Accuracy is with respect to the desired bandwidth. User Calibration requires access to the HMC900LP5E via the digital serial port (SPI) and requires a valid calibration clock (via pin CALCK). See "Filter Bandwidth Setting" for information regarding changing the bandwidth after calibration when further calibration is not possible.

HMC900LP5E Application Information

The HMC900LP5E provides an attractive alternative to other discrete filter solutions due to it's unmatched flexibility in supporting a wide range of bandwidths in today's complex multi-carrier systems and multi-standard systems.

Typical architectures supporting multiple bandwidths have required either large board real estate or compromised filter selection which come at the expense of price or performance. The HMC900LP5E overcomes this limitation by allowing the system designer to optimize the bandwidth for the required signal.

The HMC900LP5E overcomes the matching problem that discrete filters present with respect to baseband signal processing. The matched dual filter paths provide excellent gain and phase balance between the two channels eliminating the image problem which results from poor matching.

The HMC900LP5E provides selectable gain and a flexible output driver further increase system integration and reduce board area.

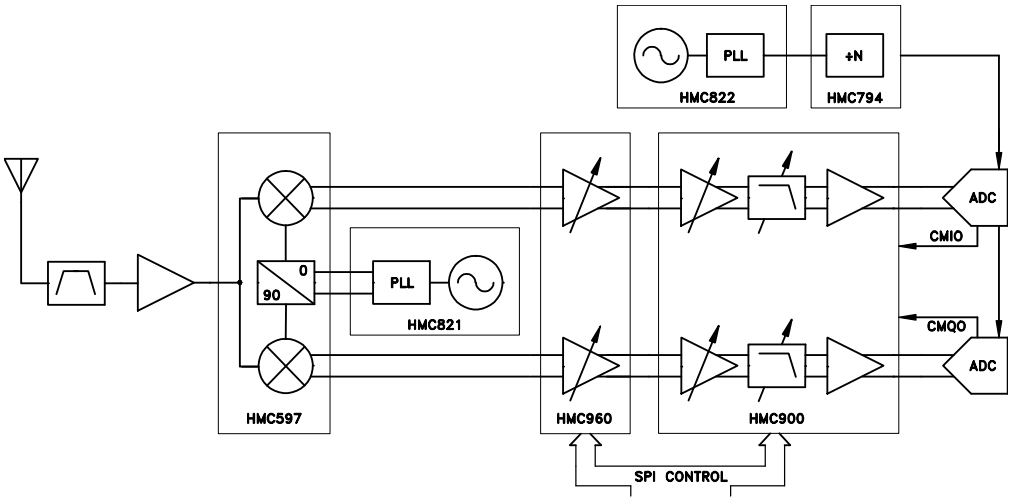


Figure 19. Typical Receive Path Block Diagram showing HMC900LP5E

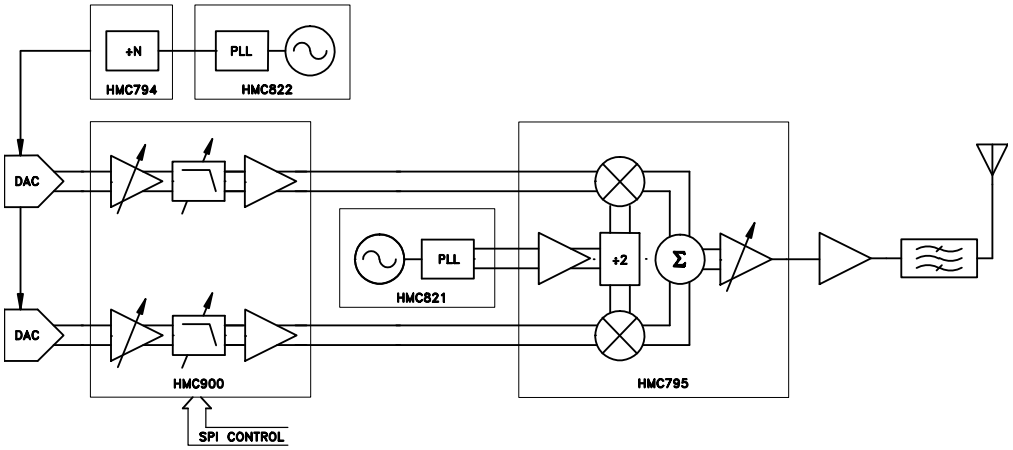


Figure 20. Typical Transmit Path Block Diagram

HMC900LP5E Ordering Information

The HMC900LP5E is available as product that is either un-programmed or pre-programmed. Programming is available to a variety of filter bandwidths (defined in this context as the 3dB bandwidth).

Other options available for pre-programmed product include the single path gain and bias state as described below. Gain and bias settings are described in Reg 02h.

When placing an order for the HMC900LP5E please observe the following guidelines.

1. To order the un-programmed standard part please place order using the part number HMC900LP5E-00000.
2. To order a pre-programmed HMC900LP5E please determine the part number as described below and then contact Hittite Sales at sales@hittite.com or call (978) 250-3343.

   2.1 Minimum quantity order for the pre-programmed HMC900LP5E-BBBGL is 500 pieces.
3. Pre-Programmed part number description: HMC900LP5E-BBBGL.

   3.1 'BBB' represents a three digit number from the following table that represents the desired bandwidth setting (3 dB bandwidth) from 3.5 MHz to 50 MHz (for example BBB = 035 specifies a 3.5 MHz corner frequency).

   3.2 'G' represents the gain setting of either 0 dB (G = 0) or 10 dB (G = 1).

   3.3 'L' represents the linearity setting of either standard (L = 0) or high linearity (L = 1). Note that the high linearity setting is recommended only for bandwidth settings above 30 MHz.[1]

For example, to order the HMC900LP5E pre-programmed for 50 MHz 3 dB frequency, 10 dB gain, and standard linearity setting please specify part number HMC900LP5E-50010.

Table 8. Custom Part Frequency Options

BBB frequency for custom part (actual frequency is BBB x 0.1 MHz)								
035	048	066	088	121	163	218	292	400
036	049	068	091	124	167	224	300	401
037	050	069	093	128	171	229	307	411
038	052	070	095	131	175	235	315	422
039	053	071	098	134	179	240	322	432
040	054	073	100	137	180	246	330	443
041	056	075	102	140	184	253	338	454
042	057	076	105	141	188	259	347	465
043	058	078	108	144	193	265	355	476
044	060	080	110	148	198	272	364	488
045	061	082	113	151	203	278	373	500
046	063	084	116	155	208	280	382	
047	064	086	119	159	213	285	392	

[1] The Output IP2 and Output IP3 for the two linearity settings are shown in Figure 8 and Figure 9. High linearity setting improves linearity for bandwidths greater than 30 MHz at the cost of increased current consumption (additional 25 mA).

Theory of Operation

The HMC900LP5E consists of the following functional blocks

1. Input Gain Stage
2. 6th Order LPF
3. Output Driver
4. RC Calibration Circuit
5. Bias Circuit
6. One Time Programmable Memory
7. Serial Port interface
8. Built in Self Test (RC-BIST)

Input Gain Stage

The HMC900LP5E input stage consists of a programmable 0 or 10 dB gain stage which in turn drives the 6th order LPF. A block diagram showing input impedance of the I channel is presented below, Q channel is similar.

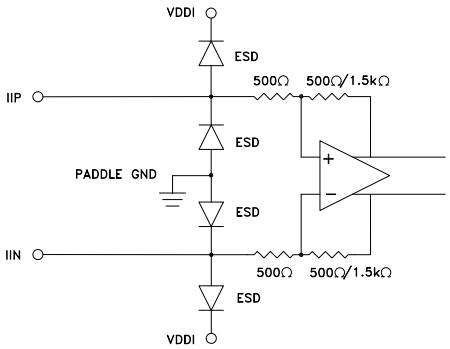


Figure 21. Input Stage Block Diagram

6th Order Low Pass Filter (LPF)

The LPF allows for coarse bandwidth tuning by varying the capacitive elements in the filter, while the fine bandwidth tuning is accomplished by varying the resistors. Note that all opamps in the LPF are class AB for minimum power consumption in the filter while maintaining excellent distortion characteristics even in large signal swing conditions.

The attenuation due to the LPF can be calculated for any frequency, f, from the standard Butterworth transfer function for a 6th order filter. Specifically the attenuation of the filter, in dB, can be calculated as:

$$\text{attenuation} = 10*\log_{10}(1+(f/f_c)^{\wedge(2*6)})$$

where f_c is the 3 dB bandwidth or corner frequency for the filter.

Note that for a 6th order Butterworth filter the 1 dB bandwidth is 90% of f_c, and the 0.3 dB bandwidth is 80% of f_c.

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Filter Bandwidth Setting

The 3 dB bandwidth of the HMC900LP5E is programmable anywhere within the range from 3.5 to 50 MHz. This is accomplished via a two step process which involves 1) running calibration, and 2) programming the appropriate coarse and fine bandwidth codes. Once the settings for a given device are found, they can be stored permanently in the non volatile memory (See "One Time Programmable Memory (OTP)".)

To program the bandwidth of the HMC900LP5E to a desired bandwidth, f_{wanted}, the procedure is as follows:

1. Run a calibration routine.

   Run a filter calibration cycle to determine the particular calibration code for the device under test (See "RC Calibration Circuit".) Once complete, the actual calibration measurement must be read from the SPI (See Reg 09h.)

2. Calculate the desired coarse bandwidth and fine bandwidth codes.

   a. From the calibration result we define a coarse tune factor, ctune as:

   $$ctune = Cal_count / 10370000$$

   b. Normalize the desired frequency

   $$f_{BW_norm_coarse} = f_{wanted} * ctune$$

   c. Lookup the coarse tune code based on $f_{BW_norm_coarse}$ from Table 9.

Table 9. Normalized Bandwidth Look up Table

coarse_bandwidth_code[3:0]	$f_{BW_norm_coarse}$		
	min (MHz)	typ (MHz)	max (MHz)
0000	2.764	3.500	4.235
0001	3.948	5.000	6.050
0010	5.527	7.000	8.470
0011	7.896	10.000	12.100
0100	11.055	14.000	16.940
0101	15.792	20.000	24.200
0110	22.109	28.000	33.880
0111	27.637	35.000	42.351
1000	39.480	50.000	60.500

   d. Calculate the fine tuning factor, fine_tune_ratio, for bandwidth based on the typical value of the coarse bandwidth center frequency, $f_{BW_norm_coarse_typ}$

   $$fine_tune_ratio = f_{BW_norm_coarse} / f_{BW_norm_coarse_typ}$$

   e. Lookup the fine tune code based on fine_tune_ratio from Table 10:

Table 10. Calibration Code Look up Table

fine_bandwidth_code [3:0]	fine_tune_ratio		
	min (MHz/MHz)	typ (MHz/MHz)	max (MHz/MHz)
0000	0.790	0.803	0.818
0001	0.818	0.832	0.846
0010	0.846	0.862	0.878
0011	0.878	0.893	0.909
0100	0.909	0.926	0.943
0101	0.943	0.959	0.976
0110	0.976	0.994	1.012
0111	1.012	1.030	1.048
1000	10.48	1.068	1.087
1001	1.087	1.107	1.128
1010	1.128	1.148	1.169
1011	1.169	1.189	1.210

3. Program the SPI for the given device with the coarse and fine bandwidth code, and instruct the device to use the provided instructions.

a. Write coarse_bandwidth_code[3:0] to Reg 02h bits [9:6]

b. Write fine_bandwidth_code[3:0] to Reg 03h bits [3:0]

c. Instruct HMC900LP5E to use provided codes by setting Reg 01h bit 4.

Filter Bandwidth Setting After Calibration

After the initial filter calibration is completed as above the filter bandwidth can be changed to an arbitrary bandwidth by recalculating coarse_bandwidth_code[3:0] and fine_bandwidth_code[3:0] from the previously determined ctune. This results in the same coarse_bandwidth_code[3:0] and fine_bandwidth_code[3:0] as if the HMC900LP5E was recalibrated as described above.

If ctune is unknown but the current desired frequency is known then the value of ctune needs to be estimated based on the values of coarse_bandwidth_code[3:0] and fine_bandwidth_code[3:0] and the corresponding nominal frequencies in Table 9 and Table 10.

For example, if the 3 dB bandwidth for the HMC900LP5E was factory pre-programmed to a customer defined requirement of 34 MHz and coarse_bandwidth_code[3:0] and fine_bandwidth_code[3:0] are "0111" and "1001" respectively (as determined from Reg 0Ah for a pre-programmed part or from Reg 02h for a non programmed part) then ctune can be estimated as follows:

1. Lookup the nominal coarse bandwidth and fine bandwidth frequencies.
   a. From Table 9 the nominal coarse frequency is 35.0 MHz
   b. From Table 10 the nominal fine normalized frequency is 1.107 MHz/ MHz or simply 1.107
2. Estimate ctune as:

   ctune=(35 MHz * 1.107)/ 34 MHz = 1.13956

This value of ctune can now be used to calculate any arbitary filter frequency as described above.

Output Driver

The HMC900LP5E output driver consists of a differential class AB driver which is designed to drive typical ADC loads directly or can drive up to 200Ω in parallel with 50 pF to AC ground per differential output. Note that the output common mode of the driver is controlled directly via the CMI/CMQ pin and can be set as per "Table 1. Electrical Specifications". Also note, that driver loading does not impact filter transfer responses. The output common mode of the driver is controlled directly via the CMI/CMQ pin and can be set as per the "Table 1. Electrical Specifications".

A block diagram showing output connections is presented below.

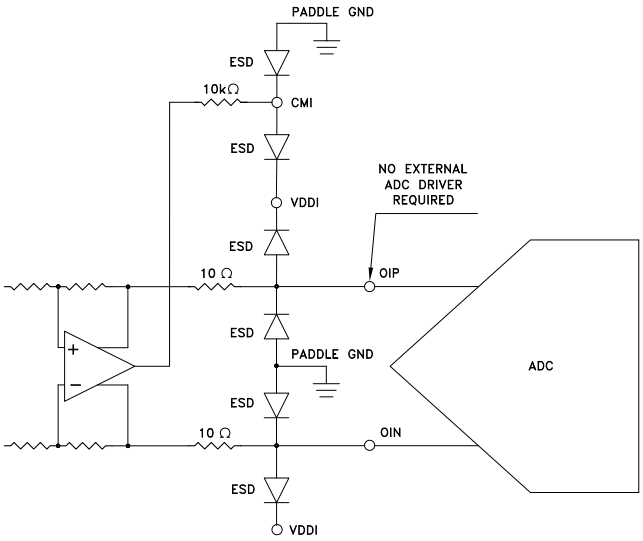


Figure 22. Output Driver Block Diagram

RC Calibration Circuit

The RC Calibration block uses a known user supplied clock to measure an on chip RC time constant. This measurement is representative of the uncorrected corner frequency error for a given bandwidth for the LPF.

Calibration is normally done at room temperature Refer to "Table 1. Electrical Specifications" for further details on the variation of the 3dB cutoff point with temperature.

With this information, the HMC900LP5E can correctly fine tune the LPF by adjusting the resistors in the LPF to center the corner frequency to the desired bandwidth.

The calibration for the HMC900LP5E proceeds as follows:

1. the clock used for calibration is programmed between 20 MHz and 100 MHz via Reg 05h. Also note that for clocks between 20 MHz and 40 MHz the doubler must be enabled via Reg 01h.
2. the RC calibration circuit is enabled via Reg 01h.
3. a calibration cycle is initialized by writing to Reg 04h.

When complete, the calibration value can be retrieved from Reg 08h and, if desired, the calibration results can be overridden via Reg 03h.

Bias Circuit

A band gap reference circuit generates the reference currents used by the different sections. The bias circuit is enabled or disabled as required with the I or Q channel as appropriate.

One Time Programmable Memory (OTP)

The HMC900LP5E features one time programmable memory which can be programmed by the end user or ordered from the factory precalibrated.

The OTP memory is programmed via the standard 4 wire serial port (SPI) as follows:

1. enable OTP write mode (see Reg 0Bh bit 0 enables OTP programming).
2. read the status of the OTP active flag (see Reg 08h, bit 5 is the OTP active flag). The Write Pulse Status (OTP active flag) must be 0 to allow the OTP to be programmed.
3. write the OTP bit address to be set (Reg 0Ch). This address is a 4 bit number representing the address of the bit to be programmed. Note that when programming a bit we change its state from 0 to 1 and this operation cannot be reversed. OTP bit addresses can be found in Reg 08h.
4. start the OTP Write operation. Write any data to the OTP strobe register (Reg 0Dh).
5. read the status of the OTP active flag (Reg 08h, bit 5 is the OTP active flag). If bit 5 is set then the Write pulse is still high. Repeat until bit 5 is 0 which indicates that the write pulse is finished.
6. Repeat steps 3 to 5 to program the remaining desired bits.

   Note that bit 13 OTP_prg_flag must be set by the user to use OTP values.
7. When completed, disable OTP write mode (Reg 0Bh).

Serial Port Interface

The HMC900LP5E features a four wire serial port for simple communication with the host controller. Typical serial port operation can be run with SCK at speeds up to 30MHz.

The details of SPI access for the HMC900LP5E is provided in the following sections. Note that the READ operation below is always preceded by a WRITE operation to Reg 0h to define the register to be queried. Also note that every READ cycle is also a WRITE cycle in that data sent to the SPI while reading the data will also be stored by the HMC900LP5E when SEN goes high. If this is not desired then it is suggested to write to Reg 0h during the READ operation as the status of the device will be unaffected.

Power on Reset and Soft Reset

The HMC900LP5E has a built in Power On Reset (POR) and also a serial port accessible Soft Reset (SR). POR is accomplished when power is cycled for the HMC900LP5E while SR is accomplished via the SPI by writing 20h to Reg 0h followed by writing 00h to Reg 0h. All chip registers will be reset to default states approximately 250us after power up.

Serial Port WRITE Operation

The host changes the data on the falling edge of SCK and the HMC900LP5E reads the data on the rising edge.

A typical WRITE cycle is shown in Figure 23. It is 32 clock cycles long.

1. The host both asserts SEN (active low Serial Port Enable) and places the MSB of the data on SDI followed by a rising edge on SCLK.

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2. HMC900LP5E reads SDI (the MSB) on the 1st rising edge of SCK after SEN.
3. HMC900LP5E registers the data bits, D23:D0, in the next 23 rising edges of SCLK (total of 24 data bits).
4. Host places the 5 register address bits, A4:A0, on the next 5 falling edges of SCLK (MSB to LSB) while the HMC900LP5E reads the address bits on the corresponding rising edge of SCK.
5. Host places the 3 chip address bits, CA2:CA0=[101], on the next 3 falling edges of SCK (MSB to LSB). Note the HMC900LP5E chip address is fixed as "5d" or "101b".
6. SEN goes from low to high after the 32th rising edge of SCK. This completes the WRITE cycle.
7. HMC900LP5E also exports data back on the SDO line. For details see the section on READ operation.

Serial Port READ Operation

The SPI can read from the internal registers in the chip. The data is available on SDO line. This line itself is tri-stated when the device is not being addressed. However when the device is active and has been addressed by the SPI master, the HMC900LP5E controls the SDO line and exports data on this line during the next SPI cycle.

HMC900LP5E changes the data to the host on the rising edge of SCLK and the host reads the data from HMC900LP5E on the falling edge.

A typical READ cycle is shown in Figure 23. Read cycle is 32 clock cycles long. To specifically read a register, **the address of that register must be written to dedicated Reg 0h**. This requires two full cycles, one to write the required address, and a 2nd to retrieve the data. A read cycle can then be initiated as follows;

1. The host asserts SEN (active low Serial Port Enable) followed by a rising edge SCLK.
2. HMC900LP5E reads SDI (the MSB) on the 1st rising edge of SCK after SEN.
3. HMC900LP5E registers the data bits in the next 23 rising edges of SCLK (total of 24 data bits). **The LSBs of the data bits represent the address of the register that is intended to be read.**
4. Host places the 5 register address bits on the next 5 falling edges of SCLK (MSB to LSB) while the HMC900LP5E reads the address bits on the corresponding rising edge of SCK. **For a read operation this is "00000".**
5. Host places the 3 chip address bits <101> on the next 3 falling edges of SCK (MSB to LSB). Note the HMC900LP5E chip address is fixed as "5d" or "101b".
6. SEN goes from low to high after the 32th rising edge of SCK. This completes the first portion of the READ cycle.
7. The host asserts SEN (active low Serial Port Enable) followed by a rising edge SCLK.
8. HMC900LP5E places the 24 data bits, 5 address bits, and 3 chip id bits, on the SDO, on each rising edge of the SCK, commencing with the first rising edge beginning with MSB.
9. The host deasserts SEN (i.e. sets SEN high) after reading the 32 bits from the SDO output. The 32 bits consists of 24 data bits, 5 address bits, and the 3 chip id bits.

Note that the data sent to the SPI during this portion of the READ operation is stored in the SPI when SEN is deasserted. This can potentially change the state of the HMC900LP5E. If this is undesired it is recommended that during the second phase of the READ operation that Reg 0h is addressed with either the same address or the address of another register to be read during the next cycle.

10. This completes the READ cycle.

Serial Port Bus Operation with Multiple Devices

The SPI bus architecture supports multiple HMC devices on the same SPI bus. Each HMC900LP5E on the bus requires a dedicated SEN line to enable the appropriate device.

The SDO pin is normally driven by the HMC900LP5E during and after an SPI read/write which is addressed directly to the HMC900LP5E (chip address = 5d or '101'b). A write to the HMC900LP5E where chip address is set to any value other than 5d or '101'b is required in order to ensure that the SDO pin remains tri-stated after accessing the HMC900LP5E. Such a write will not result in any change in the HMC900LP5E configuration because of the incorrect chip address.

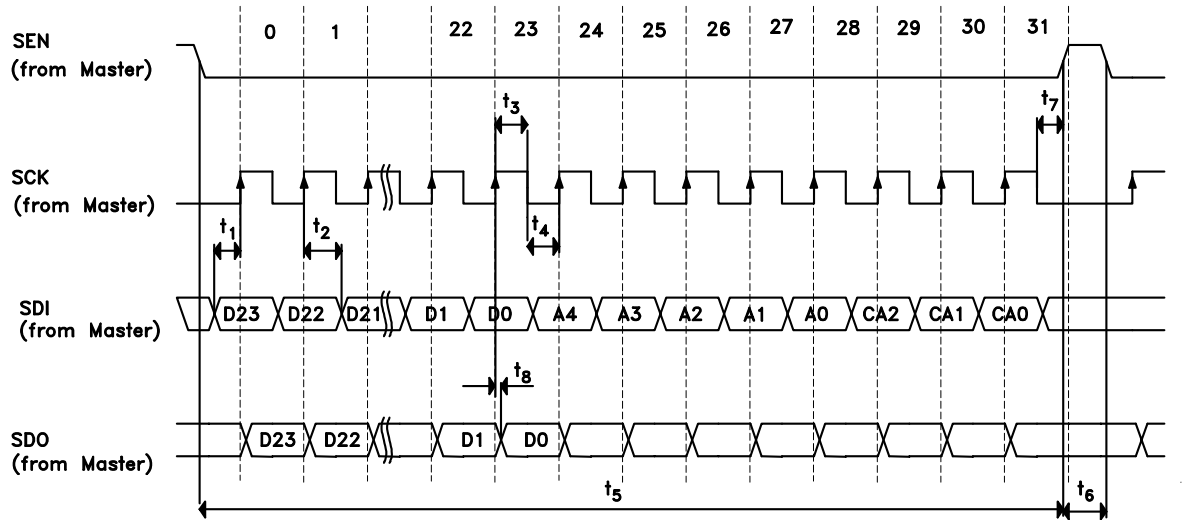


Figure 23. SPI Timing Diagram

Table 11. Main SPI Timing Characteristics

DVDD = 5V ±5%, GND = 0V

Parameter	Conditions	Min	Typ	Max	Units
t_1	SDI to SCK Setup Time	8			nsec
t_2	SDI to SCK Hold Time	8			nsec
t_3	SCK High Duration [a]	10			nsec
t_4	SCK Low Duration	10			nsec
t_5	SEN Low Duration	20			nsec
t_6	SEN High Duration	20			nsec
t_7	SCK to SEN [b]	8			nsec
t_8	SCK to SDO Out[c]			8	nsec

a. The SPI is relative insensitive to the duty cycle of SCK.

b. SEN must rise after the 32nd falling edge of SCK but before the next rising SCK edge. If SCK is shared amongst several devices this timing must be respected.

c. Typical load to SDO 10pF, max 20pF

Built In Self Test (RC-BIST)

The HMC900LP5E RC Calibration state machine features built in self test (RC-BIST) to facilitate improved device testing.

The RC-BIST can be exercised as follows:

1. apply reset to the chip via a power cycle (hard reset) or via the SPI (soft reset). Soft reset is accomplished by writing 20h to Reg 0h followed by writing 00h to Reg 0h.
2. setup the RCCAL input parameters if desired. Note that the RC-BIST will work with the default settings from power up however test coverage will improve if the following SPI registers are also accessed:
   a. program the RC clock period (Reg 05h).
   b. program the measurement adjustment setting (Reg 06h).
   c. program the threshold adjustment settings.
3. enable BIST mode (Reg 0Eh).
4. start the BIST by writing any data to the BIST strobe register (Reg 04h). Note that the BIST will take 2^18 ~ 260k clock cycles to complete.
5. read the result of the BIST test. Read the value in the BIST Out register (Reg 0F). Bit 16 is the busy flag and will be set when the BIST is still running. When this bit is reset then the BIST output value in bits 15:0 are valid.

   Note that the value of the BIST output must be compared to the expected result depending on values programmed into the registers in step 2.

The BIST procedure can be repeated as desired to ensure adequate test coverage for the RC Calibration engine. The suggested register settings to maximize test coverage with BIST is provided below.

Table 12. Test Conditions

Register Settings	Expected Result
Reg 05h[14:0]=65, Reg 06h[8:0]=255, Reg10h[4:0] to eg1Ah[4:0]=0d or 0h	Reg 0Fh[15:0]=36092, Reg 09h[23:0]=14942167
Reg 05h[14:0]=32702, Reg 06h[8:0]=36, Reg10h[4:0] to Reg1Ah[4:0]=31d or 1Fh	Reg 0Fh[15:0]=55027, Reg 09h[23:0]=14143649
Reg 05h[14:0]=10922, Reg 06h[8:0]=170, Reg10h[4:0] to Reg1Ah[4:0]=10d or Ah	Reg 0Fh[15:0]=28618, Reg 09h[23:0]=8907563
Reg 05h[14:0]=21845, Reg06h[8:0]=853, Reg10h[4:0] to Reg1Ah[4:0]=21d or 15h	Reg oFg[15:0]=16368, Reg 09h[23:0]=3396981

Register Map

Table 13. Reg 01h - Enable

Bit	Name	Width	Default	Description
[0]	OTP_DontUse	1	0	Default use stored OTP values (only if OTP is programmed)
[1]	cal_enable	1	0	Enable RC Calibration circuit
[2]	filter_I_enable	1	1	Enable I channel gain stage, filter, and driver
[3]	filter_Q_enable	1	1	Enable Q channel gain stage, filter, and driver
[4]	force_cal_code	1	0	Force calibration setting to use SPI values (Reg 03h - Calibration)
[5]	doubler_enable	1	0	0-- Doubler Disabled. RC Calibration clock 40 MHz<RC calibration clock<80 MHz 1 -- Doubler Enabled. RC Calibration clock 20 MHz<RC calibration clock<40 MHz Note: calibration clock duty cycle must be within 50% +/- 10%
[9:6]	reserved	4	0000	
[23:10]	unused			

Table 14. Reg 02h - Settings

Bit	Name	Width	Default	Description
[1:0]	opamp_bias[1:0]	2	01	Opamp bias setting. 00 -- min bias 11 -- max bias opamp_bias[1:0]=01 standard bias (characterized value) opamp_bias[1:0]=10 high linearity bias
[3:2]	drvr_bias[1:0]	2	10	Driver bias setting. 00 -- min bias 11 -- max bias drvr_bias[1:0]=10 standard bias (characterized value)
[4]	gain_10dB	1	0	VGA gain setting. 0: 0dB VGA gain 1: 10dB VGA gain
[5]	bypass_filter	1	0	Filter bypass setting. 0: Filter bypass disabled 1: Filter bypass enabled
[9:6]	coarse_bandwidth_code[3:0]	4	0000	Sets filter coarse tuning range 0000 - 3.5 MHz 0001 - 5 MHz 0010 - 7 MHz 0011 - 10 MHz 0100 -14 MHz 0101 - 20 MHz 0110 - 28 MHz 0111 - 35 MHz 1000 - 50 MHz
[10]	reserved	1	0	
[23:11]	unused			

Table 15. Reg 03h - Calibration

Bit	Name	Width	Default	Description
[3:0]	fine_bandwidth_code[3:0]	4	0000	fine bandwidth setting override bits (register 01 bit 4, force_cal_code, must be set). 0000 - Minimum frequency 0001 0010 0011 0100 0101 0110 0111 1000 1001 1010 1011 - Maximum frequency
[23:4]	unused			

Table 16. Reg 04h - Calibration/RC-BIST Strobe

Calibration strobe register is used only to initialize a calibration cycle. Writing any value to this register serves to request a new calibration cycle.

Note that this register is also used to start the Built In Self Test (RC-BIST) mode and this is used to test the fault coverage of the RC calibration engine.

Bit	Name	Width	Default	Description
[23:0]	Request calibration	1	0	Writing to any bit in this register starts a calibration cycle.

Table 17. Reg 05h - Clk Period

Bit	Name	Width	Default	Description
[14:0]	clock_period[14:0]	15	0000h	Sets the clock period for the RC calibration circuit. Clock period entered is in pico seconds. i.e. 1/40 MHz clock =25000ps= 110000110101000b=61A8h
[23:15]	unused			

Table 18. Reg 06h - Measure Adjust

Correction value used to adjust RC Calibration result. Value is in 1.024ns increments.

Bit	Name	Width	Default	Description
[8:0]	meas_adj[8:0]	9	000h	Correction value to ADD to counter output before counter is decoded for calibration setting. Number is in 2's complement format. Note this applies to all settings universally.
[23:9]	unused			

Table 19. Reg 07h Unused

Table 20. Reg 08h - Calibration Status (read only)

Bit	Name	Width	Default	Description
[3:0]	fine_bandwidth_code[3:0]	4	0000	fine_bandwidth_setting (must run a calibration cycle to get valid data) Valid states are 0000 to 1011 (see Table 3. Reg 03h - Calibration)
[4]	cal_busy	1		Calibration active flag
[5]	OPT _write_busy	1		OTP write active flag
[23:6]	unused			

Table 21. Reg 09h - Calibration Count (read-only)

Bit	Name	Width	Default	Description
[23:0]	count_read[23:0]	24		Output of calibration counter in pico seconds (unadjusted)

Table 22. Reg 0Ah - OTP Values (read-only)

Bit	Name	Width	Default	Description
[3:0]	OTP_fine_bandwidth_ code[3:0]	4		Non volatile fine_bandwidth_code[3:0]. Definition is same as per “Reg 03h - Calibration”
[6:4]	OTP_course_bandwidth_ code[2:0]	3		Non volatile version of SPI values found in “Reg 02h - Settings”
[7]	OTP_Gain_10dB	1		
[8]	OTP_bypass_filter	1		
[10:9]	OTP_opamp_bias[1:0]	2		
[12:11]	OTP_drvr_bias[1:0]	2		
[13]	OTP_prg_flag	1		This flag must be set if the OTP values are to be used and must be set by the user. If not set, this flag overrides bit 0 of Reg 01h.
[14]	OTP_Coarse_Bandwidth[3]			Non volatile version of SPI values found in Reg 02h - Settings
[15]	reserved			reserved
[23:16]	unused			

Table 23. Reg 0Bh - OTP Write Enable

Bit	Name	Width	Default	Description
[0]	EFR_Write_enable	1	0	Enables OTP Programming
[23:1]	unused			

Table 24. Reg 0Ch - OTP Write

OTP address register is used in programming of OTP.

Bit	Name	Width	Default	Description
[3:0]	OTP Address	4	0	Address of OTP bit to be set
[23:4]	unused			

Table 25. Reg 0Dh - OTP Write Pulse

OTP strobe register is used in programming of OTP.

Bit	Name	Width	Default	Description
[23:0]	reserved	1	0	reserved

Table 26. Reg 0Eh - RC-BIST Enable

Bit	Name	Width	Default	Description
[0]	enable_RCBIST_mode	1	0	RC-BIST mode enable
[23:1]	unused			

Table 27. Reg 0Fh - RC-BIST Out

Bit	Name	Width	Default	Description
[15:0]	crc_BIST[15:0]	16	0	RC-BIST CRC check result
[16]	crc_RC-BIST_busy_flag	1	0	RC-BIST busy flag. Indicates that BIST cycle is not completed and data crc_ BIST[15:0] is invalid
[23:17]	unused			

Table 28. Reg 10h to Reg1A - Window Threshold

OTP strobe register is used in programming of OTP.

Bit	Name	Width	Default	Description
[23:0]	reserved			reserved