

Ultra Low Power Stereo Audio Codec With Embedded miniDSP

Check for Samples: [TLV320AIC3253](#)

FEATURES

- Stereo Audio DAC with 100dB SNR
- 4.1mW Stereo 48ksps Playback
- PowerTune™
- Extensive Signal Processing Options
- Embedded miniDSP
- Stereo Digital Microphone Input
- Stereo Headphone Outputs
- Low Power Analog Bypass Mode
- Programmable PLL
- Integrated LDO
- 2.7mm × 2.7mm WCSP or 4mm × 4mm QFN Package

APPLICATIONS

- Mobile Handsets
- Communication
- Portable Computing

DESCRIPTION

The TLV320AIC3253 (sometimes referred to as the AIC3253) is a flexible, low-power, low-voltage stereo audio codec with digital microphone inputs and programmable outputs, PowerTune capabilities, fully-programmable miniDSP, fixed predefined and parameterizable signal processing blocks, integrated PLL, integrated LDO and flexible digital interfaces. Extensive register-based control of power, input/output channel configuration, gains, effects, effects, pin-multiplexing and clocks is included, allowing the device to be precisely targeted to its application.

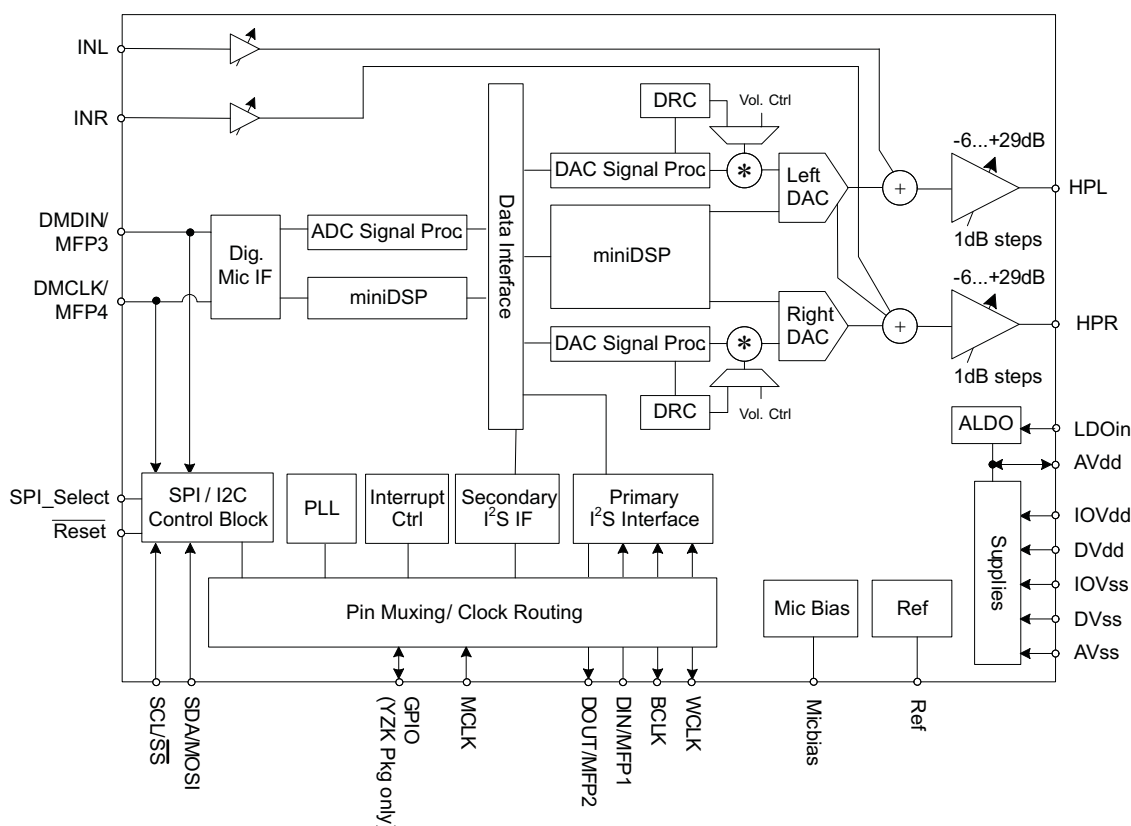


Figure 1. Simplified Block Diagram



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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

DESCRIPTION (CONTINUED)

Combined with the advanced PowerTune technology, the device can cover operations from 8kHz mono voice playback to stereo 192kHz DAC playback, making it ideal for portable battery-powered audio and telephony applications.

The record path of the TLV320AIC3253 consists of a stereo digital microphone PDM interface (not available when using SPI control interface) typically used at 64Fs or 128Fs.

The playback path offers signal processing blocks for filtering and effects, true differential output signal, flexible mixing of DAC and analog input signals as well as programmable volume controls. The TLV320AIC3253 contains two high-power output drivers which can be configured in multiple ways, including stereo, and mono BTL. The integrated PowerTune technology allows the device to be tuned to just the right power-performance trade-off. Mobile applications frequently have multiple use cases requiring very low-power operation while being used in a mobile environment. When used in a docked environment power consumption typically is less of a concern while lowest possible noise is important. With PowerTune the TLV320AIC3253 can address both cases.

The voltage supply range for the TLV320AIC3253 for analog is 1.5V–1.95V, and for digital it is 1.26V–1.95V. To ease system-level design, a low-dropout regulator (LDO) is integrated to generate the appropriate analog supply from input voltages ranging from 1.8V to 3.6V. Digital I/O voltages are supported in the range of 1.1V–3.6V.

The required internal clock of the TLV320AIC3253 can be derived from multiple sources, including the MCLK pin, the BCLK pin, the GPIO pin or the output of the internal PLL, where the input to the PLL again can be derived from the MCLK pin, the BCLK or GPIO pins. Although using the internal, fractional PLL ensures the availability of a suitable clock signal, it is not recommended for the lowest power settings. The PLL is highly programmable and can accept available input clocks in the range of 512kHz to 50MHz.

The device is available in the 2.7mm × 2.7mm WCSP or the 4mm × 4mm QFN package.

Package and Signal Descriptions

Packaging/Ordering Information

PRODUCT	PACKAGE	PACKAGE DESIGNATOR	OPERATING TEMPERATURE RANGE	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
TLV320AIC3253	S-XBGA-N25	YZK	-40°C to 85°C	TLV320AIC3253IYZKT	Tape and Reel, 250
				TLV320AIC3253IYZKR	Tape and Reel, 3000
	S-PQFP-N	RGE	-40°C to 85°C	TLV320AIC3253IRGET	Tape and Reel, 250
				TLV320AIC3253IRGER	Tape and Reel, 3000

Pin Assignments

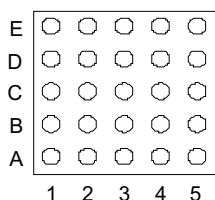


Figure 2. S-XBGA-N25 (YZK) Package, Bottom View

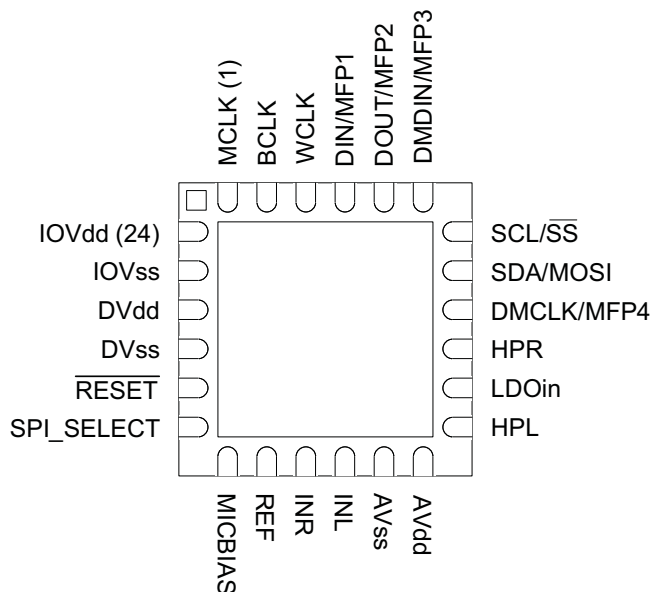


Figure 3. S-PQFP-N (RGE) Package, Bottom View

TERMINAL FUNCTIONS

TERMINAL		NAME	TYPE	DESCRIPTION
QFN PIN	WCSP BALL			
1	A1	MCLK	I	Master Clock Input
2	B2	BCLK	IO	Audio serial data bus (primary) bit clock
3	B3	WCLK	IO	Audio serial data bus (primary) word clock
4	A2	DIN/MFP1	I	Primary function Audio serial data bus data input Secondary function Digital Microphone Input General Purpose Input
5	A3	DOU/MFP2	O	Primary Audio serial data bus data output Secondary General Purpose Output Clock Output INT1 Output INT2 Output Audio serial data bus (secondary) bit clock output Audio serial data bus (secondary) word clock output
6	A5	DMDIN/ MFP3/ SCLK	I	Primary (SPI_Select = 1) SPI serial clock Secondary: (SPI_Select = 0) Digital microphone input Headset detect input Audio serial data bus (secondary) bit clock input Audio serial data bus (secondary) DAC/common word clock input Audio serial data bus (secondary) ADC word clock input Audio serial data bus (secondary) data input General Purpose Input
7	A4	SCL/ SS	I	I ² C interface serial clock (SPI_Select = 0) SPI interface mode chip-select signal (SPI_Select = 1)
8	B4	SDA/ MOSI	I	I ² C interface mode serial data input (SPI_Select = 0) SPI interface mode serial data input (SPI_Select = 1)
9	B5	DMCLK/ MFP4/ MISO	O	Primary (SPI_Select = 1) Serial data output Secondary (SPI_Select = 0) Multifunction pin #4 (MFP4) options are only available using I ² C Digital microphone clock output General purpose output CLKOUT output INT1 output INT2 output Audio serial data bus (primary) ADC word clock output Audio serial data bus (secondary) data output Audio serial data bus (secondary) bit clock output Audio serial data bus (secondary) word clock output
10	C5	HPR	O	Right high-power output driver
11	D5	LDOIN/ HPVDD	Power	LDO Input supply and Headphone Power supply 1.9V– 3.6V
12	D4	HPL	O	Left high power output driver

- (1) For multiple BGA Balls assigned to the same pin-name, it is **necessary** to connect them on the PCB.
 (2) For multiple BGA Balls assigned to the same pin-name, it is **recommended** to connect them on the PCB.

TERMINAL FUNCTIONS (continued)

TERMINAL		NAME	TYPE	DESCRIPTION
QFN PIN	WCSP BALL			
13	D3	AVDD	Power	Analog voltage supply 1.5V–1.95V Input when A-LDO disabled, Filtering output when A-LDO enabled
14	E4	AVSS	Ground	Analog ground supply
15	E5	INL	I	Left Analog Bypass Input
16	E3	INR	I	Right Analog Bypass Input
17	E2	REF	O	Reference voltage output for filtering
18	D2	MICBIAS	O	Microphone bias voltage output
19	E1	SPI_SELECT	I	Control mode select pin (1 = SPI, 0 = I2C)
20	C2	RESET	I	Reset (active low)
21	D1	DVSS	Ground	Digital Ground and Chip-substrate
22	C1	DVDD	Power	Digital voltage supply 1.26V–1.95V
23	B1	IOVSS	Ground	I/O ground supply
24	C3	IOVDD	Power	I/O voltage supply 1.1V – 3.6V
n/a	C4	GPIO/MFP5	I	Primary General Purpose digital IO Secondary CLKOUT Output INT1 Output INT2 Output Audio serial data bus ADC word clock output Audio serial data bus (secondary) bit clock output Audio serial data bus (secondary) word clock output Digital microphone clock output

Electrical Characteristics

Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) ⁽¹⁾

		VALUE	UNIT
AVdd to AVss		-0.3 to 2.2	V
DVdd to DVss		-0.3 to 2.2	V
IOVDD to IOVSS		-0.3 to 3.9	V
LDOIN to AVss		-0.3 to 3.9	V
Digital Input voltage		-0.3 to IOVDD + 0.3	V
Analog input voltage		-0.3 to AVdd + 0.3	V
Operating temperature range		-40 to 85	°C
Storage temperature range		-55 to 125	°C
Junction temperature (T _J Max)		105	°C
S-XBGA NanoFree package (YZK)	Power dissipation	(T _J Max - TA) / θ _{JA}	W
	θ _{JA} Thermal impedance	48	C/W

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

Recommended Operating Conditions

			MIN	NOM	MAX	UNIT	
LDOIN ⁽¹⁾	Power Supply Voltage Range	Referenced to AVss ⁽²⁾	1.9		3.6	V	
AVdd			1.5	1.8	1.95		
IOVDD		Referenced to IOVSS ⁽²⁾	1.1		3.6		
DVdd			Referenced to DVss ⁽²⁾	1.65	1.8		1.95
DVdd ⁽³⁾				1.26	1.8		1.95
PLL Input Frequency		Clock divider uses fractional divide (D > 0), P=1, D _{Vdd} ≥ 1.65V (See table in SLAU303, <i>Maximum TLV320AIC3253 Clock Frequencies</i>)	10		20	MHz	
		Clock divider uses integer divide (D = 0), P=1, D _{Vdd} ≥ 1.65V (Refer to table in SLAU303, <i>Maximum TLV320AIC3253 Clock Frequencies</i>)	0.512		20	MHz	
MCLK	Master Clock Frequency	MCLK; Master Clock Frequency; D _{Vdd} ≥ 1.65V			50	MHz	
SCL	SCL Clock Frequency				400	kHz	
HPL, HPR	Stereo headphone output load resistance	Single-ended configuration	14.4	16		Ω	
	Headphone output load resistance	Differential configuration	24.4	32		Ω	
C _{Lout}	Digital output load capacitance			10		pF	
C _{ref}	Reference decoupling capacitor ⁽⁴⁾		1	10		μF	

(1) Minimum spec applies if LDO is used. Minimum is 1.5V if LDO is not enabled. Using the LDO below 1.9V degrades LDO performance.

(2) All grounds on board are tied together, so they should not differ in voltage by more than 0.2V max, for any combination of ground signals.

(3) At DVdd values lower than 1.65V, the PLL does not function. Please see table in SLAU303, *Maximum TLV320AIC3253 Clock Frequencies* for details on maximum clock frequencies.

(4) For C_{ref} < 10μF, performance may decrease. Electrical characteristics are based on C_{ref}=10μF.

Electrical Characteristics, Bypass Outputs

At 25°C, AVdd, DVdd, IOVDD = 1.8V, LDO_in = 1.8V, AVdd LDO disabled, f_s (Audio) = 48kHz, Cref = 10 μF on REF PIN, PLL disabled unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
ANALOG BYPASS TO HEADPHONE AMPLIFIER, DIRECT MODE					
Device Setup	Load = 16Ω (single-ended), 50pF; Input and Output CM=0.9V; Headphone Output on LDOIN Supply; INL routed to HPL and INR routed to HPR; Channel Gain=0dB				
Gain Error			±0.4		dB
Noise, A-weighted ⁽¹⁾	Idle Channel, INL and INR ac-shortened to ground		3		μV _{RMS}
THD Total Harmonic Distortion	446mVrms, 1-kHz input signal		-82		dB

(1) All performance measurements done with 20-kHz low-pass filter and, where noted, A-weighted filter. Failure to use such a filter may result in higher THD+N and lower SNR and dynamic range readings than shown in the Electrical Characteristics. The low-pass filter removes out-of-band noise, which, although not audible, may affect dynamic specification values

Electrical Characteristics, Microphone Interface

At 25°C, AVdd, DVdd, IOVDD = 1.8V, LDO_in = 1.8V, AVdd LDO disabled, Cref = 10 μF on REF PIN, PLL disabled unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
MICROPHONE BIAS					
Bias voltage	Bias voltage CM=0.9V, LDOin = 3.3V, no load				
	Micbias Mode 0, Connect to AVdd or LDOin		1.25		V
	Micbias Mode 1, Connect to LDOin		1.7		V
	Micbias Mode 2, Connect to LDOin		2.5		V
	Micbias Mode 3, Connect to AVdd		AVdd		V
	Micbias Mode 3, Connect to LDOin		LDOin		V
	CM=0.75V, LDOin = 3.3V				
	Micbias Mode 0, Connect to AVdd or LDOin		1.04		V
	Micbias Mode 1, Connect to AVdd or LDOin		1.42		V
	Micbias Mode 2, Connect to LDOin		2.08		V
	Micbias Mode 3, Connect to AVdd		AVdd		V
	Micbias Mode 3, Connect to LDOin		LDOin		V
Output Noise	CM=0.9V, Micbias Mode 2, A-weighted, 20Hz to 20kHz bandwidth, Current load = 0mA.		10		μV _{RMS}
Current Sourcing	Micbias Mode 2, Connect to LDOin		3		mA
Inline Resistance	Micbias Mode 3, Connect to AVdd		160		Ω
	Micbias Mode 3, Connect to LDOin		110		

Electrical Characteristics, Audio Outputs

At 25°C, AVdd, DVdd, IOVDD = 1.8V, LDO_in = 1.8V, AVdd LDO disabled, f_s (Audio) = 48kHz, Cref = 10 μ F on REF PIN, PLL disabled unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Audio DAC – Stereo Single-Ended Headphone Output						
Device Setup		Load = 16 Ω (single-ended), 50pF Headphone Output on AVdd Supply, Input & Output CM=0.9V, DOSR = 128, MCLK=256* f_s , Channel Gain=0dB word length = 16 bits; Processing Block = PRB_P1 Power Tune = PTM_P3				
Full scale output voltage (0dB)				0.5		V _{RMS}
SNR	Signal-to-noise ratio, A-weighted ^{(1) (2)}	All zeros fed to DAC input, modulator in excited state	88	100		dB
DR	Dynamic range, A-weighted ^{(1) (2)}	-60dB 1kHz input full-scale signal, Word Length = 20 bits, Power Tune = PTM_P4		99		dB
THD+N	Total Harmonic Distortion plus Noise	-3dB full-scale, 1-kHz input signal		-80	-70	dB
DAC Gain Error		0dB, 1kHz input full scale signal		\pm 0.1		dB
DAC Mute Attenuation		Mute		127		dB
DAC channel separation		-1dB, 1kHz signal, between left and right HP out		92		dB
DAC PSRR		100mVpp, 1kHz signal applied to AVdd		70		dB
		100mVpp, 217Hz signal applied to AVdd		75		dB
Power Delivered		R _L =16 Ω , Output Stage on AVdd = 1.8V THDN < 1%, Input CM=0.9V, Output CM=0.9V, Channel Gain=2dB		13		mW
		R _L =16 Ω Output Stage on LDOIN = 3.3V, THDN < 1% Input CM=0.9V, Output CM=1.65V, Channel Gain=8dB		47		
Audio DAC – Stereo Single-Ended Headphone Output						
Device Setup		Load = 16 Ω (single-ended), 50pF, Headphone Output on AVdd Supply, Input & Output CM=0.75V; AVdd=1.5V, DOSR = 128, MCLK=256* f_s , Channel Gain = -2dB, word length=20-bits; Processing Block = PRB_P1, Power Tune = PTM_P4				
Full scale output voltage (0dB)				0.375		V _{RMS}
SNR	Signal-to-noise ratio, A-weighted ^{(1) (2)}	All zeros fed to DAC input, modulator in excited state		99		dB
DR	Dynamic range, A-weighted ^{(1) (2)}	-60dB 1 kHz input full-scale signal		98		dB
THD+N	Total Harmonic Distortion plus Noise	-3dB full-scale, 1-kHz input signal		-84		dB
Audio DAC – Mono Differential Headphone Output						

(1) Ratio of output level with 1-kHz full-scale sine wave input, to the output level with the inputs short circuited, measured A-weighted over a 20-Hz to 20-kHz bandwidth using an audio analyzer.

(2) All performance measurements done with 20-kHz low-pass filter and, where noted, A-weighted filter. Failure to use such a filter may result in higher THD+N and lower SNR and dynamic range readings than shown in the Electrical Characteristics. The low-pass filter removes out-of-band noise, which, although not audible, may affect dynamic specification values

Electrical Characteristics, Audio Outputs (continued)

At 25°C, AVdd, DVdd, IOVDD = 1.8V, LDO_in = 1.8V, AVdd LDO disabled, f_s (Audio) = 48kHz, C_{ref} = 10 μF on REF PIN, PLL disabled unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Device Setup	Load = 32 Ω (differential), 50pF, Headphone Output on LDOIN Supply Input CM = 0.75V, Output CM=1.5V, AVdd=1.8V, LDOIN=3.0V, DOSR = 128 MCLK=256* f _s , Channel (headphone driver) Gain = 5dB for full scale output signal, word length=16-bits, Processing Block = PRB_P1, Power Tune = PTM_P3				
Full scale output voltage (0dB)			1778		mV _{RMS}
SNR	Signal-to-noise ratio, A-weighted ^{(1) (2)}		101		dB
DR	Dynamic range, A-weighted ^{(1) (2)}		98		dB
THD	Total Harmonic Distortion		-82		dB
Power Delivered	R _L =32Ω, Output Stage on LDOIN = 3.3V, THDN < 1%, Input CM=0.9V, Output CM=1.65V, Channel Gain=8dB		125		mW
	R _L =32Ω Output Stage on LDOIN = 3.0V, THDN < 1% Input CM=0.9V, Output CM=1.5V, Channel Gain=8dB		103		mW

Electrical Characteristics, LDO

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
LOW DROPOUT REGULATOR (AVdd)					
Output Voltage	LDOmode = 1, LDOin > 1.95V, I _O = 15mA		1.63		V
	LDOmode = 0, LDOin > 2.0V, I _O = 15mA		1.68		
	LDOmode = 2, LDOin > 2.05V, I _O = 15mA		1.73		
Output Voltage Accuracy			±2		%
Load Regulation	Load current range 0 to 50mA		26		mV
Line Regulation	Input Supply Range 1.9V to 3.6V		3		mV
Decoupling Capacitor		1			μF
Bias Current			50		μA

Electrical Characteristics, Misc.

At 25°C, AVdd, DVdd, IOVDD = 1.8V, LDO_in = 3.3V, AVdd LDO disabled, f_s (Audio) = 48kHz, C_{ref} = 10 μF on REF PIN, PLL disabled unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
REFERENCE					
Reference Voltage Settings	CMMode = 0 (0.9V)		0.9		V
	CMMode = 1 (0.75V)		0.75		
Reference Noise	CM=0.9V, A-weighted, 20Hz to 20kHz bandwidth, C _{ref} = 10μF		1		μV _{RfMS}
Decoupling Capacitor		1	10		μF
Bias Current			120		μA
miniDSP					
Maximum miniDSP clock frequency - ADC	DVdd = 1.65V		55.3		MHz
Maximum miniDSP clock frequency - DAC	DVdd = 1.65V		55.3		MHz

Electrical Characteristics, Misc. (continued)

At 25°C, AVdd, DVdd, IOVDD = 1.8V, LDO_in = 3.3V, AVdd LDO disabled, f_s (Audio) = 48kHz, Cref = 10 μF on REF PIN, PLL disabled unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Shutdown Current					
Device Setup	Coarse AVdd supply turned off, LDO_select held at ground, No external digital input is toggled				
I _{DVdd}			1.4		μA
I _{AVdd}			1		
I _{LDOin}			1		
I _{IOVDD}			<0.1		

Electrical Characteristics, Logic Levels

At 25°C, AVdd, DVdd, IOVDD = 1.8V

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
LOGIC FAMILY					
CMOS					
V _{IH}	Logic Level	I _{IH} = 5 μA, IOVDD > 1.6V	0.7 × IOVDD		V
		I _{IH} = 5 μA, 1.2V ≤ IOVDD < 1.6V	0.9 × IOVDD		V
		I _{IH} = 5 μA, IOVDD < 1.2V	IOVDD		V
V _{IL}	Logic Level	I _{IL} = 5 μA, IOVDD > 1.6V	-0.3	0.3 × IOVDD	V
		I _{IL} = 5 μA, 1.2V ≤ IOVDD < 1.6V		0.1 × IOVDD	V
		I _{IL} = 5 μA, IOVDD < 1.2V		0	V
V _{OH}	I _{OH} = 2 TTL loads	0.8 × IOVDD		V	
V _{OL}	I _{OL} = 2 TTL loads		0.1 × IOVDD	V	
Capacitive Load			10		pF

Interface Timing

Typical Timing Characteristics — Audio Data Serial Interface Timing (I²S)

All specifications at 25°C, DVdd = 1.8V

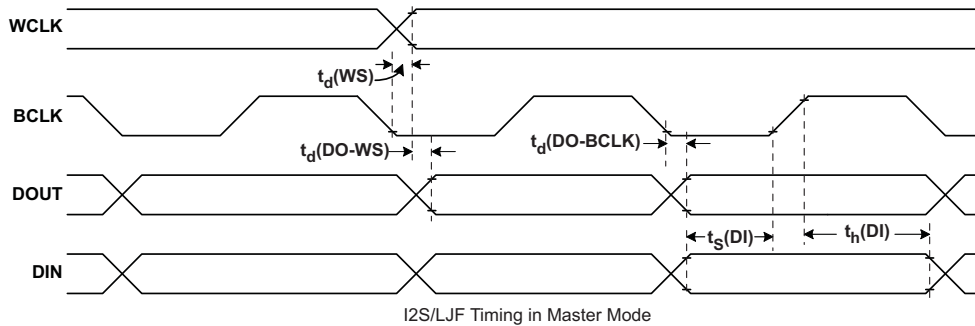


Figure 4. I²S/LJF/RJF Timing in Master Mode

Table 1. I²S/LJF/RJF Timing in Master Mode (see Figure 4)

PARAMETER		IOVDD=1.8V		IOVDD=3.3V		UNITS
		MIN	MAX	MIN	MAX	
$t_d(WS)$	WCLK delay		30		20	ns
$t_d(DO-WS)$	WCLK to DOUT delay (For LJF Mode only)		50		25	ns
$t_d(DO-BCLK)$	BCLK to DOUT delay		50		25	ns
$t_s(DI)$	DIN setup	8		8		ns
$t_h(DI)$	DIN hold	8		8		ns
t_r	Rise time		24		12	ns
t_f	Fall time		24		15	ns

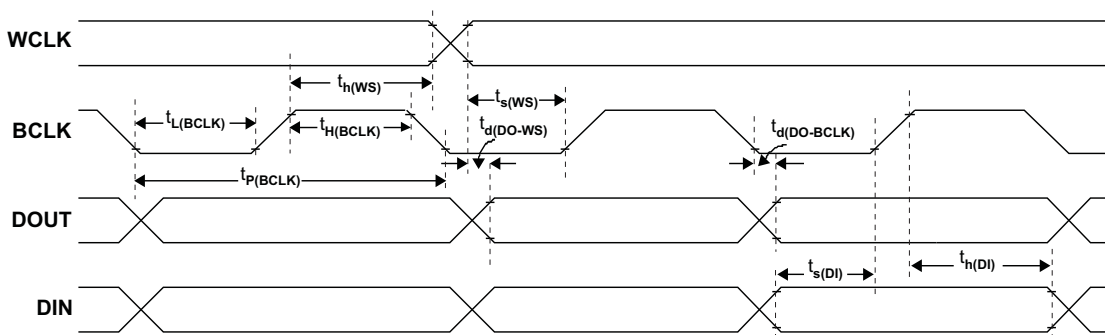


Figure 5. I²S/LJF/RJF Timing in Slave Mode

Table 2. I²S/LJF/RJF Timing in Slave Mode (see Figure 5)

PARAMETER		IOVDD=1.8V		IOVDD=3.3V		UNITS
		MIN	MAX	MIN	MAX	
t _H (BCLK)	BCLK high period	35		35		ns
t _L (BCLK)	BCLK low period	35		35		
t _s (WS)	WCLK setup	8		8		
t _h (WS)	WCLK hold	8		8		
t _d (DO-WS)	WCLK to DOUT delay (For LJF mode only)		50		25	
t _d (DO-BCLK)	BCLK to DOUT delay		50		25	
t _s (DI)	DIN setup	8		8		
t _h (DI)	DIN hold	8		8		
t _r	Rise time		4		4	
t _f	Fall time		4		4	

Typical DSP Timing Characteristics

All specifications at 25°C, DVdd = 1.8V

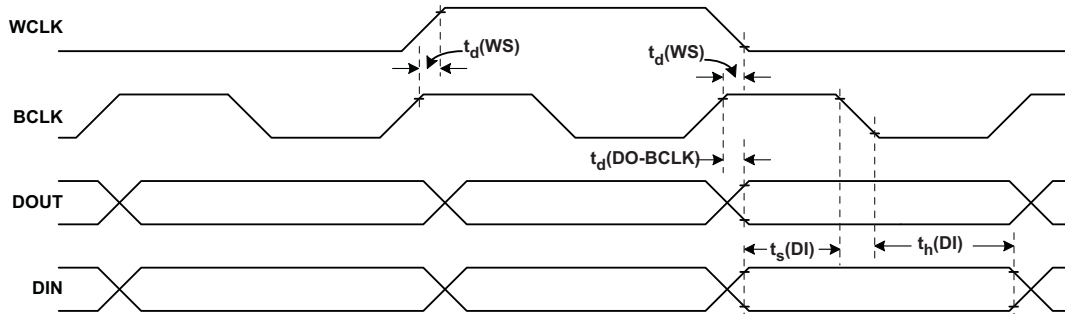


Figure 6. DSP Timing in Master Mode

Table 3. DSP Timing in Master Mode (see Figure 6)

PARAMETER		IOVDD=1.8V		IOVDD=3.3V		UNITS
		MIN	MAX	MIN	MAX	
$t_d(WS)$	WCLK delay		30		20	ns
$t_d(DO-BCLK)$	BCLK to DOUT delay		40		20	ns
$t_s(DI)$	DIN setup	8		8		ns
$t_h(DI)$	DIN hold	8		8		ns
t_r	Rise time		24		12	ns
t_f	Fall time		24		12	ns

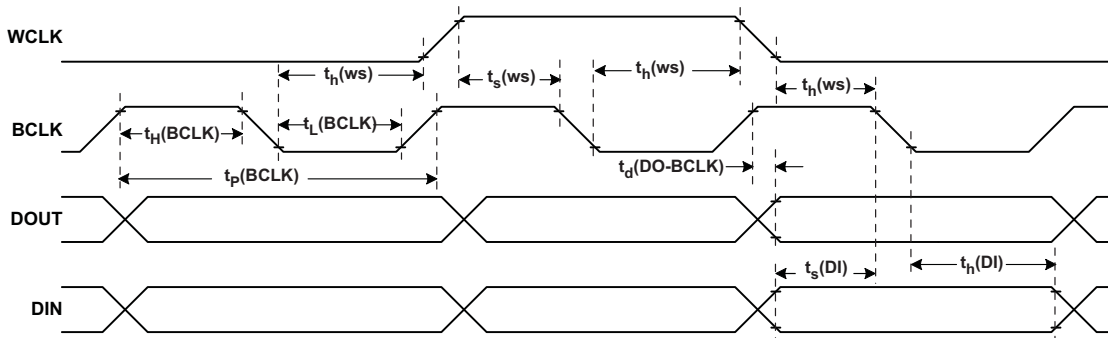


Figure 7. DSP Timing in Slave Mode

Table 4. DSP Timing in Slave Mode (see Figure 7)

PARAMETER		IOVDD=1.8V		IOVDD=3.3V		UNITS
		MIN	MAX	MIN	MAX	
$t_H(BCLK)$	BCLK high period	35		35		ns
$t_L(BCLK)$	BCLK low period	35		35		ns
$t_s(WS)$	WCLK setup	8		8		ns
$t_h(WS)$	WCLK hold	8		8		ns
$t_d(DO-BCLK)$	BCLK to DOUT delay		40		22	ns
$t_s(DI)$	DIN setup	8		8		ns
$t_h(DI)$	DIN hold	8		8		ns
t_r	Rise time		4		4	ns
t_f	Fall time		4		4	ns

I²C Interface Timing

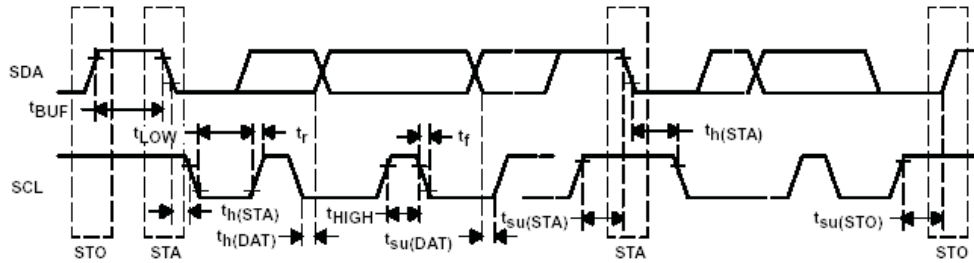


Figure 8.

Table 5. I²C Interface Timing

PARAMETER	TEST CONDITION	Standard-Mode			Fast-Mode			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
f _{SCL}	SCL clock frequency	0		100	0		400	kHz
t _{HD;STA}	Hold time (repeated) START condition. After this period, the first clock pulse is generated.	4.0			0.8			μs
t _{LOW}	LOW period of the SCL clock	4.7			1.3			μs
t _{HIGH}	HIGH period of the SCL clock	4.0			0.6			μs
t _{SU;STA}	Setup time for a repeated START condition	4.7			0.8			μs
t _{HD;DAT}	Data hold time: For I2C bus devices	0		3.45	0		0.9	μs
t _{SU;DAT}	Data set-up time	250			100			ns
t _r	SDA and SCL Rise Time			1000	20+0.1C _b		300	ns
t _f	SDA and SCL Fall Time			300	20+0.1C _b		300	ns
t _{SU;STO}	Set-up time for STOP condition	4.0			0.8			μs
t _{BUF}	Bus free time between a STOP and START condition	4.7			1.3			μs
C _b	Capacitive load for each bus line			400			400	pF

SPI Interface Timing

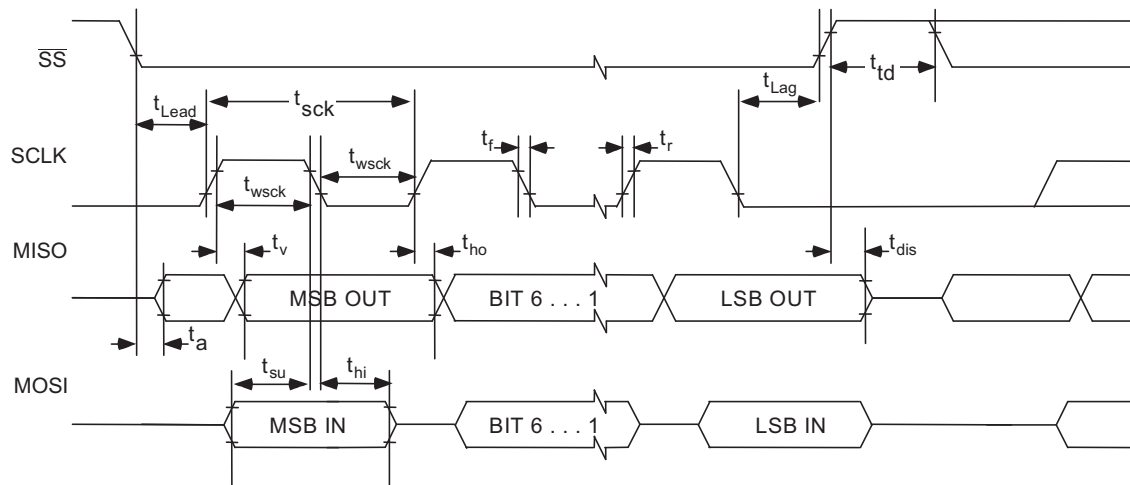


Figure 9. SPI Interface Timing Diagram

Timing Requirements (See Figure 9)

At 25°C, DVdd = 1.8V

Table 6. SPI Interface Timing

PARAMETER	TEST CONDITION	IOVDD=1.8V			IOVDD=3.3V			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
t _{sck}	SCLK Period	100			50			ns
t _{sckh}	SCLK Pulse width High	50			25			ns
t _{sckl}	SCLK Pulse width Low	50			25			ns
t _{lead}	Enable Lead Time	30			20			ns
t _{lag}	Enable Lag Time	30			20			ns
t _{d;seqxfr}	Sequential Transfer Delay	40			20			ns
t _a	Slave DOUT access time			40			20	ns
t _{dis}	Slave DOUT disable time			40			25	ns
t _{su}	DIN data setup time	15			10			ns
t _{h;DIN}	DIN data hold time	15			10			ns
t _{v;DOUT}	DOUT data valid time			45			25	ns
t _r	SCLK Rise Time			4			4	ns
t _f	SCLK Fall Time			4			4	ns

Typical Characteristics

Device Power Consumption

Device power consumption largely depends on PowerTune configuration. For information on device power consumption, see the *TLV320AIC3253 Application Reference Guide*, literature number SLAU303.

Typical Performance

TOTAL HARMONIC DISTORTION vs HEADPHONE OUTPUT POWER

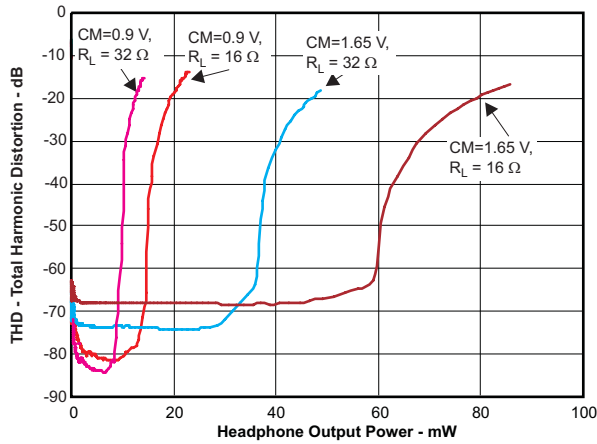


Figure 10.

TOTAL HARMONIC DISTORTION vs HEADPHONE OUTPUT POWER

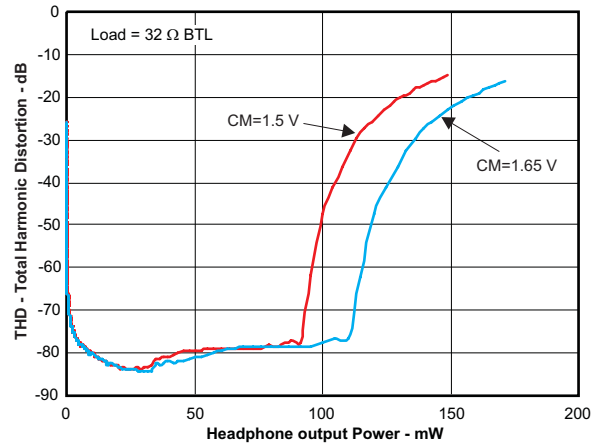


Figure 11.

HEADPHONE SNR AND SE OUTPUT POWER vs OUTPUT COMMON MODE SETTING

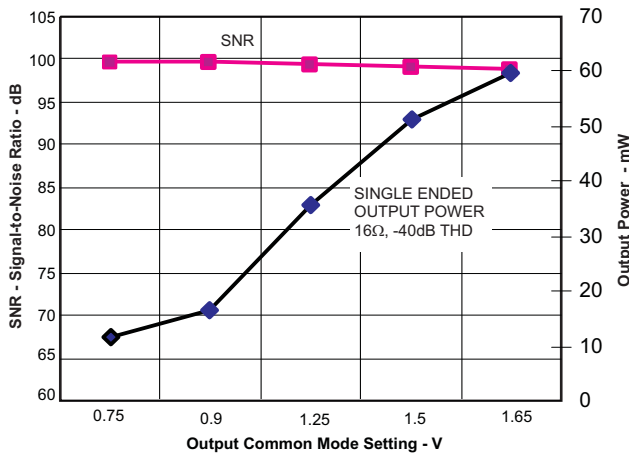


Figure 12.

LDO DROPOUT VOLTAGE vs LOAD CURRENT

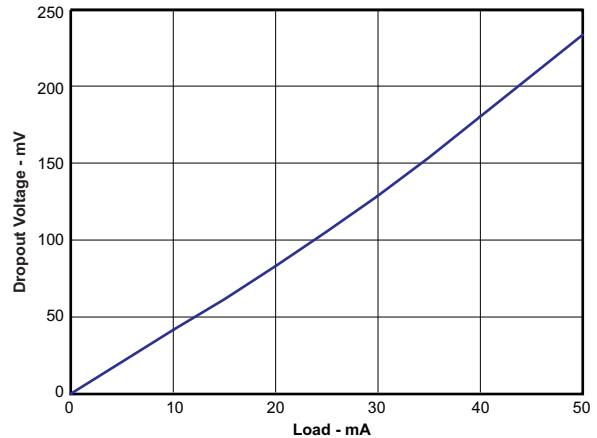


Figure 13.

LDO LOAD RESPONSE

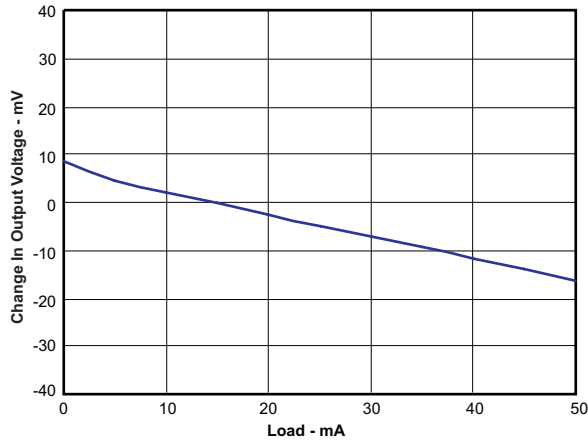


Figure 14.

MICBIAS MODE 2, CM = 0.9V, LDoin OP STAGE
vs
MICBIAS LOAD CURRENT

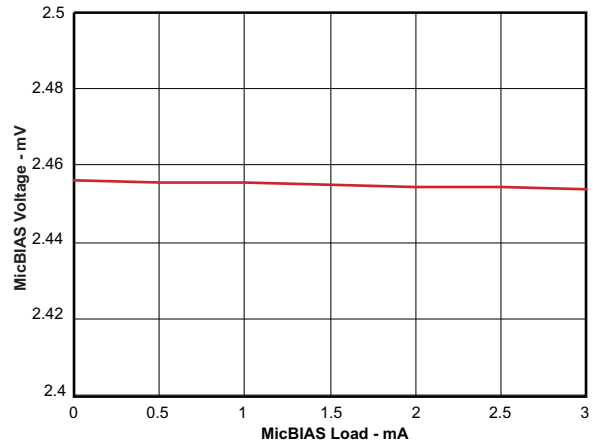


Figure 15.

FFT

DAC TO HEADPHONE FFT @ -3dBFS

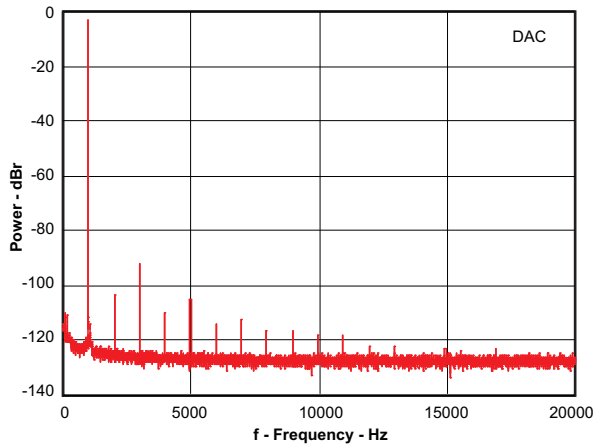


Figure 16.

ANALOG BYPASS TO HEADPHONE FFT @ -3dB BELOW
0.5Vrms

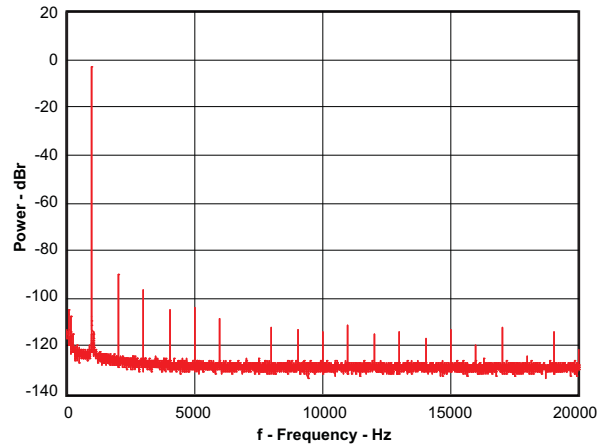


Figure 17.

Typical Circuit Configuration

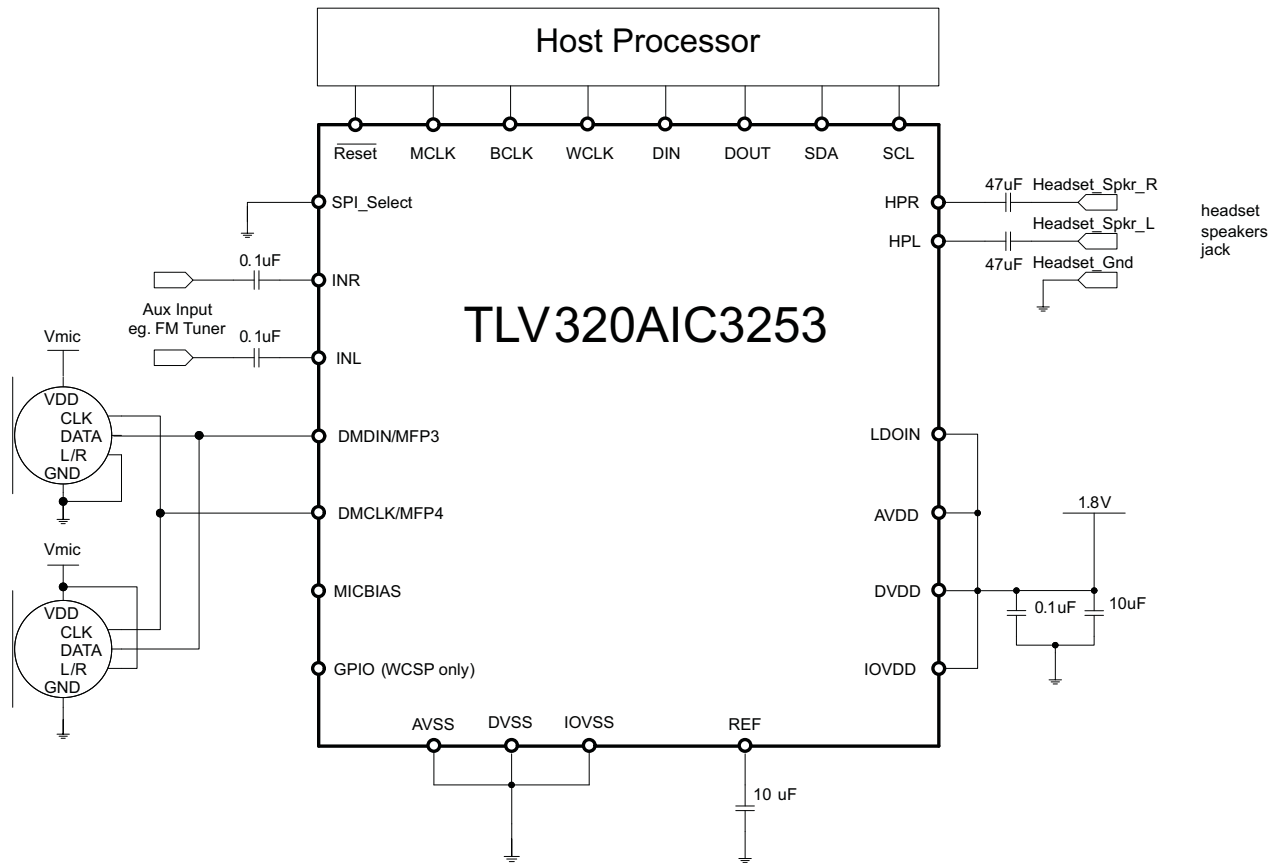


Figure 18. Typical Circuit Configuration

Application Overview

The TLV320AIC3253 offers a wide range of configuration options. [Figure 1](#) shows the basic functional blocks of the device.

Device Connections

Digital Pins

Only a small number of digital pins are dedicated to a single function; whenever possible, the digital pins have a default function, and also can be reprogrammed to cover alternative functions for various applications.

The fixed-function pins are Reset and the SPI_Select pin, which are HW control pins. Depending on the state of SPI_Select, the two control-bus pins SCL/SSZ and SDA/MOSI are configured for either I²C or SPI protocol.

Other digital IO pins can be configured for various functions via register control. An overview of available functionality is given in [Multifunction Pins](#).

Analog Pins

Analog functions can also be configured to a large degree. For minimum power consumption, analog blocks are powered down by default. The blocks can be powered up with fine granularity according to the application needs.

Multifunction Pins

Table 7 shows the possible allocation of pins for specific functions. The PLL input, for example, can be programmed to be any of 4 pins (MCLK, BCLK, DIN, GPIO).

Table 7. Multifunction Pin Assignments

		1	2	3	4	5	6	7	8
	Pin Function	MCLK	BCLK	WCLK	DIN MFP1	DOU MFP2	DMDIN/ MFP3/ SCLK	DMCLK/ MFP4/ MISO	GPIO MFP5
A	PLL Input	S ⁽¹⁾	S ⁽²⁾		E				S ⁽³⁾
B	Codec Clock Input	S ⁽¹⁾ , D ⁽⁴⁾	S ⁽²⁾						S ⁽³⁾
C	I ² S BCLK input		S ⁽²⁾ , D						
D	I ² S BCLK output		E ⁽⁵⁾						
E	I ² S WCLK input			E, D					
F	I ² S WCLK output			E					
G	I ² S ADC word clock input						E		E
H	I ² S ADC WCLK out							E	E
I	I ² S DIN				D				
J	I ² S DOU					E, D			
K	General Purpose Output I					E			
K	General Purpose Output II							E	
K	General Purpose Output III								E
L	General Purpose Input I				E				
L	General Purpose Input II						E		
L	General Purpose Input III								E
M	INT1 output					E		E	E
N	INT2 output					E		E	E
O	Digital Microphone Data Input				E		E		E
P	Digital Microphone Clock Output							E	E
Q	Secondary I ² S BCLK input						E		E
R	Secondary I ² S WCLK in						E		E
S	Secondary I ² S DIN						E		E
T	Secondary I ² S DOU							E	
U	Secondary I ² S BCLK OUT					E		E	E
V	Secondary I ² S WCLK OUT					E		E	E
W	Headset Detect Input						E		
X	Aux Clock Output					E		E	E

(1) S⁽¹⁾: The MCLK pin can be used to drive the PLL and Codec Clock inputs **simultaneously**

(2) S⁽²⁾: The BCLK pin can be used to drive the PLL and Codec Clock and audio interface bit clock inputs **simultaneously**

(3) S⁽⁴⁾: The GPIO/MFP5 pin can be used to drive the PLL and Codec Clock inputs simultaneously

(4) D: Default Function

(5) E: The pin is **exclusively** used for this function, no other function can be implemented with the same pin (e.g. if GPIO/MFP5 has been allocated for General Purpose Output, it cannot be used as the INT1 output at the same time)

Analog Audio I/O

The analog I/O path of the TLV320AIC3253 offers a variety of options for signal conditioning and routing:

- 2 headphone amplifier outputs
- Analog gain setting
- Single ended and differential modes

Analog Low Power Bypass

The TLV320AIC3253 offers an analog-bypass mode. An analog signal can be routed from the analog input pin to the output amplifier. Neither the digital-input processing blocks nor the DAC resources are required for such operation; this supports low-power operation during analog-bypass mode.

In analog low-power bypass mode, line-level signals can be routed directly from the analog inputs INL to the left headphone amplifier (HPL) and INR to HPR.

Headphone Outputs

The stereo headphone drivers on pins HPL and HPR can drive loads with impedances down to 16Ω in single-ended AC-coupled headphone configurations, or loads down to 32Ω in differential mode, where a speaker is connected between HPL and HPR. In single-ended drive configuration these drivers can drive up to 15mW power into each headphone channel while operating from 1.8V analog supplies. While running from the AVdd supply, the output common-mode of the headphone driver is set by the common-mode setting of analog inputs to allow maximum utilization of the analog supply range while simultaneously providing a higher output-voltage swing. In cases when higher output-voltage swing is required, the headphone amplifiers can run directly from the higher supply voltage on LDOIN input (up to 3.6V). To use the higher supply voltage for higher output signal swing, the output common-mode can be adjusted to either 1.25V, 1.5V or 1.65V. When the common-mode voltage is configured at 1.65V and LDOIN supply is 3.3V, the headphones can each deliver up to 40mW power into a 16Ω load.

The headphone drivers are capable of driving a mixed combination of DAC signal and bypass from analog input INL and INR. The analog input signals can be attenuated up to 72dB before routing. The level of the DAC signal can be controlled using the digital volume control of the DAC. To control the output-voltage swing of headphone drivers, the digital volume control provides a range of -6.0dB to $+29.0\text{dB}^{(6)}$ in steps of 1dB. These level controls are not meant to be used as dynamic volume control, but more to set output levels during initial device configuration. Refer to for recommendations for using headphone volume control for achieving 0dB gain through the DAC channel with various configurations.

ADC / Digital Microphone Interface

The TLV320AIC3253 includes a stereo recording path, which accepts PDM signals from digital microphones. This path has the digital functionality of a high-performance audio ADC, but the analog functions such as microphone preamplifier and delta-sigma modulator are provided by one or two external digital microphones. This device is functionally and software compatible with other audio converters in this family. For consistency with other documents, this path is called an "ADC" in this document even though it does not have the core analog-to-digital conversion functions. The ADC supports sampling rates from 8kHz to 192kHz. In order to provide optimal system power management, the stereo recording path can be powered up one channel at a time, to support the case where only mono record capability is required.

The ADC path of the TLV320AIC3253 features a large set of options for signal conditioning as well as signal routing:

- 2 ADCs (PDM input)
- Fine gain adjust of digital channels with 0.1 dB step size
- Digital volume control with a range of -12 to +20dB
- Mute function

In addition to the standard set of ADC features the TLV320AIC3253 also offers the following special functions:

- Built in microphone bias
- Stereo digital microphone interface
- Channel-to-channel phase adjustment
- Adaptive filter mode

(6) If the device must be placed into 'mute' from the -6.0dB setting, set the device at a gain of -5.0dB first, then place the device into mute.

ADC Processing Blocks — Overview

The TLV320AIC3253 ADC channel includes a built-in digital decimation filter to process the oversampled data from the PDM input to generate digital data at Nyquist sampling rate with high dynamic range. The decimation filter can be chosen from three different types, depending on the required frequency response, group delay and sampling rate.

ADC / Digital Microphone Processing Blocks

The TLV320AIC3253 offers a range of processing blocks which implement various signal processing capabilities along with decimation filtering. These processing blocks give users the choice of how much and what type of signal processing they may use and which decimation filter is applied.

The choice between these processing blocks is part of the PowerTune strategy to balance power conservation and signal-processing flexibility. Less signal-processing capability reduces the power consumed by the device. [Table 8](#) gives an overview of the available processing blocks of the ADC channel and their properties. The Resource Class Column (RC) gives an approximate indication of power consumption.

The signal processing blocks available are:

- First-order IIR
- Scalable number of biquad filters
- Variable-tap FIR filter

The processing blocks are tuned for common cases and can achieve high anti-alias filtering or low-group delay in combination with various signal processing effects such as audio effects and frequency shaping. The available first order IIR, BiQuad and FIR filters have fully user programmable coefficients.

Table 8. ADC / Digital Microphone Processing Blocks

Processing Blocks	Channel	Decimation Filter	1st Order IIR Available	Number BiQuads	FIR	Required AOSR Value	Resource Class
PRB_R1 ⁽¹⁾	Stereo	A	Yes	0	No	128,64	6
PRB_R2	Stereo	A	Yes	5	No	128,64	8
PRB_R3	Stereo	A	Yes	0	25-Tap	128,64	8
PRB_R4	Right	A	Yes	0	No	128,64	3
PRB_R5	Right	A	Yes	5	No	128,64	4
PRB_R6	Right	A	Yes	0	25-Tap	128,64	4
PRB_R7	Stereo	B	Yes	0	No	64	3
PRB_R8	Stereo	B	Yes	3	No	64	4
PRB_R9	Stereo	B	Yes	0	20-Tap	64	4
PRB_R10	Right	B	Yes	0	No	64	2
PRB_R11	Right	B	Yes	3	No	64	2
PRB_R12	Right	B	Yes	0	20-Tap	64	2
PRB_R13	Stereo	C	Yes	0	No	32	3
PRB_R14	Stereo	C	Yes	5	No	32	4
PRB_R15	Stereo	C	Yes	0	25-Tap	32	4
PRB_R16	Right	C	Yes	0	No	32	2
PRB_R17	Right	C	Yes	5	No	32	2
PRB_R18	Right	C	Yes	0	25-Tap	32	2

(1) Default

For more detailed information see the Application Reference Guide, [SLAU303](#)

DAC

The TLV320AIC3253 includes a stereo audio DAC supporting data rates from 8kHz to 192kHz. Each channel of the stereo audio DAC consists of a signal-processing engine with fixed processing blocks, a digital interpolation filter, multi-bit digital delta-sigma modulator, and an analog reconstruction filter. The DAC is designed to provide enhanced performance at low sampling rates through increased oversampling and image filtering, thereby keeping quantization noise generated within the delta-sigma modulator and signal images strongly suppressed within the audio band to beyond 20kHz. To handle multiple input rates and optimize power dissipation and performance, the TLV320AIC3253 allows the system designer to program the oversampling rates over a wide range from 1 to 1024 by configuring the Page 0 / Register 13, and Register 14. The system designer can choose higher oversampling ratios for lower input data rates and lower oversampling ratios for higher input data rates.

The TLV320AIC3253 DAC channel includes a built-in digital interpolation filter to generate oversampled data for the sigma-delta modulator. The interpolation filter can be chosen from three different types depending on required frequency response, group delay and sampling rate.

The DAC path of the TLV320AIC3253 features many options for signal conditioning and signal routing:

- 2 headphone amplifiers
 - Usable in single-ended or differential mode
 - Analog volume setting with a range of -6 to +29 dB
 - Class-D mode
- Digital volume control with a range of -63.5 to +24dB
- Mute function
- Dynamic range compression (DRC)

In addition to the standard set of DAC features the TLV320AIC3253 also offers the following special features:

- Built in sine wave generation (beep generator)
- Digital auto mute
- Adaptive filter mode

DAC Processing Blocks — Overview

The TLV320AIC3253 implements signal processing capabilities and interpolation filtering via processing blocks. These fixed processing blocks give users the choice of how much and what type of signal processing they may use and which interpolation filter is applied.

The choice between these processing blocks is part of the PowerTune strategy balancing power conservation and signal processing flexibility. Less signal processing capability will result in less power consumed by the device. The [Table 9](#) gives an overview over all available processing blocks of the DAC channel and their properties. The Resource Class Column (RC) gives an approximate indication of power consumption.

The signal processing blocks available are:

- First-order IIR
- Scalable number of biquad filters
- 3D – Effect
- Beep Generator

The processing blocks are tuned for common cases and can achieve high image rejection or low group delay in combination with various signal processing effects such as audio effects and frequency shaping. The available first-order IIR and biquad filters have fully user-programmable coefficients.

Table 9. Overview – DAC Predefined Processing Blocks

Processing Block No.	Interpolation Filter	Channel	1st Order IIR Available	Num. of Biquads	DRC	3D	Beep Generator	RC Class
PRB_P1 ⁽¹⁾	A	Stereo	No	3	No	No	No	8
PRB_P2	A	Stereo	Yes	6	Yes	No	No	12

(1) Default

Table 9. Overview – DAC Predefined Processing Blocks (continued)

Processing Block No.	Interpolation Filter	Channel	1st Order IIR Available	Num. of Biquads	DRC	3D	Beep Generator	RC Class
PRB_P3	A	Stereo	Yes	6	No	No	No	10
PRB_P4	A	Left	No	3	No	No	No	4
PRB_P5	A	Left	Yes	6	Yes	No	No	6
PRB_P6	A	Left	Yes	6	No	No	No	6
PRB_P7	B	Stereo	Yes	0	No	No	No	6
PRB_P8	B	Stereo	No	4	Yes	No	No	8
PRB_P9	B	Stereo	No	4	No	No	No	8
PRB_P10	B	Stereo	Yes	6	Yes	No	No	10
PRB_P11	B	Stereo	Yes	6	No	No	No	8
PRB_P12	B	Left	Yes	0	No	No	No	3
PRB_P13	B	Left	No	4	Yes	No	No	4
PRB_P14	B	Left	No	4	No	No	No	4
PRB_P15	B	Left	Yes	6	Yes	No	No	6
PRB_P16	B	Left	Yes	6	No	No	No	4
PRB_P17	C	Stereo	Yes	0	No	No	No	3
PRB_P18	C	Stereo	Yes	4	Yes	No	No	6
PRB_P19	C	Stereo	Yes	4	No	No	No	4
PRB_P20	C	Left	Yes	0	No	No	No	2
PRB_P21	C	Left	Yes	4	Yes	No	No	3
PRB_P22	C	Left	Yes	4	No	No	No	2
PRB_P23	A	Stereo	No	2	No	Yes	No	8
PRB_P24	A	Stereo	Yes	5	Yes	Yes	No	12
PRB_P25	A	Stereo	Yes	5	Yes	Yes	Yes	12

For more detailed information see the Application Reference Guide, [SLAU303](#)

Powertune

The TLV320AIC3253 features PowerTune, a mechanism to balance power-versus-performance trade-offs at the time of device configuration. The device can be tuned to minimize power dissipation, to maximize performance, or to an operating point between the two extremes to best fit the application. The TLV320AIC3253 PowerTune modes are called PTM_P1 to PTM_P4 for the playback (DAC) path.

For more detailed information see the Application Reference Guide, [SLAU303](#)

Digital Audio I/O Interface

Audio data is transferred between the host processor and the TLV320AIC3253 via the digital audio data serial interface, or audio bus. The audio bus on this device is very flexible, including left or right-justified data options, support for I²S or PCM protocols, programmable data length options, a TDM mode for multichannel operation, very flexible master/slave configurability for each bus clock line, and the ability to communicate with multiple devices within a system directly.

The audio bus of the TLV320AIC3253 can be configured for left or right-justified, I²S, DSP, or TDM modes of operation, where communication with standard telephony PCM interfaces is supported within the TDM mode. These modes are all MSB-first, with data width programmable as 16, 20, 24, or 32 bits by configuring Page 0, Register 27, D(5:4). In addition, the word clock and bit clock can be independently configured in either Master or Slave mode, for flexible connectivity to a wide variety of processors. The word clock is used to define the beginning of a frame, and may be programmed as either a pulse or a square-wave signal. The frequency of this clock corresponds to the maximum of the selected ADC and DAC sampling frequencies.

The bit clock is used to clock in and clock out the digital audio data across the serial bus. When in Master mode, this signal can be programmed to generate variable clock pulses by controlling the bit-clock divider in Page 0, Register 30 (see). The number of bit-clock pulses in a frame may need adjustment to accommodate various word-lengths as well as to support the case when multiple TLV320AIC3253s may share the same audio bus.

The TLV320AIC3253 also includes a feature to offset the position of start of data transfer with respect to the word-clock. This offset can be controlled in terms of number of bit-clocks and can be programmed in Page 0, Register 28.

The TLV320AIC3253 also has the feature of inverting the polarity of the bit-clock used for transferring the audio data as compared to the default clock polarity used. This feature can be used independently of the mode of audio interface chosen. This can be configured via Page 0, Register 29, D(3).

The TLV320AIC3253 further includes programmability (Page 0, Register 27, D0) to place the DOUT line into a hi-Z (3-state) condition during all bit clocks when valid data is not being sent. By combining this capability with the ability to program at what bit clock in a frame the audio data begins, time-division multiplexing (TDM) can be accomplished, enabling the use of multiple codecs on a single audio serial data bus. When the audio serial data bus is powered down while configured in master mode, the pins associated with the interface are put into a hi-Z output condition.

By default when the word-clocks and bit-clocks are generated by the TLV320AIC3253, these clocks are active only when the codec (ADC, DAC or both) are powered up within the device. This is done to save power. However, it also supports a feature when both the word clocks and bit-clocks can be active even when the codec in the device is powered down. This is useful when using the TDM mode with multiple codecs on the same bus, or when word-clock or bit-clocks are used in the system as general-purpose clocks.

Clock Generation and PLL

The TLV320AIC3253 supports a wide range of options for generating clocks for the ADC and DAC sections as well as interface and other control blocks. The clocks for ADC and DAC require a source reference clock. This clock can be provided on variety of device pins such as MCLK, BCLK or GPIO pins. The CODEC_CLKIN can then be routed through highly-flexible clock dividers to generate the various clocks required for ADC, DAC and the miniDSP sections. In the event that the desired audio or miniDSP clocks cannot be generated from the reference clocks on MCLK BCLK or GPIO, the TLV320AIC3253 also provides the option of using the on-chip PLL which supports a wide range of fractional multiplication values to generate the required clocks. Starting from CODEC_CLKIN the TLV320AIC3253 provides several programmable clock dividers to help achieve a variety of sampling rates for ADC, DAC and clocks for the miniDSP .

For more detailed information see the Application Reference Guide, [SLAU303](#)

Control Interfaces

The TLV320AIC3253 control interface supports SPI or I²C communication protocols, with the protocol selectable using the SPI_SELECT pin. For SPI, SPI_SELECT should be tied high; for I²C, SPI_SELECT should be tied low. It is not recommended to change the state of SPI_SELECT during device operation.

I²C Control

The TLV320AIC3253 supports the I²C control protocol, and will respond to the I²C address of 0011000. I²C is a two-wire, open-drain interface supporting multiple devices and masters on a single bus. Devices on the I²C bus only drive the bus lines LOW by connecting them to ground; they never drive the bus lines HIGH. Instead, the bus wires are pulled HIGH by pullup resistors, so the bus wires are HIGH when no device is driving them LOW. This way, two devices cannot conflict; if two devices drive the bus simultaneously, there is no driver contention.

SPI Control

In the SPI control mode, the TLV320AIC3253 uses the pins SCL/SSZ=SSZ, SCLK=SCLK, MISO=MISO, SDA/MOSI=MOSI as a standard SPI port with clock polarity setting of 0 (typical microprocessor SPI control bit CPOL = 0). The SPI port allows full-duplex, synchronous, serial communication between a host processor (the master) and peripheral devices (slaves). The SPI master (in this case, the host processor) generates the

synchronizing clock (driven onto SCLK) and initiates transmissions. The SPI slave devices (such as the TLV320AIC3253) depend on a master to start and synchronize transmissions. A transmission begins when initiated by an SPI master. The byte from the SPI master begins shifting in on the slave MOSI pin under the control of the master serial clock (driven onto SCLK). As the byte shifts in on the MOSI pin, a byte shifts out on the MISO pin to the master shift register.

For more detailed information see the Application Reference Guide, [SLAU303](#)

Power Supply

The TLV320AIC3253 has four power-supply connections which allow various optimizations for low system power. The four supply pins are LDOin, DVdd, AVdd and IOVDD. To power up the device, a digital supply in the range of 1.26V to 1.95V is applied to the DV_{DD} pin. The IO_{VDD} voltage can be in the range of 1.1V - 3.6V. The analog core supply can either be derived from the internal LDO accepting an LDOin voltage in the range of 1.9V to 3.6V, or the AV_{DD} pin can directly be driven with a voltage in the range of 1.5V to 1.95V.

For more detailed information see the TLV320AIC3253 Application Reference Guide, [SLAU303](#)

Device Special Functions

The following special functions are available to support advanced system requirements:

- Headset detection
- Interrupt generation
- Flexible pin multiplexing

For more detailed information see the Application Reference Guide, [SLAU303](#)

The TLV320AIC3253 features two miniDSP cores. The first miniDSP core is tightly coupled to the ADC, the second miniDSP core is tightly coupled to the DAC. The fully programmable algorithms for the miniDSP must be loaded into the device after power up. The miniDSPs have direct access to the digital stereo audio stream on the ADC and on the DAC side, offering the possibility for advanced, very-low group delay DSP algorithms. Each miniDSP can run up to 1152 instructions on every audio sample at a 48kHz sample rate. The two cores can run fully synchronized and can exchange data. Typical algorithms for the TLV320AIC3253 miniDSPs are active noise cancellation, acoustic echo cancellation or advanced DSP sound enhancement algorithms.

Software

Software development for the TLV320AIC3253 is supported through TI's comprehensive PurePath Studio Development Environment. A powerful, easy-to-use tool designed specifically to simplify software development on the TLV320AIC3xxx miniDSP audio platform. The Graphical Development Environment consists of a library of common audio functions that can be dragged-and-dropped into an audio signal flow and graphically connected together. The DSP code can then be assembled from the graphical signal flow with the click of a mouse.

Please visit the TLV320AIC3253 product folder on www.ti.com to learn more about PurePath Studio and the latest status on available, ready-to-use DSP algorithms.

Register Map Summary

Table 10. Summary of Register Map

Decimal		Hex		DESCRIPTION
PAGE NO.	REG. NO.	PAGE NO.	REG. NO.	
0	0	0x00	0x00	Page Select Register
0	1	0x00	0x01	Software Reset Register
0	2	0x00	0x02	Reserved Register
0	3	0x00	0x03	Reserved Register
0	4	0x00	0x04	Clock Setting Register 1, Multiplexers
0	5	0x00	0x05	Clock Setting Register 2, PLL P&R Values
0	6	0x00	0x06	Clock Setting Register 3, PLL J Values

Table 10. Summary of Register Map (continued)

Decimal		Hex		DESCRIPTION
PAGE NO.	REG. NO.	PAGE NO.	REG. NO.	
0	7	0x00	0x07	Clock Setting Register 4, PLL D Values (MSB)
0	8	0x00	0x08	Clock Setting Register 5, PLL D Values (LSB)
0	9-10	0x00	0x09-0x0A	Reserved Register
0	11	0x00	0x0B	Clock Setting Register 6, NDAC Values
0	12	0x00	0x0C	Clock Setting Register 7, MDAC Values
0	13	0x00	0x0D	DAC OSR Setting Register 1, MSB Value
0	14	0x00	0x0E	DAC OSR Setting Register 2, LSB Value
0	15	0x00	0x0F	miniDSP_D Instruction Control Register 1
0	16	0x00	0x10	miniDSP_D Instruction Control Register 2
0	17	0x00	0x11	miniDSP_D Interpolation Factor Setting Register
0	18	0x00	0x12	Clock Setting Register 8, NADC Values
0	19	0x00	0x13	Clock Setting Register 9, MADC Values
0	20	0x00	0x14	ADC Oversampling (AOSR) Register
0	21	0x00	0x15	miniDSP_A Instruction Control Register 1
0	22	0x00	0x16	miniDSP_A Instruction Control Register 2
0	23	0x00	0x17	miniDSP_A Decimation Factor Setting Register
0	24	0x00	0x18	Reserved Register
0	25	0x00	0x19	Clock Setting Register 10, Multiplexers
0	26	0x00	0x1A	Clock Setting Register 11, CLKOUT M divider value
0	27	0x00	0x1B	Audio Interface Setting Register 1
0	28	0x00	0x1C	Audio Interface Setting Register 2, Data offset setting
0	29	0x00	0x1D	Audio Interface Setting Register 3
0	30	0x00	0x1E	Clock Setting Register 12, BCLK N Divider
0	31	0x00	0x1F	Audio Interface Setting Register 4, Secondary Audio Interface
0	32	0x00	0x20	Audio Interface Setting Register 5
0	33	0x00	0x21	Audio Interface Setting Register 6
0	34	0x00	0x22	Digital Interface Misc. Setting Register
0	35	0x00	0x23	Reserved Register
0	36	0x00	0x24	ADC Flag Register
0	37	0x00	0x25	DAC Flag Register 1
0	38	0x00	0x26	DAC Flag Register 2
0	39-41	0x00	0x27-0x29	Reserved Register
0	42	0x00	0x2A	Sticky Flag Register 1
0	43	0x00	0x2B	Interrupt Flag Register 1
0	44	0x00	0x2C	Sticky Flag Register 2
0	45	0x00	0x2D	Sticky Flag Register 3
0	46	0x00	0x2E	Interrupt Flag Register 2
0	47	0x00	0x2F	Interrupt Flag Register 3
0	48	0x00	0x30	INT1 Interrupt Control Register
0	49	0x00	0x31	INT2 Interrupt Control Register
0	50-51	0x00	0x32-0x33	Reserved Register
0	52	0x00	0x34	GPIO/MFP5 Control Register (WCSP version only)+L998
0	53	0x00	0x35	DOOUT/MFP2 Function Control Register
0	54	0x00	0x36	DIN/MFP1 Function Control Register
0	55	0x00	0x37	MISO/MFP4 Function Control Register
0	56	0x00	0x38	SCLK/MFP3 Function Control Register

Table 10. Summary of Register Map (continued)

Decimal		Hex		DESCRIPTION
PAGE NO.	REG. NO.	PAGE NO.	REG. NO.	
0	57-59	0x00	0x39-0x3B	Reserved Registers
0	60	0x00	0x3C	DAC Signal Processing Block Control Register
0	61	0x00	0x3D	ADC Signal Processing Block Control Register
0	62	0x00	0x3E	miniDSP_A and miniDSP_D Configuration Register
0	63	0x00	0x3F	DAC Channel Setup Register 1
0	64	0x00	0x40	DAC Channel Setup Register 2
0	65	0x00	0x41	Left DAC Channel Digital Volume Control Register
0	66	0x00	0x42	Right DAC Channel Digital Volume Control Register
0	67	0x00	0x43	Headset Detection Configuration Register
0	68	0x00	0x44	DRC Control Register 1
0	69	0x00	0x45	DRC Control Register 2
0	70	0x00	0x46	DRC Control Register 3
0	71	0x00	0x47	Beep Generator Register 1
0	72	0x00	0x48	Beep Generator Register 2
0	73	0x00	0x49	Beep Generator Register 3
0	74	0x00	0x4A	Beep Generator Register 4
0	75	0x00	0x4B	Beep Generator Register 5
0	76	0x00	0x4C	Beep Generator Register 6
0	77	0x00	0x4D	Beep Generator Register 7
0	78	0x00	0x4E	Beep Generator Register 8
0	79	0x00	0x4F	Beep Generator Register 9
0	80	0x00	0x50	Reserved
0	81	0x00	0x51	ADC Channel Setup Register
0	82	0x00	0x52	ADC Fine Gain Adjust Register
0	83	0x00	0x53	Left ADC Channel Volume Control Register
0	84	0x00	0x54	Right ADC Channel Volume Control Register
0	85	0x00	0x55	ADC Phase Adjust Register
0	86-127	0x00	0x56-0x7F	Reserved Register
1	0	0x01	0x00	Page Select Register
1	1	0x01	0x01	Power Configuration Register
1	2	0x01	0x02	LDO Control Register
1	3	0x01	0x03	Playback Configuration Register 1
1	4	0x01	0x04	Playback Configuration Register 2
1	5-8	0x01	0x05-0x08	Reserved Register
1	9	0x01	0x09	Output Driver Power Control Register
1	10	0x01	0x0A	Common Mode Control Register
1	11	0x01	0x0B	Over Current Protection Configuration Register
1	12	0x01	0x0C	HPL Routing Selection Register
1	13	0x01	0x0D	HPR Routing Selection Register
1	14	0x01	0x0E	Reserved Register
1	15	0x01	0x0F	Reserved Register
1	16	0x01	0x10	HPL Driver Gain Setting Register
1	17	0x01	0x11	HPR Driver Gain Setting Register
1	18	0x01	0x12	Reserved Register
1	19	0x01	0x13	Reserved Register
1	20	0x01	0x14	Headphone Driver Startup Control Register

Table 10. Summary of Register Map (continued)

Decimal		Hex		DESCRIPTION
PAGE NO.	REG. NO.	PAGE NO.	REG. NO.	
1	21	0x01	0x15	Reserved Register
1	22	0x01	0x16	INL to HPL Volume Control Register
1	23	0x01	0x17	INR to HPR Volume Control Register
1	24-50	0x01	0x18-0x32	Reserved Register
1	51	0x01	0x33	MICBIAS Configuration Register
1	52-57	0x01	0x34-0x39	Reserved Register
1	58	0x01	0x3A	Analog Input Settings
1	59-62	0x01	0x3B-0x3E	Reserved Register
1	63	0x01	0x3F	DAC Analog Gain Control Flag Register
1	64-70	0x01	0x40-0x46	Reserved Register
1	71	0x01	0x47	Analog Input Quick Charging Configuration Register
1	72-122	0x01	0x48-0x7A	Reserved Register
1	123	0x01	0x7B	Reference Power-up Configuration Register
1	124	0x01	0x7C	Reserved Register
1	125	0x01	0x7D	Offset Calibration Register
1	126-127	0x01	0x7E-0x7F	Reserved Register
8	0	0x08	0x00	Page Select Register
8	1	0x08	0x01	ADC Adaptive Filter Configuration Register
8	2-7	0x08	0x02-0x07	Reserved
8	8-127	0x08	0x08-0x7F	ADC Coefficients Buffer-A C(0:29)
9-16	0	0x09-0x10	0x00	Page Select Register
9-16	1-7	0x09-0x10	0x01-0x07	Reserved
9-16	8-127	0x09-0x10	0x08-0x7F	ADC Coefficients Buffer-A C(30:255)
26-34	0	0x1A-0x22	0x00	Page Select Register
26-34	1-7	0x1A-0x22	0x01-0x07	Reserved.
26-34	8-127	0x1A-0x22	0x08-0x7F	ADC Coefficients Buffer-B C(0:255)
44	0	0x2C	0x00	Page Select Register
44	1	0x2C	0x01	DAC Adaptive Filter Configuration Register
44	2-7	0x2C	0x02-0x07	Reserved
44	8-127	0x2C	0x08-0x7F	DAC Coefficients Buffer-A C(0:29)
45-52	0	0x2D-0x34	0x00	Page Select Register
45-52	1-7	0x2D-0x34	0x01-0x07	Reserved.
45-52	8-127	0x2D-0x34	0x08-0x7F	DAC Coefficients Buffer-A C(30:255)
62-70	0	0x3E-0x46	0x00	Page Select Register
62-70	1-7	0x3E-0x46	0x01-0x07	Reserved.
62-70	8-127	0x3E-0x46	0x08-0x7F	DAC Coefficients Buffer-B C(0:255)
80-114	0	0x50-0x72	0x00	Page Select Register
80-114	1-7	0x50-0x72	0x01-0x07	Reserved.
80-114	8-127	0x50-0x72	0x08-0x7F	miniDSP_A Instructions
152-186	0	0x98-0xBA	0x00	Page Select Register
152-186	1-7	0x98-0xBA	0x01-0x07	Reserved.
152-186	8-127	0x98-0xBA	0x08-0x7F	miniDSP_D Instructions

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV320AIC3253IRGER	VQFN	RGE	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
TLV320AIC3253IRGET	VQFN	RGE	24	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
TLV320AIC3253IYZKR	DSBGA	YZK	25	3000	180.0	8.4	2.75	2.75	0.81	4.0	8.0	Q1
TLV320AIC3253IYZKT	DSBGA	YZK	25	250	180.0	8.4	2.75	2.75	0.81	4.0	8.0	Q1

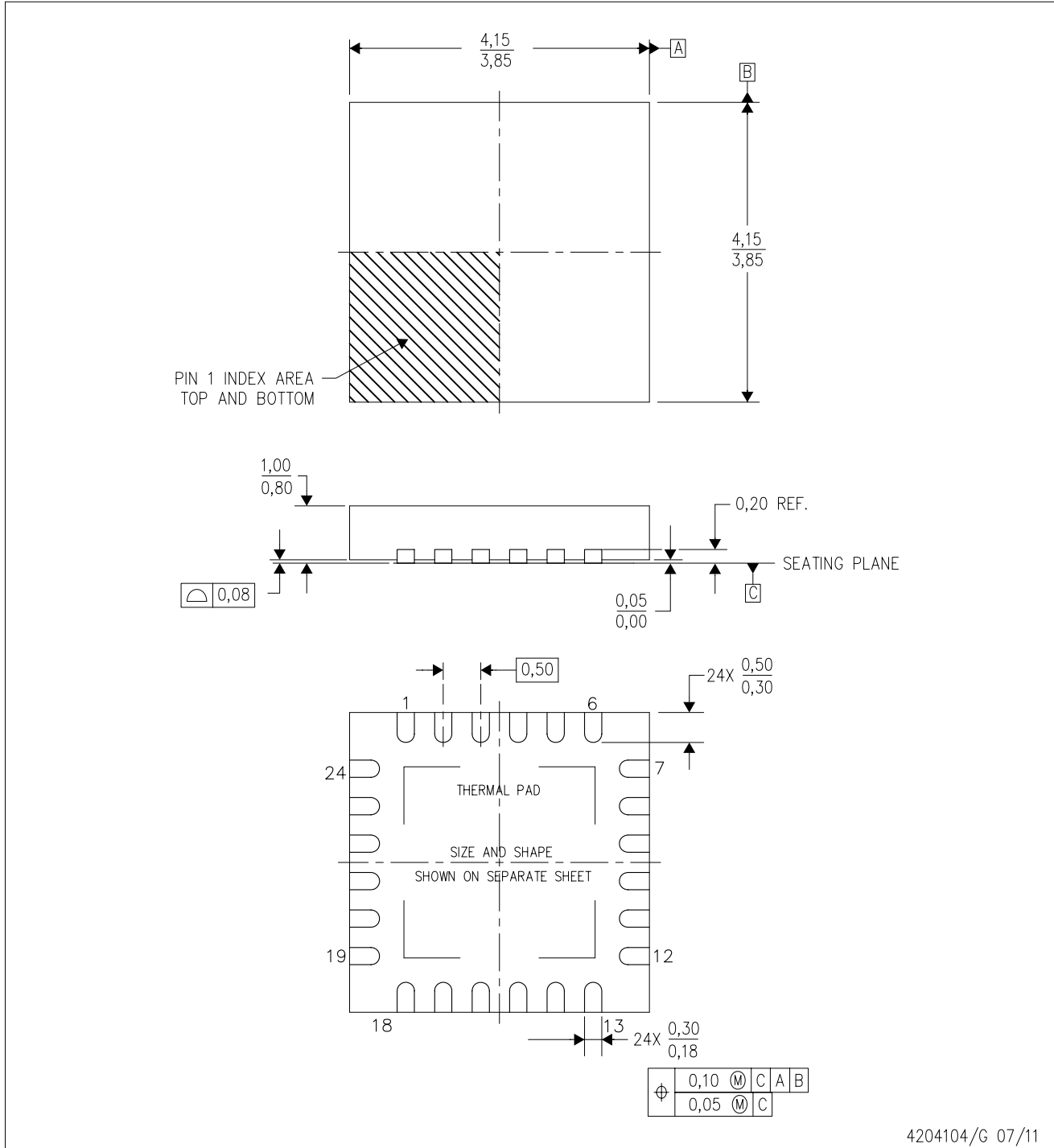
TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV320AIC3253IRGER	VQFN	RGE	24	3000	367.0	367.0	35.0
TLV320AIC3253IRGET	VQFN	RGE	24	250	210.0	185.0	35.0
TLV320AIC3253IYZKR	DSBGA	YZK	25	3000	182.0	182.0	17.0
TLV320AIC3253IYZKT	DSBGA	YZK	25	250	182.0	182.0	17.0

RGE (S-PVQFN-N24)

PLASTIC QUAD FLATPACK NO-LEAD



4204104/G 07/11

- NOTES:
- All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - This drawing is subject to change without notice.
 - Quad Flatpack, No-Leads (QFN) package configuration.
 - The package thermal pad must be soldered to the board for thermal and mechanical performance.
 - See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
 - Falls within JEDEC MO-220.

THERMAL PAD MECHANICAL DATA

RGE (S-PVQFN-N24)

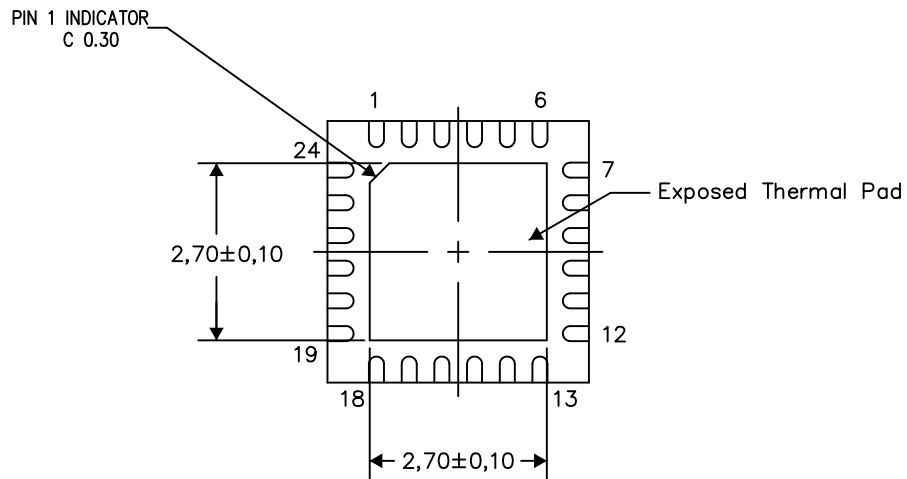
PLASTIC QUAD FLATPACK NO-LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

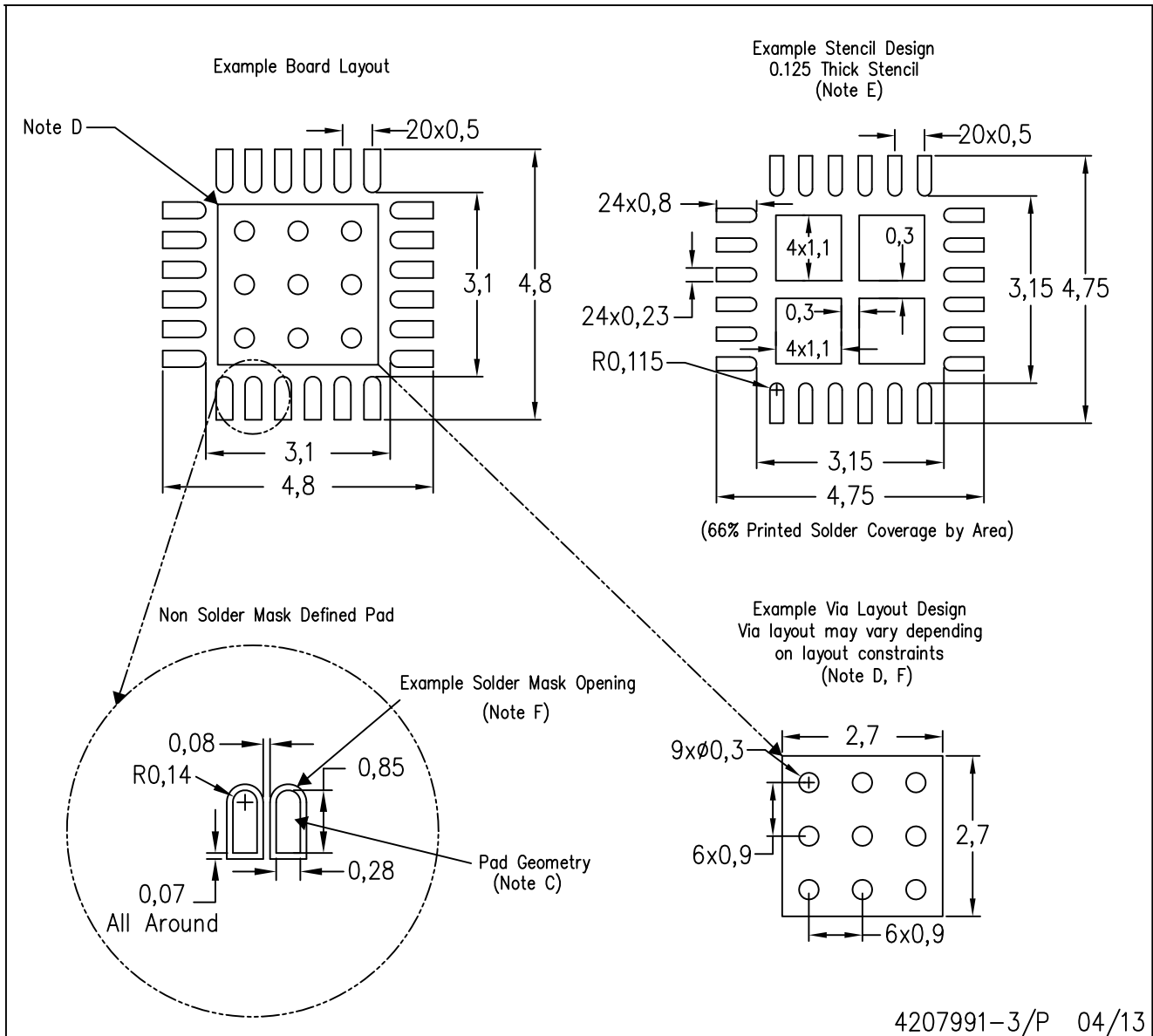
Exposed Thermal Pad Dimensions

4206344-4/AD 04/13

NOTES: A. All linear dimensions are in millimeters

RGE (S-PVQFN-N24)

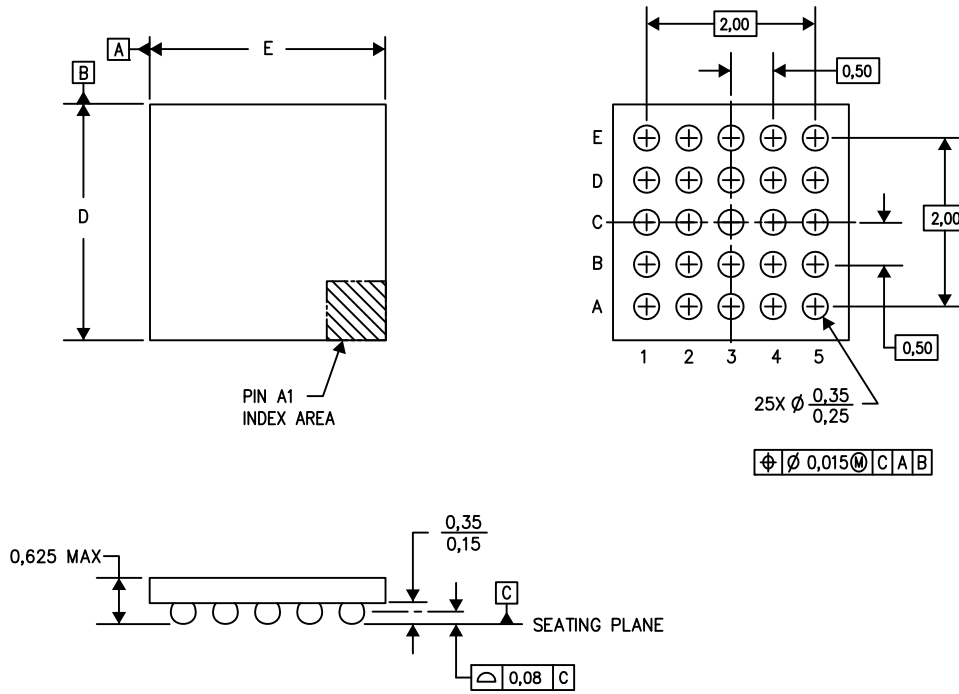
PLASTIC QUAD FLATPACK NO-LEAD



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <<http://www.ti.com>>.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
 - Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

YZK (S-XBGA-N25)

DIE-SIZE BALL GRID ARRAY



4205062-3/F 07/13

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. NanoFree™ package configuration.

NanoFree is a trademark of Texas Instruments.

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