

# 64K x 4 Static RAM with Separate I/O

## Features

- **High speed**  
— 12 ns
- **CMOS for optimum speed/power**
- **Low active power**  
— 880 mW
- **Low standby power**  
— 220 mW
- **TTL-compatible inputs and outputs**
- **Automatic power-down when deselected**

## Functional Description

The CY7C192 is a high-performance CMOS static RAM organized as 65,536 x 4 bits with separate I/O. Easy memory ex-

pansion is provided by active LOW Chip Enable ( $\overline{CE}$ ) and three-state drivers. It has an automatic power-down feature, reducing the power consumption by 75% when deselected.

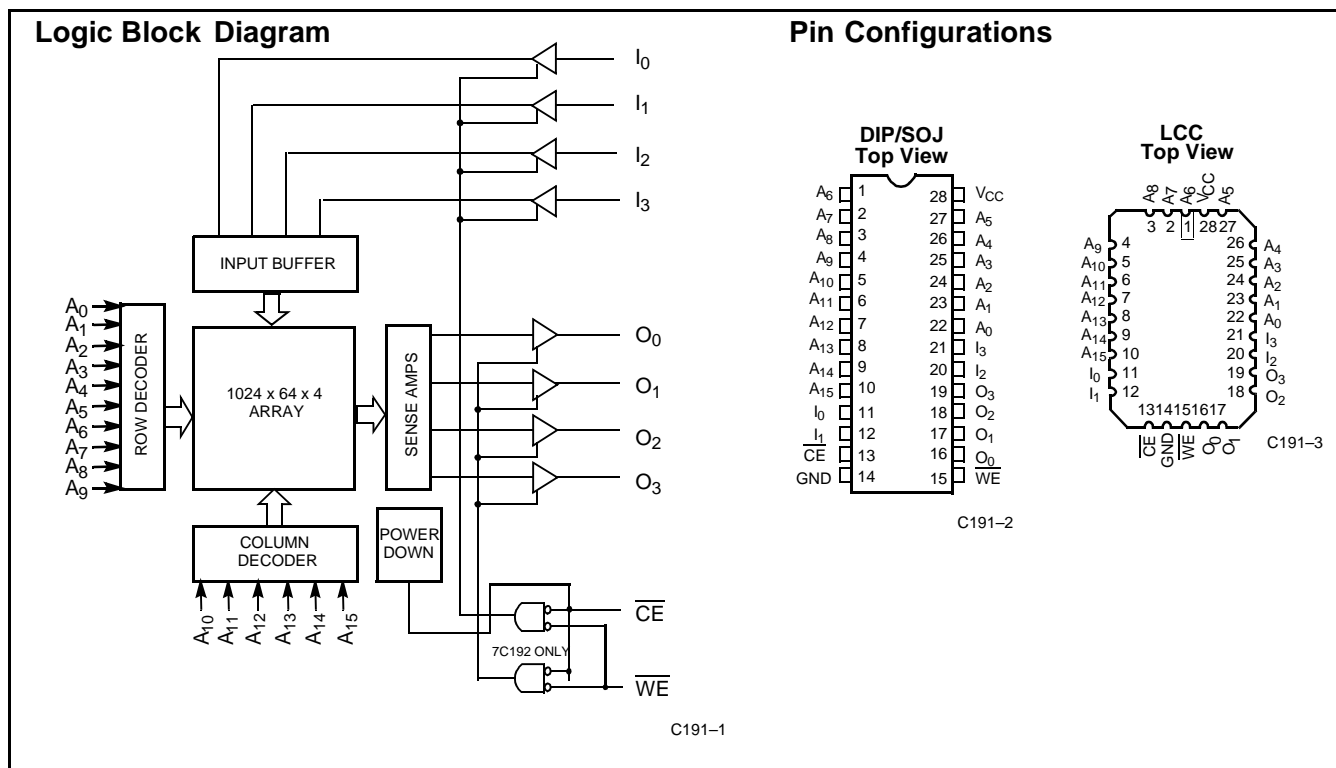
Writing to the device is accomplished when the Chip Enable ( $\overline{CE}$ ) and write enable ( $\overline{WE}$ ) inputs are both LOW.

Data on the four input pins ( $I_0$  through  $I_3$ ) is written into the memory location specified on the address pins ( $A_0$  through  $A_{15}$ ).

Reading the device is accomplished by taking the Chip Enable ( $\overline{CE}$ ) LOW while the Write Enable ( $\overline{WE}$ ) remains HIGH. Under these conditions the contents of the memory location specified on the address pins will appear on the four data output pins.

The output pins stay in high-impedance state when Write Enable ( $\overline{WE}$ ) is LOW, or Chip Enable ( $\overline{CE}$ ) is HIGH.

A die coat is used to insure alpha immunity.



## Selection Guide

	7C192-12	7C192-15	7C192-20	7C192-25
Maximum Access Time (ns)	12	15	20	25
Maximum Operating Current (mA)	155	145	135	115
Maximum Standby Current (mA)	30	30	30	30

**Maximum Ratings**

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... -65°C to +150°C  
 Ambient Temperature with Power Applied..... -55°C to +125°C  
 Supply Voltage to Ground Potential (Pin 28 to Pin 14)..... -0.5V to +7.0V  
 DC Voltage Applied to Outputs in High Z State<sup>[1]</sup> ..... -0.5V to  $V_{CC} + 0.5V$

DC Input Voltage<sup>[1]</sup>..... -0.5V to  $V_{CC} + 0.5V$   
 Output Current into Outputs (LOW)..... 20 mA  
 Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)  
 Latch-Up Current..... >200 mA

**Operating Range**

Range	Ambient Temperature <sup>[2]</sup>	$V_{CC}$
Commercial	0°C to +70°C	5V ± 10%

**Electrical Characteristics** Over the Operating Range

Parameter	Description	Test Conditions	7C192-12		7C192-15		Unit
			Min.	Max.	Min.	Max.	
$V_{OH}$	Output HIGH Voltage	$V_{CC} = \text{Min.}, I_{OH} = -4.0 \text{ mA}$	2.4		2.4		V
$V_{OL}$	Output LOW Voltage	$V_{CC} = \text{Min.}, I_{OL} = 8.0 \text{ mA}$		0.4		0.4	V
$V_{IH}$	Input HIGH Voltage		2.2	$V_{CC} + 0.3V$	2.2	$V_{CC} + 0.3V$	V
$V_{IL}$	Input LOW Voltage <sup>[1]</sup>		-0.5	0.8	-0.5	0.8	V
$I_{IX}$	Input Load Current	$GND \leq V_I \leq V_{CC}$	-5	+5	-5	+5	μA
$I_{OZ}$	Output Leakage Current	$GND \leq V_O \leq V_{CC}$ , Output Disabled	-5	+5	-5	+5	μA
$I_{OS}$	Output Short Circuit Current <sup>[3]</sup>	$V_{CC} = \text{Max.}, V_{OUT} = GND$		-300		-300	mA
$I_{CC}$	$V_{CC}$ Operating Supply Current	$V_{CC} = \text{Max.}, I_{OUT} = 0 \text{ mA}, f = f_{MAX} = 1/t_{RC}$		155		145	mA
$I_{SB1}$	Automatic $\overline{CE}$ Power-Down Current—TTL Inputs	Max. $V_{CC}$ , $\overline{CE} \geq V_{IH}$ , $V_{IN} \geq V_{IH}$ or $V_{IN} \leq V_{IL}$ , $f = f_{MAX}$		30		30	mA
$I_{SB2}$	Automatic $\overline{CE}$ Power-Down Current—CMOS Inputs	Max. $V_{CC}$ , $\overline{CE} \geq V_{CC} - 0.3V$ , $V_{IN} \geq V_{CC} - 0.3V$ or $V_{IN} \leq 0.3V$ , $f = 0$		10		10	mA

**Notes:**

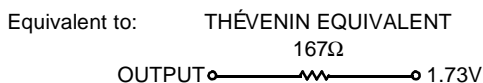
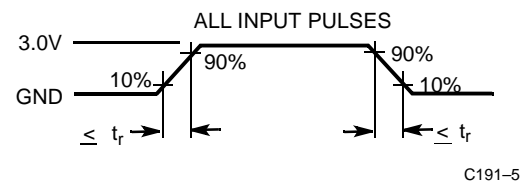
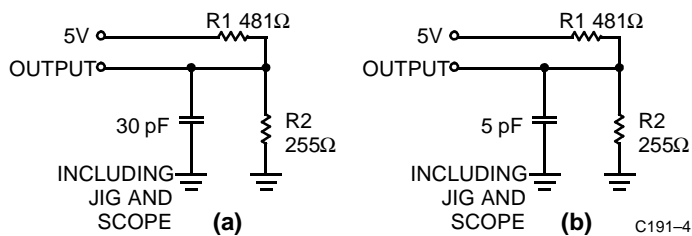
- Minimum voltage is equal to -2.0V for pulse durations of less than 20 ns.
- $T_A$  is the case temperature.
- Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.

**Electrical Characteristics** Over the Operating Range

Parameter	Description	Test Conditions	7C192-20		7C192-25		Unit
			Min.	Max.	Min.	Max.	
V <sub>OH</sub>	Output HIGH Voltage	V <sub>CC</sub> = Min., I <sub>OH</sub> = -4.0 mA	2.4		2.4		V
V <sub>OL</sub>	Output LOW Voltage	V <sub>CC</sub> = Min., I <sub>OL</sub> = 8.0 mA		0.4		0.4	V
V <sub>IH</sub>	Input HIGH Voltage		2.2	V <sub>CC</sub> + 0.3V	2.2	V <sub>CC</sub> + 0.3V	V
V <sub>IL</sub>	Input LOW Voltage <sup>[1]</sup>		-0.5	0.8	-3.0	0.8	V
I <sub>IX</sub>	Input Load Current	GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub>	-5	+5	-5	+5	μA
I <sub>OZ</sub>	Output Leakage Current	GND ≤ V <sub>O</sub> ≤ V <sub>CC</sub> , Output Disabled	-5	+5	-5	+5	μA
I <sub>OS</sub>	Output Short Circuit Current <sup>[3]</sup>	V <sub>CC</sub> = Max., V <sub>OUT</sub> = GND		-300		-300	mA
I <sub>CC</sub>	V <sub>CC</sub> Operating Supply Current	V <sub>CC</sub> = Max., I <sub>OUT</sub> = 0 mA, f = f <sub>MAX</sub> = 1/t <sub>RC</sub>		135		115	mA
I <sub>SB1</sub>	Automatic $\overline{CE}$ Power-Down Current—TTL Inputs	Max. V <sub>CC</sub> , $\overline{CE} \geq V_{IH}$ , V <sub>IN</sub> ≥ V <sub>IH</sub> or V <sub>IN</sub> ≤ V <sub>IL</sub> , f = f <sub>MAX</sub>		30		30	mA
I <sub>SB2</sub>	Automatic $\overline{CE}$ Power-Down Current—CMOS Inputs	$\overline{CE} \geq V_{CC} - 0.3V$ , V <sub>IN</sub> ≤ V <sub>CC</sub> - 0.3V or V <sub>IN</sub> ≤ 0.3V, f = 0		15		15	mA

**Capacitance<sup>[4]</sup>**

Parameter	Description	Test Conditions	Max.	Unit
C <sub>IN</sub>	Input Capacitance	T <sub>A</sub> = 25°C, f = 1 MHz, V <sub>CC</sub> = 5.0V	8	pF
C <sub>OUT</sub>	Output Capacitance		10	pF

**AC Test Loads and Waveforms<sup>[5]</sup>**

**Notes:**

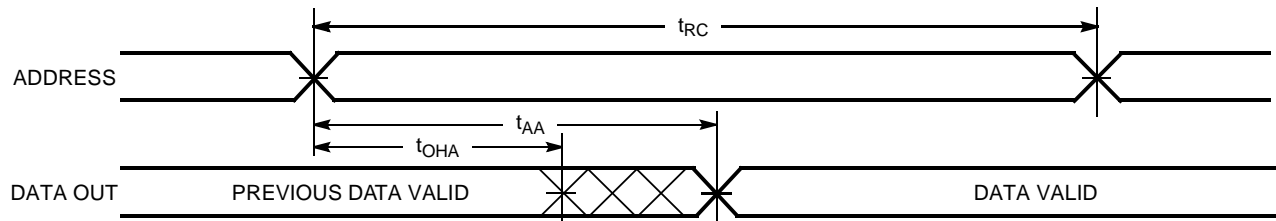
- Tested initially and after any design or process changes that may affect these parameters.
- t<sub>r</sub> = ≤ 3 ns for the -12 and -15 speeds. T<sub>r</sub> = ≤ 5 ns for the -20 and slower speeds.

**Switching Characteristics** Over the Operating Range<sup>[6]</sup>

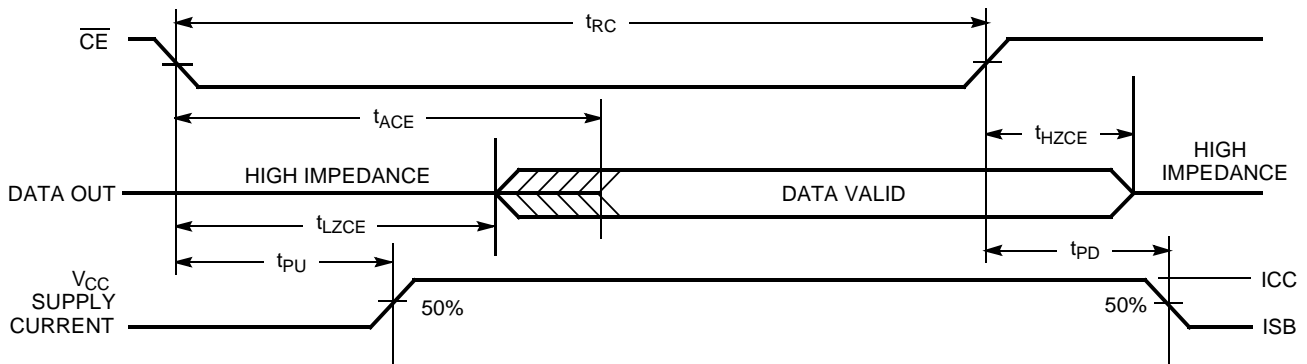
Parameter	Description	7C192-12		7C192-15		7C192-20		7C192-25		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
<b>READ CYCLE</b>										
t <sub>RC</sub>	Read Cycle Time	12		15		20		25		ns
t <sub>AA</sub>	Address to Data Valid		12		15		20		25	ns
t <sub>OHA</sub>	Output Hold from Address Change	3		3		3		3		ns
t <sub>ACE</sub>	$\overline{\text{CE}}$ LOW to Data Valid		12		15		20		25	ns
t <sub>LZCE</sub>	$\overline{\text{CE}}$ LOW to Low Z <sup>[7]</sup>	3		3		3		3		ns
t <sub>HZCE</sub>	$\overline{\text{CE}}$ HIGH to High Z <sup>[7,8]</sup>		5		7		9		11	ns
t <sub>PU</sub>	$\overline{\text{CE}}$ LOW to Power-Up	0		0		0		0		ns
t <sub>PD</sub>	$\overline{\text{CE}}$ HIGH to Power-Down		12		15		20		25	ns
<b>WRITE CYCLE<sup>[9]</sup></b>										
t <sub>WC</sub>	Write Cycle Time	12		15		20		25		ns
t <sub>SCE</sub>	$\overline{\text{CE}}$ LOW to Write End	9		10		15		18		ns
t <sub>AW</sub>	Address Set-Up to Write End	9		10		15		20		ns
t <sub>HA</sub>	Address Hold from Write End	0		0		0		0		ns
t <sub>SA</sub>	Address Set-Up to Write Start	0		0		0		0		ns
t <sub>PWE</sub>	$\overline{\text{WE}}$ Pulse Width	8		9		15		18		ns
t <sub>SD</sub>	Data Set-Up to Write End	8		9		10		10		ns
t <sub>HD</sub>	Data Hold from Write End	0		0		0		0		ns
t <sub>LZWE</sub>	$\overline{\text{WE}}$ HIGH to Low Z (7C192) <sup>[7]</sup>	3		3		3		3		ns
t <sub>HZWE</sub>	$\overline{\text{WE}}$ LOW to High Z (7C192) <sup>[7,8]</sup>		7		7		10		11	ns
t <sub>DWE</sub>	$\overline{\text{WE}}$ LOW to Data Valid (7C191)		12		15		20		25	ns
t <sub>ADV</sub>	Data Valid to Output Valid (7C191)		12		15		20		20	ns
t <sub>DCE</sub>	$\overline{\text{CE}}$ LOW to Data Valid (7C191)		12		15		20		25	ns

**Notes:**

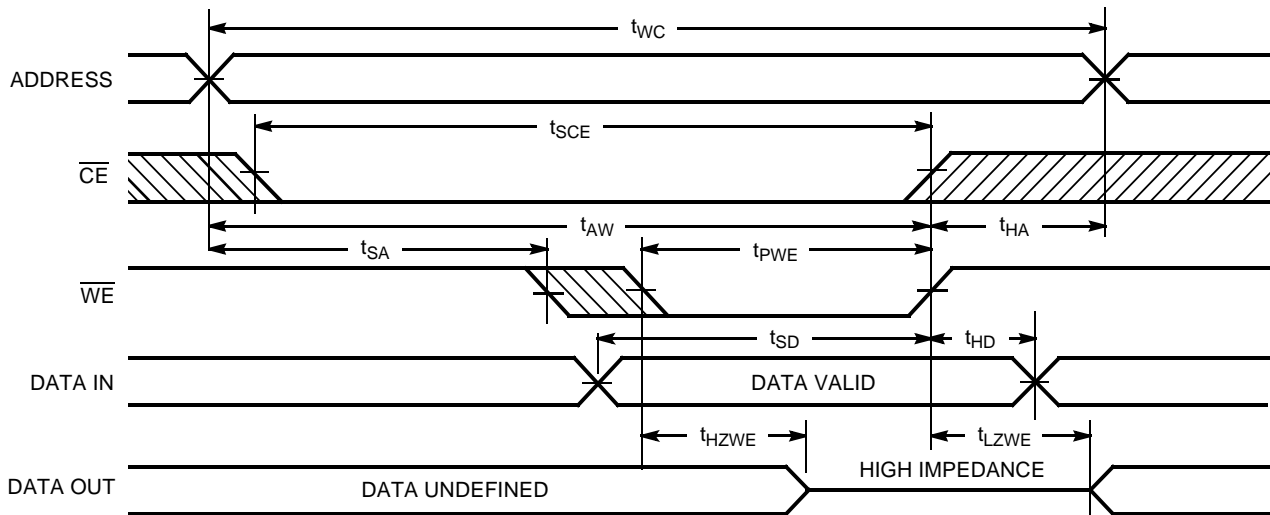
- Test conditions assume signal transition time of 3 ns or less for -12 and -15 speeds and 5 ns or less for -20 through -25 speeds, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I<sub>OL</sub>/I<sub>OH</sub> and 30-pF load capacitance.
- At any given temperature and voltage condition, t<sub>HZCE</sub> is less than t<sub>LZCE</sub>, t<sub>HZWE</sub> is less than t<sub>LZWE</sub> for any given device. These parameters are guaranteed by design and not 100% tested.
- t<sub>HZCE</sub> and t<sub>HZWE</sub> are specified with C<sub>L</sub> = 5 pF as in part (b) of AC Test Loads. Transition is measured ±500 mV from steady-state voltage.
- The internal write time of the memory is defined by the overlap of  $\overline{\text{CE}}$  LOW and  $\overline{\text{WE}}$  LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.

**Switching Waveforms**
**Read Cycle No. 1<sup>[10, 11]</sup>**


C191-6

**Read Cycle No. 2<sup>[10, 12]</sup>**


C191-7

**Write Cycle No. 1 (WE Controlled)<sup>[9]</sup>**


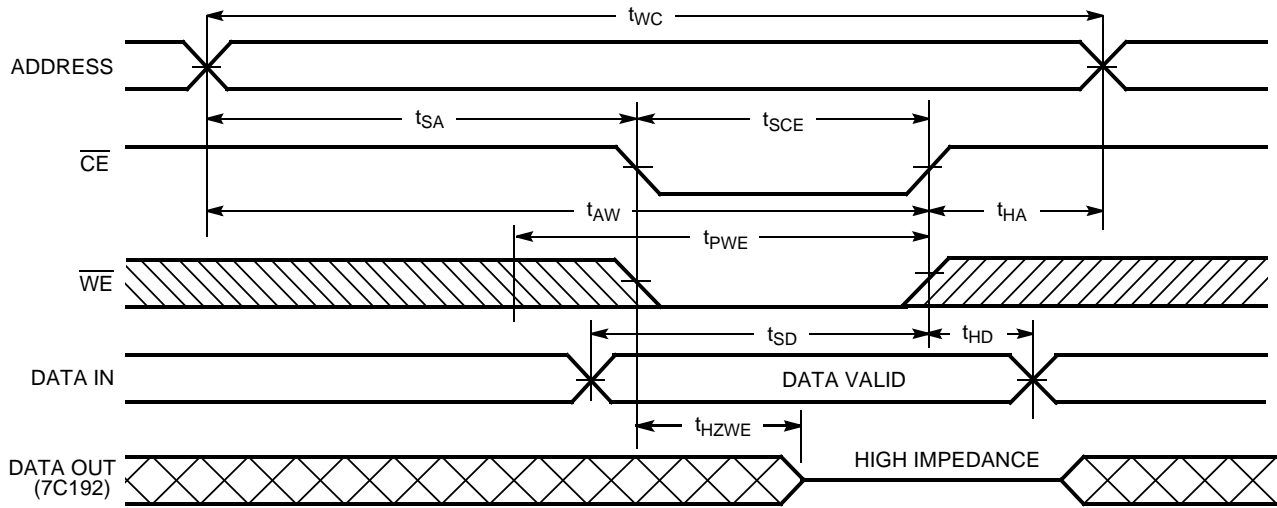
C191-8

**Notes:**

10. WE is HIGH for read cycle.
11. Device is continuously selected,  $\overline{CE} = V_{IL}$ .
12. Address valid prior to or coincident with  $\overline{CE}$  transition LOW.

Switching Waveforms (continued)

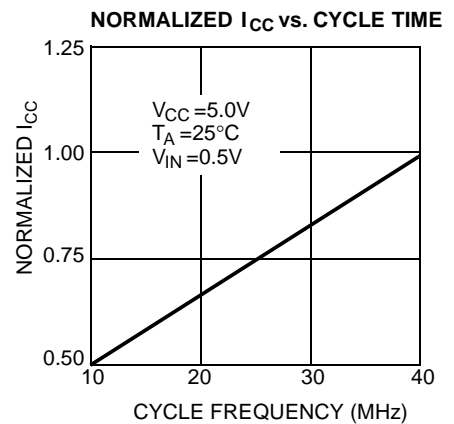
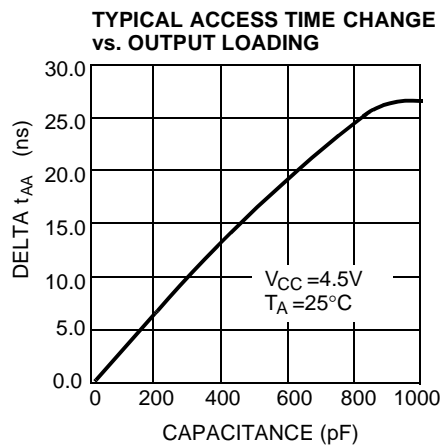
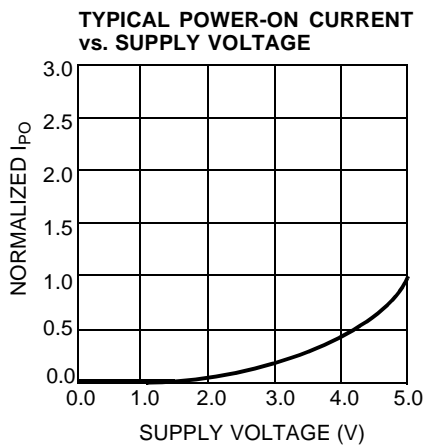
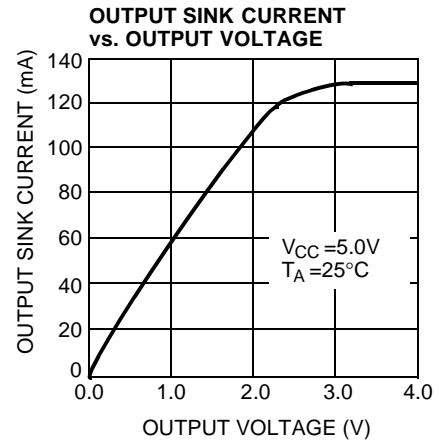
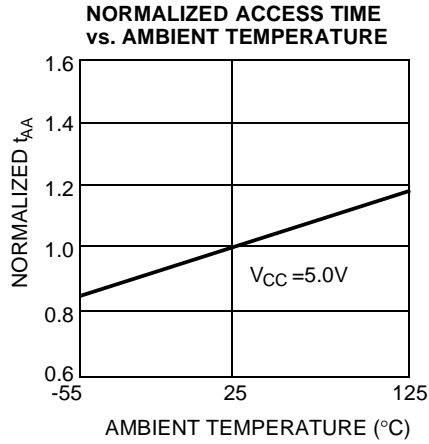
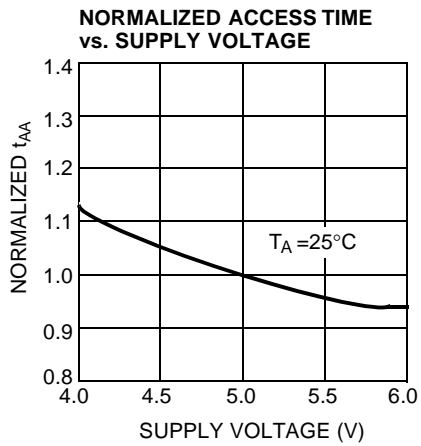
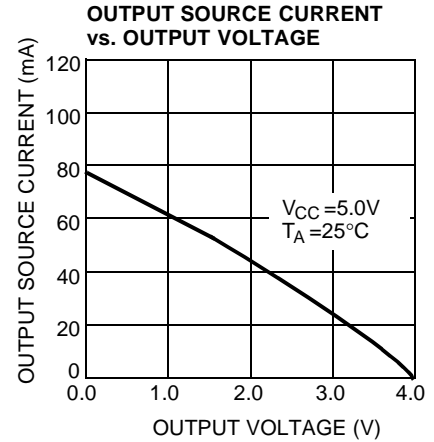
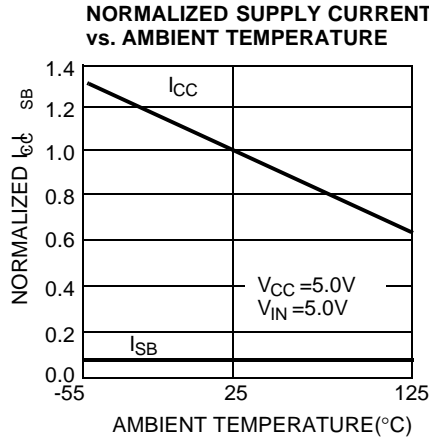
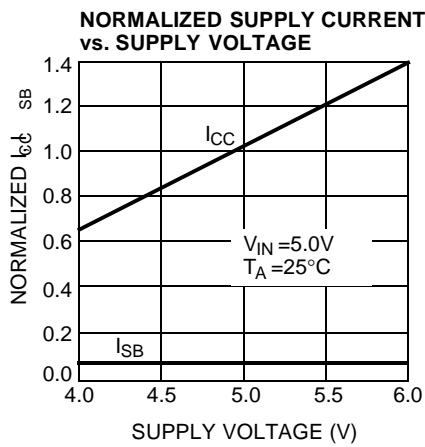
Write Cycle No. 2 ( $\overline{CE}$  Controlled)<sup>[9, 13]</sup>



C191-9

Notes:

- 13. If  $\overline{CE}$  goes HIGH simultaneously with  $\overline{WE}$  HIGH, the output remains in a high-impedance state.

**Typical DC and AC Characteristics**


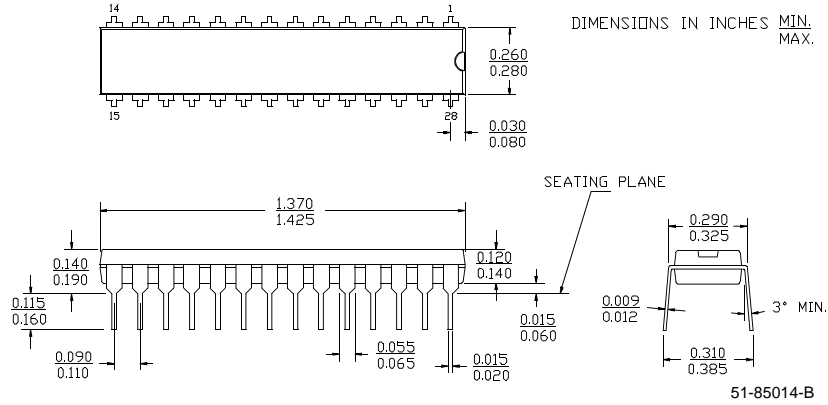
**Ordering Information**

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
12	CY7C192-12PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C192-12VC	V21	28-Lead Molded SOJ	
15	CY7C192-15PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C192-15VC	V21	28-Lead Molded SOJ	
20	CY7C192-20PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C192-20VC	V21	28-Lead Molded SOJ	
25	CY7C192-25PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C192-25VC	V21	28-Lead Molded SOJ	



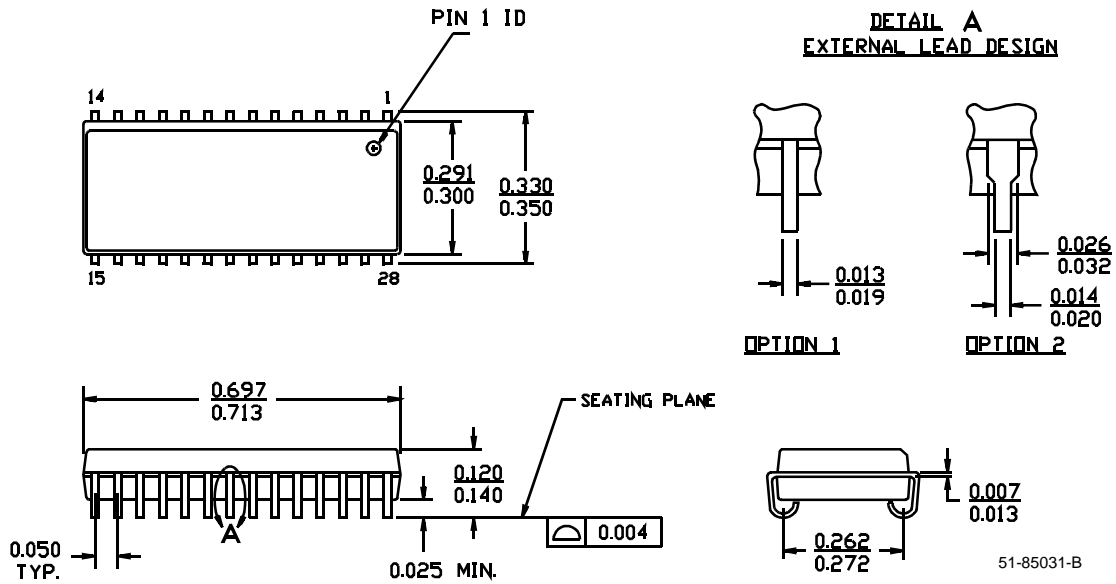
Package Diagrams

28-Lead (300-Mil) Molded DIP P21



28-Lead (300-Mil) Molded SOJ V21

DIMENSIONS IN INCHES MIN. MAX.



Document Title: CY7C192 64K x 4 Static RAM with Separate I/O  
Document Number: 38-05047

REV.	ECN NO.	Issue Date	Orig. of Change	Description of Change
**	107149	09/10/01	SZV	Change Spec number from: 38-00076 to 38-05047