APPROVAL SHEET

RF Switch Series – RoHS Complianc

DP21T MIPI Switch

Halogens Free Product

Any 2G/3G/4G Handset Application

P/N: RMASMS535ATF03

*Contents in this sheet are subject to change without prior notice.

FEATURES

- Low Insertion Loss and Low Distortion
- Broadband frequency range：0.4 to 2.7 GHz
- High Isolation and linearity
- Integrated MIPI RFFE Slave Controller
- High ESD tolerance of 2kV HBM at all pins
- Small LGA package(28-pin, 3.6 x 2.8 x 0.85 mm^3)
- **M**oisture **S**ensitive **L**evel 3 (MSL3)

Description

- The RMASMS535ATF03 is an SP12T and SP9T antenna switch with an integrated Mobile Industry Processor Interface (MIPI) controller. Using an advanced switching technology, the RMASMS535ATF03 maintains low insertion and high isolation, which makes it an ideal choice for UMTS, CDMA2000, EDGE, GSM, and LTE applications.
- The design integrated twenty one low loss TRX ports. The switch also has an excellent 2^{nd}/3^{rd} Order Intermodulation Distortion (IMD2/IMD3) performance.
- Switching is controlled by the MIPI decoder and High ESD tolerance of 2kV HBM at all pins.
- No blocking capacitor requirements on the RF paths as long as no DC voltage is applied. The RMASMS535ATF03 is manufactured in a compact, 3.6 x 2.8 x 0.85 mm^3 package.
- The functional block diagram is shown in Figure 1. The pin assignment and package are shown in Figure 2. Signal pin assignments and functional pin descriptions are provided in Table 1.

Application

- 2G/3G/4G multimode cellular handsets (LTE, UMTS, CDMA2000, EDGE, GSM, TDD-LTE, TD-SCDMA)
- Carrier aggregation

Block Diagram and Pin Out (Top View)

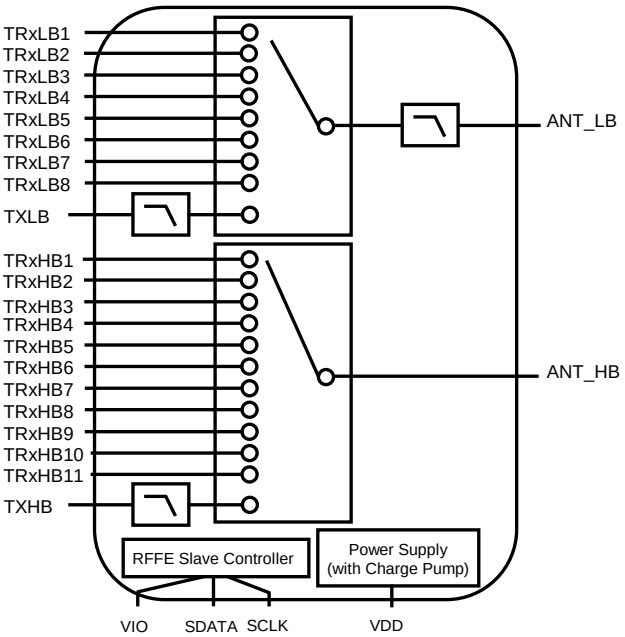


Figure 1. RMASMS535ATF03 Block Diagram

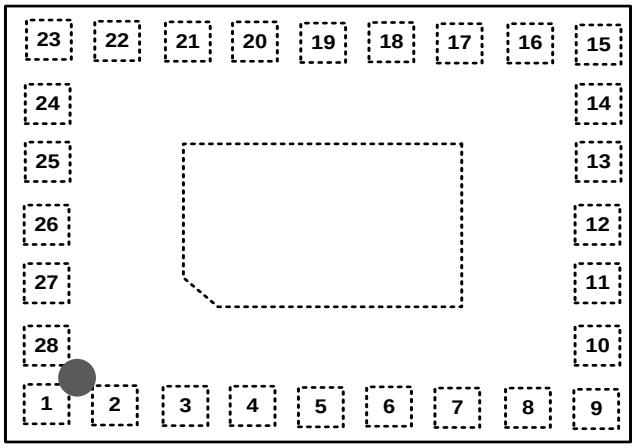


Figure 2. RMASMS535ATF03 Pin assignment

Table 1. RMASMS535ATF03 Pin Descriptions

Pin #	Name	Description	Pin #	Name	Description
1	TRxHB9	HB transmit/receive arm 9	15	TRxLB2	LB transmit/receive arm 2
2	TRxHB10	HB transmit/receive arm 10	16	TRxLB1	LB transmit/receive arm 1
3	TRxHB11	HB transmit/receive arm 11	17	ANT_LB	Antenna low band
4	TxHB	GSM high band TX	18	VIO	MIPI decoder enable voltage
5	SDATA	RFFE Data Input	19	VDD	DC power supply
6	SCLK	RFFE Clock Input	20	ANT_HB	Antenna high band
7	GND	Ground	21	TRxHB1	HB transmit/receive arm 1
8	TxLB	GSM low band TX	22	TRxHB2	HB transmit/receive arm 2
9	TRxLB8	LB transmit/receive arm 8	23	TRxHB3	HB transmit/receive arm 3
10	TRxLB7	LB transmit/receive arm 7	24	TRxHB4	HB transmit/receive arm 4
11	TRxLB6	LB transmit/receive arm 6	25	TRxHB5	HB transmit/receive arm 5
12	TRxLB5	LB transmit/receive arm 5	26	TRxHB6	HB transmit/receive arm 6
13	TRxLB4	LB transmit/receive arm 4	27	TRxHB7	HB transmit/receive arm 7
14	TRxLB3	LB transmit/receive arm 3	28	TRxHB8	HB transmit/receive arm 8

Note 1：Bottom ground paddles must be connected to ground.

Application Circuit

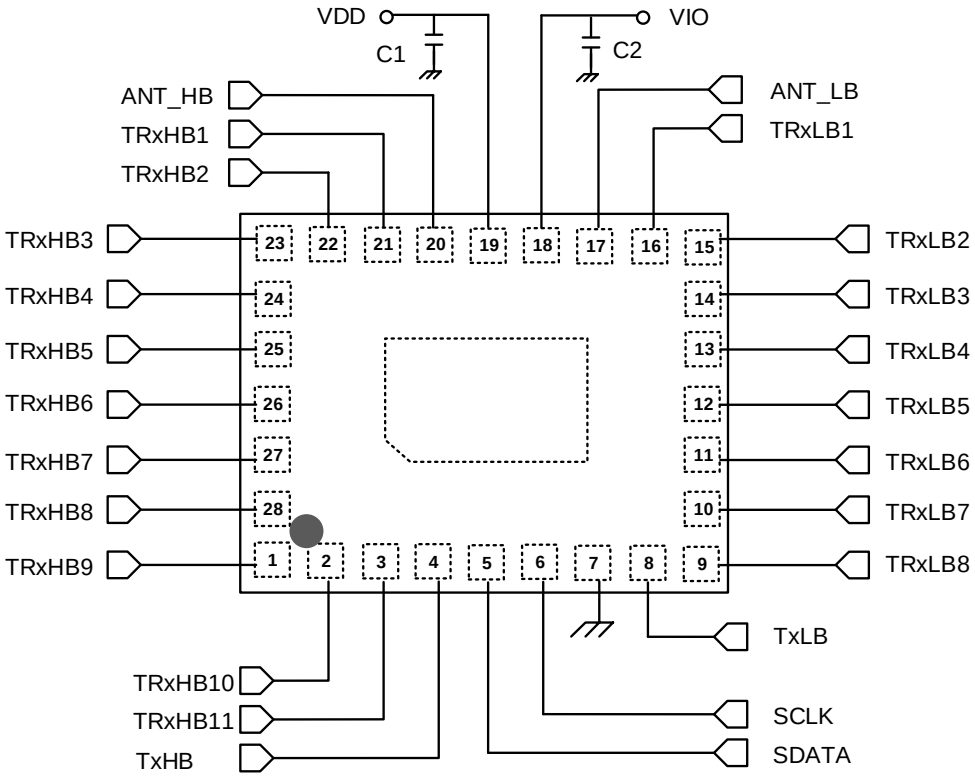


Figure 3. RMASMS535ATF03 Application Circuit

Parts List

Parts No.	Value
C1-C2	0.1 μF

Table 2. RMASMS535ATF03 Absolute Maximum Ratings

Parameter	Symbol	Minimum	Maximum	Units
Supply Voltage	VDD		5.5	V
Interface Supply Voltage	VIO		2	V
Control Input/ Output Voltage Range (SDATA, SCLK)	V_{IN_OUT}		2	V
TRXx Input Power (f = 824 ~ 915 MHz, 50Ω, Duty = 50%)	PIN		37	dBm
TRXx Input Power (f = 1710 ~ 1910 MHz, 50Ω, Duty = 50%)			35	dBm
TRXx Input Power (f = 698 ~ 2690 MHz, 50Ω, CW)			33	dBm
Storage temperature	T_{STG}	-45	+125	°C
Operating temperature	T_{OP}	-30	+90	°C
HBM ESD Voltage, All Pins	V_{ESD}[1]		2000	V
MM ESD Voltage, All Pins	V_{ESD}[2]		190	V

Note 1 : Human Body Model ESD Voltage (HBM, JEITA EIAJ ED-4701)
Note 2 : Machine Model ESD Voltage (MM, JEITA EIAJ ED-4701)
Exceeding absolute maximum ratings may cause permanent damage. Operation between operating range maximum and absolute maximum for extended periods may reduce reliability.

Electrical and Mechanical Specifications

- The absolute maximum ratings of the RMASMS535ATF03 are provided in Table 2. Electrical specifications are provided in Tables 3 and 5.
- Figure 4, 5 and Table4 describes the RMASMS535ATF03 has four operating states.
- IMD2 and IMD3 test conditions for various frequencies are listed in Tables 6 and 7, respectively.
- Figure 6, 7, 8, 9 and Table8 show the important parameters for SCLK and SDATA required for proper operations of the Toshiba MIPI RFFE slave interface.
- Table 9 register mapping shows the list of the registers inside the RMASMS535ATF03.
- Table 10, 11 provides the switch control register.
- Table 12, 13 and 14 describes the detail information of RFFE status, power mode and trigger states, respectively.
- Figure 10 and Table 15 describes the solder land pad and dimensions.

Table 3. RMASMS535ATF03 DC Electrical Specifications (Note 1)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	V_{DD}	2.5	2.85	4.8	V
Supply current, active mode (VDD=2.85V)	I_{DD}		80		μA
Interface supply voltage	VIO	1.65	1.80	1.95	V
Interface signal: High Low	SDATA	 0.8 × VIO 0		 0.2 × VIO	 V V
Control current: High Low	I_{VIO}		9		μA

Note 1 : Performance is guaranteed only under the conditions listed in this Table.

Operating States

The RMASMS535ATF03 has four operating states, that are ACTIVE, SHUTDOWN, STATUP and LOW POWER. The transitions between these four states are set writing the PWR_MODE register or VIO as shown in Figure 4. The internal circuit operations in each operating state are shown in Table 4.

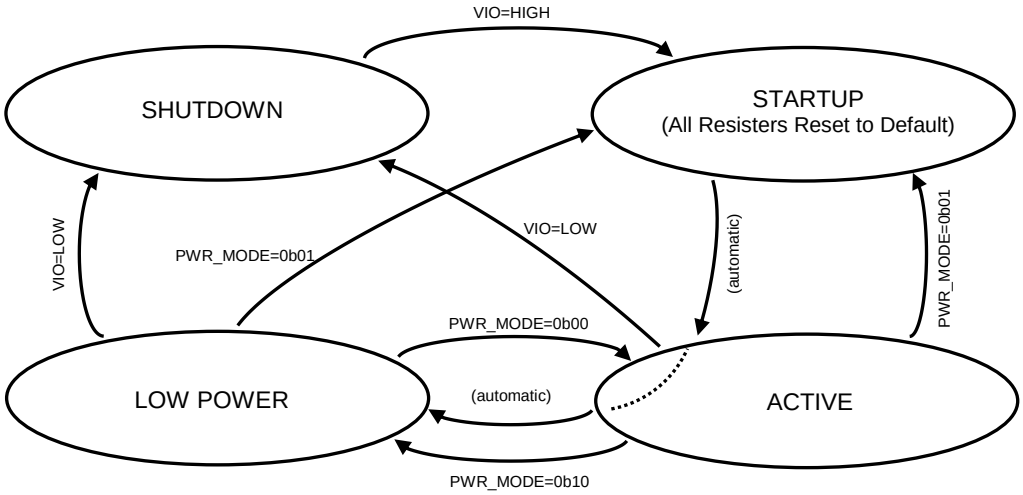


Figure 4. Slave State Diagram

Table 4. RMASMS535ATF03 Internal Operations (Note 1)

Operating State	RFFE Slave Controller	RF Switch Core	Charge Pump
SHUTSOWN	Inactive	Undetermined (Note1)	Off
STARTUP	All registers are set to Default value	Undetermined (Note1)	Off
ACTIVE	Active	Controllable by mipi-command	On
LOW POWER	Active	Undetermined (Note1)	Off

Note 1 : All switch are insufficiently On or Off as the Charge pump is not powered up.

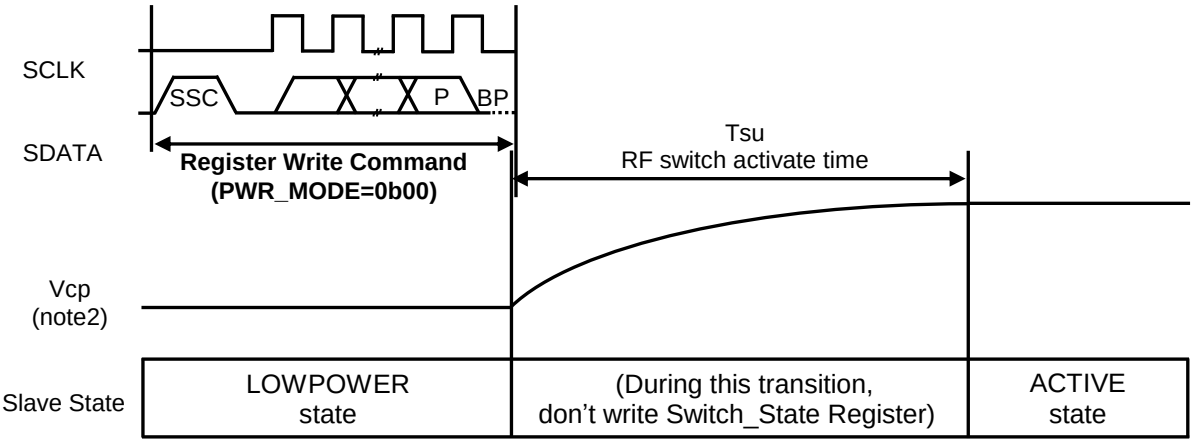


Figure 5. LOW POWER to AVTIVE Process

Note 2 : Vcp is the output voltage of internal charge-pump circuit. The Vcp traces in above figure are only image for illustrative purpose.

Table 5. RMASMS535ATF03 RF Electrical Specifications (Note 1)

(T_{op}= 25°C, VDD = 2.85 V, VIO=1.8V, Characteristic Impedance Z_O= 50 Ω, Unless Otherwise Noted)

Parameter	Symbol	Test Condition	Min	Typ.	Max	Units
Operating frequency	f		0.7		3.0	GHz
Insertion loss	IL	TxLB, 824 to 915 MHz		1.0	1.3	dB
		TxLB1 to B8, 704 to 960 MHz		0.65	1.0	dB
		TxHB, 1710 to 1910 MHz		1.1	1.5	dB
		TxHB1 to B11, 1710 to 2170 MHz		0.8	1.35	dB
		TxHB1 to B11, 2170 to 2690 MHz		1.1	1.55	dB
Isolation (TRx to any off TRx ports) [Non-adjacent ports]	Iso	700 to 960 MHz 960 to 1910 MHz 1910 to 2690 MHz	23 17 15	33 25 23		dB dB dB
Isolation (TRx to any off TRx ports) [Adjacent ports]	Iso	700 to 960 MHz 960 to 1910 MHz 1910 to 2690 MHz	21 15 14	26 20 17		dB dB dB
On state match	VSWR	Up to 2.7 GHz		2		-
TRxLBx harmonics	2fo	TRxLB1 to 8, PIN= +25 dBm, f= 900MHz		-65		dBm
	3fo			-70		dBm
Input power P1dB Compression Point	P_{1dB}	f=900MHz		38		dBm
Turn-on time	t_{ON}	From application of VDD and VIO		10	20	µs
Switching speed	t_S	Port to port		2		µs
GSM Attenuation	TxLB, 2f0, 1648 to 1830 MHz		20	26		dB
	TxLB, 3f0, 2472 to 2745 MHz		25	28		dB
	TxHB, 2f0, 3420 to 3820 MHz		20	26		dB
	TxHB, 3f0, 5130 to 5730 MHz		25	28		dB

Note 1 : Performance is guaranteed only under the conditions listed in this Table.

Table 6. IMD2 Test Conditions

Band	Transmit Frequency (MHz)	Transmit Power (dBm)	Frequency Blocker, Low (MHz)	Frequency Blocker, High (MHz)	Power Blocker (dBm)	Receive Frequency (MHz)
1	1950.0	+20	190	4090	–15	2140.0
2	1880.0		80	3840		1960.0
4	1732.0		400	3864		2132.0
5	836.5		45	1718		881.5
7	2535.0		120	5187		2655.0
8	897.0		45	1839		942.0

Table 7. IMD3 Test Conditions

Band	Transmit Frequency (MHz)	Transmit Power (dBm)	Frequency Blocker (MHz)	Power Blocker (dBm)	Receive Frequency (MHz)
1	1950.0	+20	1760.0	–15	2140.0
2	1880.0		1800.0		1960.0
4	1732.0		1332.0		2132.0
5	836.5		791.5		881.5
7	2535.0		2415.0		2655.0
8	897.0		852.0		942.0

Table 8. Digital Interface Timing Specifications

(T_{op}= 25°C, VDD = 2.85 V, VIO=1.8V, Characteristic Impedance Z_O= 50 Ω, Unless Otherwise Noted)

Parameter	Symbol	Condition	Min.	Max.	Unit
Data Setup Time (Note 1)	T_S	See the Figure 6, input Tr/Tf = 3.5 to 6.5ns	1	-	ns
Data Hold Time (Note 1)	T_H	See the Figure 6, input Tr/Tf = 3.5 to 6.5ns	5	-	ns
Time for Data Output Valid from SCLK rising edge (Note 2)	T_D	Half Speed Read See the Figure 6 and 7, input Tr/Tf = 3.5 to 10ns	0	22	ns
SDATA Output Transition (Rise/Fall) Time	$T_{SDATAOTR}$	Half Speed Read See the Figure 6 and 7, input Tr/Tf = 3.5 to 10ns	2.1	10	ns
Data Drive Release Time	T_{SDATAZ}	Half Speed Read See the Figure 6 and 7, input Tr/Tf = 3.5 to 10ns	-	18	ns
Vio Supply Rise Time	T_{VIO-R}	See the Figure 8	-	400	µs
RFFE I/O Voltage Reset Timing	$T_{VIO-RST}$	See the Figure 8	10	-	µs
Signal Reset Delay Time	T_{SIGOL}	See the Figure 8	120	-	µs
RF Switching Time	T_{SW}	See the Figure 9	-	5	µs
Switching Interval (Note 3)	T_{int}	See the Figure 9	20	-	µs
Startup Time (Note 4)	T_{SU}	See the Figure 4	-	20	µs

Note 1 : Input SDATA is sampled at the falling edge of the SCLK.
Note 2 : Output SDATA changes at the rising edge of the SCLK.
Note 3 : The time between the consecutive Register Write Command Sequences for the Switch State register.
Note 4 : The time for the switch to reach Active State.

Note : The table of input SCLK signal conditions as below.

Parameter	Symbol	Ratings		Unit
SCLK Frequency	F_{SCLK}	Full Speed	0.032 to 26	MHz
		Half Speed	0.032 to 13	
SCLK Period	T_{SCLK}	Full Speed	0.038 to 32	µs
		Half Speed	0.077 to 32	
SCLK Rise/Fall Time	$T_{SCLKITR}$	Full/Half Speed	3.5 to 6.5	ns
SCLK Input Duty Cycle, High/Low Time	$T_{SCLKDCH}$ $T_{SCLKDCL}$	50		%

AC Waveforms

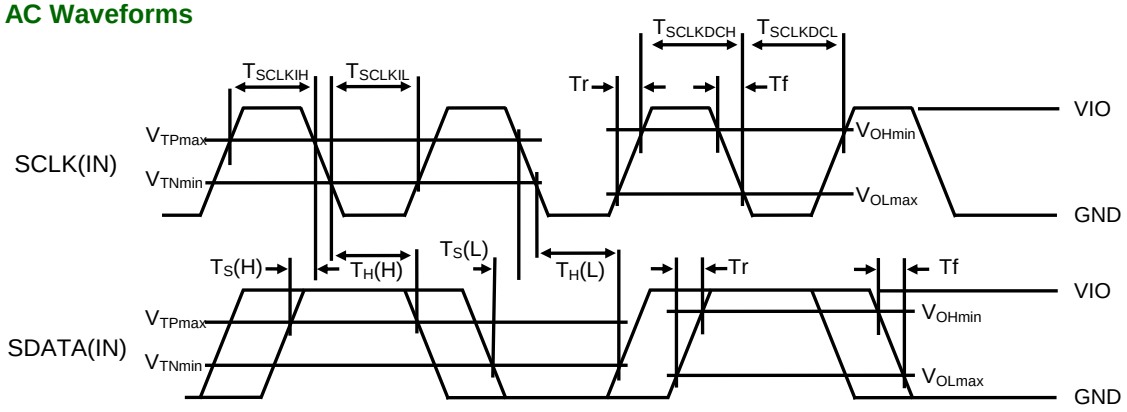


Figure 6. T_{SCLKDH}, $T_{SCLKDCL}$, T_{SCLKIH}, T_{SCLKIL}, T_S, T_H

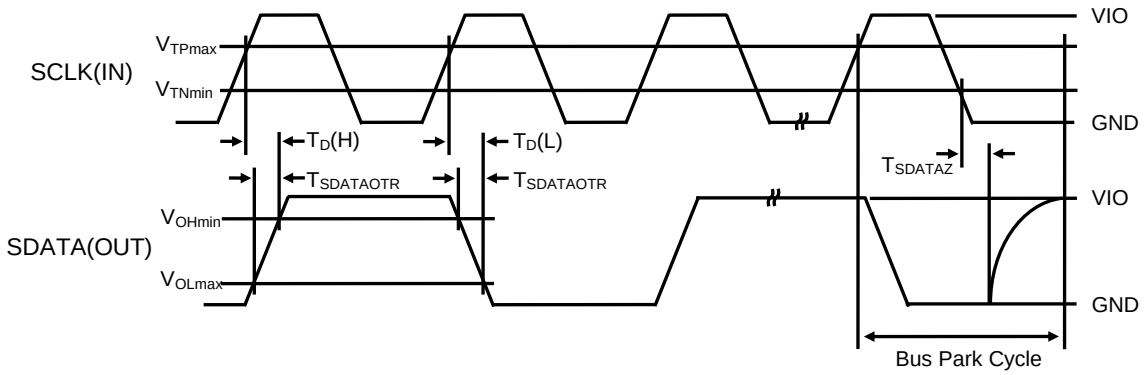


Figure 7. T_D, $T_{SDATAOTR}$, T_{SDATAZ}

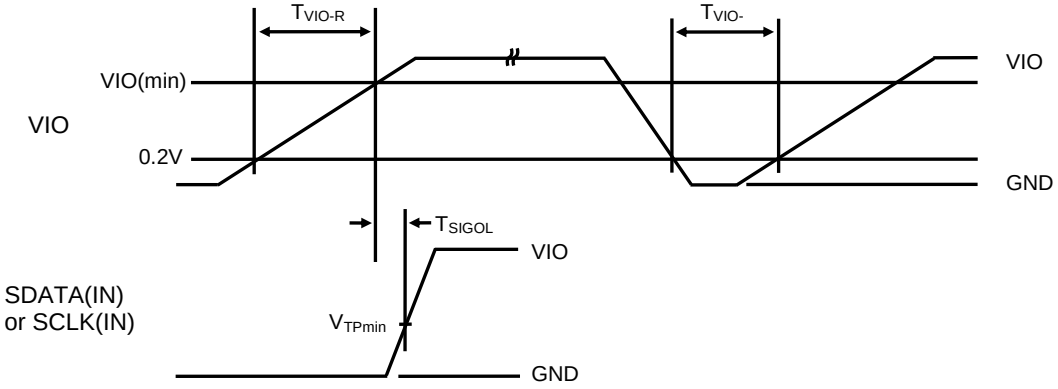


Figure 8. T_{VIO-R}, $T_{VIO-RST}$, T_{SIGOL}

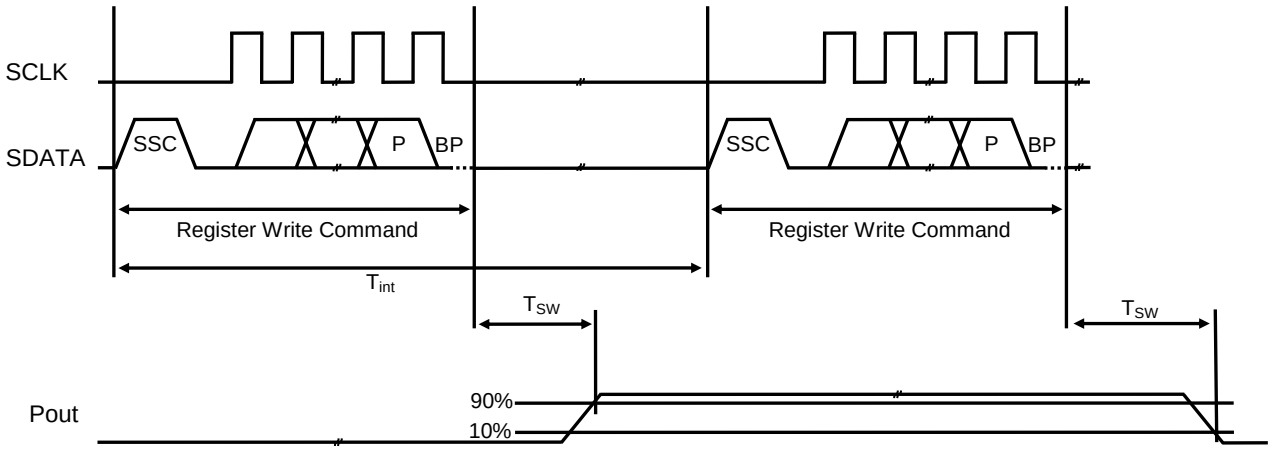


Figure 9. RF Switch Timing

Table 9. Register Mapping

Table 9. shows the list of the registers inside the RMASMS535ATF03.

Register Address		Bits	Read/Write	Description	Default Value (binary)
Hex	Binary				
0x00	00000	[7:0]	R/W	LB Switch Control Register	See Table 10
0x01	00001	[7:0]	R/W	HB Switch Control Register	See Table 11
0x1A	11010	[7:0]	R/W	RFFE Status (see Table 12)	0000 0000
0x1B	11011	[3:0]	R/W	GSID	0000 0000
0x1C	11100	[7:6] [5:0]	R/W	Power Mode (see Table 13) Triggers (see Table 14)	00 000000
0x1D	11101	[7:0]	R	Product ID	0011 1101
0x1E	11110	[7:0]	R	Manufacturer ID [7:0]	0010 0110
0x1F	11111	[7:6] [5:4] [3:0]	R	SPARE	00
				Manufacturer ID [9:8]	01
				USID	1011

Note : The RMASMS535ATF03 start-up procedure as below description.
The RMASMS535ATF03 requires to be disabled the triggers before programming the switch control registers when RMASMS535ATF03 operating in the active mode. The table of register address setup as below.

Register Address		Bits	Read/Write	Value (binary)
Hex	Binary			
0x1C	11100	[7:6] [5:0]	R/W	00 111000

Table 10. Switch Control Register

Bank A Antenna Path	Register_0 Bits							
	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]
TRxLB1	X	0	0	0	0	0	0	1
TRxLB2	X	0	0	0	0	0	1	0
TRxLB3	X	0	0	0	0	1	0	0
TRxLB4	X	0	0	0	0	1	1	1
TRxLB5	X	0	0	0	1	0	1	1
TRxLB6	X	0	0	1	0	0	0	0
TRxLB7	X	0	0	1	0	1	1	0
TRxLB8	X	0	0	1	1	1	0	1
TXLB	X	1	0	0	0	0	1	1
Isolation mode	X	0	0	0	0	0	0	0
	Define: X= not used							

Table 11. Switch Control Register

Bank B Antenna Path	Register_1 Bits							
	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]
TRxHB1	X	0	0	0	0	0	0	1
TRxHB2	X	0	0	0	0	0	1	0
TRxHB3	X	0	0	0	0	1	0	0
TRxHB4	X	0	0	0	0	1	1	1
TRxHB5	X	0	0	0	1	0	1	1
TRxHB6	X	0	0	1	0	0	0	0
TRxHB7	X	0	0	1	0	1	1	0
TRxHB8	X	0	0	1	1	1	0	1
TRxHB9	X	0	1	0	0	1	0	1
TRxHB10	X	0	1	0	1	1	1	0
TRxHB11	X	0	1	1	1	0	0	0
TXHB	X	1	0	0	0	0	1	1
Isolation mode	X	0	0	0	0	0	0	0
	Define: X= not used							

Table 12. RFFE Status

D[7:0]	Read/Write	Description
D[7]	R/W	SOFTWARE RESET
D[6]	R	COMMAND_FRAME_ PARITY_ERR
D[5]		COMMAND_LENGTH_ERR
D[4]		ADDRESS_FRAME_PARITY_ERR
D[3]		DATA_FRAME_PARITY_ERR
D[2]		READ_UNUSED_REG
D[1]		WRITE_UNUSED_REG
D[0]		BID_GID_ERR

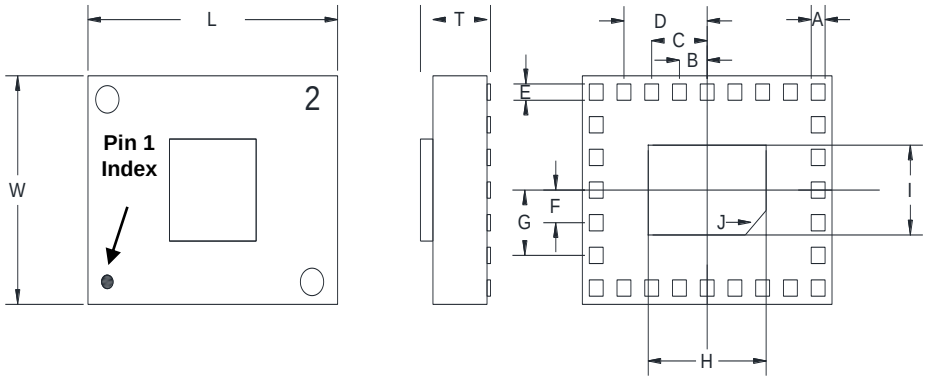
Table 13. Power Mode

D[7:6]	Read/Write	Status
00b	W	Part enters Active mode
	R	Part is in Active mode
01b	W	Part enters Start Up mode - part is reset
	R	Start Up mode will immediately transition to Low Power mode
10b	W	Part enters Low Power mode
	R	Part is in Low Power mode
11b	N/A	Will not occur - The state is discarded
		Will not occur - The state is discarded

Table 14. Trigger States

D[5:0]	Read/Write	Status
D[5]	R/W	1 = Trigger 2 Disabled, 0 = Trigger 2 Enabled
D[4]		1 = Trigger 1 Disabled, 0 = Trigger 1 Enabled
D[3]		1 = Trigger 0 Disabled, 0 = Trigger 0 Enabled
D[2]	W	1 = Load Bits to Trigger 2, Trigger 2 states is Disabled
D[1]		1 = Load Bits to Trigger 1, Trigger 1 states is Disabled
D[0]		1 = Load Bits to Trigger 0, Trigger 0 states is Disabled

Table 15. Dimensions

Figure	Symbol	Dimension
 **Top View** **Side View** **Bottom View**	L	3.60 ± 0.10mm
	W	2.80 ± 0.10mm
	T	0.85 ± 0.05mm
	A	0.20 ± 0.10mm
	B	0.40 ± 0.10mm
	C	0.80 ± 0.10mm
	D	1.20 ± 0.10mm
	E	0.20 ± 0.10mm
	F	0.40 ± 0.10mm
	G	0.80 ± 0.10mm
	H	1.50 ± 0.10mm
	I	0.90 ± 0.10mm
	J	0.30 ± 0.05mm

Solder land pattern for reference only

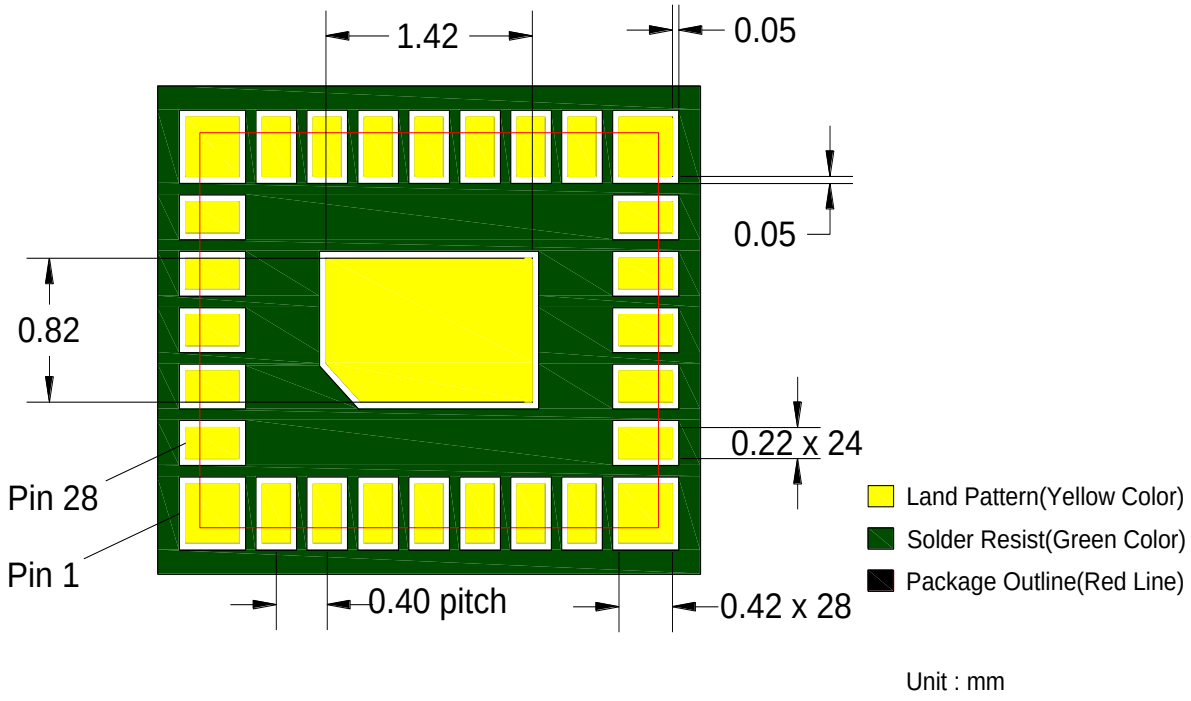


Figure 10. Solder Land Pattern Top View

Reliability test

TEST	PROCEDURE / TEST METHOD	REQUIREMENT
Solderability JIS C 0050-4.6 JESD22-B102D	*Solder bath temperature：255 ± 5°C *Immersion time：5 ± 0.5 sec Solder：Sn3Ag0.5Cu for lead-free	At least 95% of a surface of each terminal electrode must be covered by fresh solder.
High temperature JIS C 0021	*Temperature：90°C±2°C *Test duration：1000+24/-0 hours Measurement to be made after keeping at room temperature for 24±2 hrs	No mechanical damage. Electrical specification shall satisfy the descriptions in electrical characteristics under the operational temperature range within -30 ~ 90°C.
Low temperature JIS C 0020	*Temperature：-30°C±2°C *Test duration：1000+24/-0 hours Measurement to be made after keeping at room temperature for 24±2 hrs	No mechanical damage. Electrical specification shall satisfy the descriptions in electrical characteristics under the operational temperature range within -30 ~ 90°C.
Temperature cycle JIS C 0025	1. 30±3 minutes at -30±3°C, 2. 10~15 minutes at room temperature, 3. 30±3 minutes at +90±3°C, 4. 10~15 minutes at room temperature, Total 100 continuous cycles Measurement to be made after keeping at room temperature for 24±2 hrs	No mechanical damage. Electrical specification shall satisfy the descriptions in electrical characteristics under the operational temperature range within -30 ~ 90°C.
High temperature operation life (HTOL)	*Temperature：90°C *VDD = 5.5V *Time：1000+24/-0 hrs. Measurement to be made after keeping at room temperature for 24±2 hrs	No mechanical damage. Electrical specification shall satisfy the descriptions in electrical characteristics under the operational temperature range within -30 ~ 90°C.

Soldering condition

Typical examples of soldering processes that provide reliable joints without any damage are given in Figure 11.

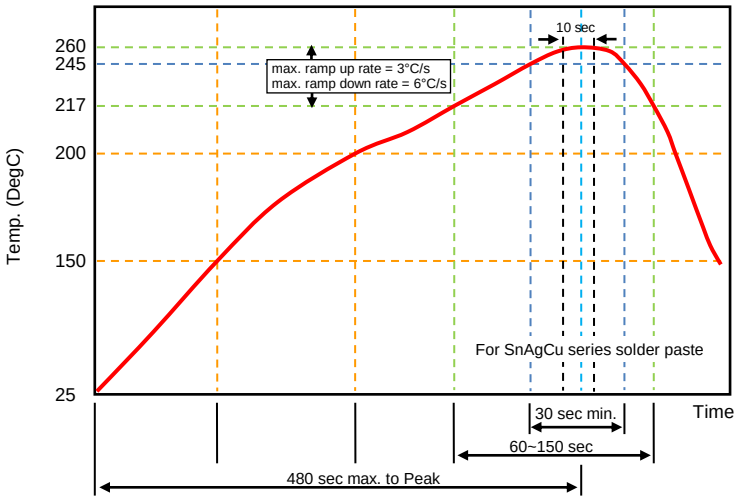


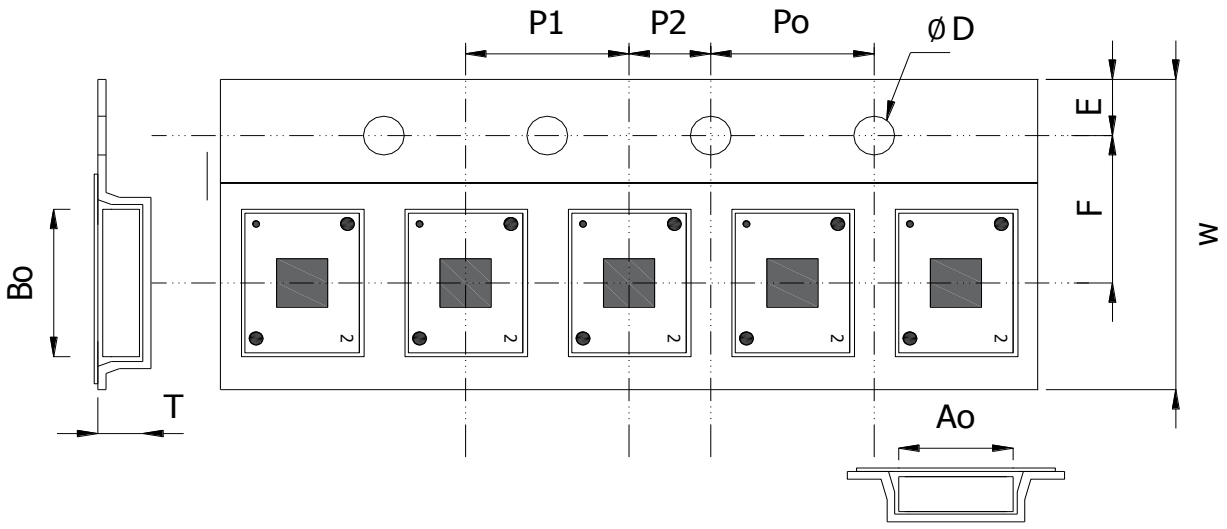
Figure 11. Infrared soldering profile

Ordering code

RM	ASM	S	535A	T
RF module RM: Walsin RF Module Device	**Module type** ASM: Antenna Switch Module	**Application** S: DP21T	**Design Code**	**Packing** T: Taping

Minimum Ordering Quantity: 3000 pcs per reel.

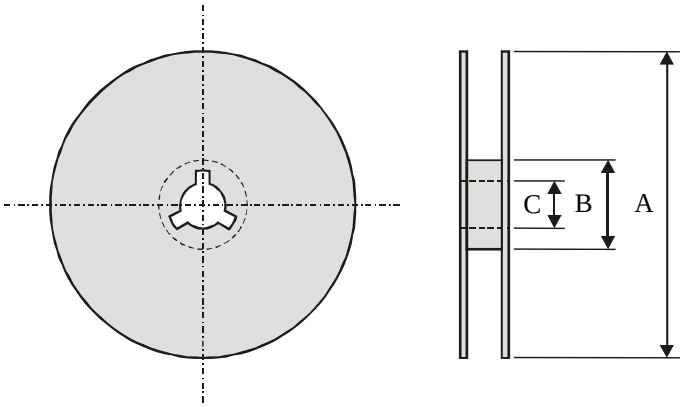
Packaging



Plastic Tape specifications (unit :mm)

Index	Ao	Bo	ΦD	T	W
Dimension (mm)	3.00 ± 0.10	3.8 ± 0.10	1.50 ± 0.05	1.05 ± 0.10	12.0 ± 0.20
Index	E	F	Po	P1	P2
Dimension (mm)	1.75 ± 0.10	5.50 ± 0.10	4.00 ± 0.10	4.00 ± 0.10	2.00 ± 0.05

Reel dimensions



Index	A	B	C
Dimension (mm)	Φ178.0	Φ60.0	Φ13.0

Taping Quantity : 3000 pieces per 7” reel

Caution of handling

Limitation of Applications

Please contact us before using our products for the applications listed below which require especially high reliability for the prevention of defects, which might directly cause damage to the third party's life, body or property.

(1) Aircraft equipment
(2) Aerospace equipment
(3) Undersea equipment
(4) Medical equipment
(5) Disaster prevention / crime prevention equipment
(6) Traffic signal equipment
(7) Transportation equipment (vehicles, trains, ships, etc.)
(8) Applications of similar complexity and /or reliability requirements to the applications listed in the above.

Storage condition

(1) Products should be used in 6 months from the day of WALSIN outgoing inspection, which can be confirmed.

(2) Storage environment condition.

- Products should be storage in the warehouse on the following conditions.
- Temperature : -10 to +40°C
- Humidity : 30 to 70% relative humidity
- Don't keep products in corrosive gases such as sulfur. Chlorine gas or acid or it may cause oxidization of electrode, resulting in poor solderability.
- Products should be storage on the palette for the prevention of the influence from humidity, dust and son on.
- Products should be storage in the warehouse without heat shock, vibration, direct sunlight and so on.
- Products should be storage under the airtight packaged condition.