M5M29KE131BTP

**134,217,728-BIT (16,777,216-WORD BY 8-BIT / 8,388,608-WORD BY 16-BIT)
CMOS FLASH MEMORY**

Stacked-uMCP (micro Multi Chip Package)

DESCRIPTION

The M5M29KE131BTP is a Stacked micro Multi Chip Package that contents 2 Dies of 64M-bit Flash memory in a 52-pin TSOP(II) for lead free use.

128M-bit Flash memory is a 16,777,216 bytes / 8,388,608 words, single power supply and high performance non-volatile memory fabricated by CMOS technology for the peripheral circuit and DINOR IV (Divided bit-line NOR IV) architecture for the memory cell. All memory blocks are locked and can not be programmed or erased, when WP# is Low. Using Software Lock Release function, program or erase operation can be executed.

The M5M29KE131BTP is suitable for a high performance cellular phone and a mobile PC that are required to be small mounting area, weight and small power dissipation.

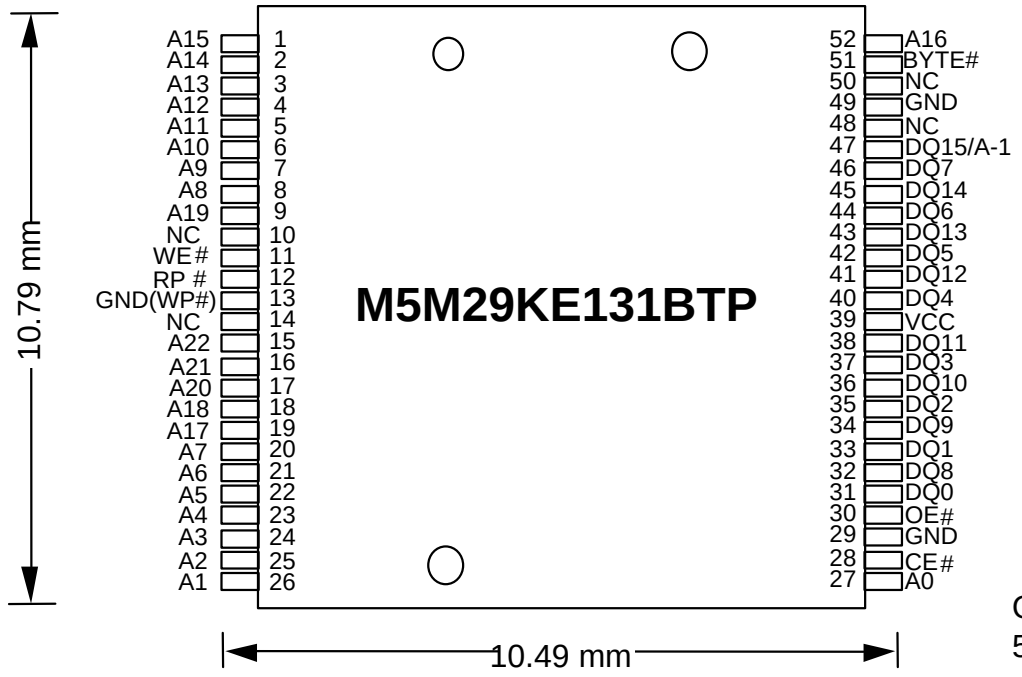
FEATURES

Access time	Random	70ns (Max.)
	Page	25ns(Max.)
Supply voltage		VCC= 3.0 ~ 3.6V
Ambient temperature		Ta=-40 ~ 85 °C
Package		52pin TSOP(Type-II), Lead pitch 0.4mm
		Outer-lead finishing : Sn-Cu

APPLICATION

Digital Cellar Phone, Telecommunication,
PDA, Car Navigation System, Video Game Machine

PIN CONFIGURATION (TOP VIEW)

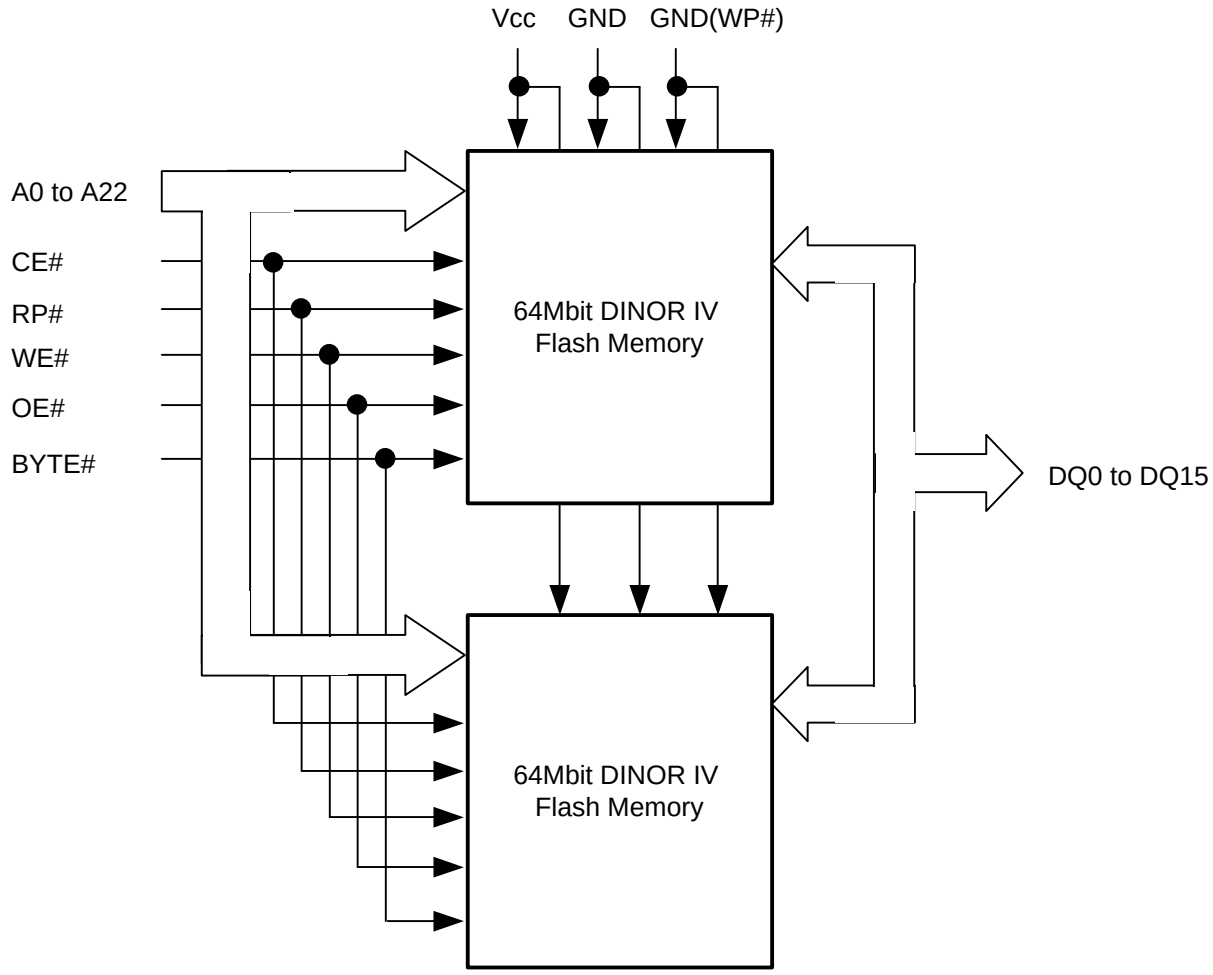


Outline
52PTG-A

VCC	: VCC
GND	: GND
A0-A22	: Address
DQ0-DQ15	: Data I/O
CE#	: Chip enable
OE#	: Output enable
WE#	: Write enable
GND(WP#)	: Write protect (recommend to fix to GND) (Background information No. : REJ06C0052)
RP#	: Reset power down
BYTE#	: Byte enable

Renesas Technology Corp.

MCP Block Diagram



Capacitance

Symbol	Parameter		Conditions	Limits			Unit
				Min.	Typ.	Max.	
CIN	Input capacitance	A22-A0, OE#, WE#, CE#, WP#, RP#,BYTE#	Ta=25°C, f=1MHz, Vin=Vout=0V			24	pF
COUT	Output Capacitance	DQ15-DQ0				24	pF

Flash Memory Part

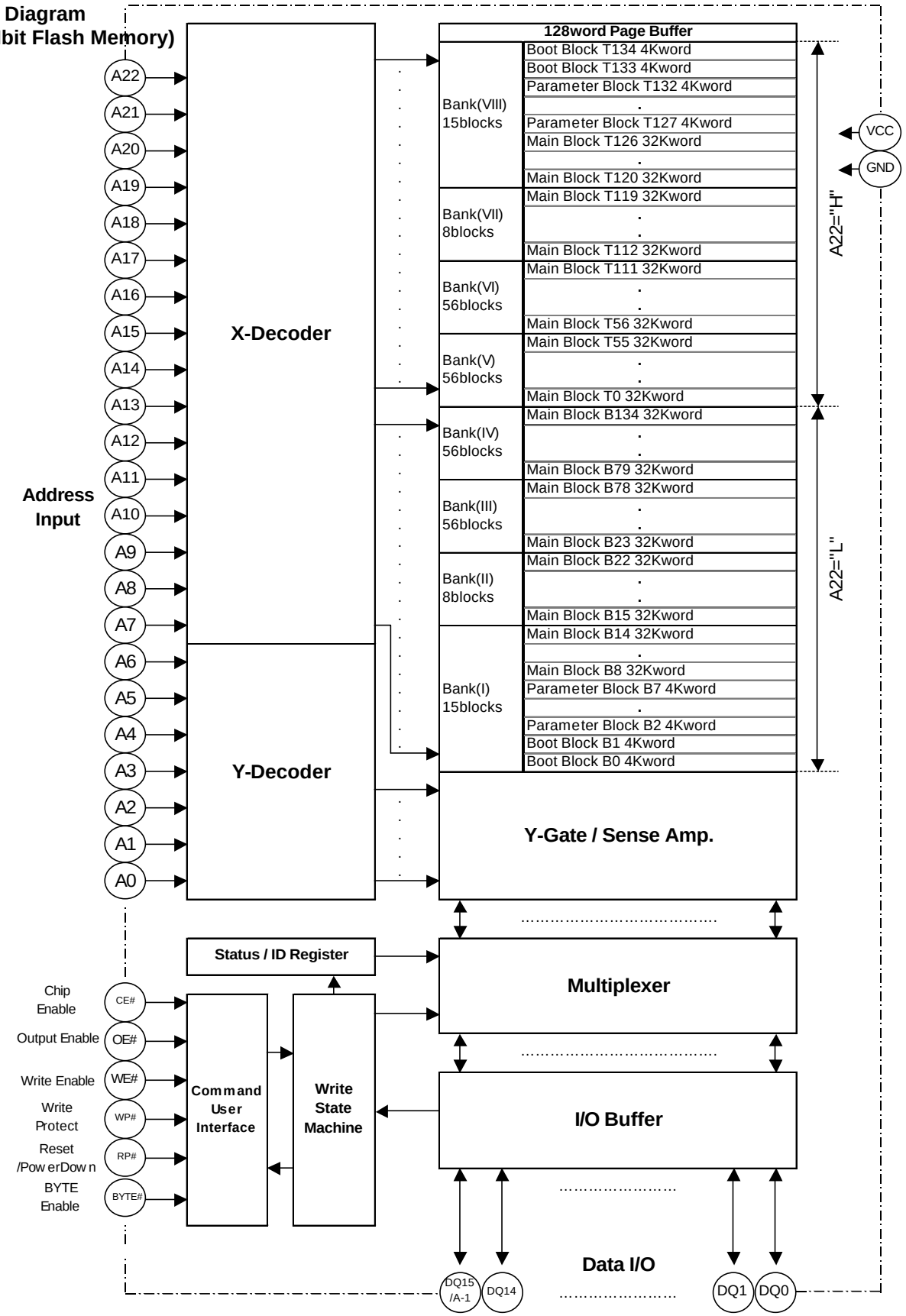
Description

The 128M-bit DINOR IV(Divided bit line NOR IV) Flash Memory is 3.3V-only high speed 134,217,728-bit CMOS boot block Flash Memory. Alternating BGO(Back Ground Operation) feature of the device allows Program or Erase operations to be performed in one bank while the device simultaneously allows Read operations to be performed on the other bank in each 64M-bit area which is selected by A22=L or H. This BGO feature is suitable for communication products and cellular phone.The Flash Memory is fabricated by CMOS technology for the peripheral circuits and DINOR IV architecture for the memory cells.

Features

- Organization 8,388,608-word x 16-bit
  16,777,216-word x 8-bit
- Supply Voltage VCC = 3.0 ~ 3.6V
- Access time
  - Random Access 70ns(Max.)
  - Random Page Read 25ns(Max.)
- Read 108mW (Max. at 5MHz)
- Page Read 36mW (Max.)
  (After Automatic Power Down) 0.66µW(typ.)
- Program/Erase 126mW(Max.)
  - Standby 0.66µW(typ.)
  - Deep Power Down mode 0.66µW(typ.)
- Auto Program for Bank(I) – Bank(IV)
  - Program Time
    - Word Program 30µs/1word(typ.)
    - Byte Program 30µs/1byte(typ.)
    - Page Program 4ms(typ.)
  - Program Unit
    - Word Program 1 word
    - Byte Program 1 byte
    - Page Program 128 words/256 bytes
- Auto Erase
  - Erase time 150ms(typ.)
  - Erase unit
    - Bank(I) ,Bank(VIII)
      - Boot Block 4K-word /8K-byte x 2
      - Parameter Block 4K-word /8K-byte x 6
      - Main Block 32K-word /64K-byte x 7
    - Bank(II) ,Bank(VII)
      - Main Block 32K-word /64K-byte 8
    - Bank(III) ,Bank(VI)
      - Main Block 32K-word /64K-byte x 56
    - Bank(IV) ,Bank(V)
      - Main Block 32K-word /64K-byte x 56
- Program/Erase cycles 100Kcycles
- Dual Boot Block Architecture
  There are Bottom and Top boot blocks in both sides.
  - Bottom Boot (A22=VIL)
  - Top Boot (A22=VIH)
- The Other Functions
  - Software Command Control
  - Quick Data Reclaim
  - Software Lock Release(while WP# is low)
  - Erase Suspend/Resume
  - Program Suspend/Resume
  - Status Register Read
  - Alternating Back Ground Program/Erase Operation
    Among Bank (I)-Bank(IV)
    in Bottom 64Mbit area (A22=VIL),
    Among Bank (V)-Bank(VIII)
    in Top 64Mbit area (A22=VIH)
  - Random Page Read

Block Diagram (128Mbit Flash Memory)



Function of Flash Memory

The 128M-bit DINOR IV Flash Memory includes on-chip program/erase control circuitry. The Write State Machine (WSM) controls block erase and word/page program operations. Operational modes are selected by the commands written to the Command User Interface (CUI). The Status Register indicates the status of the WSM and when the WSM successfully completes the desired program or block erase operation.

A Deep Power Down mode is enabled when the RP# pin is at GND, minimizing power consumption.

Read

The 128M-bit DINOR IV Flash Memory has four read modes, which accesses to the memory array ,the Page read, the Device Identifier and the Status Register. The appropriate read commands are required to be written to the CUI. Upon initial device power up or after exit from deep power down, the 128M-bit DINOR IV Flash Memory automatically resets to read array mode. In the read array mode and in the conditions are low level input to OE#, high level input to WE# and RP#, low level input to CE# and address signals to the address inputs (A22 - A0:Word Mode, A22-A-1:Byte Mode) the data of the addressed location to the data input/output (DQ15-DQ0:Word Mode, DQ7-DQ0:Byte Mode) is output.

Write

Writes to the CUI enables reading of memory array data, device identifiers and reading and clearing of the Status Register. They also enable block erase and program. The CUI is written by bringing WE# to low level and OE# is at high level, while CE# is at low level. Address and data are latched on the earlier rising edge of WE# and CE#. Standard micro processor write timings are used.

Alternating Background Operation (BGO)

The 128M-bit DINOR IV Flash Memory allows to read array from one bank while the other bank operates in software command write cycling or the erasing / programming operation in the background. Array Read operation with the other bank in BGO is performed by changing the bank address without any additional command. When the bank address points the bank in software command write cycling or the erasing / programming operation, the data is read out from the status register. The access time with BGO is the same as the normal read operation.

Output Disable

When OE# is at VIH, output from the devices is disabled. Data input/output are in a high-impedance (High-Z) state.

Standby

When CE# is at VIH, the device is in the standby mode and its power consumption is reduced. Data input/output are in a high-impedance (High-Z) state. If the memory is deselected during block erase or program, the internal control circuits remain active and the device consumes normal active power until the operation completes.

Deep Power Down

When RP# is at VIL, the device is in the deep power down mode and its power consumption is substantially low. During read modes, the memory is deselected and the data input/output are in a high-impedance (High-Z) state. After return from power down, the CUI is reset to Read Array, and the Status Register is cleared to value 80H.

During block erase or program modes, RP# low will abort either operation. Memory array data of the block being altered become invalid.

Automatic Power Down (Auto-PD)

The Automatic Power Down minimizes the power consumption during read mode. The device automatically turns to this mode when any addresses or CE# isn't changed more than 200ns after the last alternation. The power consumption becomes the same as the stand-by mode. During this mode, the output data is latched and can be read out. New data is read out correctly when addresses are changed.

BBR(Back Bank array Read)

In the 128M-bit DINOR IV Flash Memory , when one memory address is read according to a Read Mode in the case of the same as an access when a Read Mode command is input, an another Bank memory data can be read out (Read Array or Page Read) by changing an another Bank address.

Software Command Definitions

The device operations are selected by writing specific software command into the Command User Interface.

Read Array Command (FFH)

The device is in Read Array mode on initial device power up and after exit from deep power down, or by writing FFH to the Command User Interface. After starting the internal operation the device is set to the read status register mode automatically.

Read Device Identifier Command (90H)

We can normally read device identifier codes when Read Device Identifier Code Command (90H) is written to the command latch. Following the command write, the manufacturer code and the device code can be read from A0 address 0H and 1H in a bank address, respectively.

Read Status Register Command (70H)

The Status Register is read after writing the Read Status Register command of 70H to the Command User Interface. Also, after starting the internal operation the device is set to the Read Status Register mode automatically.

The contents of Status Register are latched on the later falling edge of OE# must be toggled every status read.

Page Read Command (F3H)

The Page Read command (F3H) timing can be used by writing the first command to CUI and CE# falls VIL or changing the address(A22-A2) is necessary to start activating page read mode. This command is fast random 4 words read. During the read it is necessary to fix CE# low and change addresses that are defined by A0 and A1(0h - 3h) at random continuously. The mode is kept until RP# is set to L or this chip is powered down.

The first read of Page Read timing is the same as normal read (ta(CE)). CE# should be fallen “L”. The read timing after the first is the same as ta(PAD).

In the page read mode the upper address(A22-A2) or CE# are supposed not to be clocked during read operation. Otherwise the access time is as same as normal read.

Clear Status Register Command (50H)

The Erase Status, Program Status and Block Status bits are set to "1"s by the Write State Machine and can only be reset by the Clear Status Register command of 50H. These bits indicate various failure conditions.

Block Erase / Confirm Command (20H/D0H)

Automated block erase is initiated by writing the Block Erase command of 20H followed by the Confirm command of D0H. An address within the block to be erased is required. The WSM executes iterative erase pulse application and erase verify operation.

Program Commands

A) Word / Byte Program (40H)

Word/Byte program is executed by a two-command sequence. The Word/Byte program Setup command of 40H is written to the Command Interface, followed by a second write specifying the address and data to be written. The WSM controls the program pulse application and verify operation.

B) Page Program for Data Blocks (41H)

Page Program allows fast programming of 128words /256bytes of data. Writing of 41H initiates the page program operation for the Data area. From 2nd cycle to 129th cycle :Word Mode, 257th cycle :Byte Mode, write data must be serially inputted. Address A6-A0:Word Mode, A6-A-1:Byte Mode have to be incremented from 00H to 7FH. After completion of data loading, the WSM controls the program pulse application and verify operation.

C) Single Data Load to Page Buffer (74H) / Page Buffer to Flash (0EH/D0H)

Single data load to the page buffer is performed by writing 74H followed by a second write specifying the column address(A6-A0:Word Mode, A6-A-1:Byte Mode) and data. Distinct data up to 128word/256bytes can be loaded to the page buffer by this two-command sequence. On the other hand, all of the loaded data to the page buffer is programmed simultaneously by writing Page Buffer to Flash command of 0EH followed by the confirm command of D0H. After completion of programming the data on the page buffer is cleared automatically.

Flash to Page Buffer Command (F1H/D0H)

Array data load to the page buffer is performed by writing the Flash to Page Buffer command of F1H followed by the Confirm command of D0H. An address within the page to be loaded is required. Then the array data can be copied into the other pages within the same bank by using the Page Buffer to Flash command.

Clear Page Buffer Command (55H/D0H)

Loaded data to the page buffer is cleared by writing the Clear Page Buffer command of 55H followed by the Confirm command of D0H. This command is valid for clearing data loaded by Single Data Load to Page Buffer command.

Data Protection

The 128M-bit DINOR IV Flash Memory has a master Write Protect pin (WP#). When WP# is at VIH, all blocks can be programmed or erased. When WP# is low, all blocks are in locked mode which prevents any modifications to memory blocks. Software Lock Release function is only command which allows to program or erase.

Suspend/Resume Command (B0H/D0H)

Writing the Suspend command of B0H during block erase operation interrupts the block erase operation and allows read out from another block of memory. Writing the Suspend command of B0H during program operation interrupts the program operation and allows read out from another block of memory. The Bank address is required when writing the Suspend/Resume Command. The device continues to output Status Register data when read, after the Suspend command is written to it. Polling the WSM Status and Suspend Status bits will determine when the erase operation or program operation has been suspended. At this point, writing of the Read Array command to the CUI enables reading data from blocks other than that which is suspended. When the Resume command of D0H is written to the CUI, the WSM will continue with the erase or program processes.

Erase All Unlocked Blocks Command (A7H/D0H)

The command sequence enable us to erase all blocks. The command can be used by writing Setup command A7H(1^{st} cycle) and confirm command D0H(2^{nd} cycle). The sequence is not valid in case of WP#=VIL.

Power Supply Voltage

When the power supply voltage is less than VLKO, Low VCC Lock-Out voltage, the device is set to the Read-only mode.

A delay time of 60µs is required before any device operation is initiated. The delay time is measured from the time Flash VCC reaches Flash VCCmin (3.0V).

During power up, RP# = GND is recommended. Falling in Busy status is not recommended for possibility of damaging the device.

Memory Organization

The 128M-bit DINOR IV Flash Memory is constructed by 2 boot blocks of 4K words, 6 parameter blocks of 4K words and 7 main blocks of 32K words in Bank(I) and Bank(VIII), by 8 main blocks of 32K words in Bank(II) and Bank(VII), and by 56 main blocks of 32K words in Bank(III), BANK(IV) , BANK(V) and Bank(VI).

A block is erased independently of other blocks in the array.

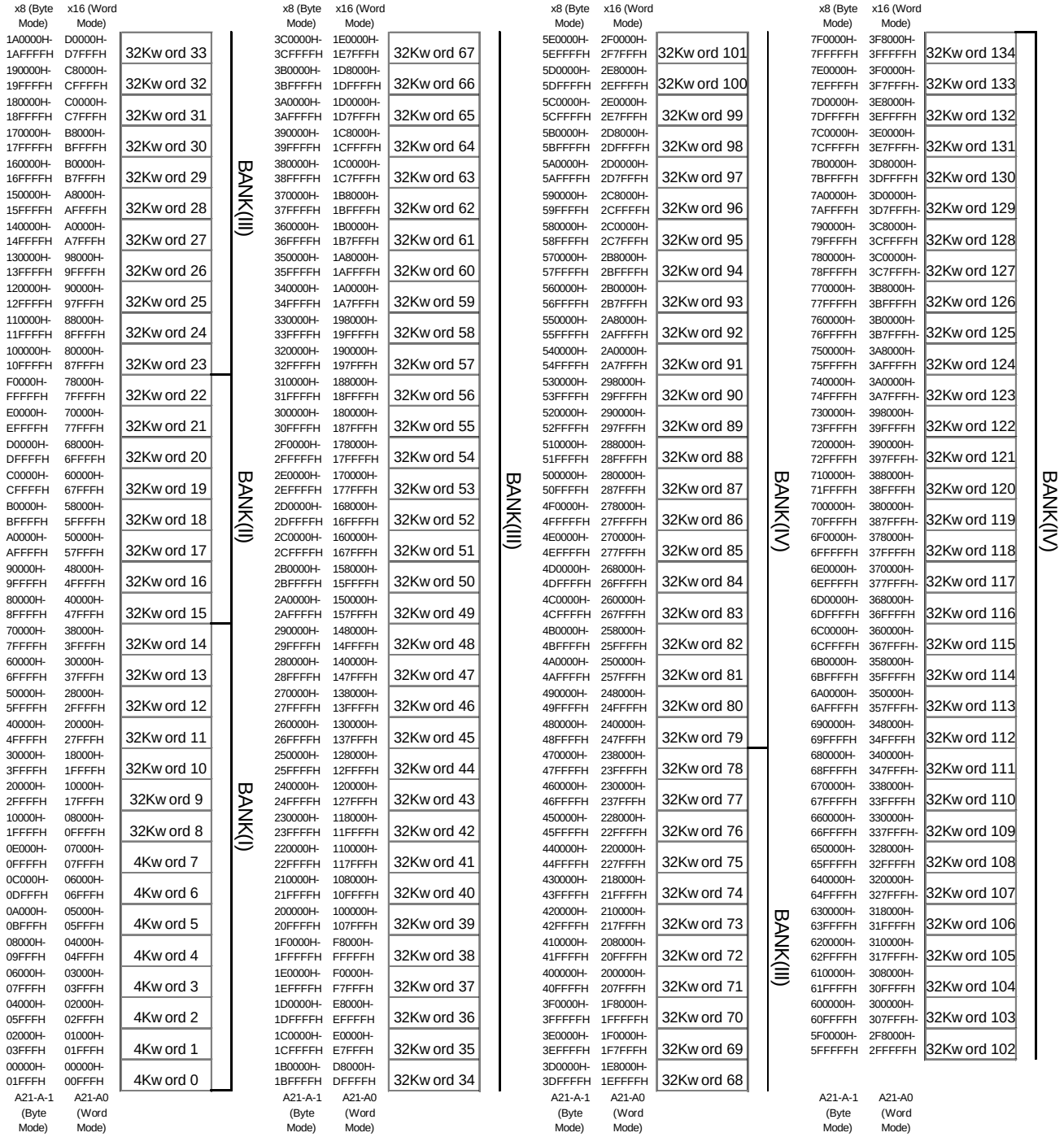
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Stacked-uMCP (micro Multi Chip Package)

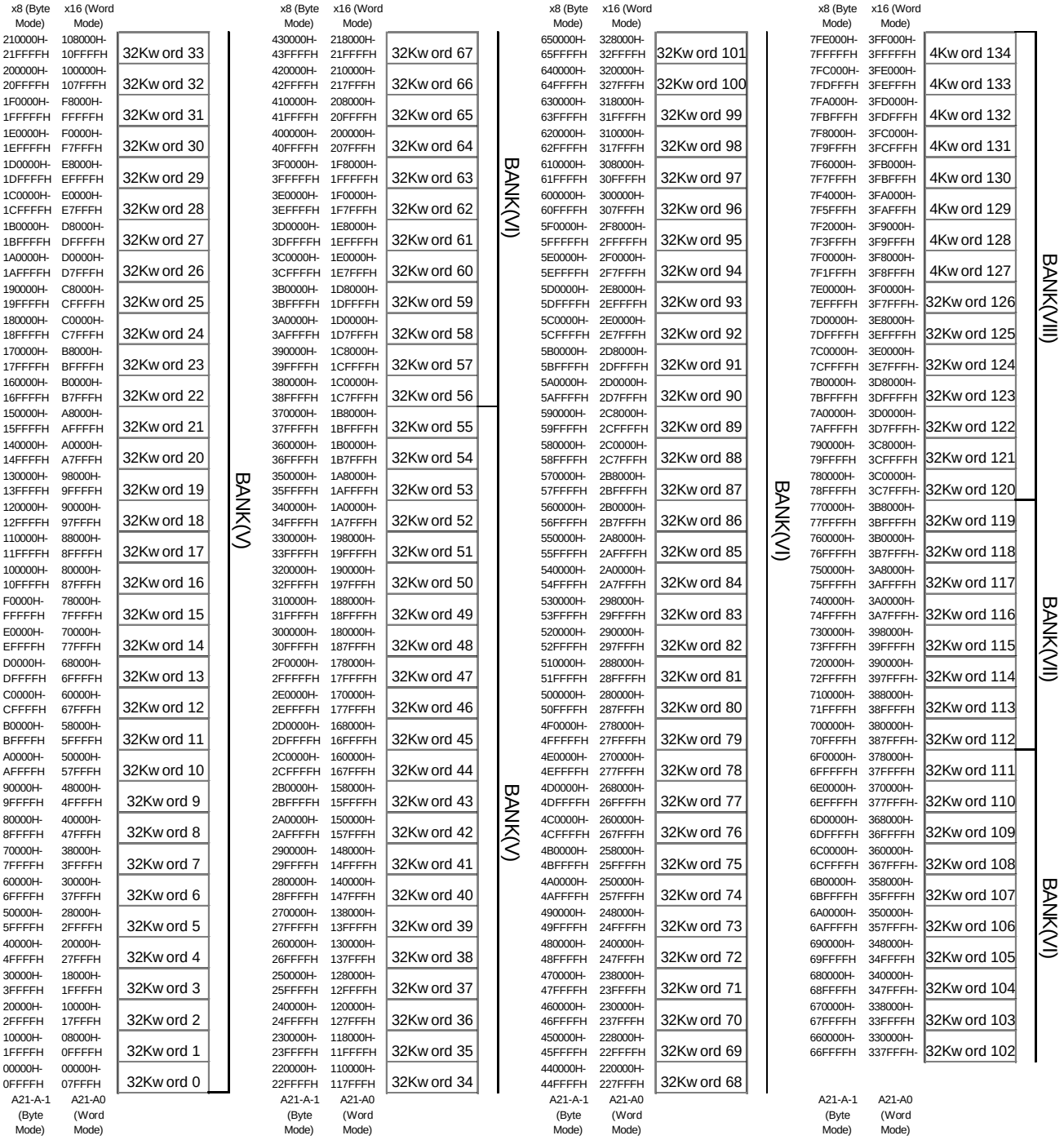
Block Organization

128M-bit DINOR(IV) Flash Memory Map (Bottom 64Mbit / A22=VIL)



Block Organization

128M-bit DINOR(IV) Flash Memory Map (Top 64Mbit / A22=VIH)



Bus Operation

BYTE#=VIH

Mode \ Pins		CE#	OE#	WE#	RP#	DQ0-15
Read	Array	VIL	VIL	VIH	VIH	Data Output
	Status Register	VIL	VIL	VIH	VIH	Status Register Data
	Identifier Code	VIL	VIL	VIH	VIH	Identifier Code
	Page	VIL	VIL	VIH	VIH	Data Output
Output Disable		VIL	VIH	VIH	VIH	High-Z
Write	Program	VIL	VIH	VIL	VIH	Command/Data in
	Erase	VIL	VIH	VIL	VIH	Command
	Others	VIL	VIH	VIL	VIH	Command
Stand by		VIH	X[1)]	X[1)]	VIH	High-Z
Deep Power Down		X[1)]	X[1)]	X[1)]	VIL	High-Z

BYTE#=VIL

Mode \ Pins		CE#	OE#	WE#	RP#	DQ0-7
Read	Array	VIL	VIL	VIH	VIH	Data Output
	Status Register	VIL	VIL	VIH	VIH	Status Register Data
	Identifier Code	VIL	VIL	VIH	VIH	Identifier Code
	Page	VIL	VIL	VIH	VIH	Data Output
Output Disable		VIL	VIH	VIH	VIH	High-Z
Write	Program	VIL	VIH	VIL	VIH	Command/Data in
	Erase	VIL	VIH	VIL	VIH	Command
	Others	VIL	VIH	VIL	VIH	Command
Stand by		VIH	X[1)]	X[1)]	VIH	High-Z
Deep Power Down		X[1)]	X[1)]	X[1)]	VIL	High-Z

1) X can be VIH or VIL for control pins.

Software Command Definition

Command List (WP# =VIH or VIL)

Command	1st Bus Cycle			2nd Bus Cycle				3rd-5th Bus Cycle		
	Mode	Address	Data[1] (DQ0-15)(DQ0-7)	Mode	Address A22-A18	Address A0	Data[1] (DQ0-15)(DQ0-7)	Mode	Address	Data[1] (DQ0-15)(DQ0-7)
Read Array	Write	A22[7] A0-A21=X[8]	FFH							
Page Read	Write	A22[7] A0-A21=X[8]	F3H	Read	SA[5]		RD0	Read	SA+i[6]	RDi
Device Identifier	Write	A22=VIL A0-A21=X[8]	90H	Read	A22=VIL Bank[2]	IA[3]	ID			
Read Status Register	Write	Bank[2]	70H	Read	Bank[2]		SRD[4]			
Clear Status Register	Write	A22[7] A0-A21=X[8]	50H							
Suspend	Write	Bank[2]	B0H							
Resume	Write	Bank[2]	D0H							

1) In the case of Word mode(BYTE#=VIH), upper byte data (DQ15-DQ8) is ignored.
2) Bank=Bank address (Bank(I)-Bank(VIII): A22-18)
3) IA=ID code address: A0=VIL (Manufacturer's code): A0=VIH (Device code), ID=ID code
4) SRD=Status Register Data
5) SA=A21-A2:1st Page Address, A1,A0:voluntary address / RD0=1st Page read data
6) SA+i: Page address(is equal to 1st Page Address of A21-A2), A1,A0: voluntary address / RDi: 2nd Page read data
7) In case of Bottom 64M-bit area, A22 must be set to VIL.
In case of Top 64M-bit area, A22 must be set to VIH.
8) X can be VIH or VIL.

Command List (WP# =VIH)

Command	1st Bus Cycle			2nd Bus Cycle			3rd-129th Bus Cycles 3rd-257th Bus Cycles(Byte mode)		
	Mode	Address	Data[1] (DQ0-15)(DQ0-7)	Mode	Address	Data[1] (DQ0-15)(DQ0-7)	Mode	Address	Data[1] (DQ0-15)(DQ0-7)
Word Program	Write	Bank[7]	40H	Write	WA[2]	WD[2]			
Page Program	Write	Bank[7]	41H	Write	WA0[3]	WD0[3]	Write	WAn[3]	WDn[3]
Page Buffer to Flash	Write	Bank[7]	0EH	Write	WA[4]	D0H[1]			
Block Erase/Confirm	Write	Bank[7]	20H	Write	BA[5]	D0H[1]			
Erase All Unlocked Blocks	Write	A22[8] A0-A21=X[9]	A7H	Write	A22[8] A0-A21=X[9]	D0H[1]			
Clear Page Buffer	Write	A22[8] A0-A21=X[9]	55H	Write	A22[8] A0-A21=X[9]	D0H[1]			
Single Data Load to Page Buffer	Write	A22[8] A0-A21=X[9]	74H	Write	WA[2]	WD[2]			
Flash to Page Buffer	Write	Bank[7]	F1H	Write	RA[6]	D0H[1]			

1) In the case of Word mode(BYTE#=VIH), upper byte data (DQ15-DQ8) is ignored.
2) WA=Write Address, WD=Write Data
3) WA0, WAn=Write Address, WD0, WDn=Write Data.
Word mode (BYTE#=VIH) : Write address and write data must be provided sequentially from 00H to 7FH for A6-A0. Page size is 128 words (128-word x 16-bit), and also A22-A7 (block address, page address) must be valid.
Byte mode (BYTE#=VIL) : Write address and write data must be provided sequentially from 00H to FFH for A6-A-1. Page size is 256 Bytes (256-byte x 8-bit), and also A22-A7 (block address, page address) must be valid.
4) WA=Write Address: A22-A7 (block address, page address) must be valid.
5) BA=Block Address : A22-A12[Bank(I),Bank(VIII)], A22-A15 [Bank(II) ~ Bank(VII)]
6) RA=Read Address: A22-A7 (block address, page address) must be valid.
7) Bank=Bank address (Bank(I)-Bank(VIII): A22-18)
8) In case of Bottom 64M-bit area, A22 must be set to VIL. In case of Top 64M-bit area, A22 must be set to VIH.
9) X can be VIH or VIL.

Software Command Definition

Command List (WP# =VIL)

Software lock release operation needs following consecutive 7bus cycles.Moreover, additional 127(255) bus cycles are needed for page program operation.

Setup Command for Software Lock Release	1st Bus Cycle			2nd Bus Cycle			3rd Bus Cycle		
	Mode	Address	Data[1] (DQ0-15/DQ0-7)	Mode	Address	Data[1] (DQ0-15/DQ0-7)	Mode	Address	Data[1] (DQ0-15/DQ0-7)
Word Program	Write	Bank[8]	60H	Write	Bank[8]	Block[6]	Write	Bank[8]	ACH
Page Program	Write	Bank[8]	60H	Write	Bank[8]	Block[6]	Write	Bank[8]	ACH
Page Buffer to Flash	Write	Bank[8]	60H	Write	Bank[8]	Block[6]	Write	Bank[8]	ACH
Block Erase/Confirm	Write	Bank[8]	60H	Write	Bank[8]	Block[6]	Write	Bank[8]	ACH
Clear Page Buffer	Write	Bank[8]	60H	Write	Bank[8]	Block[6]	Write	Bank[8]	ACH
Single Data Load to Page Buffer	Write	Bank[8]	60H	Write	Bank[8]	Block[6]	Write	Bank[8]	ACH
Flash to Page Buffer	Write	Bank[8]	60H	Write	Bank[8]	Block[6]	Write	Bank[8]	ACH

Setup Command for Software Lock Release	4th Bus Cycle			5th Bus Cycle		
	Mode	Address	Data[1] (DQ0-15/DQ0-7)	Mode	Address	Data[1] (DQ0-15/DQ0-7)
Word Program	Write	Bank[8]	Block#[6]	Write	Bank[8]	7BH
Page Program	Write	Bank[8]	Block#[6]	Write	Bank[8]	7BH
Page Buffer to Flash	Write	Bank[8]	Block#[6]	Write	Bank[8]	7BH
Block Erase/Confirm	Write	Bank[8]	Block#[6]	Write	Bank[8]	7BH
Clear Page Buffer	Write	Bank[8]	Block#[6]	Write	Bank[8]	7BH
Single Data Load to Page Buffer	Write	Bank[8]	Block#[6]	Write	Bank[8]	7BH
Flash to Page Buffer	Write	Bank[8]	Block#[6]	Write	Bank[8]	7BH

Setup Command for Program or Erase Operations	6th Bus Cycle			7th Bus Cycle			8th-134th Bus Cycles 8th-262th Bus Cycles(Byte mode)		
	Mode	Address	Data[1] (DQ0-15/DQ0-7)	Mode	Address	Data (DQ0-15/DQ0-7)	Mode	Address	Data (DQ0-15/DQ0-7)
Word Program	Write	Bank[8]	40H	Write	WA[2]	WD[2]			
Page Program	Write	Bank[8]	41H	Write	WA0[3]	WD0[3]	Write	WAn[3]	WDn[3]
Page Buffer to Flash	Write	Bank[8]	0EH	Write	WA[4]	D0H[1]			
Block Erase/Confirm	Write	Bank[8]	20H	Write	BA[5]	D0H[1]			
Clear Page Buffer	Write	A22[9] A0-A21=X[10]	55H	Write	A22[9] A0-A21=X[10]	D0H[1]			
Single Data Load to Page Buffer	Write	A22[9] A0-A21=X[10]	74H	Write	WA[2]	WD[2]			
Flash to Page Buffer	Write	Bank[8]	F1H	Write	RA[7]	D0H[1]			

1) In the case of word mode(BYTE#=VIH) upper byte data (DQ15-DQ8) is ignored.

2) WA=Write Address, WD=Write Data

3) WA0, WAn=Write Address, WD0, WDn=Write Data. Write address and write data must be provided sequentially from 00H to 7FH for A6-A0(word mode) and from 00H to FFH for A6-A-1(byte mode), respectively. Page size is 128 words (128-word x 16-bit/ word mode) or Page size is 256 bytes (256-word x 8-bit/ byte mode), and also A22-A7 (block address, page address) must be valid.

4) WA=Write Address: A22-A7 (block address, page address) must be valid.

5) BA=Block Address : A21-A12[Bank(I),Bank(VIII)], A21-A15 [Bank(II) ~ Bank(VII)]

6) Block=Block Address: A21-A15, Block#=A21#-A15#

Address	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0
Block	fixed 0	A21	A20	A19	A18	A17	A16	A15
Block#	fixed 0	A21#	A20#	A19#	A18#	A17#	A16#	A15#

7) RA=Read Address: A22-A7 (block address, page address) must be valid.

8) Bank=Bank address (Bank(I)-Bank(VIII): A22-18)

9) In case of Bottom 64M-bit area, A22 must be set to VIL.
In case of Top 64M-bit area, A22 must be set to VIH.

10) X can be VIH or VIL.

Block Locking

RP#	WP#	Write Protection Provided					Notes
		Bank (I),(VIII)		Bank (II),(VII)	Bank (III),(VI)	Bank (IV),(V)	
		Boot	Parameter/Main	Main	Main	Main	
VIL	X	Locked	Locked	Locked	Locked	Locked	Deep Power Down Mode
VIH	VIL	Locked	Locked	Locked	Locked	Locked	All Blocks Locked(Valid to operate Softw are Lock Release)
	VIH	Unlocked	Unlocked	Unlocked	Unlocked	Unlocked	All Blocks Unlocked

WP# pin must not be switched during performing Read / Write operations or WSM busy (WSMS=0).

Status Register

Symbol (I/O Pin)	Status	Definition	
		"1"	"0"
S.R. 7 (DQ7)	Write State Machine Status	Ready	Busy
S.R. 6 (DQ6)	Suspend Status	Suspended	Operation in Progress/Completed
S.R. 5 (DQ5)	Erase Status	Error	Successful
S.R. 4 (DQ4)	Program Status	Error	Successful
S.R. 3 (DQ3)	Block Status after Erase	Error	Successful
S.R. 2 (DQ2)	Reserved	-	-
S.R. 1 (DQ1)	Reserved	-	-
S.R. 0 (DQ0)	Reserved	-	-

Device ID Code

Pins / Code	A22	A0	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0	Hex. Data
Manufacturer Code	VIL	VIL	"0"	"0"	"0"	"1"	"1"	"1"	"0"	"0"	1CH
Device Code	VIL	VIH	"1"	"0"	"1"	"1"	"1"	"0"	"0"	"1"	B9H

The output of upper byte data (DQ15-DQ8) is “0H”. A22 must be set “VIL”.

Absolute Maximum Ratings

Symbol	Parameter	Conditions	Min.	Max.	Units
VCC	VCC Voltage	With Respect to GND	-0.2	4.6	V
VI1	All Input or Output Voltage[1)]		-0.6	4.6	V
Ta	Ambient Temperature		-40	85	°C
Tbs	Temperature under Bias		-50	95	°C
Tstg	Storage Temperature		-65	125	°C
Iout	Output Short Circuit Current			100	mA

1)Minimum DC voltage is –0.6V on input / output pins. During transitions, the level may undershoot to –2.0V for periods <20ns. Maximum DC voltage on input / output pins is VCC+0.5V which, during transitions, may overshoot to VCC+1.5V for periods <20ns.

DC electrical characteristics

(Ta= -40 ~85 °C and Flash VCC=3.0V~3.6V, unless otherwise noted)

Symbol	Parameter	Test Conditions		Limits		
				Min.	Typ.[1)]	Max.
ILI	Input Leakage Current	0V≤ VIN≤ VCC		-2		2
ILO	Output Leakage Current	0V≤ VOUT≤ VCC		-20		20
ISB2	VCC Stand by Current	VCC= 3.6V, VIN= GND/VCC, CE#= RP#= WP#= VCC±0.3V			0.2	12
ISB3	VCC Deep Power Down Current	VCC= 3.6V, VIN= VIL/VIH, RP#= VIL			10	50
ISB4		VCC= 3.6V, VIN= GND or VCC, RP#= GND± 0.3V			0.2	12
ICC1	VCC Read Current for Word	Vcc = 3.6V, VIN = VIL/VIH, RP# = OE# = VIH, CE# =VIL, Iout = 0mA	5MHz		20	30
			1MHz		4	8
ICC1P	VCC Page Read Current for Word	Vcc = 3.6V, VIN = VIL/VIH, RP# = OE# = VIH, CE# = VIL, Iout = 0mA	5MHz		5	10
ICC2	VCC Write Current for Word	Vcc = 3.6V, VIN = VIL/VIH, RP# = OE# = VIH, CE# = WE# = VIL				15
ICC3	VCC Program Current	VCC = 3.6V, VIN = VIL/VIH, CE#= RP# = WP# = VIH				35
ICC4	VCC Erase Current	VCC = 3.6V, VIN = VIL/VIH, CE#= RP# = WP# = VIH				35
ICC5	VCC Suspend Current	VCC = 3.6V, VIN = VIL/VIH, CE#= RP# = WP# = VIH				400
VIL	Input Low Voltage			-0.5		0.4
VIH	Input High Voltage			2.4		VCC+0.5
VOL	Output Low Voltage	IOL = 4.0mA				0.45
VOH1	Output High Voltage	IOH = -2.0mA		0.85xVCC		
VOH2		IOH = -100uA		VCC-0.4		
VLKO	Low VCC Lock Out Voltage[2)]			1.5		2.2

All currents are in RMS unless otherwise noted.
1) Typical values at Flash VCC=3.3V, Ta=25 °C.
2) To protect against initiation of write cycle during Flash VCC power up / down, a write cycle is locked out for Flash VCC less than VLKO. If Flash VCC is less than VLKO, Write State Machine is reset to read mode. When the Write State Machine is in Busy state, if Flash VCC is less than VLKO, the alteration of memory contents may occur.

AC electrical characteristics

(Ta=-40 ~85 °C and Flash VCC=3.0V~3.6V, unless otherwise noted)

Read Only Mode

Symbol		Parameter	Limits			Units
			Flash VCC=3.0-3.6V			
			Min.	Typ.	Max.	
tRC	tAVAV	Read Cycle Time	70			ns
ta(AD)	tAVQV	Address Access Time			70	ns
ta(CE)	tELQV	Chip Enable Access Time			70	ns
ta(OE)	tGLQV	Output Enable Access Time			30	ns
ta(PAD)	tPAVQV	Page Read Access Time			25	ns
tCEPH		CE# "H"Pulse width	30			ns
tCLZ	tELQX	Chip Enable to Output in Low-Z	0			ns
tDF(CE)	tEHQZ	Chip Enable High to Output in High-Z			25	ns
tOLZ	tGLQX	Output Enable to Output in Low-Z	0			ns
tDF(OE)	tGHQZ	Output Enable to High to Output in High-Z			25	ns
tPHZ	tPLQZ	RP# Low to Output High-Z			150	ns
ta(BYTE)	tFL/HQV	BYTE# access time			70	ns
tBHZ	tFLQZ	BYTE# low to output high-Z			25	ns
tOH	tOH	Output Hold from CE#, OE# and Addresses	0			ns
tBCD	tELFL/H	CE# low to BYTE# high or low			5	ns
tBAD	tAVFL/H	Address to BYTE# high or low			5	ns
tOEH	tWHGL	OE# Hold from WE# High	10			ns
tPS	tPHEL	RP# Recovery to CE# Low	150			ns

-Timing measurements are made under AC waveforms for read operations.

AC electrical characteristics (Ta=-40 ~85 °C and Flash VCC=3.0V~3.6V, unless otherwise noted)

Read / Write Mode (WE# control)

Symbol		Parameter	Limits			Units
			Flash VCC=3.0-3.6V			
			Min.	Typ.	Max.	
tWC	tAVAV	Write Cycle Time	70			ns
tAS	tAVWH	Address Setup Time	35			ns
tAH	tWHAX	Address Hold Time	0			ns
tDS	tDVWH	Data Setup Time	35			ns
tDH	tWHDX	Data Hold Time	0			ns
tOEH	tWHGL	OE# Hold from WE# High	10			ns
tCS	tELWL	Chip Enable Setup Time	0			ns
tCH	tWHEH	Chip Enable Hold Time	0			ns
tWP	tWLWH	Write Pulse Width	35			ns
tWPH	tWHWL	Write Pulse Width High	30			ns
tBS	tFL/HWH	Byte enable high or low set-up time	35			ns
tBH	tWHFL/H	Byte enable high or low hold time	70			ns
tGHWL	tGHWL	OE# Hold to WE# Low	0			ns
tBLS	tPHHWH	Block Lock Setup to Write Enable High	70			ns
tBLH	tQVPH	Block Lock Hold from Valid SRD	0			ns
tDAP	tWHRH1	Duration of Auto Program Operation(Word Mode)		30	300	µs
tDAP	tWHRH1	Duration of Auto Program Operation(Byte Mode)		30	300	µs
tDAP	tWHRH1	Duration of Auto Program Operation(Page Mode)		4	80	ms
tDAE	tWHRH2	Duration of Auto Block Erase Operation		150	600	ms
tWHRL	tWHRL	Delay Time During Internal Operation			70	ns
tPS	tPHWL	RP# Recovery to CE# Low	150			ns

-Read timing parameters during command write operations mode are the same as during read only operation mode.
-Typical values at Flash VCC=3.3V and Ta=25 °C.

Read / Write Mode (CE# control)

Symbol		Parameter	Limits			Units
			Flash VCC=3.0-3.6V			
			Min.	Typ.	Max.	
tWC	tAVAV	Write Cycle Time	70			ns
tAS	tAVEH	Address Setup Time	35			ns
tAH	tEHAX	Address Hold Time	0			ns
tDS	tDVEH	Data Setup Time	35			ns
tDH	tEHDX	Data Hold Time	0			ns
tOEH	tEHGL	OE# Hold from CE# High	10			ns
tWS	tWLEL	Write Enable Setup Time	0			ns
tWH	tEHWH	Write Enable Hold Time	0			ns
tCEP	tELEH	CE# Pulse Width	35			ns
tCEPH	tEHEL	CE#"H" Pulse Width	30			ns
tBS	tFL/HEH	Byte enable high or low set-up time	35			ns
tBH	tEHFL/H	Byte enable high or low hold time	70			ns
tGHEL	tGHEL	OE# Hold to CE# Low	0			ns
tBLS	tPHHEH	Block Lock Setup to Write Enable High	70			ns
tBLH	tQVPH	Block Lock Hold from Valid SRD	0			ns
tDAP	tEHRH1	Duration of Auto Program Operation(Word Mode)		30	300	µs
tDAP	tEHRH1	Duration of Auto Program Operation(Byte Mode)		30	300	µs
tDAP	tEHRH1	Duration of Auto Program Operation(Page Mode)		4	80	ms
tDAE	tEHRH2	Duration of Auto Block Erase Operation		150	600	ms
tEHRL	tEHRL	Delay Time During Internal Operation			70	ns
tPS	tPHEL	RP# Recovery to CE# Low	150			ns

-Timing measurements are made under AC waveforms for read operations.
-Typical values at Flash VCC=3.3V and Ta=25 °C.

Program / Erase Time

Parameter	Min.	Typ.	Max.	Units
Block Erase Time		150	600	ms
Main Block Write Time (Byte Mode)		2	8	sec
Main Block Write Time (Word Mode)		1	4	sec
Page Write Time		4	80	ms
Flash to Page Buffer Time		100	150	µs

Program Suspend / Erase Suspend Time

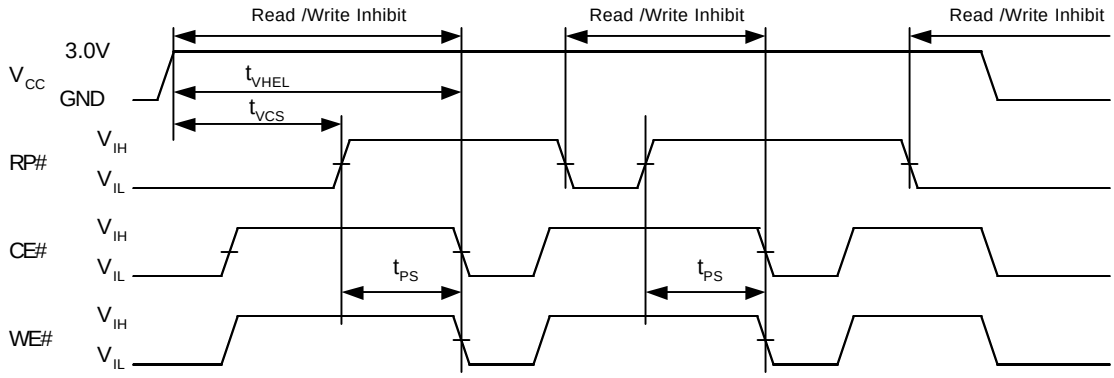
Parameter	Min.	Typ.	Max.	Unit
Program Susupend Time			15	µs
Erase Susupend Time			15	µs

Flash VCC Power Up / Down Timing

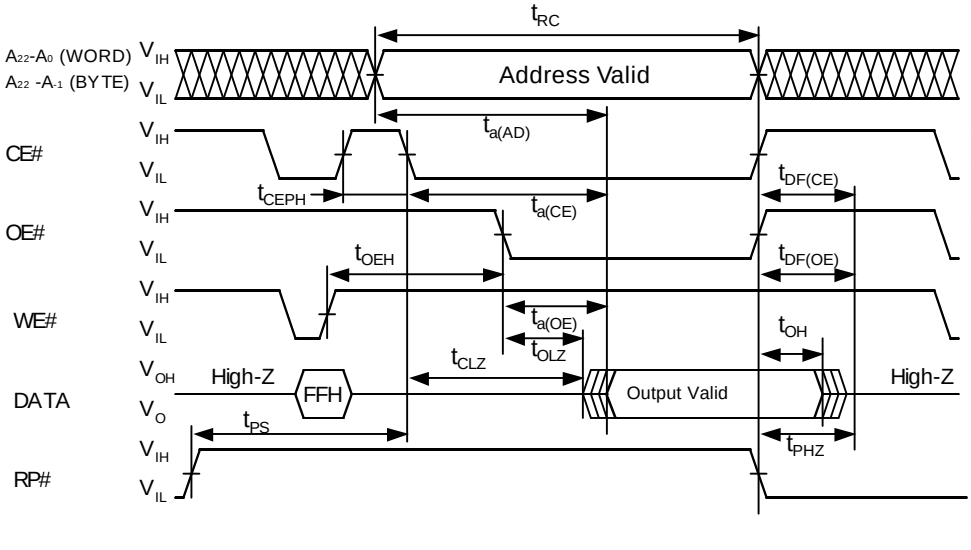
symbol	Parameter	Min.	Typ.	Max.	Unit
tVCS	RP#=VIH Setup Time from Flash VCC min.	2			µs
tVHEL	CE#=VIL Setup Time from Flash VCC min.	60			µs

During power up / down, by the noise pulses on control pins, the device has possibility of accidental erase of programming. The device must be protected against initiation of write cycle for memory contents during power up / down. The delay time of min. 60 µsec is always required before read operation or write operation is initiated from the time Flash VCC reaches Flash VCC min. during power up /down. By holding RP#=VIL, the contents of memory is protected during Flash VCC power up / down. During power up, RP# must be held VIL for min. 2µs from the time Flash VCC reaches Flash VCC min.. During power down, RP# must be held VIL until Flash VCC reaches GND. RP# doesn't have latch mode, therefore RP# must be held VIH during read operation or erase / program operation.

Flash VCC Power up / down Timing



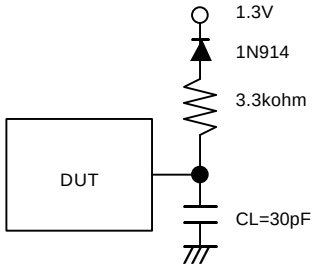
AC Waveforms for Read Operation and Test Conditions



Test Conditions for AC Characteristics

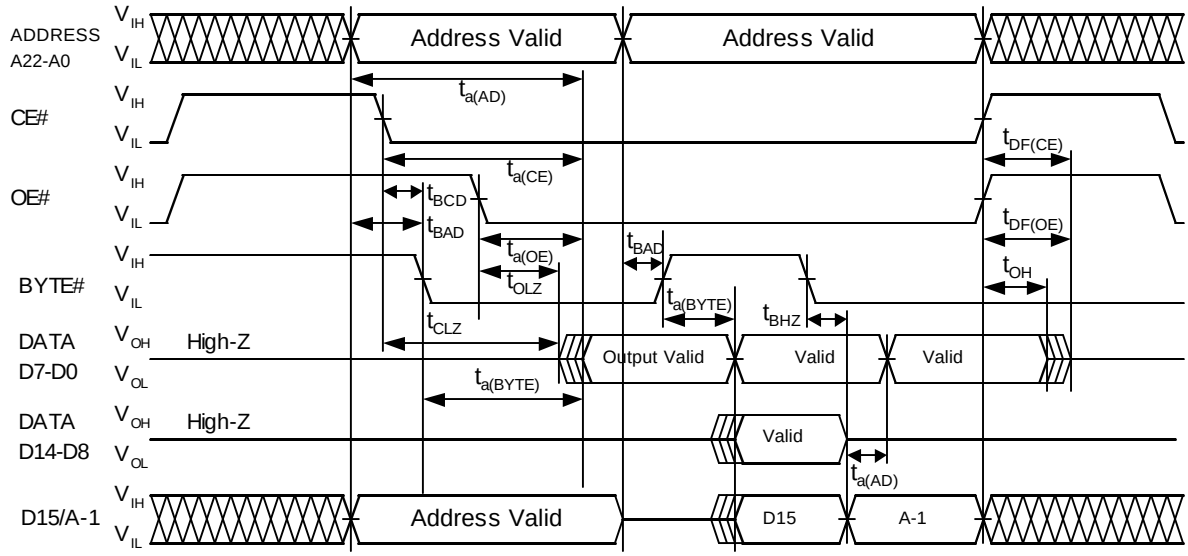
Input Voltage : V_{IL}=0V, V_{IH}=Flash Vcc
Input Rise and Fall Times : ≤5ns
Reference Voltage
at timing measurement : (Flash Vcc)/2
Output Load : 1 TTL gate +
CL(30pF)

or



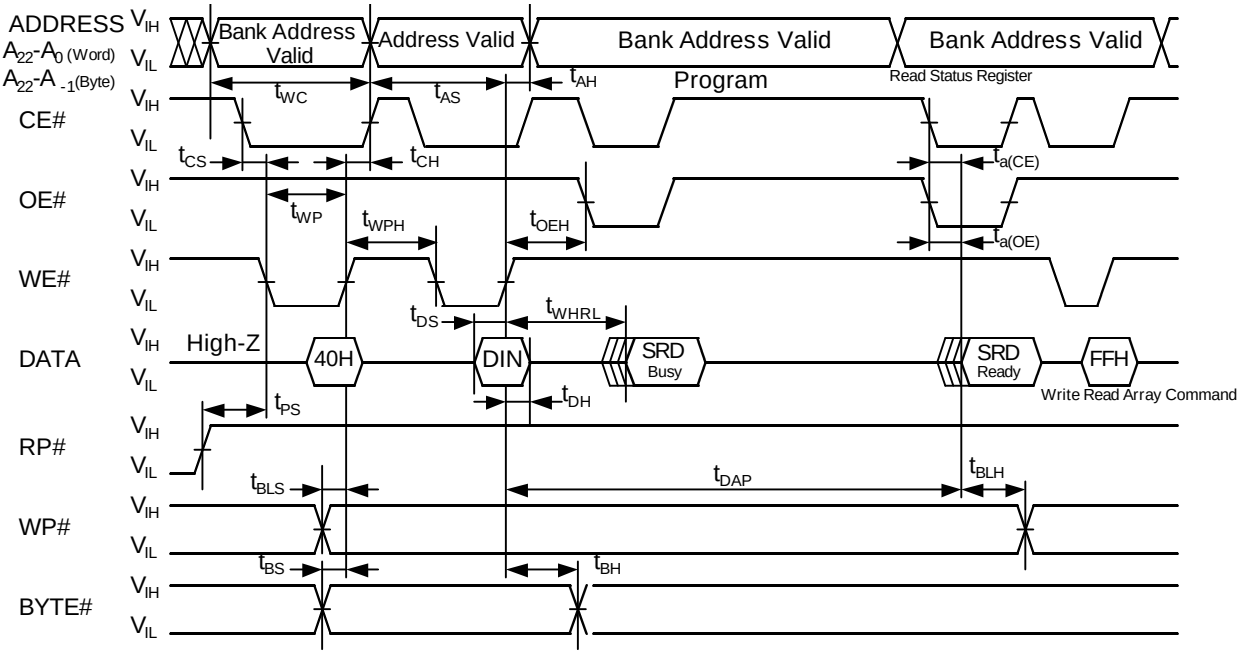
- After inputting Read Array Command FFH, it is necessary to make CE# “H” pulse more than 30ns (tCEPH).
And after inputting Read Array Command FFH, it is also necessary to keep 30ns to recover before starting read after WE# rises “H” in case of changing a part or all of addresses(A22~A0/A22~A-1) and CE#=“L”.

Byte AC Waveforms for Read Operation

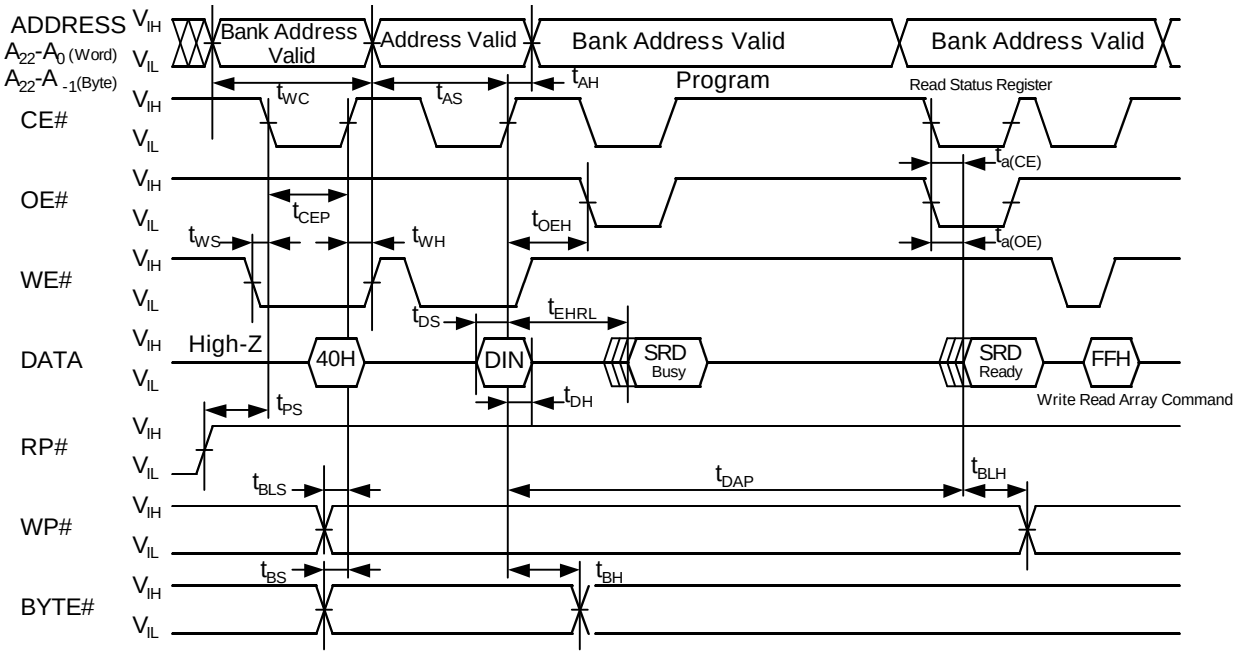


When BYTE# = VIH, CE# = OE# = VIL, D15/A-1 is output status. At this time, input signal must not be applied.

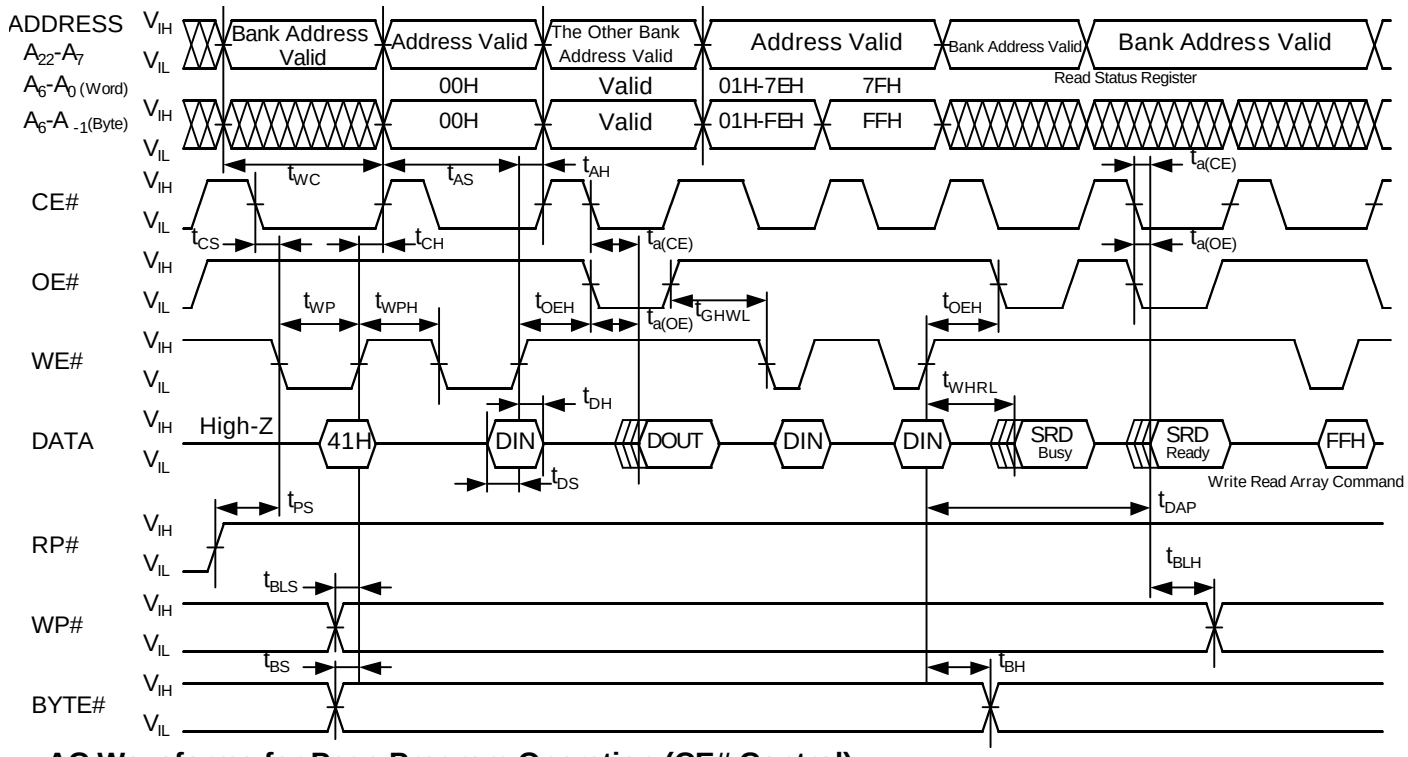
AC Waveforms for Word / Byte Program Operation (WE# Control)



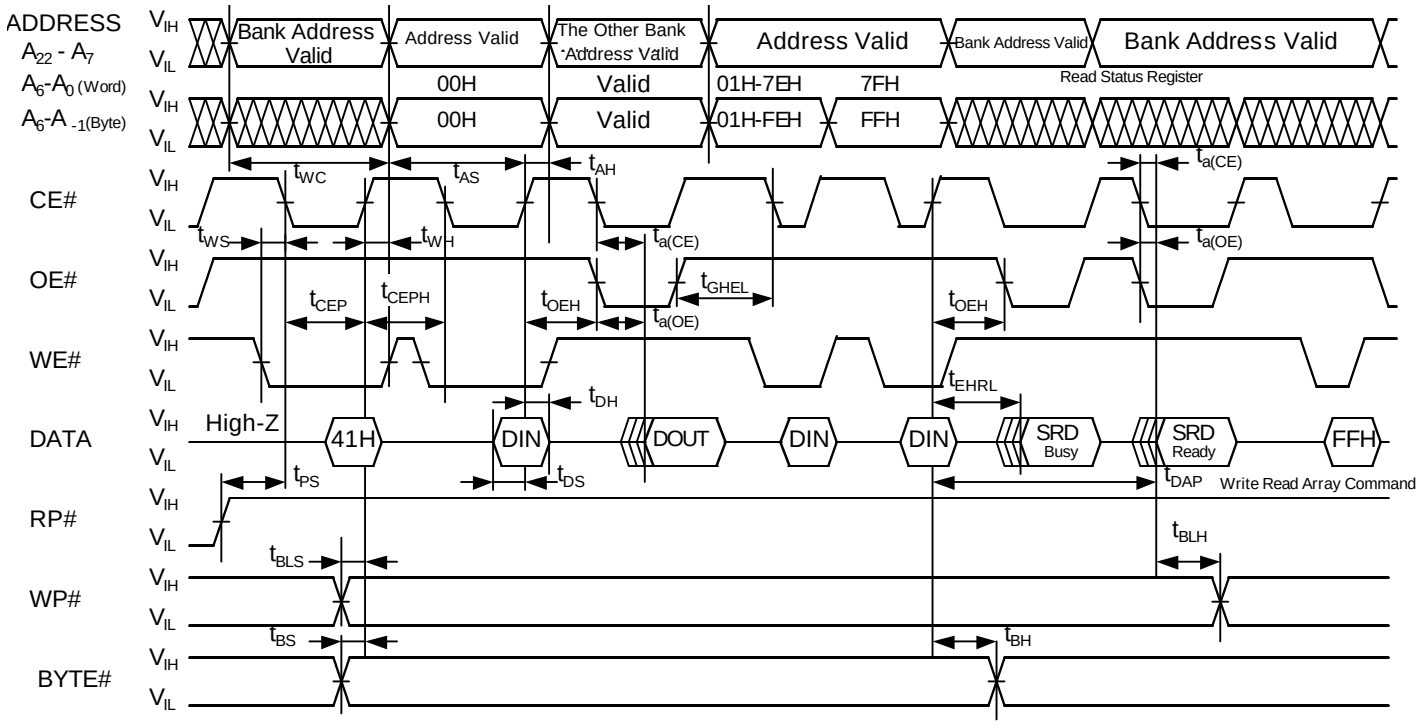
AC Waveforms for Word / Byte Program Operation (CE# Control)



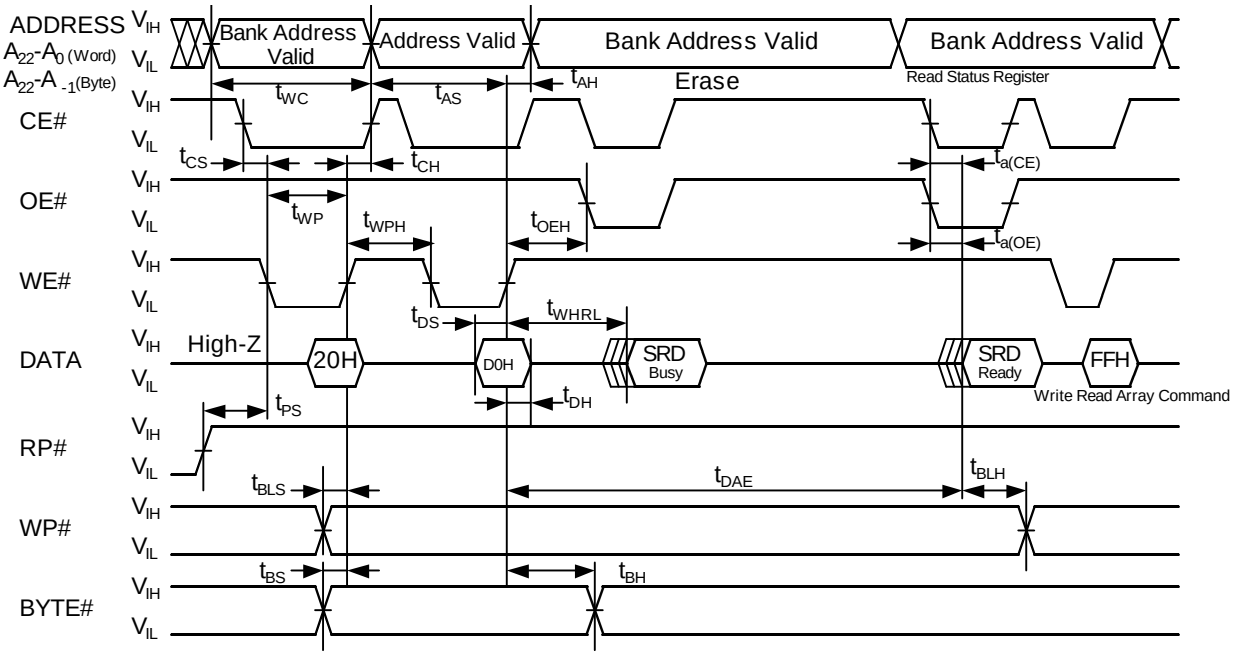
AC Waveforms for Page Program Operation (WE# Control)



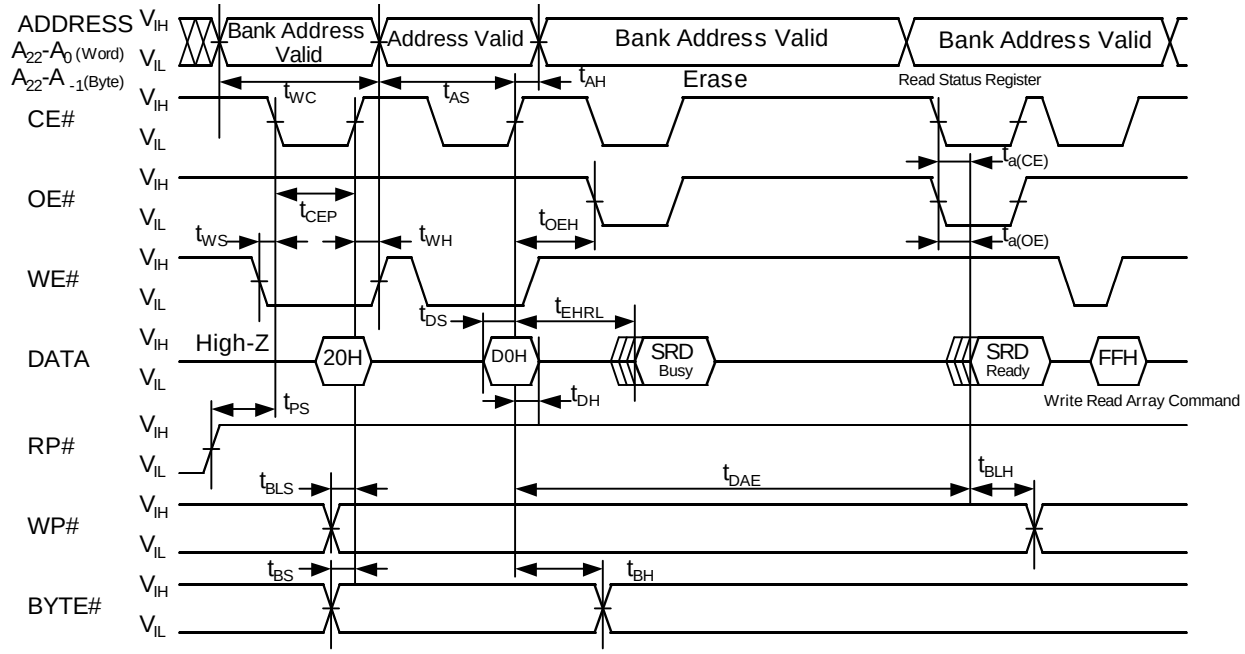
AC Waveforms for Page Program Operation (CE# Control)



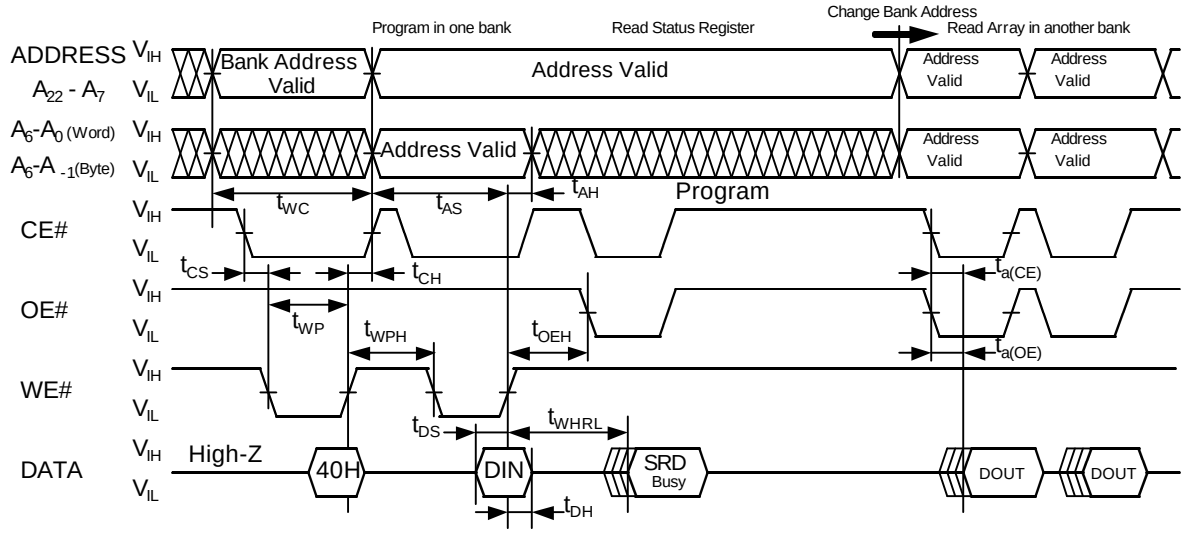
AC Waveforms for Erase Operation (WE# Control)



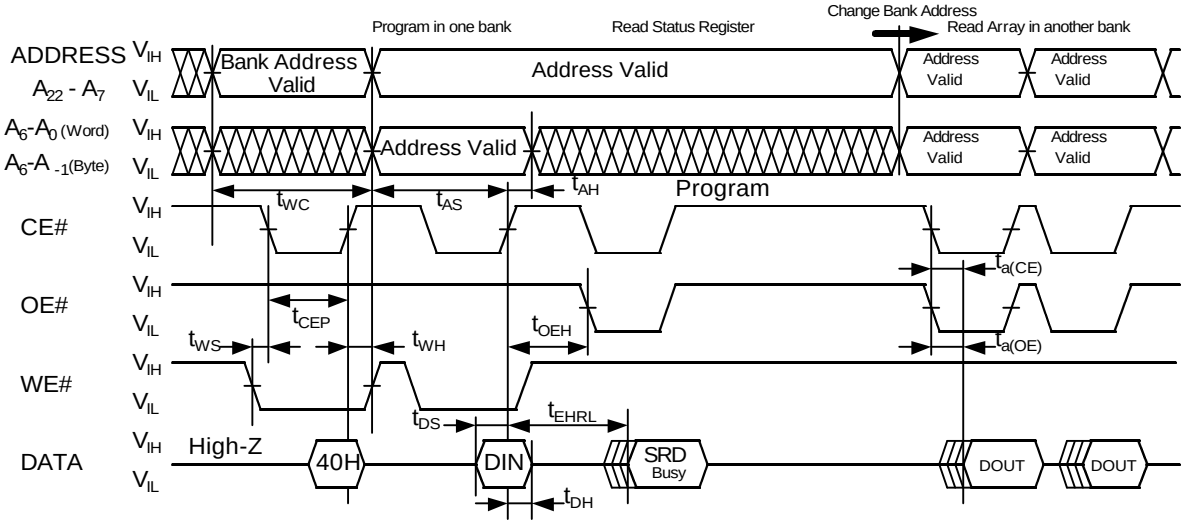
AC Waveforms for Erase Operation (CE# Control)



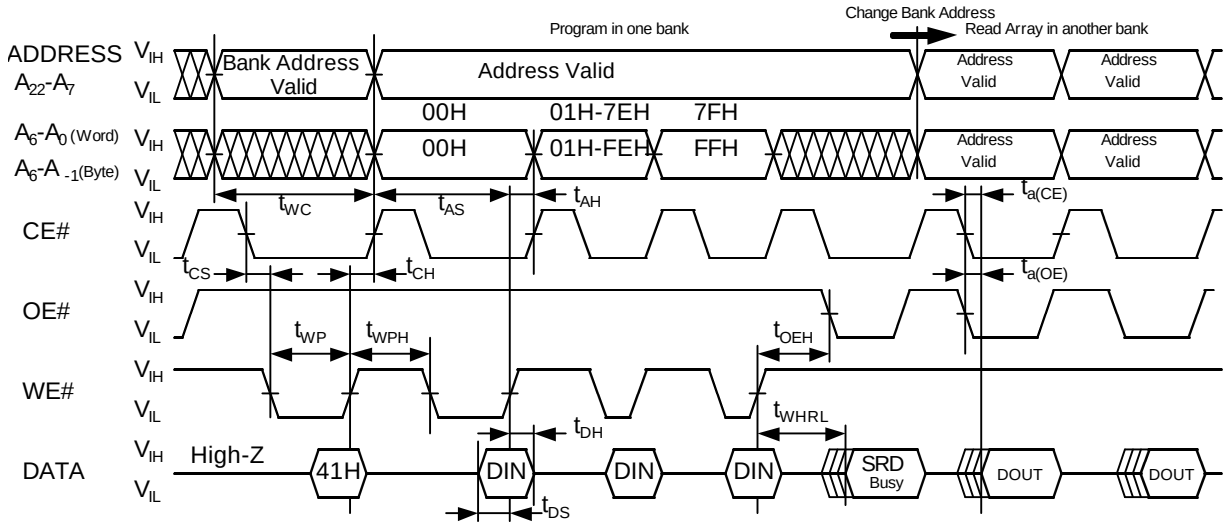
AC Waveforms for Word / Byte Program Operation with BGO (WE# Control)



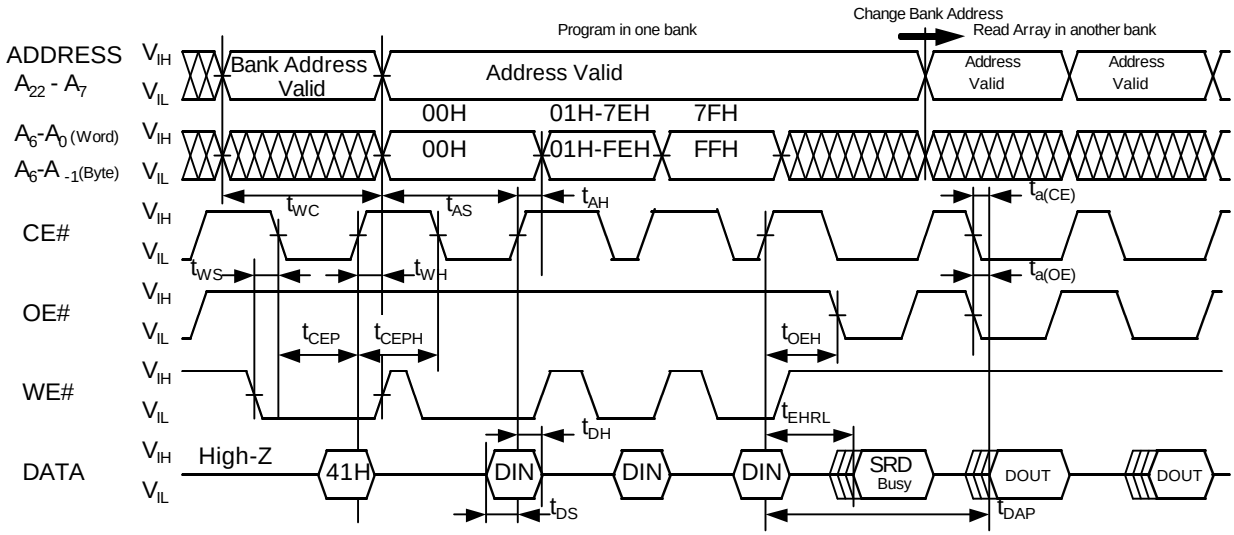
AC Waveforms for Word / Byte Program Operation with BGO (CE# Control)



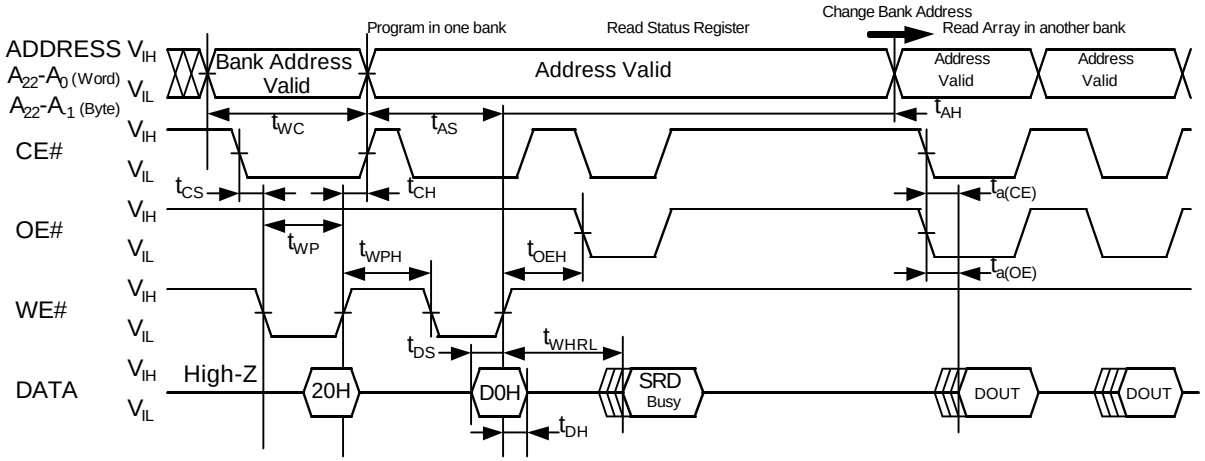
AC Waveforms for Page Program Operation with BGO (WE# Control)



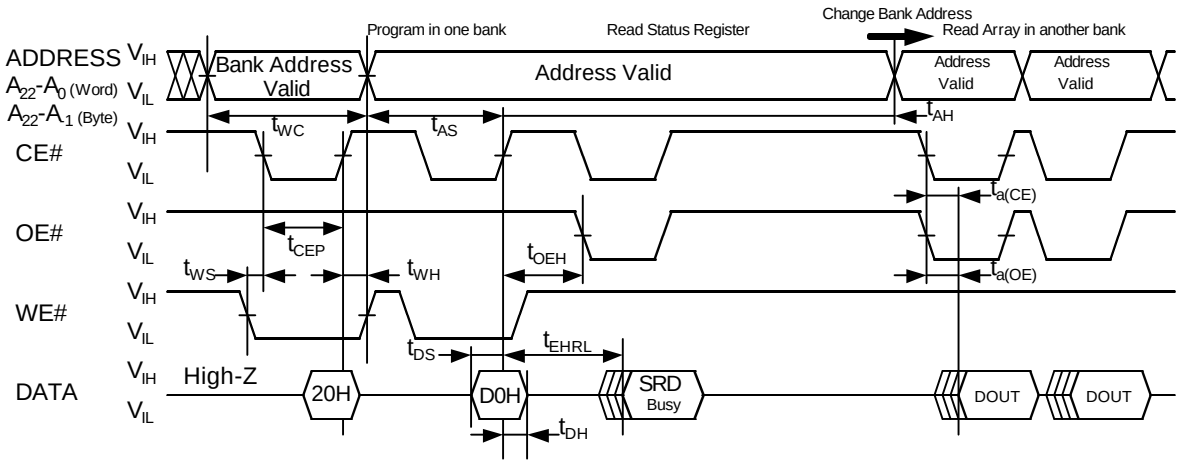
AC Waveforms for Page Program Operation with BGO (CE# Control)



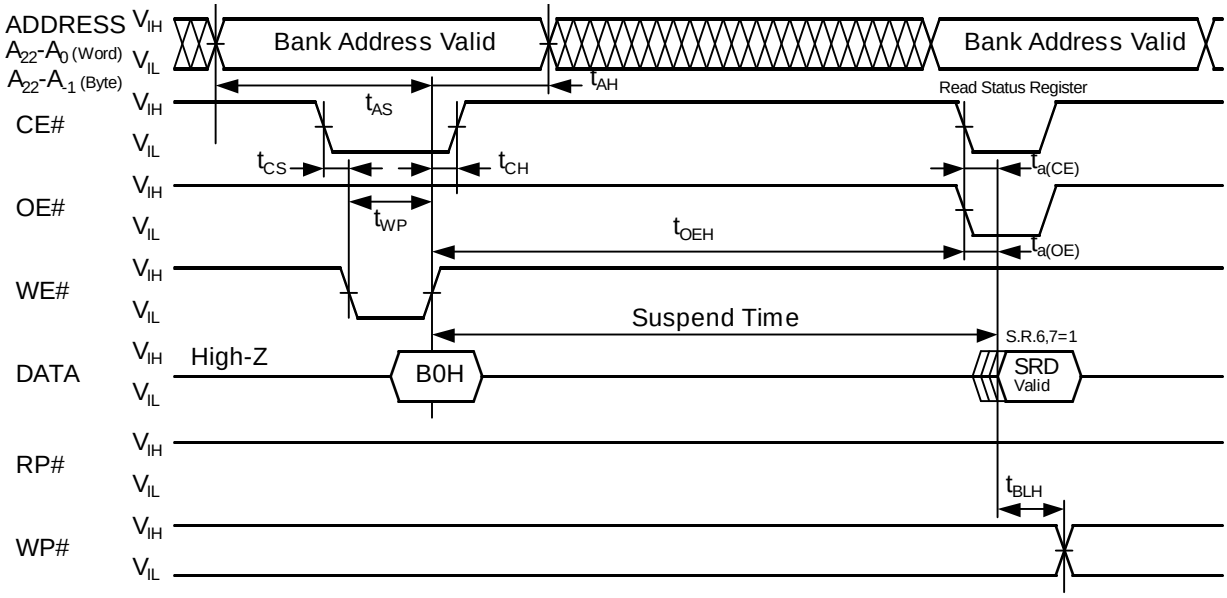
AC Waveforms for Erase Operation with BGO (WE# Control)



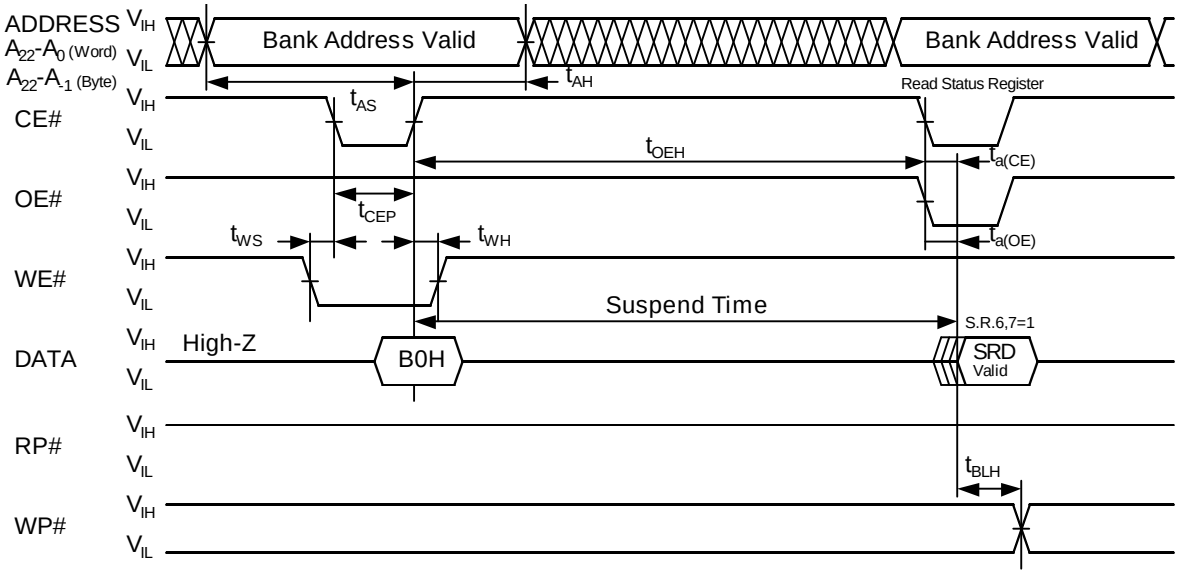
AC Waveforms for Erase Operation with BGO (CE# Control)



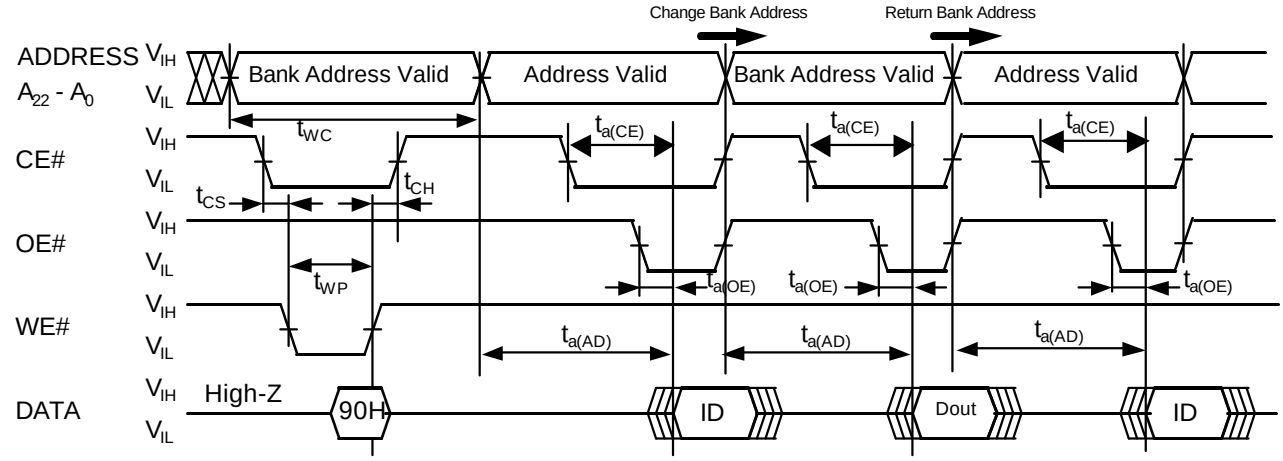
AC Waveforms for Suspend Operation (WE# Control)



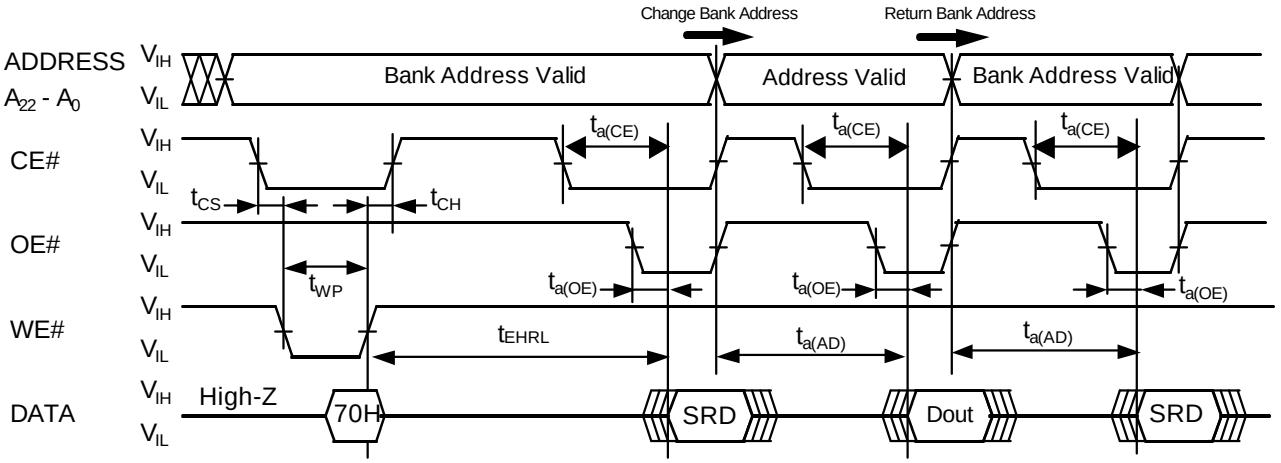
AC Waveforms for Suspend Operation (CE# Control)



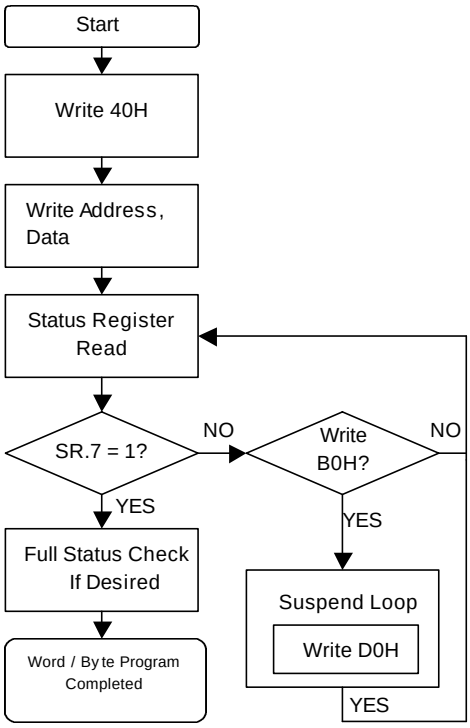
AC Waveforms for Device ID Read Operation with BBR(Back Bank Read)



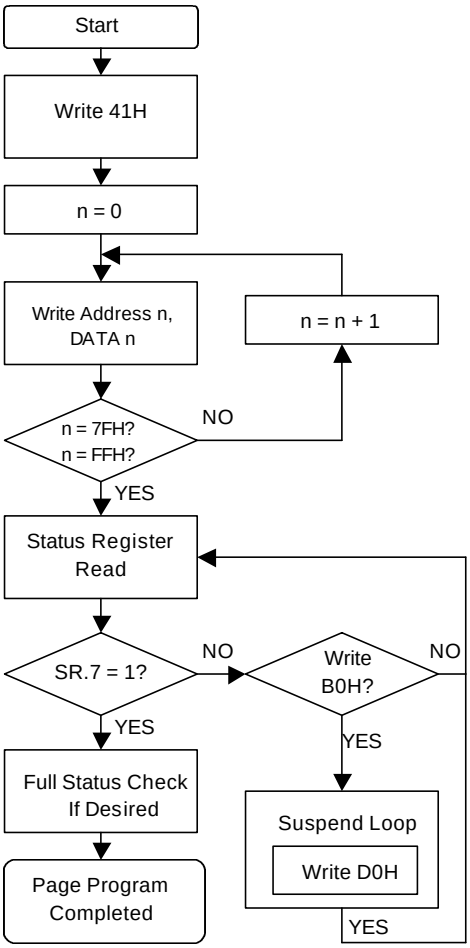
AC Waveforms for Status Register Read Operation with BBR(Back Bank Read)



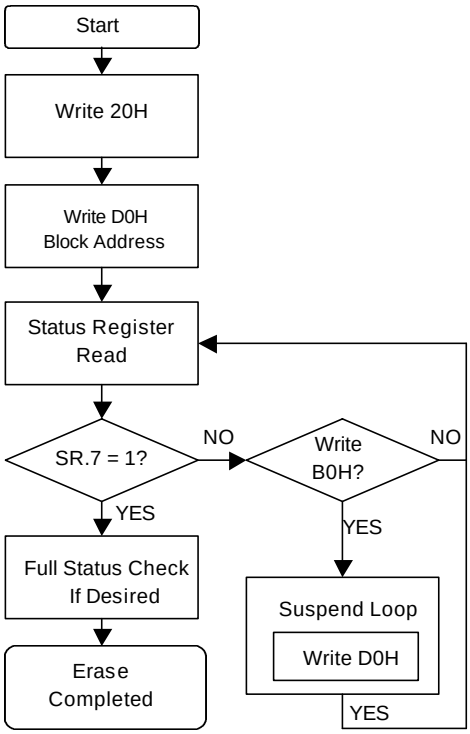
Word / Byte Program Flow Chart



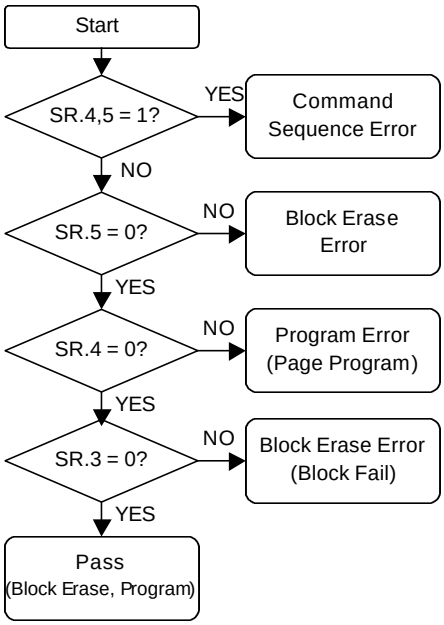
Page Program Flow Chart



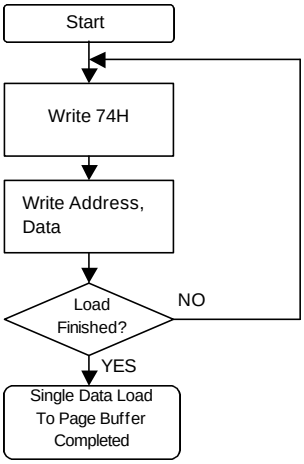
Block Erase Flow Chart



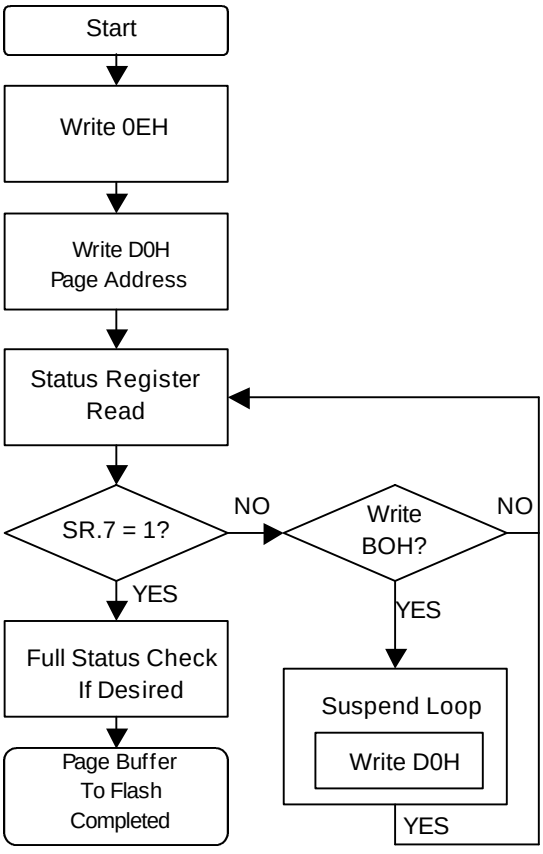
Status Register Check Flow Chart



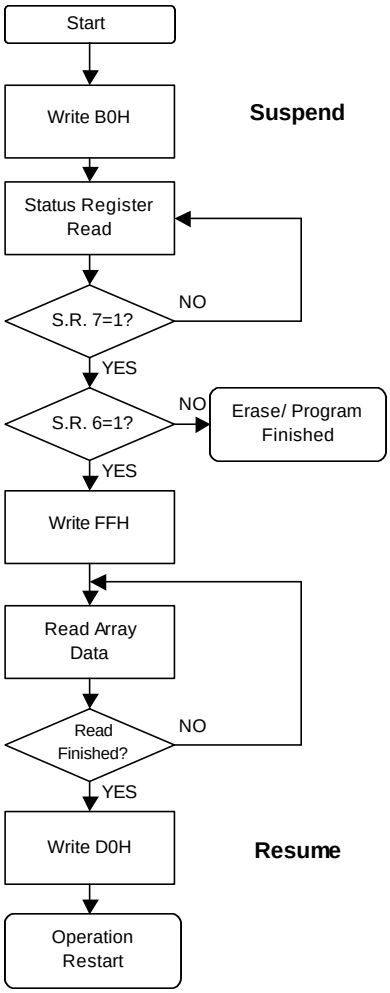
Single Data Load to Page Buffer Flow Chart



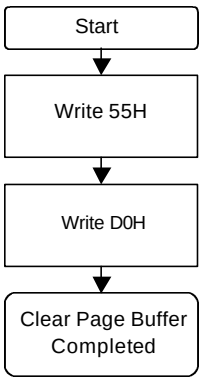
Page Buffer to Flash Flow Chart



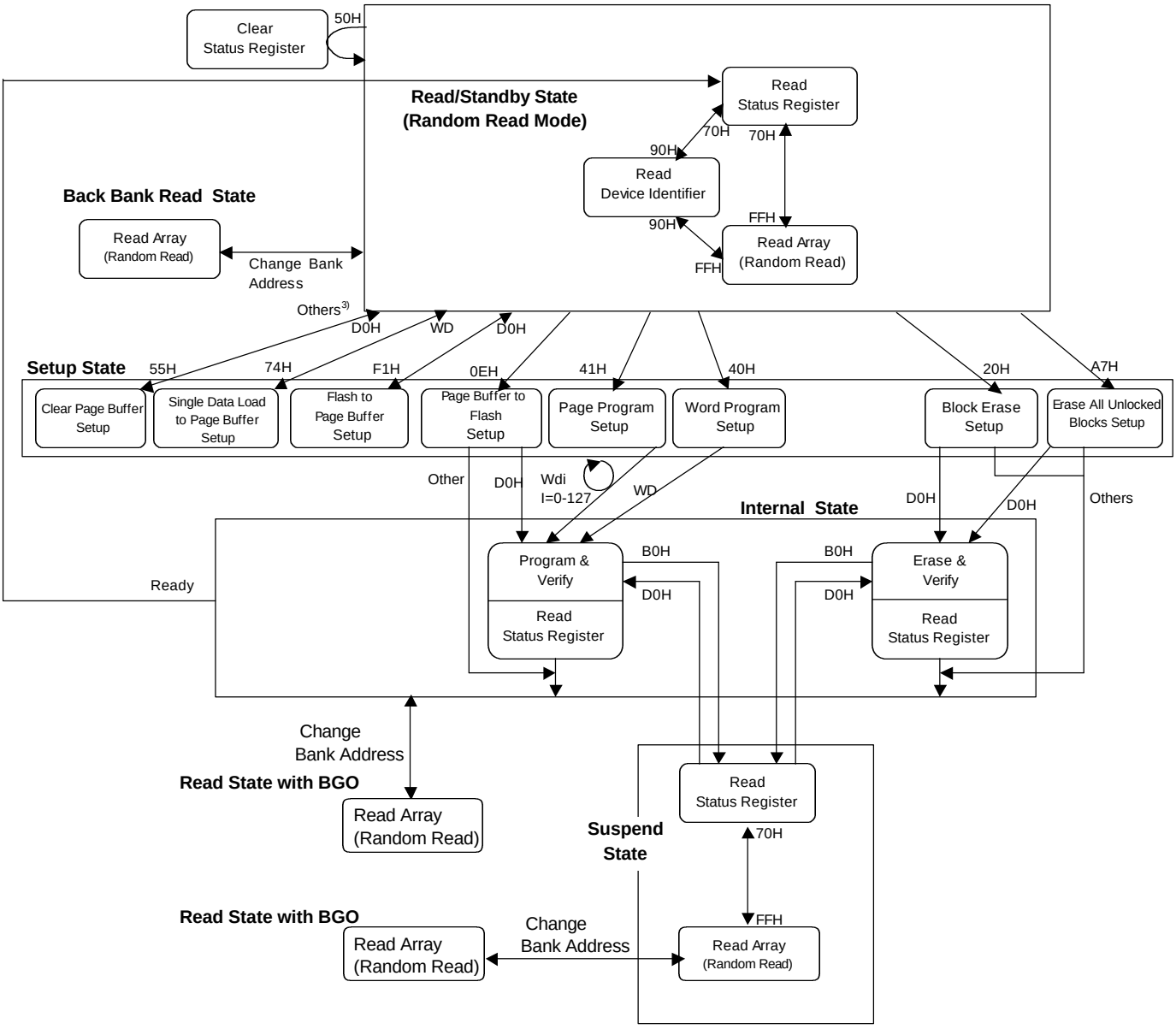
Suspend / Resume Flow Chart



Clear Page Buffer Flow Chart



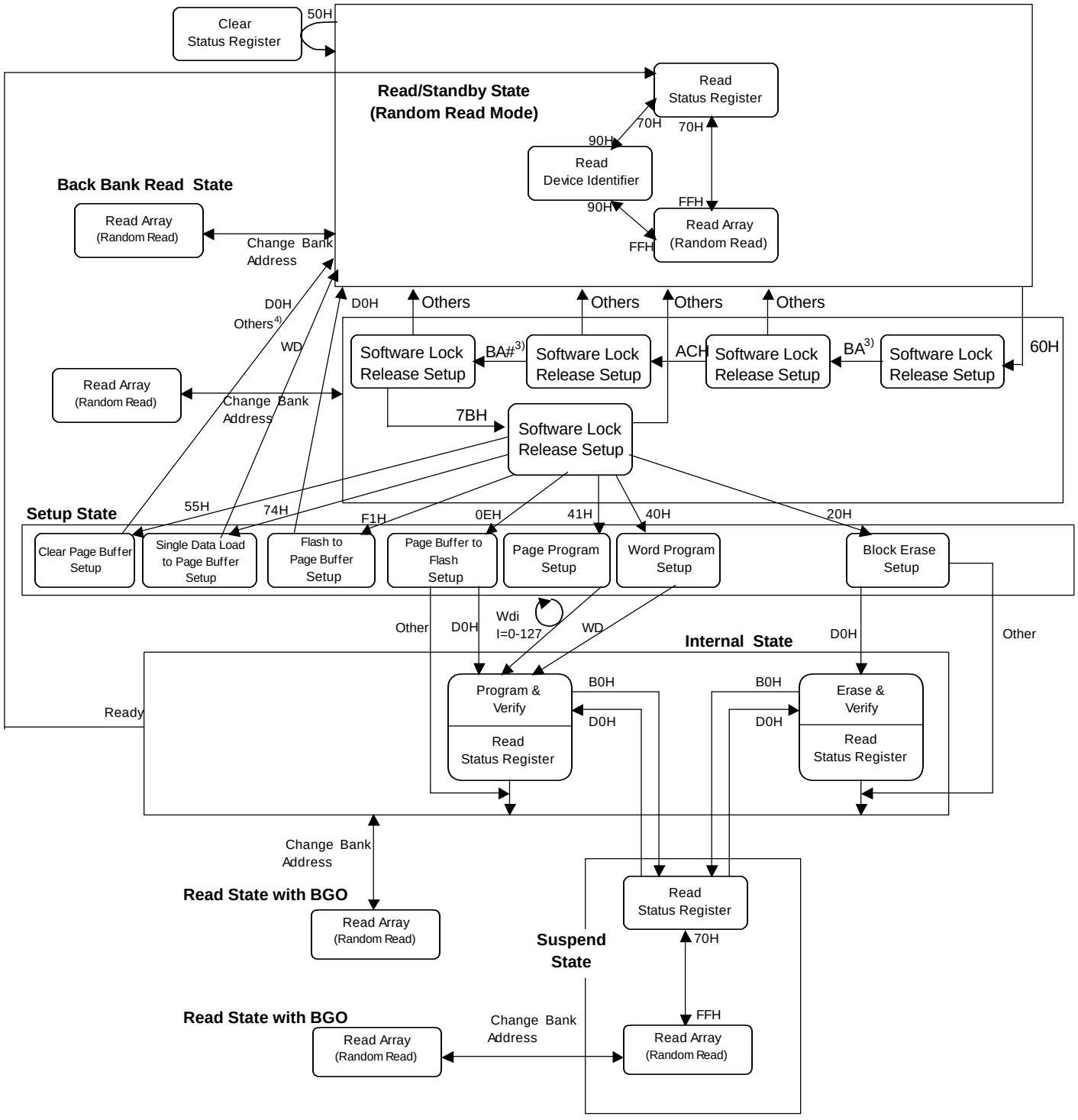
Operation Status (WP#=VIH)



1) After setting up Clear Page Buffer, D0H enables to clear Page Buffer.

2) To access any bank during Erase All Unlocked Block results Status Register Read.
Although Read Status Register Command and Read Array Command can be issued under Suspend State, output data make no sense.

Operation Status (WP#=VIL)



1) BA, BA#: Block Address, Block Address# (Shown in Command List(WP#=VIL) in detail).

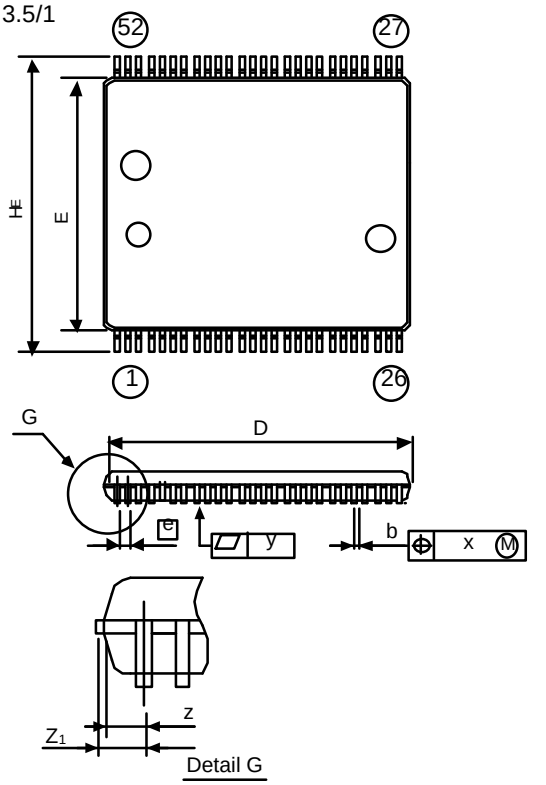
2) After setting up Clear Page Buffer, D0H enables to clear Page Buffer.

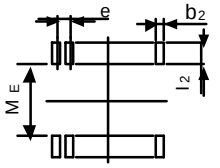
Package Dimension

52PTG-A

EIAJ Package Code	Jedec Code	Weight(g)	Lead Material
TSOPII52-P-350-0.40	—	—	Alloy 42

Scale: 3.5/1





Recommended Mount Pad

Symbol	Dimension in Millimeters		
	Min.	Nom.	Max.
A	—	—	1.2
A_1	0.05	0.125	0.2
A_2	—	1.0	—
b	0.12	0.17	0.27
c	0.105	0.125	0.175
D	10.69	10.79	10.89
E	8.79	8.89	8.99
e	—	0.4	—
H_E	10.29	10.49	10.69
L	0.45	0.5	0.65
L_1	—	0.8	—
L_p	0.45	0.6	0.75
A3	—	0.25	—
z	—	0.4	—
Z_1	—	—	0.55
x	—	—	0.08
y	—	—	0.1
Theta	0°	—	10°
M_E	—	9.09	—
l_2	0.9	—	—
b_2	—	0.225	—

M5M29KE131BTP

**134,217,728-BIT (16,777,216-WORD BY 8-BIT / 8,388,608-WORD BY 16-BIT)
CMOS FLASH MEMORY**

Stacked-uMCP (micro Multi Chip Package)

Renesas Technology Corp.
Nippon Bldg.,6-2,Otemachi 2-chome,Chiyoda-ku,Tokyo,100-0004 Japan

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