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NEC

NEC Electronics Inc.

μPD2364A
8,192 x 8-BIT MASK-PROGRAMMABLE NMOS ROM

Revision 1

Description

The μPD2364A is a 65,536-bit Read-only Memory utilizing NMOS silicon gate technology. The device is static in operation, organized as 8,192 words by 8 bits and operates from a single +5V ± 10% power supply. The μPD2364A has three-state outputs. All inputs and outputs are fully TTL-compatible. The Output Enable/Chip Enable pin is mask-programmable and can be specified by selecting 1, 0 or don't-care data and standby mode. The μPD2364A is available in a plastic (μPD2364AC) 24-pin DIP. Pinout is compatible with Mostek MK36000®

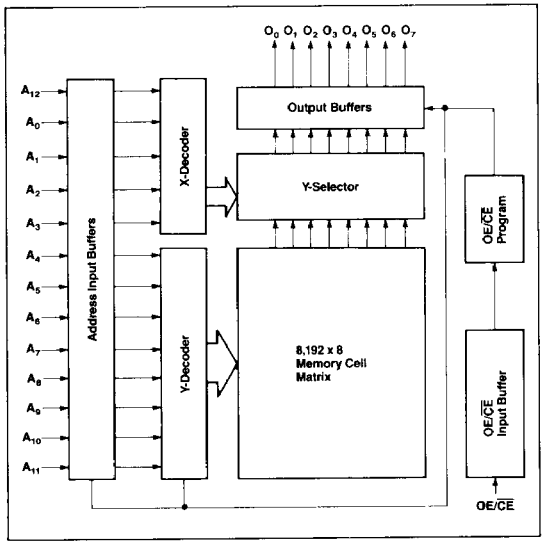
® = Registered trademark.

Features

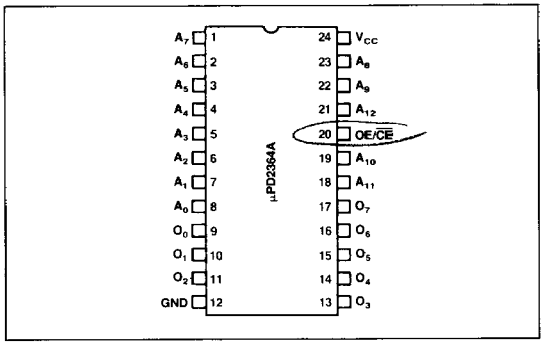
- ☐ 8,192-word by 8-bit organization
- ☐ I/O TTL-compatible
- ☐ Three-state outputs
- ☐ Single +5V ± 10% power supply
- ☐ Mask-programmable OE/$\overline{CE}$
- ☐ 24-pin plastic DIP
- ☐ 2 performance ranges:

Device	Access Time	Power Supply	
		Active	Standby
μPD2364A	200ns	70mA	15mA
μPD2364A-1	150ns	70mA	15mA

Block Diagram



Pin Configuration



Pin Identification

Pin No.	Symbol	Description
1–8, 18–19, 21–23	A_0–A_{12}	Address Inputs
9–11, 13–17	O_0–O_7	Three-state Data Outputs
12	GND	Ground
20	OE/$\overline{CE}$	Mask-programmable Output Enable/Chip Enable ①
24	V_{CC}	+5V ± 10% Power Supply

Note: ① Pin 20 may be mask-programmed as an OE or a $\overline{CE}$ function. If it is defined as OE, it may be specified as active high (1), active low (0), or don't-care (X). If it is defined as $\overline{CE}$, it will be active low (0) and a high (1) for standby mode.

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Absolute Maximum Ratings*

Supply Voltage, V_{CC}	−0.5V to +7V
Input Voltage, V_I	−0.5V to +7V
Output Voltage, V_O	−0.5V to +7V
Operating Temperature, T_{OPR}	−10°C to +70°C
Storage Temperature, T_{STG}	−65°C to +150°C

*COMMENT: Exposing the device to stresses above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of this specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Capacitance

T_A = −10°C to +70°C; V_{CC} = +5V ± 10%

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input Capacitance	C_I			10	pF	f = 1MHz
Output Capacitance	C_O			15	pF	f = 1MHz

DC Characteristics

T_A = −10°C to +70°C; V_{CC} = +5V ± 10%

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input High Voltage	V_{IH}	+2.0		V_{CC} + 1.0	V	
Input Low Voltage	V_{IL}	−0.5		+0.8	V	
Output High Voltage	V_{OH}	+2.4			V	I_{OH} = −400μA
Output Low Voltage	V_{OL}			+0.4	V	I_{OL} = +2.1mA
Input Leakage Current High	I_{LIH}			+10	μA	$V_I = V_{CC}$
Input Leakage Current Low	I_{LIL}			−10	μA	V_I = 0V
Output Leakage Current High	I_{LOH}			+10	μA	$V_O = V_{CC}$ (chip deselected)
Output Leakage Current Low	I_{LOL}			−10	μA	V_O = 0V (chip deselected)
Power Supply Current	I_{CC2}		40	70	mA	$\overline{CE}$ = V_{IL}
	I_{CC1} ①		8	15	mA	$\overline{CE}$ = V_{IH} (standby mode)

Note: ① OE $\overline{CE}$ = $\overline{CE}$.

AC Characteristics

T_A = −10°C to +70°C; V_{CC} = +5V ± 10%

Parameter	Symbol	Limits μPD2364A Min	μPD2364A Max	μPD2364A-1 Min	μPD2364A-1 Max	Unit	Test Conditions
Access Time	t_{ACC}		200		150	ns	Input Voltage: t_R, t_F = 20ns Timing Reference Levels: Input and Output = 0.8V and 2.0V Load = 1 TTL + 100pF
Chip Enable Access Time	t_{CE} ①		200		150	ns	
OE Output On Time	t_{OE} ②	10	100	10	100	ns	
Output Hold Time	t_{OH}	0		0		ns	
Output Disable Time	t_{DF}	0	90	0	90	ns	

Notes: ① OE/$\overline{CE}$ = $\overline{CE}$.
② OE/$\overline{CE}$ = $\overline{OE}$.

Timing Waveform

