MT312

Satellite Channel Decoder

Design Manual

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Key Features

- Conforms to EBU specification for DVB-S and DirecTV specification for DSS.
- On-chip digital filtering supports 1 to 45MBaud Symbol rates.
- On-chip 6-bit 60 or 90MHz dual-ADC.
- High speed scanning mode for blind symbol rate/code rate acquisition.
- Automatic IQ phase resolution.
- No signal indicator.
- Up to ±15MHz LNB frequency tracking.
- Fully digital timing and phase recovery loops.
- High level software interface for minimum development time.
- DiSEqC™ v2.2: receive/transmit for full control of LNB and dish.

Applications

- DVB 1 to 45MBaud compliant satellite receivers.
- DSS 20MBaud compliant satellite receivers.
- SCPC receivers. (Single Channel Per Carrier)
- SMATV trans-modulators. (Single Master Antenna TV)
- LMDS (Local Multipoint Distribution Service)
- Satellite PC applications.

Ordering Information

MT312C/CG/GP1N

The MT312 is a QPSK/BPSK 1 to 45MBaud demodulator and channel decoder for digital satellite television transmissions to the European Broadcast Union ETS 300 421 specification (ref. 1). It receives analogue I and Q signals from the tuner, digitises and digitally demodulates this signal, and implements the complete DVB/DSS FEC (Forward Error Correction), and de-scrambling function. The output is in the form of MPEG2 or DSS transport stream data packets. An external MPEG clock input is provided for synchronisation to MPEG decoders and DVB Common Interface Modules. The MT312 also provides automatic gain control to the RF front-end devices.

The MT312 has a serial 2-wire bus interface to the control microprocessor. Minimal software is required to control the MT312 because of the built in automatic search and decode control functions.

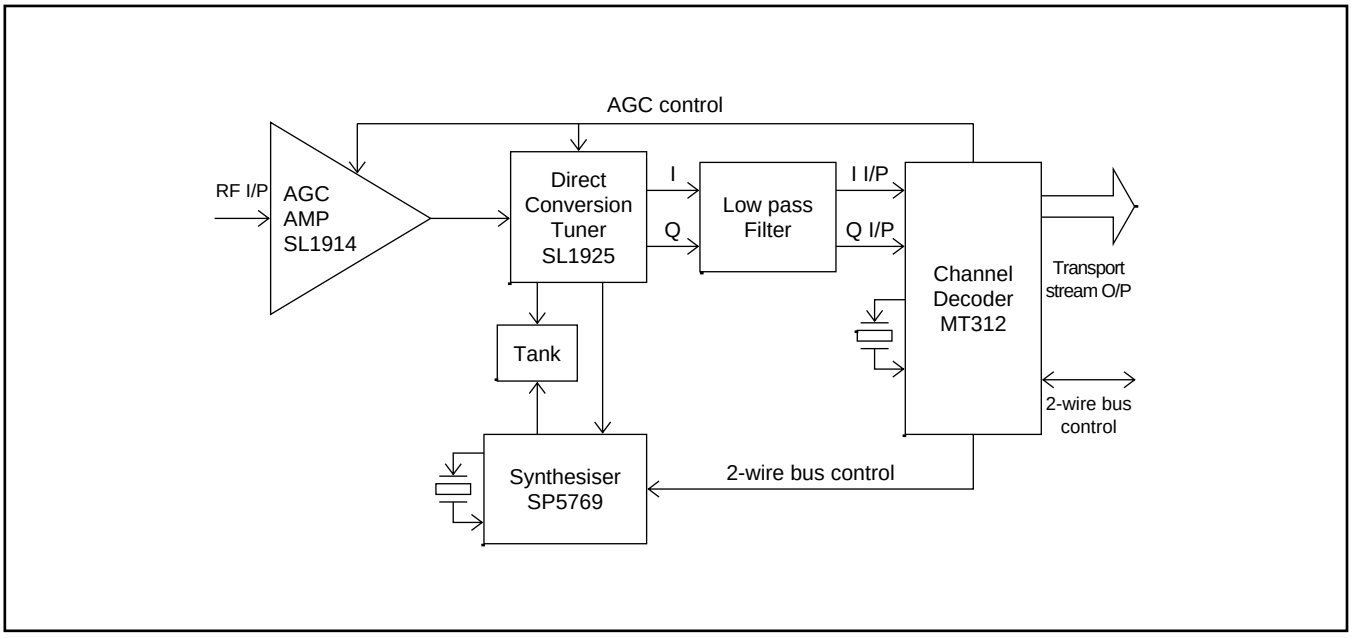


Figure 1 - System Block Diagram - SNIM5

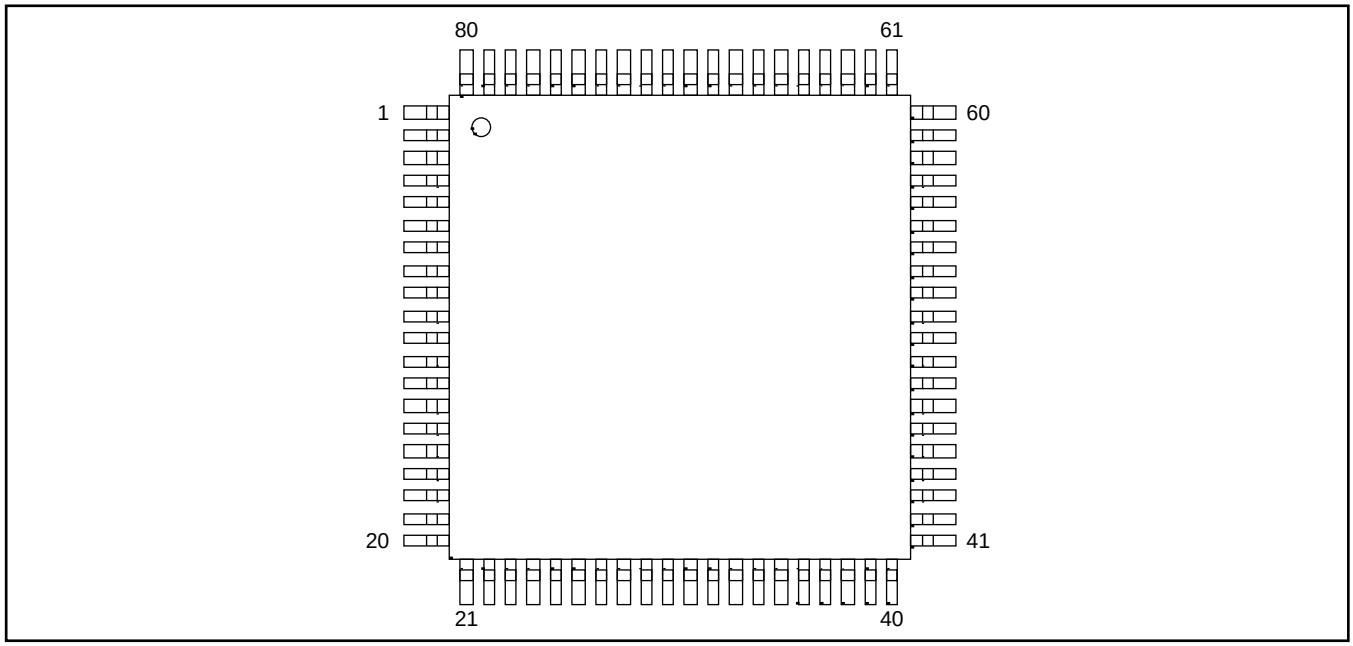


Figure 2 - System Block Diagram - SNIM5

PIN	FUNCTION	PIN	FUNCTION	PIN	FUNCTION	PIN	FUNCTION
1	CVSS	21	PLLVDD	41	CVSS	61	MDO[1]
2	CVDD	22	PLLGND	42	CVDD	62	CVDD
3	IIN[1]	23	PLL1	43	AGC	63	MDO[2]
4	ADDR[7]	24	ADCFGND	44	CLK2/GPP0	64	MDO[3]
5	ADDR[6]	25	ADCFVDD	45	DATA2/GPP1	65	MDO[4]
6	ADDR[5]	26	VRT	46	DISEQC2/GPP2	66	MDO[5]
7	ADDR[4]	27	IREF	47	DISEQC1 HV	67	CVDD
8	ADDR[3]	28	ISINGP	48	DISEQC0 22kHz	68	MDO[6]
9	CVDD	29	NC	49	$\overline{\text{RESET}}$	69	MDO[7]
10	CVSS	30	ADCDVDD	50	CVDD	70	CVSS
11	ADDR[2]	31	ADCDGND	51	CVSS	71	$\overline{\text{MDOEN}}$
12	ADDR[1]	32	VRM	52	STATUS	72	MOVAL
13	VDD	33	QSINGP	53	CLK1	73	VDD
14	MICLK	34	QREF	54	DATA1	74	VSS
15	VSS	35	VRB	55	CVDD	75	$\overline{\text{BKERR}}$
16	TESTCLK	36	ADCAGND	56	VSS	76	MOSTRT
17	CVDD	37	ADCAVDD	57	$\overline{\text{IRQ}}$	77	IIN[5]
18	$\overline{\text{XTI}}$	38	RREF	58	MOCLK	78	IIN[4]
19	XTO	39	TEST1	59	MDO[0]	79	IIN[3]
20	CVSS	40	TEST2	60	CVSS	80	IIN[2]

Table 1 - MT312 pin-out

Quick start overview

The MT312 is a QPSK/BPSK 1 to 45MBaud demodulator and channel decoder for digital satellite television transmissions compliant to both DVB-S and DSS standards and other systems, such as LMDS, that use the same architecture.

A Command Driven Control (CDC) system is provided making the MT312 very simple to program. After the tuner has been programmed to the required frequency, to acquire a DVB transmission, the MT312 requires a minimum of five registers to be written. Activity flow diagrams for initialisation and basic channel change are included in section 2.

The MT312 provides a monitor of Bit Error Rate after the QPSK module and also after the Viterbi module.

For receiver installation, a high speed scan or 'blind search' mode is available. This allows all signals from a given satellite to be evaluated for frequency, symbol rate and convolutional coding scheme. The phase of the IQ signals can be automatically determined.

Full DiSEqC™ v2.2 is provided for both writing and reading DiSEqC™ messages. Storage in registers for up to eight data bytes sent and eight data bytes received is provided.

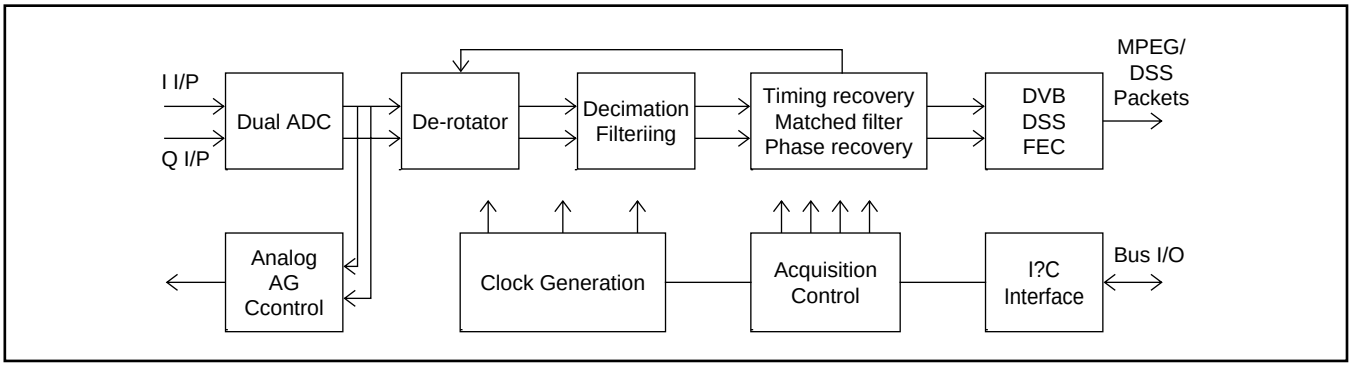


Figure 3 - MT312 Functional Block Diagram

Additional Features

- 2-wire bus microprocessor interface.
- All digital clock and carrier recovery.
- On-chip PLL clock generation using low cost 10 to 15MHz crystal.
- 3.3V operation.
- 80 pin MQFP package.
- Low external component count.
- Commercial temperature range 0 to 70°C.

Demodulator

- BPSK or QPSK programmable.
- Optional fast acquisition mode for low symbol rates.

Viterbi

- Programmable decoder rates 1/2, 2/3, 3/4, 5/6, 6/7, 7/8.
- Automatic spectrum resolution of IQ phase.
- Constraint length k=7.
- Trace back depth 128.
- Extensive SNR and BER monitors.

De-Interleaver

- Compliant with DVB and DSS standards.

Reed Solomon

- (204, 188) for DVB and (146,130) for DSS.
- Reed Solomon Bit-error-rate monitor to indicate Viterbi performance.

De-Scrambler

- EBU specification De-scrambler for DVB mode.

Outputs

- MPEG transport parallel & serial output.
- MPEG clock input for external synchronising of MPEG data output.
- Integrated MPEG2 TEI bit processing for DVB only.

Application Support

- Channel decoder system evaluation board.
- Windows based evaluation software.
- ANSI C generic software.

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PLEASE NOTE: This manual has the following convention:

All numerical values are shown as decimal numbers, unless otherwise defined.

1. Functional Overview

1.1 Introduction

MT312 is a single-chip variable rate digital QPSK/ BPSK satellite demodulator and channel decoder. The MT312 accepts base-band in-phase and quadrature analogue signals and delivers an MPEG or DSS packet data stream. Digital filtering in MT312 removes the need for programmable external anti-alias filtering for all symbol rates from 1 to 45Mbaud. Frequency, timing and carrier phase recovery are all digital and the only feed-back to the analogue front-end is for automatic gain control. The digital phase recovery loop enables very fine bandwidth control that is needed to overcome performance degradation due to phase and thermal noise.

All acquisition algorithms are built into the MT312 controller. The MT312 can be operated in a Command Driven Control (CDC) mode by specifying the Symbol rate and Viterbi code rate. There is also a provision for a search for unknown Symbol rates and Viterbi code rates.

1.2 Analogue-to-Digital Converter

The MT312 contains dual 6-bit A/D converters which each sample a 500mVpp single-ended analogue input at up to 90MHz. The fixed rate sampling clock is provided on-chip using a programmable PLL needing only a low cost 10 to 15MHz crystal. Different crystal frequencies can be combined with different PLL ratios, depending on the maximum symbol rate, allowing a flexible approach to clock generation.

1.3 QPSK Demodulator

The demodulator in the MT312 consists of signal amplitude offset compensation, frequency offset compensation, decimation filtering, carrier recovery, symbol recovery and matched filtering.

The decimation filters give continuous operation from 2Mbits/s to 90Mbits/s allowing one receiver to cover the needs of the consumer market as well as the single carrier per channel (SCPC) market with the same components without compromising performance, that is, the channel reception is within 0.5dB from theory. For a given Symbol rate, control algorithms on the chip detect the number of decimation stages needed and switch them in automatically.

The frequency offset compensation circuitry is capable of tracking out up to ±15MHz frequency offset. This allows the system to cope with relatively large frequency uncertainties introduced by the Low Noise Block (LNB). Full control of the LNB is provided by the DiSEqC™ outputs from the MT312. Horizontal / Vertical polarisation and an instruction modulated 22kHz signal are available under register control. All DiSEqC™ v2.2 functions are implemented on the MT312 (ref. 2).

An internal state machine that handles all the demodulator functions controls the signal tracking and acquisition. Various pre-set modes are available as well as blind acquisition where the receiver has no prior knowledge of the received signal. Fast acquisition algorithms have been provided for low Symbol rate applications. Full interactive control of the acquisition function is possible for debug purposes.

In the event of a signal fade or a cycle slip, QPSK demodulator allows sufficient time for the FEC to re-acquire lock, for example, via a phase rotation in the Viterbi decoder. This is to minimise the loss of signal due to the signal fade. Only if the FEC fails to re-acquire lock for a long period (which is programmable) would QPSK try to re-acquire the signal.

The matched filter is a root-raised-cosine filter with either 0.20 or 0.35 roll-off, compliant with DSS and DVB standards. Although not a part of the DVB standard, MT312 allows a roll-off of 0.20 to be used with other DVB parameters.

An AGC signal is provided to control the signal levels in the tuner section of the receiver and ensure the signal level fed to the MT312 is set at an optimal value under all reception conditions.

The MT312 provides comprehensive information on the input signal and the state of the various parts of the device. This information includes Signal to Noise Ratio (SNR), signal level, AGC lock, timing and carrier lock signals. A maskable interrupt output is available to inform the host controller when events occur.

1.4 Forward Error Correction

The MT312 contains FEC blocks to enable error correction for DVB-S and DSS transmissions. The Viterbi decoder block can decode the convolutional code with rates 1/2, 2/3, 3/4, 5/6, 6/7 or 7/8. The block features automatic synchronisation, automatic IQ phase resolution and automatic code rate detection. The trace back depth of 128 provides better performance at high code rates and the built-in synchronisation algorithm allows the Viterbi decoder to lock onto signals with very poor signal-to-noise ratios. Viterbi bit error rate monitor provides an indication of the error rate at QPSK output.

The 24-bit error count register in the Viterbi decoder allows the bit error rate at the output of the QPSK demodulator to be monitored. The 24-bit bit error count register in the Reed-Solomon decoder allows the Viterbi output bit error rate to be monitored. The 16-bit uncorrectable packet counter yields information about the output packet error rate. These three monitors and the QPSK SNR register allows the performance of the device and its individual components, such as the QPSK demodulator and the Viterbi decoder, to be monitored extensively by the external microprocessor.

The frame/byte align block features a sophisticated synchronisation algorithm to ensure reliable recovery of DVB and DSS framed data streams under worst case signal conditions. The de-interleaver uses on-chip RAM and is compatible with the DVB and DSS algorithms.

The Reed-Solomon decoder is a truncated version of the (255, 239) code. The code block size is 204 for DVB and 146 for DSS. The decoder provides a count of the number of uncorrectable blocks as well as the number of bit errors corrected. The latter gives an indication of the bit error rate at the output of the Viterbi decoder.

In DVB mode, spectrum de-scrambling is performed compatible with the DVB specification. The final output is a parallel or serial transport data stream; packet sync; data clock; and a block error signal. The data clock may be inverted under software control.

1.4.1.1 Viterbi Error Count Measurement

A method of estimating the bit error rate at the output of the QPSK block has been provided in the Viterbi decoder. The incoming data bit stream is delayed and compared with the re-encoded and punctured version of the decoded bit stream to obtain a count of errors see Figure 4 - Viterbi block diagram.

The measurement system has a programmable register to determine the number of data bits (the error count period) over which the count is being recorded. A read register indicates the error count result and an interrupt can be generated to inform the host microprocessor that a new count is available.

The VIT ERRPER H-M-L group of three registers is programmed with required number of data bits (the error count period) (VIT ERRPER[23:0]). The actual value is four times VIT ERRPER[23:0]. The count of errors found during this period is loaded by the MT312 into the VIT ERRCNT H-M-L trio of registers when the bit count VIT ERRPER[23:0] is reached. At the same time an interrupt is generated on the $\overline{\text{IRQ}}$ line. Setting the IE FEC[2] bit in the IE FEC register enables the interrupt, see page 32. Reading the register does not clear VIT ERRCNT [23:0], it is only loaded with the error count.

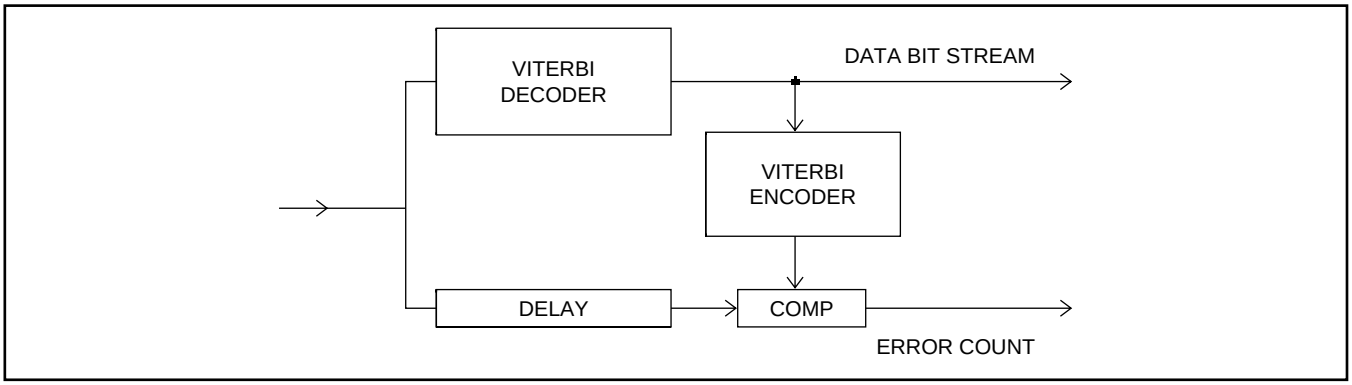


Figure 4 - Viterbi block diagram

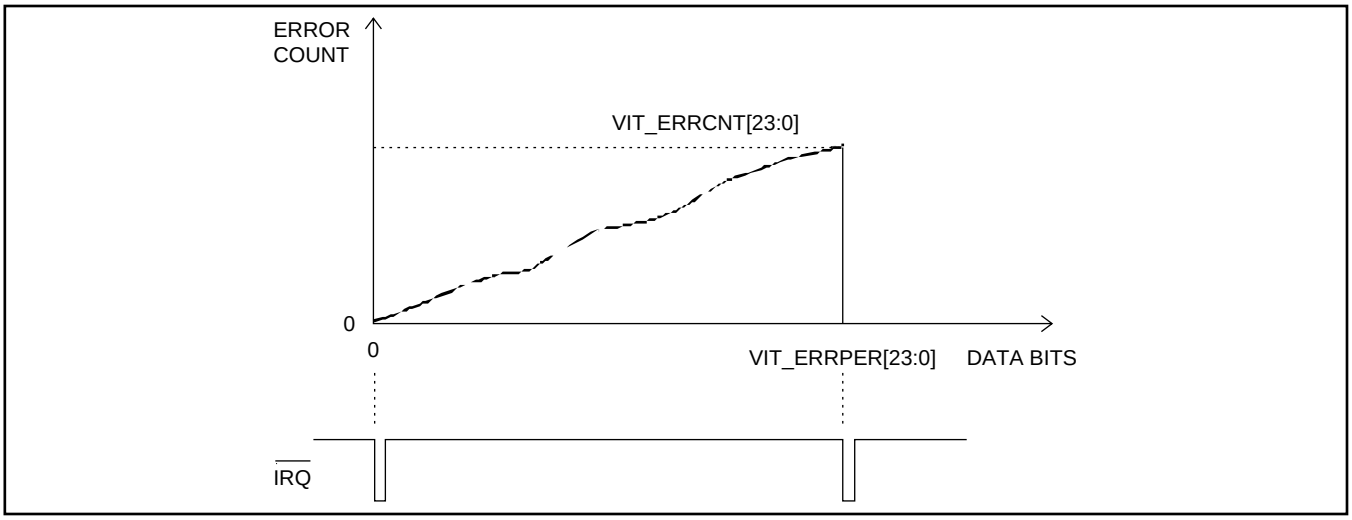


Figure 5 - Viterbi error count measurement

Figure 5 shows the bit errors rising until the maximum programmed value of VIT ERRPER[23:0] is reached, when an interrupt is generated on the $\overline{IRQ}$ line to advise the host microprocessor that a new value of bit error count has been loaded into the VIT ERRCNT [23:0] register. The $\overline{IRQ}$ line will go high when the IE FEC register is read by the host microprocessor. The error count may be expressed as a ratio:

$$\frac{VIT_ERRCNT[23:0]}{VIT_ERRPER[23:0]*4}$$

1.4.1.2 Viterbi Error Count Coarse Indication

To assist in the process of aligning the receiver dish aerial, a coarse indication of the number of bit errors being received can be provided by monitoring the STATUS line with the following set up conditions.

The frequency of the output waveform will be a function of the bit error count (triggering the maximum value programmed into the VIT MAXERR[7:0] register and the dish alignment on the satellite. This VIT MAXERR mode is enabled by setting the FEC STAT EN register bit B0. Figure 5 above shows the bit errors rising to the maximum value programmed and triggering a change of state on the STATUS line.

1.4.2 The Frame Alignment Block

The frame alignment algorithm detects a sequence of correctly spaced synchronising bytes in the Viterbi decoded bit-stream and arranges the input into blocks of data bytes. Each block consists of 204 bytes for DVB and 147 bytes for DSS. In the DSS mode, the synchronising byte is removed from the data stream, so only 146 bytes of a block are passed to the next stage. The frame alignment block also removes the 180° phase ambiguity not removed by Viterbi decoder.

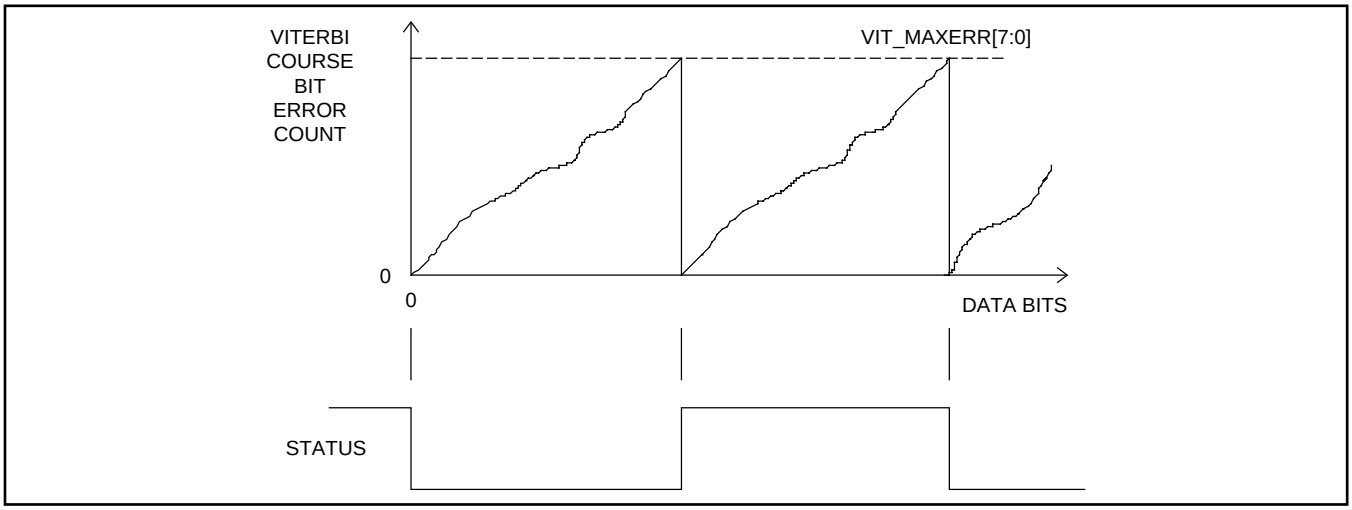


Figure 6 - Viterbi error count coarse indication

1.4.3 The De-interleaver Block

1.4.3.1 DVB

Before transmission, the data bytes are interleaved with each other in a cyclic pattern of twelve. This ensures the bytes are spaced out to avoid the possibility of a noise spike corrupting a group of consecutive message bytes. The diagram below shows conceptually how the convolutional de-interleaving system works. The synchronisation byte is always loaded into the First-In-First-Out (FIFO) memory in branch 0. The switch is operated at regular byte intervals to insert successively received bytes into successive branches. After 12 bytes have been received, byte 13 is written next to the synchronisation byte in branch 0, etc. In the MT312, this de-interleaving function is realised using on-chip Random Access Memory (RAM).

1.4.3.2 DSS

Before transmission, the data bytes are interleaved with each other in a cyclic pattern of thirteen. This ensures the bytes are spaced out to avoid the possibility of a noise spike corrupting a group of consecutive message bytes. The diagram below shows conceptually how the convolutional de-interleaving system works. On the MT312, this function is realised in the same Random Access Memory (RAM) as used for DVB, but utilising different addressing algorithm.

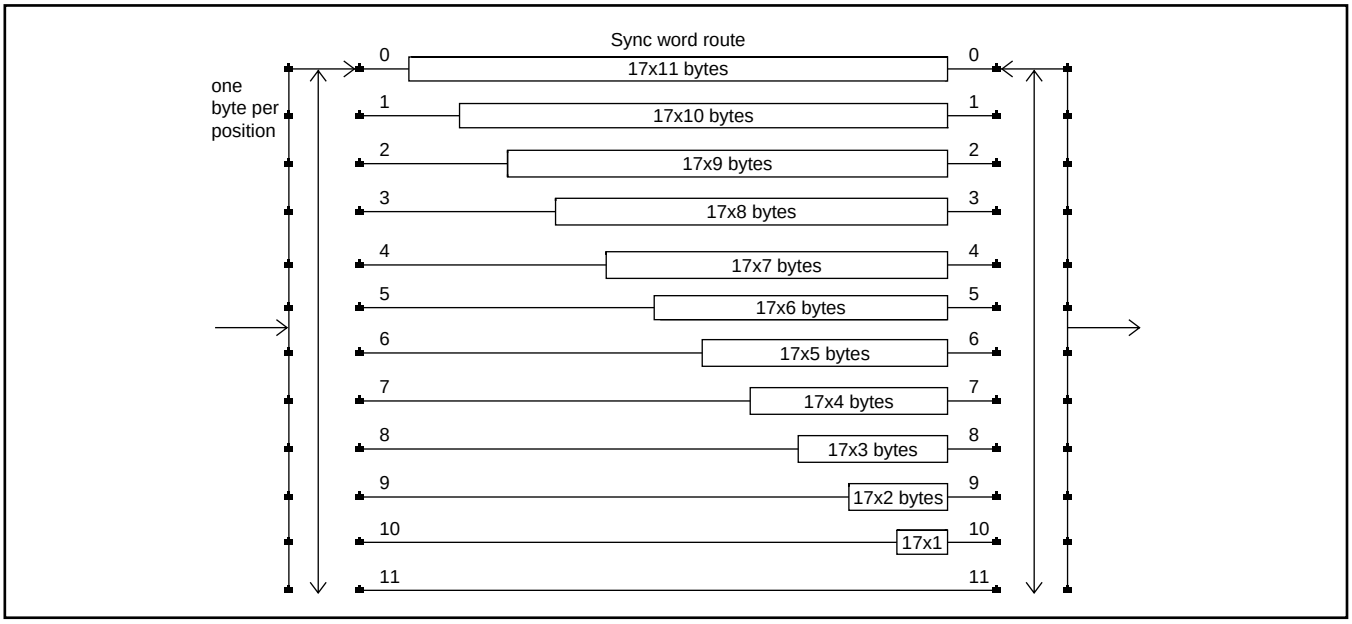


Figure 7 - DVB Conceptual diagram o f the conoluntional de-interleaver block

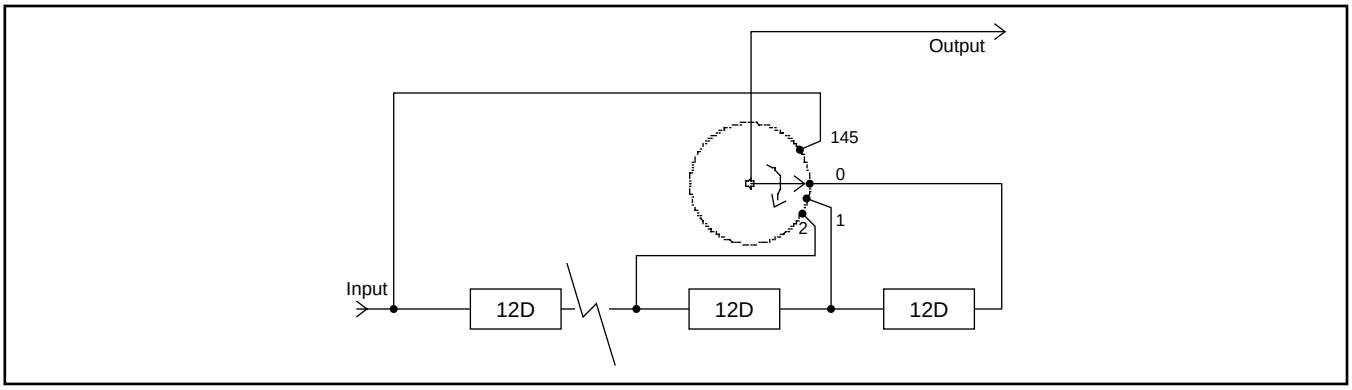


Figure 8 - DSS Conceptual diagram of the convolutional de-interleaver block

1.4.4 The Reed Solomon Decoder Block

DVB and DSS data are encoded using shortened versions of the Reed-Solomon code of block length 255, containing 239 message bytes and 16 check bytes, that is (255,239) with T = 8. Both encoders use the same generator polynomial. The code block size for DVB is 204 and that for DSS is 146. Hence DVB code is (204, 188) and DSS code is (146, 130), with both having T = 8. The block structure of the DVB and DSS Reed-Solomon codes are as shown in Figure 9 and Figure 10 below.

The Reed-Solomon decoder can correct up to eight byte errors per packet. If there are more than 8 bytes containing errors, the packet is flagged as uncorrectable using the pin $\overline{\text{BKERR}}$. In the case of DVB the transport error indicator (TEI) bit of the MPEG packet is set to 1, if setting of TEI is enabled.

1.4.5 The Energy Dispersal (De-Scrambler) Block, DVB only

Before Reed Solomon encoding in the DVB transmission system, the MPEG2 data stream is randomised using the configuration shown in Figure 11 below. This is a Pseudo Random Binary Sequence (PRBS) generator, with the polynomial:

$$1 + X^{14} + X^{15}$$

The PRBS registers are loaded with the initialisation sequence as shown, at the start of the first transport packet in a group of eight packets. This point is indicated by the inverted sync byte B8hex. The normal DVB sync byte is 47hex. The data starting with the first byte after the sync byte is randomised by exclusive-ORing data bits with the PRBS. (The sync bytes themselves are not randomised).

In the decoder, the process of de-randomising or de-scrambling the data is exactly the same as described above. The de-scrambler also inverts the sync byte B8hex so that all MPEG output packets have the same synch byte 47hex.

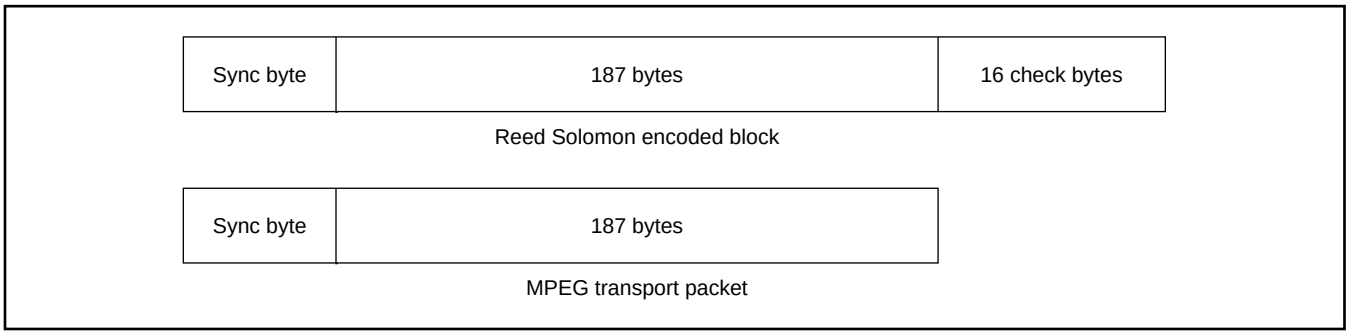


Figure 9 - DVB block structure

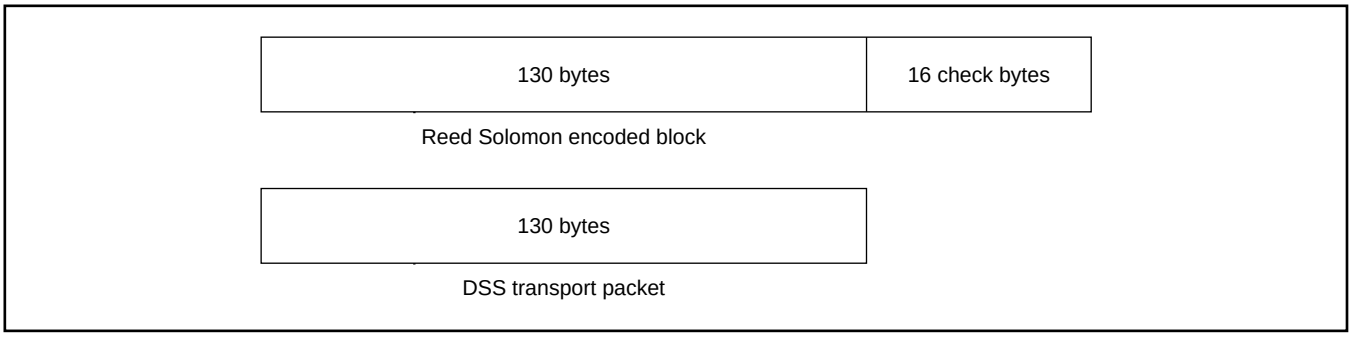


Figure 10 - DSS block structure

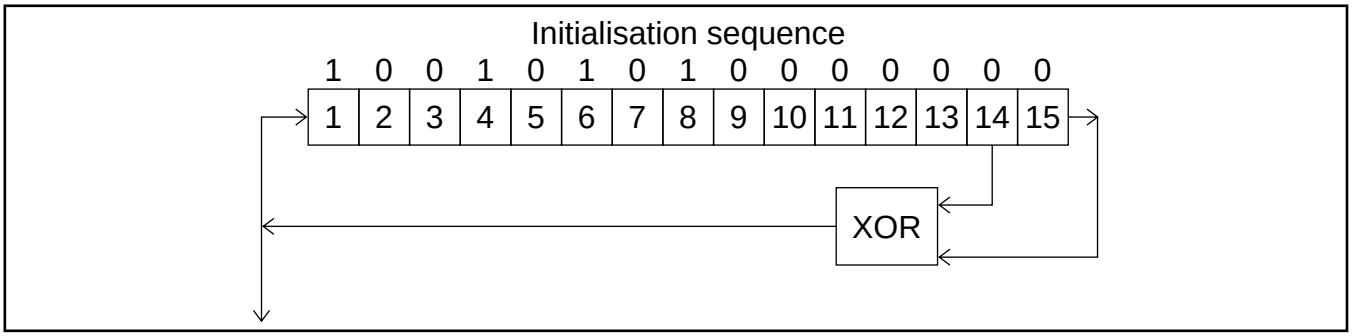


Figure 11 - DVB Energy dispersal conceptual diagram

1.4.6 Output Stage

Transport stream can be output in a byte-parallel or bit-serial mode. The output interface consists of an 8-bit output, output clock, a packet validation level, a packet start pulse and a block error indicator.

The output clock rate depends on the Symbol rate, QPSK/BPSK choice, convolutional (Viterbi) coding rate, DVB/DSS choice and byte-parallel or bit-serial output mode. This rate is computed by MT312 to be very close to the minimum required to output packet data without packet overlap. Furthermore, the packets at the output of MT312 are as evenly spaced as possible to minimise packet position movement in the transport layer. The maximum movement in the packet synchronisation byte position is limited to ± one output clock period.

An external MPEG clock can be input to synchronise the MPEG data output to MPEG decoders.

1.5 Control

Automatic Symbol Rate Search, Code Rate Search, Signal Acquisition and Signal Tracking algorithms are built into the MT312 using a sophisticated on-chip controller. The software interaction with the device is via a simple Command Driven Control (CDC) interface. This CDC maps high level inputs such as symbol rates in MBaud and frequencies in MHz, to low level on-chip register settings. The on-chip control state machine and the CDC significantly reduces the software overhead as well as the channel search times. There is also an option for the host processor to by-pass both the CDC as well as the on-chip controller and take direct control of the QPSK demodulator.

Once the MT312 has locked up, any frequency offset can be read from the LNB FREQ error registers 7 and 8. The frequency synthesiser under the software control can be re-tuned in frequency to optimise the received signal within the SAW bandwidth. Note that MT312 compensates for any frequency offsets before QPSK demodulation. Hence a frequency offset will not necessarily lead to a performance loss. Performance loss will occur only if a significant part of the signal is cut off by the SAW or base-band filter, due to this frequency offset. This will happen only if the symbol rate is close to maximum supported by that filter. In such an event it is recommended that front-end be re-tuned to neutralise this error before the SAW filter. It is then necessary for the MT312 to re-acquire the signal.

The MT312 can generate control signals to enable full control of the dish and LNB. The chip implements the signals needed for the full DiSEqC™ v2.2 specification. This includes high/low band selection, polarisation and dish position.

In this mode, the Symbol rate in MBaud and Viterbi code rate are the only values needed to start the MT312 searching for the signal. The CDC module maps the high level parameters into the various low level register settings needed to acquire and track the signal. The low level registers may be read and directly modified to suit very specific requirements. However, this is not recommended.

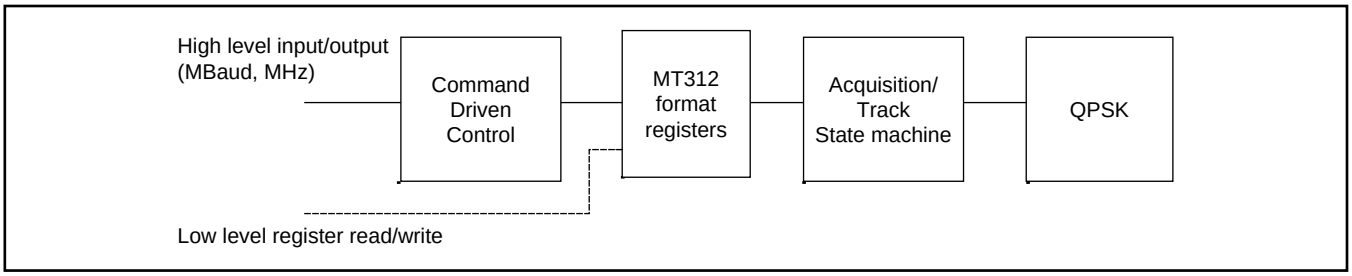


Figure 12 - MT312 Control Structure

1.5.2 Symbol Rate and Code Rate Search Mode

Where the Symbol rate and/or the Viterbi code rate are unknown, the MT312 can be programmed to search for QPSK/BPSK signals. The user should define the range(s) over which the search is required. The MT312 will then locate and track any signal detected. Failure to find a QPSK signal in the specified frequency and specified symbol rate ranges will be indicated by interrupts (see 6.2 QPSK Demodulator Read Registers). MT312 will carry on searching these ranges after issuing these interrupts. When the MT312 has locked onto a signal, the Symbol rate in MBaud may be read from the MONITOR registers. The Viterbi code rate may be read from the FEC STATUS register. This search facility is primarily for the initial installation of a set top box.

1.6 Direct Conversion Application

Figure 1 shows a direct conversion system that mixes the L-band input to the tuner directly down to I and Q baseband channels at zero intermediate frequency.

The RF AGC amp and tracking filter provide the required tuner noise figure and limit the total power reaching the SL1925. These elements also give isolation between the SL1925 local oscillator and the L-band tuner input. This is an important factor since both signals are at the same frequency.

The baseband filter is an anti-alias filter. This replaces the filtering normally carried out with a SAW filter in conventional single conversion tuners.

It is important to note that all the channel filtering needed to isolate low Baud rate signals is contained within the MT312. The low pass filter before MT312 is designed not to filter channels, but to minimise any aliasing due to sampling. To illustrate this, let the sampling frequency be 90 MHz and the maximum symbol rate be 45 MBaud. The bandwidth of the 45 MBaud QPSK signal, with 0.35 roll-off, is about 60 MHz. If the channel has been mapped precisely to base-band, the pass-band of the low pass filter should extend up to 30 MHz. However, it is preferable to make this bandwidth larger by about 5 MHz, partly to reduce the in-band phase distortion introduced by the filter and partly to reduce the loss of signal due to LNB offset. The filter must attenuate signals beyond 60 MHz by about 30 dB, as these signal will alias to the useful frequency range with 90 MHz sampling.

Although the system is designed for 45 MBaud, if the actual symbol rate is much lower, say 1 MBaud, then MT312 will automatically introduce all the digital filtering needed to isolate the 1 MBaud signal.

Figure 13 - Alternative System Block Diagram - SNIM6 shows an alternative application when a reduced Symbol rate is acceptable. The SL1935 combines the functions of the RF pre-amp, direct conversion zero IF tuner and synthesiser.

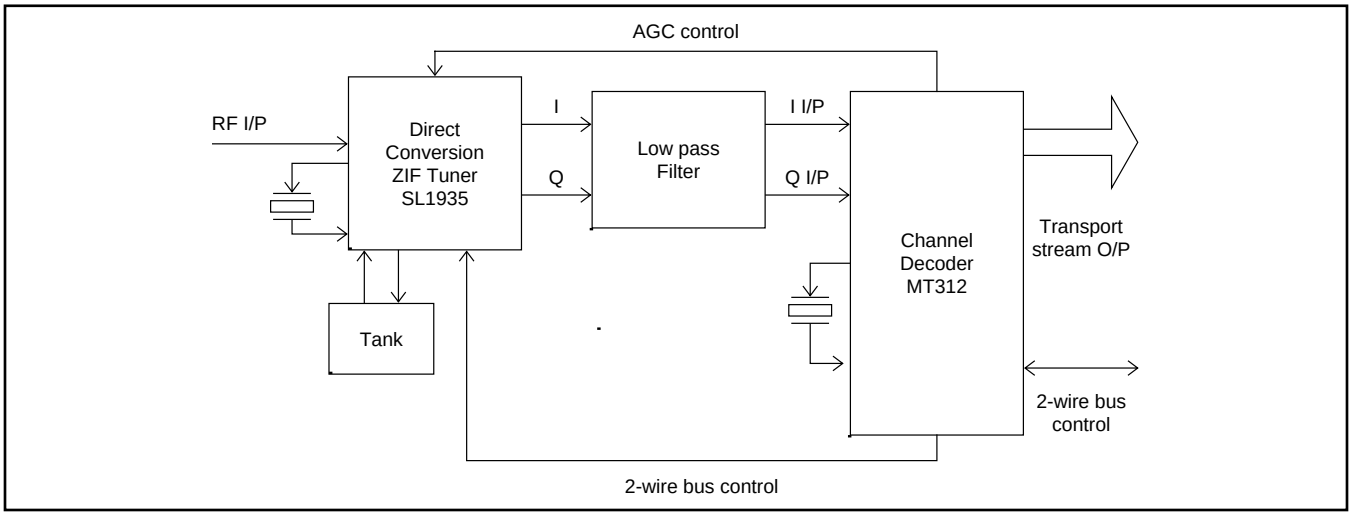


Figure 13 - Alternative System Block Diagram - SNIM6

1.7 DiSEqC™ Transmit and Receive Messages

The MT312 has the capability to send and receive DiSEqC™ messages. Eight registers are provided to store a message for transmission and a further eight registers are provided to store a received message. The received bytes have a parity bit and a parity error bit in addition to the eight data bits. These additional bits are read out in following the data bits, so two byte reads are required for each data byte.

1.7.1 DiSEqC™ Transmitting Messages

The sequence of events to send a message are as follows:

1. Load the required message bytes into the DiSEqC™ Instruction register 36, see page 34. Sequential writes to the same register is achieved by setting the Inhibit Auto Incrementing (IAI) bit 7 in RADD, the register address byte.
2. Load the number of bytes (less one) in the DiSEqC™ instruction in the register DISEQC MODE[5:3], see page 32.
3. Set DISEQC MODE[2:0] = 4 to command the MT312 to encode the data and transmit the message.
4. Reset DISEQC MODE[2:0] to either 0 or 1 depending on previous setting of 22kHz off or on.

The data loaded into DISEQC INSTR register is retained, so that if the same message is to be repeated, the data loading stage 1 above can be omitted.

1.7.2 DiSEqC™ Receiving Messages

The MT312 will automatically listen for DiSEqC™ messages 5ms after a message has been transmitted. If a return message is expected, the DISEQC MODE[2:0] must be set to zero in order to leave the LNB control signal free for another DiSEqC™ transmitter to respond.

The sequence of events to receive a message are as follows:

1. Enable DiSEqC2 GPP2 pin 46 as an input by setting GPP CTRL register 20 B5 to zero.
2. Enable interrupts if the $\overline{\text{IRQ}}$ pin is being used to interrupt the host processor in DISEQC2 CTRL1 register 121.
3. Monitor DISEQC2 INT register.
4. If B3 = 1 and B1 = 0, there has been no message received.
5. If a message has been received, B0 will be set, If B1 is also set the message is complete. DISEQC2 INT register B7-4 indicate how many bytes have been received.
6. Read the received message from DISEQC2 FIFO register 120 by setting the Inhibit Auto Incrementing (IAI) bit 7 in RADD, the register address byte and sequentially reading DISEQC2 FIFO for the indicated number of bytes. Each data byte read requires two 2-wire bus reads. The second or the pair of bytes contains the parity bit and a parity bit error indicator.

The user may choose to wait for the end of message indication, before reading the message, if it is known that the message is not greater than eight bytes. However, if the length of message is not known, the message should be read out of the FIFO by the host as it is being received. Care must be taken to avoid a FIFO buffer overflow. DISEQC2 INT register B7-4 will indicate how many bytes remain in the FIFO.

2 MT312 Software Control

This section describes the sequences of register operations needed to acquire DVB and DSS channels with known or unknown parameters.

Communication with the MT312 is via a standard 2-wire bus and the first byte following the chip address, in write mode, is the register address (RADD).

The register map is organised to group important Read registers at the lowest addresses, then the main control Write registers in the next block of addresses.

The first register to be written must be the Configuration register, which has been placed at the highest register address, because it is only written once during the initialisation sequence.

The CONFIG register can only be reset by the hardware reset. The MT312 is held in a power saving mode following the hardware reset.

After a hardware reset, the MT312 must be taken out of the power save mode by writing a one to the MSB of the CONFIG register (see 1.1 Introduction). When MT312 is not being used it can be put back into the power save mode by writing a zero to the MSB of CONFIG.

2.1 MT312 Register Map Overview

Address	Description	Section	Type
00 - 06	Interrupt and Status	5.1to 5.4-	read
07 - 19, 108 - 117, 123, 124	Primary signal monitors	5.5 to 5.17	read
20 - 39, 41, 96, 103	Primary control parameters	4 to 4.20	write / read
40, 42 - 49, 50 - 106, 125	Secondary parameters	11.1.1 to 11.1.52	write / read
107, 118 - 122	Secondary monitors	11.2.1 to 4.22	read
126	Chip identification	5.18	read
127	Chip configuration	4.22	write / read

Table 2 - MT312 register map overview

All write / read registers take on default values on full software reset, except for the configuration register (127), that is only reset to the default value by a hardware reset.

3 MT312 Initialisation

3.1 The Configuration Register (127)

CONFIG[B7-0]: This register is for setting up the MT312. It must be loaded first before any other register. It can only be reset to the default value by the $\overline{\text{RESET}}$ pin being pulled low. After loading this register, wait 150µs for the Clock PLL to settle before writing to the RESET register. During this wait period, the tuner may be programmed via the General Purpose Port. Note that the GPP register occupies the address space before the RESET register.

CONFIG[B7]: 312 ENHigh = MT312 enable.
Low = MT312 disable to save power.

CONFIG[B6-5]: DSS BDSS A

0	0: DVB mode
0	1: DSS mode 1 - code rate 2/3
1	0: DSS mode 2 - code rate 6/7
1	1: DSS Code Rate search

If both DSS A and DSS B are set high, the MT312 will search for the code rate in DSS mode. If either of the DSS A or DSS B are set high, the Symbol rate is automatically set to 20Mbaud and SYM RATE registers (23 & 24) are ignored. The matched filter root-raised-cosine roll-off is set to 0.20 and bit B0 of QPSK CTRL (26) is ignored. Also, any code rate programmed into VIT MODE register (25) and VIT SETUP register (86) will be ignored.

Also in DSS mode TS SW RATE register (50) must be set to 20, see 10.2.10 Timing Synchronisation Sweep Rate. Register 50 (R/W).

CONFIG[B4]: BPSK High = BPSK
Low = QPSK

CONFIG[B3-2]: PLL FACTOR[1:0]:

B3-2	Multiplication factor
00:	3
01:	4
10:	6
11:	9

CONFIG[B1]: CRYS15 High = 15MHz crystal.
Low = 10MHz crystal.

CONFIG[B0]: ADCEXT High = ADC external.
Low = ADC internal.

e.g. For a crystal frequency of 10MHz, a system clock frequency of 60MHz, the PLL ratio will be 6, requiring the PLL FACTOR[1:0] = 2.

For QPSK reception and ADC internal, the MT312 is enabled by writing 88 hex to register 127.

MT312 computes the System clock frequency using bits B3-B1 above. This frequency is used internally for computing parameters needed for acquiring the QPSK signal.

It is possible to use a crystal frequency other than 10 or 15 MHz. As an example, let the crystal frequency be 10.25MHz and the PLL multiplication factor be 6. Then B3 is set to 1 and B2 to 0. Bit B1 may be given an arbitrary value (0 or 1). The external software must compute the system clock frequency and load this value (multiplied by 2) to the SYS CLK register (Address 34). In the above example, the system clock frequency is 61.5 MHz and hence the value 123 has to be loaded into SYS CLK register.

The QPSK demodulator checks the SYS CLK register and if this is non-zero, it uses the contents of this as the system clock frequency, for internal calculations mentioned above. If this register is zero (which is the default setting), QPSK demodulator works out the system clock frequency from bits B3-B1 of the CONFIG register assuming that the crystal frequency is either 10 or 15 MHz, as defined by bit B1.

3.2 Power Supplies

To avoid the possibility of destructive latch-up, the CVDD supply must never, at any time during power-up, exceed 0·5V above the VDD supply and must also remain within the absolute maximum ratings, see section 12.2 on page 78.

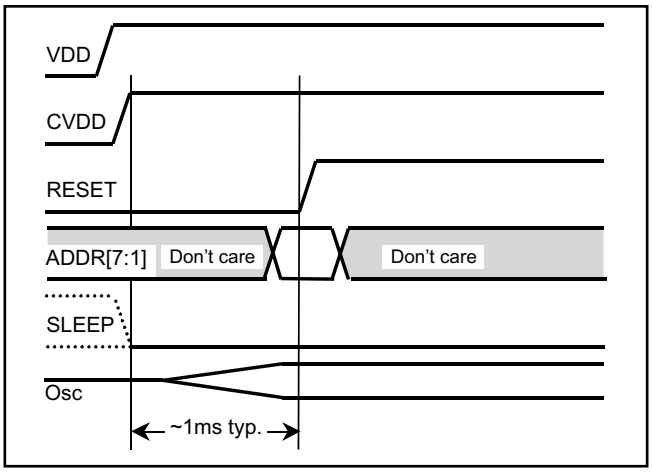


Figure 14 - MT351 power-up sequence

In general therefore, the VDD supply should be established ahead of, or simultaneously with the C_{VDD} supply.

3.3 Initialisation Sequence

MT312 will be in the power save mode after a hardware reset. The first command to be written must be to the CONFIGURATION register at address 127. After loading this register, wait 150µs before writing to the RESET register. During this wait, the tuner can programmed to the required channel frequency via the General Purpose Port (register 20). If the AGC slope control bit of AGC CTRL(39) or the AGC REF(41) are to be changed, it is best to write to these registers after writing to the RESET register. This will allow the front-end AGC loop to settle while the other registers are being written.

Next write 128 to the RESET register (21) to reset the MT312 state machine and all parameter registers to the default settings. It is then necessary to change the default setting of register 49 to 50 (decimal).

If necessary, other default parameters may need to be changed. These may include:

- Slope of AGC control signal - see register (39) ACG CTRL[B0] AGC SL bit
- AGC Reference value - see register (41) AGC REF
- Relative phase of IQ spectrum - see register (25) VIT MODE[B6]
- LNB frequency search range, default is ±6MHz - see register (37) FR LIM
- For low Baud rates only, set fast frequency acquisition mode - see register (26) set QPSK CTRL[B2] = 1

To invert MOCLK or $\overline{\text{BKERR}}$ output signals - see register (96) OP CTRL

After this, the LNB controls are defined, in register (22) DISEQC MODE.

The signal parameters should then be written to the MT312. The symbol rate (registers 23 & 25 SYM RATE) may be specified within ±2% of the required value, absolute precision is not required to achieve successful lock and tracking. If the symbol rate is unknown, a search mode is available.

Selecting the correct bit of register (25) VIT MODE, if known, programs the convolutional code rate. If the code rate is unknown, some or all of the bits of VIT MODE may be set to force the MT312 to search for the code rate.

Finally, the MT312 is given a GO command, register (27) GO =1, to release the state machine and to start the signal acquisition sequence. This is summarised as an example in the following flow diagram.

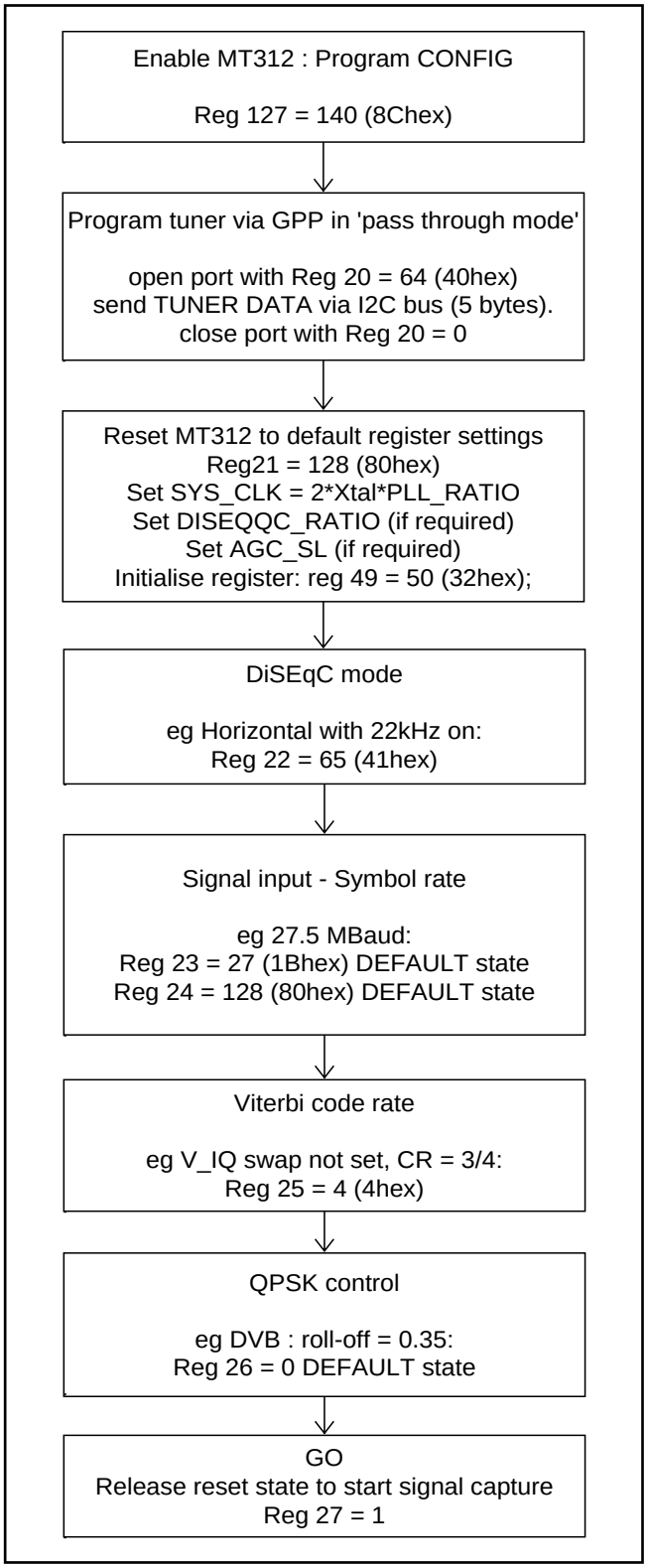


Figure 15 - Initialisation sequence in DVB mode

3.4 Spectral Inversion

Spectral inversion of the QPSK signal can be caused by the transmitter or the receiver front-end. In the latter case, this could happen due to the way I-Q conversion is carried out or because the I and Q wires are swapped between the I-Q converter and the MT312. If spectral inversion is caused by the receiver front-end, then this must be removed by swapping I and Q (within MT312) before QPSK demodulation, by setting Q IQ SP bit B6 of QPSK CTRL register (26) to 1.

If no spectral inversion is caused by the receiver front-end design, then bit B6 of QPSK CTRL must always be held at zero. If the transmitted signal is known to be spectrally inverted, then V IQ SP bit B6 of the VIT MODE register (25) must be set to 1. Then I and Q are swapped after QPSK demodulation. If the spectral inversion status of the transmitted signal is not known, then after QPSK has locked (i.e. QPSK CT LOCK = 1), the software must try to achieve FEC lock with the bit B6 of VIT MODE register first at zero and then at one.

3.5 MT312 Initialisation Read/Write Registers

3.5.1 Reset. Register 21 (R/W)

NAME	ADR	B7	B6	B5	B4	B3	B2	B1	B0		Def hex
RESET	21	FR 312	PR 312	FR QP	PR QP	FR VIT	PR VIT	PR BA	PR DS	R/W	00

B7: FR 312 High = Full reset of MT312 device.

B6: PR 312 High = Partial reset of MT312 device.

B5: FR QP High = Full reset of QPSK block.

B4: PR QP High = Partial reset of QPSK block.

B3: FR VIT High = Full reset of Viterbi block.

B2: PR VIT High = Partial reset of Viterbi block.

B1: PR BA High = Partial reset of Byte Align block.

B0: PR DS High = Partial reset of De-scrambler block.

Writing a one to these register locations generates a reset pulse three crystal clock periods wide.

The register automatically resets to zero after use.

A full reset does reset the registers to their default values.

A partial reset does not reset the registers to their default values.

3.5.2 MT312 Configuration. Register 127 (R/W)

NAME	ADR	B7	B6	B5	B4	B3	B2	B1	B0		Def hex
CONFIG	127	312 EN	DSS B	DSS A	BPSK	PLL FACTOR [1:0]		CRYS 15	ADC EXT	R/W	08

CONFIG[7:0]: This register is for setting up the MT312. It must be loaded first before any other register. It can only be reset by the $\overline{\text{RESET}}$ pin being pulled low.

B7: 312 EN — High = MT312 enable.
Low = MT312 disable to save power.

B6-5:

DSS B	DSS A	
0	0:	DVB mode
0	1:	DSS mode 1 - code rate 2/3
1	0:	DSS mode 2 - code rate 6/7
1	1:	DSS search mode

If both DSS A and DSS B are set high, the MT312 will search for the code rate in DSS mode. Then the Symbol rate is automatically set to 20Mbaud and SYM RATE registers (23 & 24) are ignored. Also, any code rate programmed into VIT MODE register (25) and VIT SETUP register (86) will be ignored.

Also in DSS mode TS SW RATE register (50) must be set to 20, see page 70.

B4: BPSK — High = BPSK
Low = QPSK

B3-2: PLL FACTOR[1:0]:

B3-2	Multiplication factor
00:	3
01:	4
10:	6
11:	9

B1: CRYS15 — High = 15MHz crystal.
Low = 10MHz crystal.

B0: ADCEXT — High = ADC external.
Low = ADC internal.

e.g. For a crystal frequency of 10MHz, a system clock frequency of 60MHz, the PLL ratio will be 6, requiring the PLL FACTOR[1:0] = 2.

When MT312 is not being used it can be put into power save mode by setting bit B7 to 0.

3.5.3 System Clock Frequency. Register 34 (R/W)

NAME	ADR	B7	B6	B5	B4	B3	B2	B1	B0		Def hex
SYS CLK	34	SYS CLK[7:0] - System clock frequency x2 in MHz								R/W	00

SYS CLK[7:0] = System clock frequency * 2 in MHz.

The SYS CLK register must be programmed to indicate the system clock frequency to the calculation unit. The maximum system clock frequency allowed is 90MHz.

e.g. for a crystal frequency = 10MHz, if the PLL multiplication ratio is 9,

The system clock frequency = 90MHz.

Then SYS CLK[7:0] = 180.

The system clock frequency is NOT affected by the setting of SYS CLK[7:0] register.

3.6 MT312 Initialisation Read Register

3.6.1 Identification. Register 126 (R)

NAME	ADR	B7	B6	B5	B4	B3	B2	B1	B0		Def hex
ID	126	ID[7:0] Chip identification.								R	03

ID[7:0]: This register provides an identification number related to the MT312 version.

4 Tuner Control

4.1 Simple Channel Change Sequence

If the MT312 is running, to change channel keeping the same signal conditions, it is only necessary to change the tuner data and possibly the DiSEqC™ data. NO reset is necessary.

4.2 Channel Change Sequence with a new Symbol Rate

If the MT312 is running, to change channel and Symbol rate but not Viterbi coding rate, change the tuner data and possibly the DiSEqC™ data and Symbol rate. NO reset is necessary.

4.3 Channel Change Sequence with Search Mode

If the signal parameters are unknown, it is possible to instruct the MT312 to find a digital signal and report the parameters found. Registers 24 and 25 are programmed with the expected range(s) and the search mode bit SYM RATE[B15] is set high. A code rate search is forced by programming more than one bit in VIT MODE (26) register. The IQ spectrum phase can be automatically determined by setting bit 7 in the VIT MODE (26) register.

Note: code rate 6/7 is not searched for DVB mode.

If a signal with the specified symbol rate range (or ranges) is not found in the frequency range searched, a QPSK Baud End interrupt (Bit B6, QPSK INT L (2)) is issued.

When the MT312 QPSK section has locked to the signal, this is indicated in register (6) by QPSK STAT H[B0] = 1. The symbol rate found can be read from registers (123 - 124) MONITOR, provided the register (103) MON CTRL = 3. The tolerance of the result is ±0.25%. The 14 MSBs of this result (discarding two LSBs) may be written as the 14 LSBs of the 16-bit register pair (23 and 24) SYM RATE in the non-search mode for re-acquisition of the same channel.

The FEC is locked to the signal, when the Byte Align lock in FEC STATUS[B2] = 1. Then the code rate found can be read from FEC STATUS[B6-4], see register 6 49 for details.

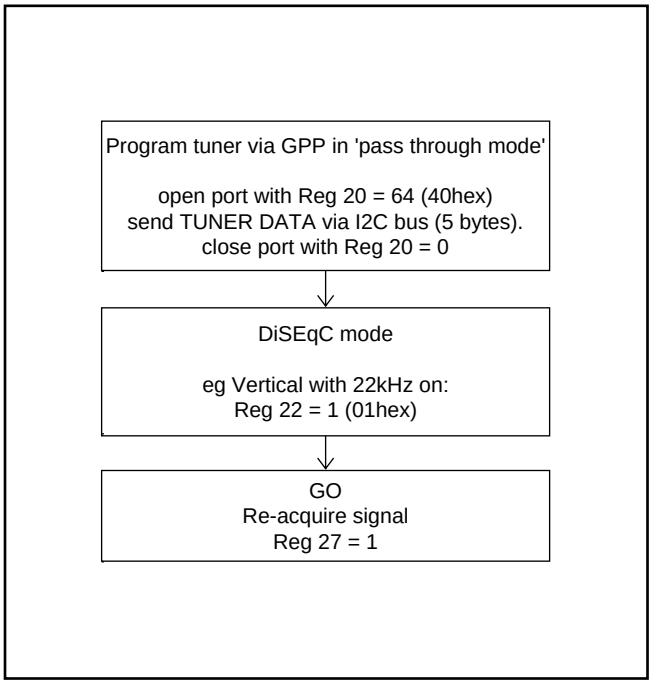


Figure 16 - Simple channel change sequence

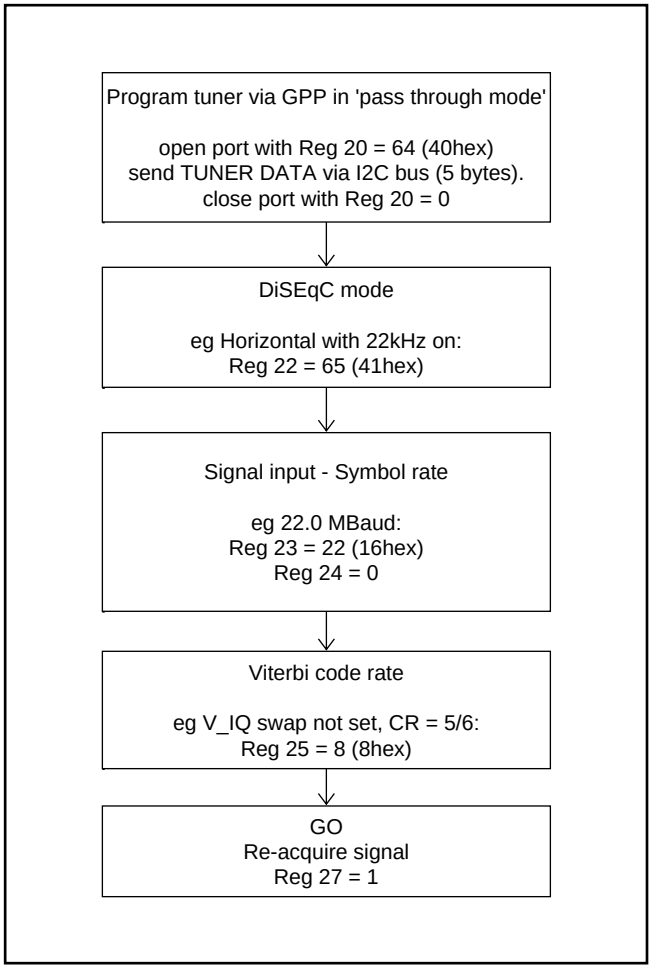


Figure 17 - Channel change sequence with new Symbol rate, DVB mode

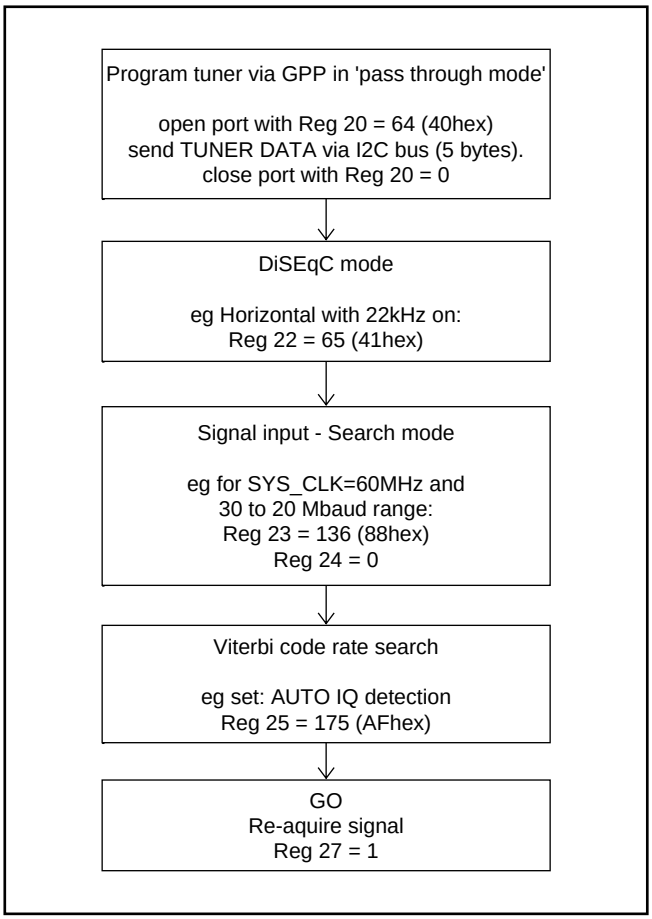


Figure 18 - Channel change sequence with search mode, DVB mode

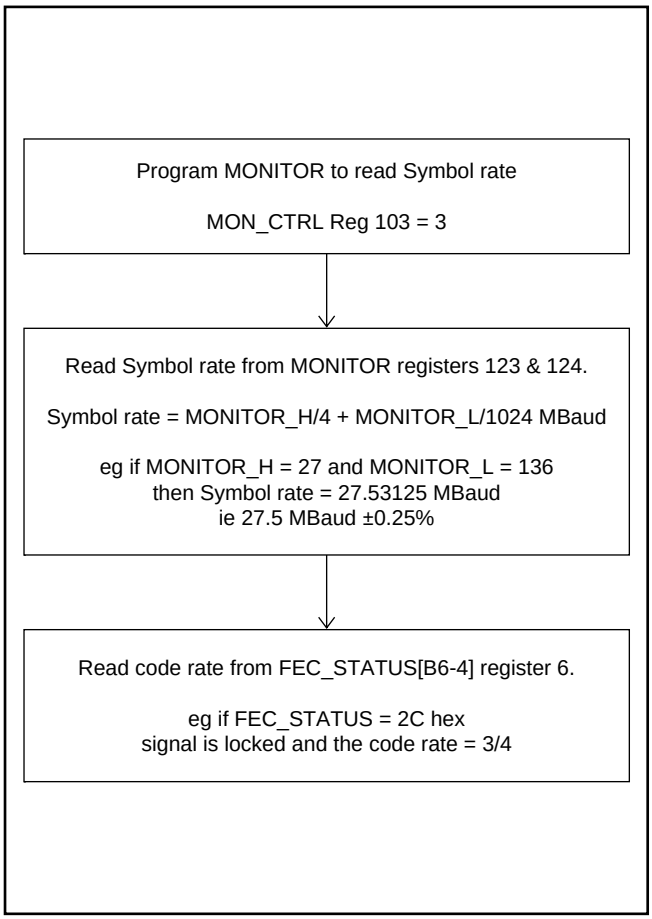


Figure 19 - Results of Symbol rate and code rate search, DVB or DSS mode

4.4 Tuner Control Read/Write Registers

4.4.1 General Purpose Port Control. Register 20 (R/W)

NAME	ADR	B7	B6	B5	B4	B3	B2	B1	B0		Def hex
GPP CTRL	20	Reserved	2W PAS	GPP DIR[2:0]			GPP PIN[2:0]			R/W	20

B7: Reserved. Must be set low.

B6: 2W PAS: High = 2-wire bus Pass-through.
Low = GPP pin I/O direction set by GPP DIR[2:0].

B5-3: GPP DIR[2:0] Any bit set high configures the corresponding GPP[2:0] pin as output
Any bit set low configures the corresponding GPP[2:0] pin as input
Mixed use of pins as inputs and outputs is allowed.

If B6 = 1, pass-through mode, then:
GPP DIR[1:0] are ignored,
B2: = Input or output set by GPP DIR[2] - relating to pin 46.

Pin 45 = DATA2, this is a transparent, bi-directional connection to the primary DATA1.
Pin 44 = CLK2, this is a transparent, bi-directional connection to the primary CLK1.

If B6 = 0 then: GPP DIR[2:0] defines the input/output conditions of the GPP pins and:
If a pin[n] is defined as output then:
GPP PIN[n] high forces GPP[n] pin high
GPP PIN[n] low forces GPP[n] pin low

If a pin[n] is defined as input then:
GPP[n] pin high sets bit GPP PIN[n] high
GPP[n] pin low sets bit GPP PIN[n] low

Allocation of GPP PIN[2:0] is:

GPP PIN[2] = DiSEqC™ v2.2 input, 3 wire bus Enable or can be used for any other application
GPP PIN[1] = DATA2 or 3 wire bus Data
GPP PIN[0] = CLK2 or 3 wire bus Clock

The register default state of 20 hex allows the GPP[2] pin to be used for the 3 wire bus Enable line and to be kept low at all times, except when programming the Synthesiser.

When GPP[2] pin is used for DiSEqC™ v2.2 input, the GPP CTRL register will need to be set to zero after every full reset to make GPP[2] an input.

4.4.2 FR LIM: Frequency Limit. Register 37 (R/W)

NAME	ADR	B7	B6	B5	B4	B3	B2	B1	B0		Def hex
FR LIM	37	Reserved	FR LIM[6:0] - Freq. Limit in MHz							R/W	30

B7: Reserved. Must be set low.

FR LIM[6:0] Frequency search range MHz x 8. This unsigned 7 bit number represents a search range of +/-0 to +/- 15.875MHz. Default value 30 (hex) = +/- 6MHz.

4.4.3 FR OFF: Frequency Offset. Register 38 (R/W)

NAME	ADR	B7	B6	B5	B4	B3	B2	B1	B0		Def hex
FR OFF	38	FR OFF[7:0] - Freq. Offset in MHz								R/W	00

FR OFF[7:0] Frequency offset correction value in MHz x 32. This 2's complement 8 bit number represents an offset from -4MHz to +3.96875MHz. Default value 0.

The frequency search is carried out in the range [(-FR LIM + FR OFF), (FR LIM + FR OFF]. Frequency offset register can be useful in reducing frequency search during channel hopping, especially with low symbol rates. If the location of the wanted channel with respect to the current channel is known and if the synthesiser step size is too large to set the precise frequency of that channel, then the FR OFF register can be used to take up any residual frequency offset.

4.5 Tuner Control Read Registers

4.5.1 Measured LNB Frequency Error. Registers 7 - 8 (R)

NAME	ADR	B7	B6	B5	B4	B3	B2	B1	B0		Def hex
LNB FREQ H	07	LNB FREQ15:8] Measured LNB frequency error (high byte)								R	00
LNB FREQ L	08	LNB FREQ[7:0] Measured LNB frequency error (low byte)								R	00

LNB FREQ[15:0]: Once the chip is in lock these two registers provide a measurement of the frequency of the signal at the input to MT312. Ideally, this frequency is zero. Due to LNB frequency uncertainty this frequency may take a positive or negative value. Then the analogue front-end may be re-tuned to bring this offset close to zero. Note that MT312 indicates the frequency location of the QPSK spectrum with respect to zero frequency. The direction in which the synthesiser frequency has to be stepped depends on the design of the analogue front-end. Also note that in many instances it will not be necessary to re-tune even when there is a relatively large frequency offset. This is because MT312 compensates for this frequency offset before it demodulates the signal. Re-tune only if a substantial part of the QPSK spectrum is affected by the SAW or base-band filter which precedes MT312. This will be the case only for symbol rates which are close to the maximum symbol rate supported by the above mentioned filters.

When MT312 locks part of the frequency offset is taken up by the frequency compensation mixer and part by the carrier synchroniser. LNB FREQ gives only the value in the frequency compensation mixer. Over a short period of about 1 s after lock, the carrier synchroniser will transfer all the frequency compensation to the mixer. Hence the LNB FREQ reading will have an error less than ±5% of the symbol rate, during this short period after lock. If an accurate frequency reading is needed immediately after lock, the calculation given in section on FREQ ERR2 has to be performed by external software.

LNB FREQ[15:0] Frequency offset MHz x 512. This is a 2's complement 16 bit number. e.g. a hex value of F680 (=-2432) represents an offset of -4.75MHz.

4.5.2 Frequency Error 1 and 2. Registers 111 - 115 (R)

NAME	ADR	B7	B6	B5	B4	B3	B2	B1	B0		Def hex
FREQ ERR1 H	111	FREQ ERR1[23:16] Input frequency error coarse (high byte)								R	00
FREQ ERR1 M	112	FREQ ERR1[15:8] Input frequency error coarse (middle byte)								R	00
FREQ ERR1 L	113	FREQ ERR1[7:0] Input frequency error coarse (low byte)								R	00

FREQ ERR1[23:0] Ratio of Frequency Compensation Mixer offset to System Clock x 2^{24}. 24 bit signed number. For most purposes the LS byte can be ignored hence the alternative definition is more useful: FREQ ERR1[23:8] Ratio of Frequency Compensation Mixer offset to System Clock x 2^{16}. 16 bit signed number.

NAME	ADR	B7	B6	B5	B4	B3	B2	B1	B0		Def hex
FREQ ERR2 H	114	FREQ ERR2[15:8] Input frequency error fine (high byte)								R	00
FREQ ERR2 L	115	FREQ ERR2[7:0] Input frequency error fine (low byte)								R	00

FREQ ERR2 [16:0] Ratio of Carrier Synchroniser offset to Symbol Rate x 2^{8}. 16 bit signed number. This value drops to near zero within a second or so of signal lock.

To obtain an accurate value for the frequency offset at any time, especially immediately after lock, the error from each of these registers can be calculated and add together. In practice only the two most significant bytes of FREQ ERR 1 are required, so that the net offset can be calculated as:

$$\text{Frequency offset} = \frac{\text{FREQ_ERR1(23:8)* PLL_CLK}}{65536} + \frac{\text{FREQ_ERR2(15:0)*Rs}}{256}$$

Where PLL CLK is the sytem clock frequency (e.g. 60 MHz) and Rs is the symbol rate in MBd.

Any frequency error in FREQ ERR2 transfers to FREQ ERR1 very rapidly after lock, so that any delay between reading the two values will cause an error in the calculation. It is therefore recommended that the five bytes above are read as a block, especially if the two wire bus is subject to congestion or other delays.

5 DiSEqC Control

5.1 Screen Printouts of DiSEqC™ Waveforms

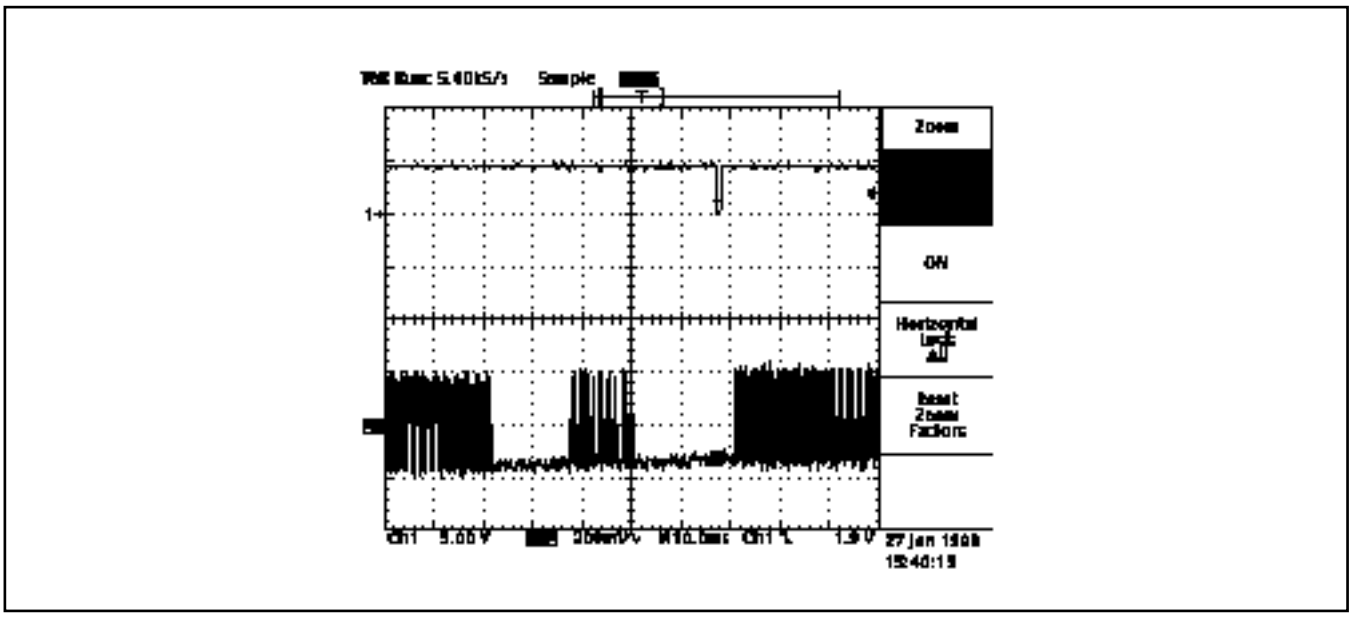


Figure 20 - A DiSEqC™ data byte interrupting a continuous 22kHz tone

The timing periods of the 16ms before the data byte and 16ms afterwards to the interrupt being asserted are clearly shown. The restoration of the 22kHz after the interrupt is controlled by software.

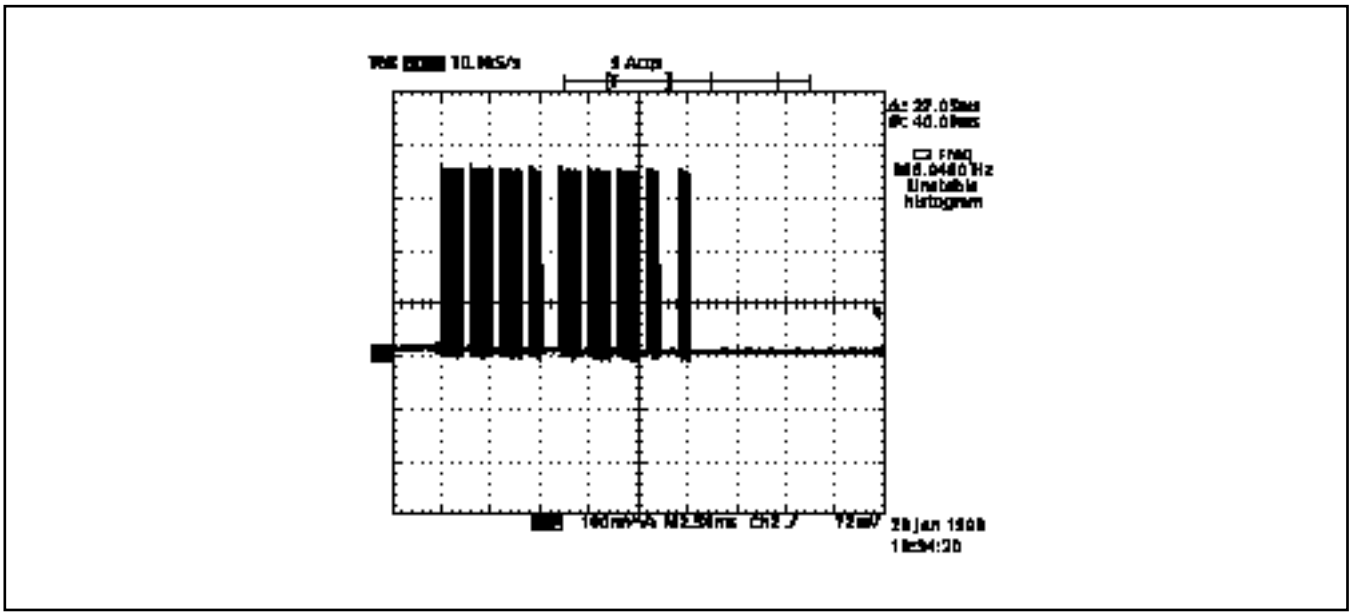


Figure 21 - One DiSEqC™ data byte - 0x11 (hex) plus parity bit

A 'zero' comprises 22kHz on for 1ms then off for 0.5ms. A 'one' comprises 22kHz on for 0.5ms then off for 1ms. The ninth bit is an odd parity bit.

5.2 DiSEqC Control Read/Write Registers

5.2.1 DiSEqC™ Mode Control. Register 22 (R/W)

NAME	ADR	B7	B6	B5	B4	B3	B2	B1	B0		Def hex
DISEQC MODE	22	Reserved	HV	DISEQC instruction length			22kHz mode			R/W	00

B7: Reserved. Must be set low.

B6: HV H/V polarisation control: High = Horizontal, DISEQC[1] pin = high
Low = Vertical, DISEQC[1] pin = low
The DISEQC[1] pin controls the externally generated 13/18V LNB voltage.

B5-3: Number of bytes in DiSEqC™ instruction minus 1, to output on DISEQC[0] pin.
i.e. if the message contains four bytes, program B5-3 with the value three.

B2-0: DiSEqC™ mode:

0:	22kHz off
1:	22kHz on continuous
2:	Burst mode - on for 12.5ms = '0'
3:	Burst mode - modulated 1:2 for 12.5ms = '1'
4:	Modulated with bytes from DISEQC INSTR
5-7:	Reserved.

Note: for modes 2 and 3, an interrupt is generated 16ms after the '0' or '1' burst.
for mode 4, there is a 16ms delay before the message bytes, then an interrupt is generated 16ms after the last message byte has been sent. The requisite number of bytes must be pre-loaded into DISEQC INSTR (register 36) before this bit is set, see 31.

5.2.2 DiSEqC(tm) Ratio. Register 35 (R/W)

NAME	ADR	B7	B6	B5	B4	B3	B2	B1	B0		Def hex
DISEQC RATIO	35	DISEQC RATIO[7:0]								R/W	00

DISEQC RATIO[7:0] This must be programmed to set the Diseqc output tone frequency.

$$F_{out} = \frac{F_{xtal}}{4*DISEQC_RATIO[7:0]}$$

Where F_{out} is in kHz and F_{xtal} is in MHz.

For a 22kHz output tone, DISEQC RATIO[7:0] = 11.364 * F_{xtal}

e.g. with F_{xtal} = 10MHz, DISEQC RATIO[7:0] = 114, or for 15 MHz 170.

For this example, the DiSEqC™ frequency = $\frac{11E6}{4*125}$ = 22kHz.
For a 10MHz crystal, the tone frequency range is from 9.8kHz with DISEQC RATIO = 255 to 250kHz with DISEQC RATIO = 10. A lower value than 10 causes the tone frequency to become unstable, until the DISEQC RATIO = 0, the default, value giving a 22kHz tone frequency. This range is not guaranteed, the maximum tone frequency should be used with caution.

5.2.3 DiSEqC™ Instruction (R/W). Register 36 (R/W)

NAME	ADR	B7	B6	B5	B4	B3	B2	B1	B0		Def hex
DISEQC INSTR	36	DISEQC Instruction [7:0]								R/W	00

Up to eight instruction data bytes are first loaded into a bank of registers through this register. The 2-wire automatic register address incrementing is turned off during this loading by setting B7: IAI = 1 in RADD, (register address). The number of bytes (less one) must be defined in the DiSEqC™ instruction register DISEQC MODE[5:3].

i.e. DISEQC MODE[5:3] = (number of bytes in the DiSEqC™ instruction) - 1

When the DiSEqCTM instruction data bytes have been loaded, set DISEQC MODE[2:0] = 4. At the same time program DISEQC MODE[5:3] as required. The instruction data is modulated onto the 22kHz signal and output from the DISEQC[0] pin.

An interrupt is generated 16ms after all the data bytes have been sent and the MT312 then resets DISEQC MODE[5:0] to zero, see Figure 19 on page 33.

5.2.4 DiSEqC™ 2 Control 1. Registers 121 (R/W)

NAME	ADR	B7	B6	B5	B4	B3	B2	B1	B0		Def hex
DISEQC2 CTRL1	121	DISEQC2 CTRL1[7:0]								R/W	00

B7-6: MIN TONE PER Minimum Tone Period.

B7-6:	MIN TONE PER
00	3.0 * DISEQC RATIO
01	3.125 * DISEQC RATIO
10	2.875 * DISEQC RATIO
11	2.75 * DISEQC RATIO

B7:6 are for controlling (or fine tuning) the DiSEqC™ 2 receive algorithm.

B5: Send extended pulse to the Status pin 52. This is a test or diagnostics bit. If it is set to 1, then the cleaned up and extended pulse stream is sent to the status pin so that it can be recorded or observed.

B4: DiSEqC™ 2 Reset only the DiSEqCTM 2 receive module. Automatically set low again after use.

This is the software (partial) reset for DISEQC2 module. If this is set to 1 in the DISEQC2 listen (or receive) period, any listen operations will be aborted and DISEQC2 will wait until the end of the next transmission to expect a reply.

Note that the host beginning the next DISEQC2 transmission will have a similar effect to writing bit 4.

B3: Interrupt enable for bit B3 of DISEQC2 INT STAT register 118.

B2: Interrupt enable for bit B2 of DISEQC2 INT STAT register 118.

B1: Interrupt enable for bit B1 of DISEQC2 INT STAT register 118.

B0: Interrupt enable for bit B0 of DISEQC2 INT STAT register 118.

Bits B0 and B3 are interrupt enables. These determine whether bits B0 to B3 of DISEQC2 INT (register 118, see 33) have any impact on the pin $\overline{IRQ}$ 57 of the MT312.

Note that buffer overflow interrupt does not have an interrupt enable and hence this cannot be brought out to the $\overline{IRQ}$ pin.

5.2.5 DiSEqCTM 2 Control 2. Registers 122 (R/W)

NAME	ADR	B7	B6	B5	B4	B3	B2	B1	B0		Def hex
DISEQC2 CTRL2	122	MIN PULS PER			TONE EXT PER			MAX TONE PER		R/W	D4

B[7:5]: MIN PULS PER Minimum Pulse Period.

B7-5:	MIN PULS PER	
000	24 * DISEQC RATIO	
001	25 * DISEQC RATIO	
010	26 * DISEQC RATIO	
011	27 * DISEQC RATIO	
100	28 * DISEQC RATIO	
101	29 * DISEQC RATIO	
110	30 * DISEQC RATIO	(default)
111	31 * DISEQC RATIO	

B[4-2]: TONE EXT PER Tone Impulse Extended Period.

B1-0:	TONE EXT PER	
000	7 * DISEQC RATIO	
001	8 * DISEQC RATIO	
010	9 * DISEQC RATIO	
011	10 * DISEQC RATIO	
100	11 * DISEQC RATIO	

B1-0:	TONE EXT PER	
101	12 * DISEQC RATIO	(default)
110	13 * DISEQC RATIO	
111	14 * DISEQC RATIO	

B[1-0]: MAX TONE PER Maximum Tone Period.

B1-0:	MAX TONE PER	
00	6.0 * DISEQC RATIO	(default)
01	6.25 * DISEQC RATIO	
10	5.75 * DISEQC RATIO	
11	5.5 * DISEQC RATIO	

5.3 DiSEqC Control Read Registers

5.3.1 DiSEqC™M 2 Interrupt Indicators. Register 118 (R)

NAME	ADR	B7	B6	B5	B4	B3	B2	B1	B0		Def hex
DISEQC2 INT	118	DISEQC2 INT[7:0]								R	00

Note that the most significant four bits are not reset on read. The least significant four bits are interrupt bits which are reset when the register is read. Interrupts indicate events in history. The interrupts may be enabled to drive the $\overline{IRQ}$ pin 57 by setting required bit(s) in the DISEQC2 CTRL1 register 121, see 31.

B7-4: Bits B7-4 denote the following number of bytes received:

B7-4 = (Number of bytes received - Number of bytes read)

Hence this is the number of bytes that would be in the FIFO BUFFER if this buffer had unlimited capacity. Since the size of this buffer is only 8 bytes, if the above difference, given by bits B7-4, exceeds eight, that indicates buffer overflow.

B3: Silent period exceeds 176 ms interrupt (reset on read)

The host may enable interrupts B1 and B3. Then when an interrupt is received, the host may read the DISEQC2 INT register. Then if bit B3 is one and bit B1 is 0, this indicates there has been a continuous period 176ms of silence since the end of the transmission. If the host is expecting a reply, then this silence may be taken to signify a hardware fault in the system.

There is a 5-bit number in the DISEQC2 STATUS BYTE which indicates the length of a continuous period of silence up to the read time, in multiples of 16 ms.

B2: Receive error interrupt (reset on read).

Bit B2 indicates an error in the received message. This does not refer to a parity error. It indicates that a bit has been lost due to excessive noise or interference in the return channel. This is identified within MT312 by the occurrence of an excessively long tone or silence period within a byte.

B1: End of message interrupt (reset on read).

Bit B1 indicates a new message has been received. The end of a message is identified by a silent period of about 6 ms following a byte. The end-of-message interrupt bit makes it easier for the host processor to read DiSEqC™ data from MT312. Instead of reading a byte at a time, it can read the message as a whole.

It is important to note that MT312 does not stop accepting bytes after setting end-of-message interrupt. It will receive new messages, if any, whilst the current message is being read by the host. Since 2-wire bus read rate is higher than the byte receive rate, there is no reason for FIFO buffer overflow. After every received message there will be an interrupt.

B0: End of byte interrupt (reset on read).

Bit B0 is set when a new byte is received. The host may wish to ignore byte interrupts and opt to read received messages, as described below.

It is important to note that MT312 does not stop accepting bytes after setting end-of-message interrupt. It will receive new messages, if any, whilst the current message is being read by the host. Since 2-wire bus read rate is higher than the byte receive rate, there is no reason for FIFO buffer overflow.

After every received message there will be an interrupt.

5.3.2 DiSEqC™M 2 Status Indicators. Register 119 (R)

NAME	ADR	B7	B6	B5	B4	B3	B2	B1	B0		Def hex
DISEQC2 STAT	119	DISEQC2 STATUS[7:0]								R	00

B7-5: DISEQC2 Finite State Machine State. This is primarily for debugging the device.

B4-0: Silent period since last received bit, in multiples of 16 ms.

Bits B4-0 is reset to zero when a bit is received. When this 5-bit number reaches 176, the interrupt bit B3 of DISEQC2 INT register is set. This is saturated to 31. Hence if the total period exceeds 496 ms this counter will continue to indicate 31.

5.3.3 DiSEqC™ 2 FIFO. Register 120 (R)

Odd byte read of register 120:

NAME	ADR	B7	B6	B5	B4	B3	B2	B1	B0		Def hex
DISEQC2 FIFO	120	DISEQC2 FIFO[7:0]								R	00

Even byte read of register 120:

This FIFO contains data bytes and parity bits collected. This can hold a maximum of 8 data bytes, 8 parity bits and 8 parity error bits. The parity error bit is defined as the inverse of the exclusive-OR combination (or modulo-2 addition) of all 9 bits (8 data and 1 parity). This bit will be zero when there is no parity error.

NAME	ADR	B7	B6	B5	B4	B3	B2	B1	B0		Def hex
DISEQC2 FIFO	120	Reserved						Par error	Par bit	R	00

Refer to preceding section for buffer overflow.

The received bytes are read from this location with 2-wire bus auto-increment bit set to zero. The received bytes will be available in the order received, i.e. the buffer is a First In First Out (FIFO) memory.

Note that two read operations are needed for each byte. The first read operation will give the data byte and the second will provide the associated parity bit(B0) and the parity-error bit(B1), the other 6 bits will be zero. For example, if four bytes are received, then eight read operations (with auto-increment bit set to zero) are needed to get all data bytes as well as the parity bits.

The number of bytes received is given by bits B3-0 of DISEQC2 STATUS BYTES register 119.

6 QPSK demodulator

6.1 QPSK Demodulator Read/Write Registers

6.1.1 Symbol Rate. Registers 23 - 24 (R/W)

NAME	ADR	B7	B6	B5	B4	B3	B2	B1	B0		Def hex
SYM RATE H	23	SEARCH	Reserved	SYM RATE[13:8] in MBaud (high byte)						R/W	80
SYM RATE L	24	SYM RAT[7:0] in Mbaud (low byte)								R/W	80

B15: SEARCH

B14: Reserved. Must be set low
B14: S FMT Sweep MT312 Format.

If SYM RATE[15:14] = 0 this is the non-search mode, i.e. the known Symbol rate mode.

B13-0: Required Symbol rate in Mbaud x 256. Unsigned 14 bit number. e.g. for a symbol rate of 27.5 MBd

SYM RATE = 27.5 * 256 = 7040 = 1B80 (hex)

If any of the two DSS bits are set in the CONFIG register, then the SYM RATE register contents are ignored and the symbol rate is taken as 20 MBaud. Hence it is not necessary to program the SYM RATE register for DSS applications.

If SYM RATE[15:14] = 1x this is the Search Mode where x = don't care.

B11-0: Sub-ranges to be searched (scaled by clock rate).

The total symbol rate range is divided into 12 sub-ranges. A bit in the above register pair is assigned to each sub-range, as defined in the tables below. The symbol rate sub-range or sub-ranges to be searched are defined by setting the appropriate bits high. Small overlaps are automatically provided between successive sub-ranges. Note that the lowest sub-ranges have been provided for 90 MHz operation and the device has not been optimised for operation below 1 MBaud.

Bit	Symbol Rate Sub Range MBaud
11	SYS CLK /2 to SYS CLK/3
10	SYS CLK/3 to SYS CLK/4
9	SYS CLK/4 to SYS CLK/6
8	SYS CLK/6 to SYS CLK/8
7	SYS CLK/8 to SYS CLK/12
6	SYS CLK/12 to SYS CLK/16
5	SYS CLK/16 to SYS CLK/24
4	SYS CLK/24 to SYS CLK/32
3	SYS CLK /32 to SYS CLK/48
2	SYS CLK/48 to SYS CLK/64
1	SYS CLK /64 to SYS CLK/96
0	SYS CLK/96 to SYS CLK/128

Table 3 - Symbol sweep ranges for general case

Bit	Symbol Rate Sub Range MBaud
11	45 - 30
10	30 - 22.5
9	22.5 - 15
8	15 - 11.25
7	11.25 - 7.5
6	7.5 - 5.625
5	5.625 - 3.75
4	3.75 - 2.8125
3	2.81325 - 1.875
2	1.875 - 1.40625
1	1.40625 - 0.9375
0	0.9375 - 0.703125

Table 4 - Symbol sweep ranges for 90MHz system clock

6.1.2 Viterbi mode. Register 25 (R/W)

NAME	ADR	B7	B6	B5	B4	B3	B2	B1	B0		Def hex
VIT MODE	25	AUT IQ	V IQ SP	CR 7/8	CR 6/7	CR 5/6	CR 3/4	CR 2/3	CR 1/2	R/W	44

B7: AUT IQ Automatic IQ phaseHigh = Search for correct IQ phase.
Low = Use IQ phase setting in V IQ SP.

When this bit is set high, the Viterbi decoder will start with the IQ phase defined in V IQ SP and the code rate defined in VIT MODE[5:0], to establish the correct IQ phase of the incoming signal. When this is established, the V IQ SP bit will be set to that phase indication so that it can be read by software for subsequent re-tuning to the same channel.

B6: V IQ SP Swap I and Q inputs to the Viterbi decoder to overcome spectral inversion caused by the transmitter.
High = I-Q swap
Low = No I-Q swap

If the transmitted signal is known to be spectrally inverted then set this bit to 1. If the spectral inversion status of the transmitted signal is not known, then after QPSK CT lock, try to achieve FEC lock with this bit first at zero and then at one.

When AUT IQ is set high, this bit will indicate the IQ phase following successful channel acquisition. In manual mode, when AUT IQ is set low, software is required to determine the spectrum phase and control this bit externally.

B5: CR 7/8 High = Viterbi code rate 7/8.

B4: CR 6/7 High = Viterbi code rate 6/7.

B3: CR 5/6 High = Viterbi code rate 5/6.

B2: CR 3/4 High = Viterbi code rate 3/4.

B1: CR 2/3 High = Viterbi code rate 2/3.

B0: CR 1/2 High = Viterbi code rate 1/2.

The Viterbi decoder will search for a signal with the code rates selected by this register. If one code rate is selected, the MT312 will search for a signal with only that code rate. If the code rate is unknown then all B5:0 may be set, when the MT312 will search all code rates. It is possible to choose the starting point for the code rate search by setting a bit in VIT SETUP[B3:1] register (86). After searching for a signal with the initial code rate, if no signal is found the search proceeds to the next higher code rate, see 69.

In the DSS mode the code rate is not specified using VIT MODE register. If any of the two DSS bits of Configuration Register (127) is set, then the code rates selected by the VIT MODE register are ignored. The DSS code rate selection is carried out as described in section 1.1, see 10.

The result of the search is reported in the FEC STAT register (6), see 49.

6.1.3 QPSK Control. Register 26 (R/W)

NAME	ADR	B7	B6	B5	B4	B3	B2	B1	B0		Def hex
QPSK CTRL	26	Reserved	Q IQ SP	Reserved	Reserved	Reserved	AFC M	Reserved	ROLL 20	R/W	00

B7: Reserved — Must be set low.

B6: Q IQ SP — Swap I and Q inputs before QPSK demodulation to overcome spectral inversion caused by the receiver front-end, for example through the swapping I and Q wires on the board.

High = I-Q swap
Low = No I-Q swap

B5: Reserved — Must be set low.Q MANHigh = QPSK manual programming

B4: Reserved — Must be set low.OP CALHigh = Output calculation disable

B3: Reserved — Must be set low.FLD LKHigh = Use Frequency Lock Detector lock

B2: AFC M — High = Use AFC mode, for low Symbol rates only, < 10MSym/s.

B1: Reserved — Must be set low.

B0: ROLL 20 — High = Roll-off 0.20
Low = Roll-off 0.35

If any of the two DSS control bits of the Configuration Register (127) is active (see section 1.1 10), then bit B0 (ROLL 20) is ignored and the matched filter root-raised-cosine roll-off factor is taken as 0.20. Hence bit only allows the choice of roll-off in the DVB mode.

6.1.4 Go Command. Register 27 (R/W)

NAME	ADR	B7	B6	B5	B4	B3	B2	B1	B0		Def hex
GO	27	Reserved							GO	R/W	00

B7-1: Reserved - not used.

B0: GO High = release reset state to start signal capture, automatically reset to zero.
Low = no action.

If this register is read, it will return zero.

6.1.5 QPSK Interrupt Output Enable. Registers 28 - 30 (R/W)

When the bits of these three registers are set high, they enable an event to generate an interrupt on the $\overline{IRQ}$ pin 57. All interrupts may be enabled together. These registers do not affect the indication of events in the read registers 0 - 3.

NAME	ADR	B7	B6	B5	B4	B3	B2	B1	B0		Def hex
IE QPSK H	28	IE QPSK[23:16] Interrupt enable QPSK (high byte)								R/W	00

B7: High = Enable QPSK CT LOCK indication on interrupt pin.

B6: High = Enable QPSK CT UNLOCK indication on interrupt pin.

B5: High = Enable QPSK LOCK indication on interrupt pin.

B4: High = Enable QPSK UNLOCK indication on interrupt pin.

B3: High = Enable QPSK TS LOCK indication on interrupt pin.

B2: High = Enable QPSK TS UNLOCK indication on interrupt pin.

B1: High = Enable QPSK CS LOCK indication on interrupt pin

B0: High = Enable QPSK CS UNLOCK indication on interrupt pin.

NAME	ADR	B7	B6	B5	B4	B3	B2	B1	B0		Def hex
IE QPSK M	29	IE QPSK[15:8] Interrupt enable QPSK (middle byte)								R/W	00

B7: High = Enable QPSK FE AGC LOCK indication on interrupt pin.

B6: High = Enable QPSK TS AGC LOCK indication on interrupt pin.

B5: High = Enable QPSK TS AGC UNLOCK indication on interrupt pin.

B4: High = Enable QPSK FR LOCK indication on interrupt pin.

B3: High = Enable QPSK FR UNLOCK indication on interrupt pin.

B2: High = Enable QPSK calculation complete indication on interrupt pin.

B1: High = Enable QPSK TS MAX indication on interrupt pin.

B0: High = Enable QPSK CS MAX indication on interrupt pin.

NAME	ADR	B7	B6	B5	B4	B3	B2	B1	B0		Def hex
IE QPSK L	30	IE QPSK [7:0] Interrupt enable QPSK (low byte)								R/W	00

B7: High = Enable QPSK ST CHA indication on interrupt pin.

B6: High = Enable QPSK frequency end indication on interrupt pin.

B5: High = Enable QPSK BAUD end indication on interrupt pin.

B4: High = Enable QPSK AFC success indication on interrupt pin.

B3: High = Enable QPSK AFC fail indication on interrupt pin.

B2: High = Enable QPSK next FRS21 indication on interrupt pin.

B1: High = Enable QPSK same FRS21 indication on interrupt pin.

B0:High = Enable QPSK LTV limit indication on interrupt pin.

6.1.6 QPSK STATUS Output Enable. Register 32 (R/W)

If more than one bit is enabled then the logical-OR combination of the selected status signals will appear on the STATUS pin 52.

NAME	ADR	B7	B6	B5	B4	B3	B2	B1	B0		Def hex
QPSK STAT EN	32	QPSK STAT EN[7:0] Enable various QPSK outputs on STATUS pin								R/W	00

B7: High = QPSK TS sweep on

B6: High = QPSK CS sweep on

B5: High = QPSK FR LOCK

B4: High = QPSK TS AGC LOCK

B3: High = QPSK TS LOCK

B2: High = QPSK CS LOCK

B1: High = QPSK CT LOCK

B0: Reserved. Must be set low.

6.2 QPSK Demodulator Read Registers

6.2.1 QPSK Interrupt. Registers 0 - 2 (R)

The majority of these interrupts are for diagnostic purposes and generally not useful in normal operation, unless otherwise indicated.

NAME	ADR	B7	B6	B5	B4	B3	B2	B1	B0		Def hex
QPSK INT H	00	QPSK INT [23:16] Interrupt QPSK (high byte)								R	00

B7: High = QPSK Carrier and Timing LOCK important indicator.

B6: High = QPSK Carrier and Timing UNLOCK

B5: High = QPSK LOCKimportant indicator.

B4: High = QPSK UNLOCK

B3: High = QPSK Timing LOCK

B2: High = QPSK Timing UNLOCK

B1: High = QPSK Carrier LOCK

B0: High = QPSK Carrier UNLOCK

Reading an Interrupt register resets that register.

After the QPSK demodulator achieves Carrier and Timing Lock, from now on referred to as QPSK CT Lock, it waits some time for the FEC to confirm this lock. When the FEC locks, the QPSK enters QPSK Lock state. The time QPSK waits for the FEC to gain lock is programmable via register 81 (see section 10.2.31 FEC Lock Time. Register 81 (R/W)). If the FEC does not achieve lock during this period (very unlikely), then MT312 drops its QPSK CT Lock status and resumes search for another QPSK signal.

NAME	ADR	B7	B6	B5	B4	B3	B2	B1	B0		Def hex
QPSK INT M	01	QPSK INT [15:8] Interrupt QPSK (middle byte)								R	00

B7: High = QPSK FE AGC LOCK

B6: High = QPSK Digital Internal AGC LOCK

B5: High = QPSK Digital Internal AGC UNLOCK

B4: Reserved High = QPSK FR LOCK

B3: Reserved High = QPSK FR UNLOCK

B2: High = QPSK calculation complete

B1: High = QPSK TS MAX

B0: High = QPSK CS MAX

Reading an Interrupt register resets that register.

NAME	ADR	B7	B6	B5	B4	B3	B2	B1	B0		Def hex
QPSK INT L	02	QPSK INT [7:0] Interrupt QPSK (low byte)								R	00

The majority of these interrupts are for diagnostic purposes and generally not useful in normal operation, unless otherwise indicated.

B7: High = QPSK state change

B6: High = QPSK frequency end of search rangeimportant indicator.

B5: High = QPSK BAUD end of rangeimportant indicator.

B4: High = QPSK AFC success

B3: High = QPSK AFC fail

B2: High = QPSK next frequency search

B1: High = QPSK same frequency search

B0: High = QPSK LTV limit

Reading an Interrupt register resets that register.

Frequency and symbol rate search is carried out as follows. If the symbol rate is known then MT312 will search the specified frequency range for this symbol rate. Once the end of this range has been reached, "QPSK end of frequency range search" interrupt will be issued and MT312 will resume the search beginning from frequency zero. A "QPSK end of Symbol rate range(s) search" interrupt will not be issued.

If the symbol rate is not known, then MT312 can be made to search several sub-ranges of symbol rates, by setting 12 bits of the pair of SYM RATE registers, as described in section 4.4. For illustration purposes, assume that the symbol rate sub-ranges SYS CLK/2 to SYS CLK/3 and SYS CLK/4 to SYS CLK/6 are to be searched. Then MT312 will begin the search from the upper sub-range SYS CLK/2 to SYS CLK/3. MT312 will search for a channel with a symbol rate in this range over the specified frequency range, for example ± 10 MHz. If no channel is found then MT312 will issue a "QPSK end of frequency range search" interrupt and will go on to search the sub-range SYS CLK/4 to SYS CLK/6 over the specified frequency range. If no channel is found, then MT312 will issue a "QPSK end of frequency range search" interrupt as well as a "QPSK end of Symbol rate range(s) search" interrupt. Then MT312 will return to search the specified frequency range for a symbol rate in the range SYS CLK/2 to SYS CLK/3. This process continues indefinitely, unless it is interrupted by host processor software.

6.2.2 QPSK Status. Registers 4 - 5 (R)

NAME	ADR	B7	B6	B5	B4	B3	B2	B1	B0		Def hex
QPSK STAT H	04	QPSK STATUS[15:8] (high byte)								R	00

B7: High = QPSK SNR MSB

B6: High = QPSK SNR LSB

B5: High = QPSK FR LOCK

B4: High = QPSK Timing AGC LOCK

B3: High = QPSK Timing LOCK

B2: High = QPSK Carrier LOCK

B1: High = QPSK Carrier and Timing (CT) Lock

B0: High = QPSK LOCK

NAME	ADR	B7	B6	B5	B4	B3	B2	B1	B0		Def hex
QPSK STAT L	05	QPSK STATUS[7:0] (low byte)								R	00

B7: High = QPSK Timing sweep on

B6: High = QPSK Carrier sweep on

B5-0: Reserved

6.2.3 Symbol Rate Output. Registers 116 - 117 (R)

NAME	ADR	B7	B6	B5	B4	B3	B2	B1	B0		Def hex
SYM RAT OP H	116	SYM RAT OP[15:8] Symbol Rate Output (high byte)								R	00
SYM RAT OP L	117	SYM RAT OP[7:0] Symbol Rate Output (low byte)								R	00

SYM RAT OP[15:0] These two bytes contain a positive number that is inversely proportional to the Symbol rate. The decimation ratio index must also be read from the MONITOR register bits B[7:5] and divided by 32 to normalise the result.

$$Rs = \frac{PLL_CLK * 8192}{SYM_RAT_OP + 8192} * 2^{-DEC\ RATIO}$$

Where: Rs = Symbol rate in MBaud
PLL CLK = PLL clock frequency in MHz
SYM RAT OP = value of registers 116 and 117.
DEC RATIO = MONITOR H[7:5] when MON CTRL[2:0] = 5.

6.2.4 Monitor Registers. Registers 123 - 124 (R)

NAME	ADR	B7	B6	B5	B4	B3	B2	B1	B0		Def hex
MONITOR H	123	MONITOR[15:8] Monitor (high byte)								R	00
MONITOR L	124	MONITOR[7:0] Monitor (low byte)								R	00

For details, see MON CTRL register (103) on page 62.

MON CTRL[3:0] = 0: MONITOR H = CS SYM I and MONITOR L = CS SYM Q.

This is a snapshot of two I and Q samples (of the same symbol) after carrier synchroniser. This information could be used to produce a scatter diagram. Keep reading these continuously and mark these as points on a 2-D I-Q plane to get a scatter diagram.

MON CTRL[3:0] = 1: MONITOR H = DC OFFSET I and MONITOR L = DC OFFSET Q.

This will give the amount of DC offset in the I and Q inputs from the ADC compensated by the QPSK. Each of these is a two's complement number. If the 6-bit ADC range is taken to be in the scale -32 to 31, then it is necessary divide DC OFFSET I by 16, to bring it to the same scale as the ADC. For example, if we get the DC OFFSET I as "11111101", the corresponding two's complement number is -3. However, the actual offset with respect to the ADC scale of [-32, 31] is actually -3/16. The same applies to DC OFFSET Q.

MON CTRL[3:0] = 3: MONITOR H = MBAUD OP H and MONITOR L = MBAUD OP L.

When the QPSK demodulator is in lock following a symbol rate search, the locked symbol rate may be read from the MONITOR register. Then:

Symbol Rate = MONITOR[15:0]/ 1024.

The accuracy of this reading is within ±0.25% of the actual symbol rate. Note that the channel with this symbol rate can be subsequently re-acquired without a search by programming the 14 MSBs of the above read-out (discarding the two LSBs) as the 14 LSBs of the 16-bit SYM RATE register (23,24), see page 27.

MON CTRL[3:0] = 5:

Decimation ratio = MONITOR[15:13]/32.

MON CTRL[3:0] = 6: MONITOR H = M FLD[7:0] and MONITOR L = M FLD[7:0].

M FLD[7:0]: This byte contains a number calculated in the TS FLD Timing synchroniser frequency lock detector and is used for frequency lock detection in the manual programming mode.

MON CTRL[3:0] = 7: MONITOR H = M TLD H and MONITOR L = M TLD L.

M TLD[15:0]: Measurement of the Timing lock detector value. Reading the bytes does NOT reset the value.

MON CTRL[3:0] = 8: MONITOR H = M PLD H and MONITOR L = M PLD L.

M PLD[15:0]: Measurement of the Phase lock detector value. Reading the bytes does NOT reset the value.

The remaining settings of MON CTRL[3:0] are either reserved for diagnostic purposes or not used.

7 Forward Error Correction

7.1 Forward Error Correction Read/Write Registers

7.1.1 FEC Interrupt Enable. Register 31 (R/W)

When the bits of this register are set high, they enable an event to generate an interrupt on the pin 57. All interrupts may be enabled together.

NAME	ADR	B7	B6	B5	B4	B3	B2	B1	B0		Def hex
IE FEC	31	IE FEC[7:0] Interrupt enable FEC								R/W	00

B7: High = Enable DiSEqC™ indication on interrupt pin.

B6: High = Enable Byte Align lock lost indication on interrupt pin.

B5: High = Enable Byte Align lock indication on interrupt pin.

B4: High = Enable Viterbi lock lost indication on interrupt pin.

B3: High = Enable Viterbi lock indication on interrupt pin.

B2: High = Enable Viterbi BER monitor period reached indication on interrupt pin.

B1: High = Enable De-scrambler lock lost indication on interrupt pin.

B0:High = Enable De-scrambler lock indication on interrupt pin.

7.1.2 FEC STATUS Output Enable. Register 33 (R/W)

If more than one bit is enabled then the logical-OR combination of the selected status signals will appear on the STATUS pin 52.

NAME	ADR	B7	B6	B5	B4	B3	B2	B1	B0		Def hex
FEC STAT EN	33	MOCLK RATIO[3:0]				DS lock	BA lock	VIT lock	BER tog	R/W	14

B7-4: MOCLK RATIO[3:0] MPEG clock ratio - 6. I.e. range is from 6 to 21
see section 9.1.3 on 54.

B3: DS lock High = De-scrambler lock

B2: BA lock High = Byte Align lock

B1: VIT lock High = Viterbi lock. High = Viterbi lock

B0: BER tog High = BER toggle. This bit enables the audio signal output on the STATUS pin it indicates BER during dish alignment, see 12, section 1.4.1.2. The frequency of the signal is controlled by VIT MAXERR register (94), see 70.

7.1.3 FEC Set Up. Register 97 (R/W)

NAME	ADR	B7	B6	B5	B4	B3	B2	B1	B0		Def hex
FEC SETUP	97	DIS SR	ENCL KO	DIS DS	DIS RS	DIS VIT	EN PRS	DS LK[1:0]		R/W	03

B7: When MANUAL MOCLK (register 96 bit 7) is Low then:
DIS SR High = Disable use of Symbol Rate for MOCLK generation.
Low = Use Symbol Rate for MOCLK generation.

When MANUAL MOCLK (register 96 bit 7) is High then:
DIS SR High = Use external MICLK (pin 14) signal for MOCLK.
Low = Manually set MOCLK period from MOCLK RATIO (reg. 33).

B6: ENCLKO High = Enable clock out for test purposes.

B5: DIS DS High = Disable de-scrambler.

B4: DIS RS High = Disable Reed Solomon decoder.

B3: DIS VIT High = Disable Viterbi (Viterbi by pass mode)

B2: EN PRS High = Enable programmed synchronisation byte in register 98.

B1-0:DS LK[1:0] + 2 =Number of bytes for de-scrambler to lose lock. The default register value of 3 is equivalent to 5 bad sync words.

7.2 Forward Error Correction Read Registers

7.2.1 FEC Interrupt. Register 3 (R)

NAME	ADR	B7	B6	B5	B4	B3	B2	B1	B0		Def hex
FEC INT	03	FEC INT[7:0] Interrupt FEC								R	00

B7: High = DiSEqC™

B6: High = Byte Align lock lost

B5: High = Byte Align lockimportant indicator.

B4: High = Viterbi lock lost

B3: High = Viterbi lock

B2: High = Viterbi BER monitor period reached

B1: High = De-scrambler lock lost

B0: High = De-scrambler lock

Reading an Interrupt register resets that register.

7.2.2 FEC Status. Register 6 (R)

NAME	ADR	B7	B6	B5	B4	B3	B2	B1	B0		Def hex
FEC STATUS	06	FEC STATUS[7:0]								R	00

B7: Reserved

B6-4: Viterbi coding rate

B6-4	Code rate indication
0	1/2
1	2/3
2	3/4
3	5/6
4	6/7
5	7/8

Table 3 - Viterbi code rate indication

B3: High = De-scrambler lock

B2: High = Byte Align lock

B1: High = Viterbi lock

B0: Reserved

7.2.3 Measured Signal to Noise Ratio. Registers 9 - 10 (R)

NAME	ADR	B7	B6	B5	B4	B3	B2	B1	B0		Def hex
M SN R H	09	Reserved	M SNR[14:8] Measured SNR (high byte)							R	00
M SNR L	10	M SNR[7:0] Measured SNR (low byte)								R	00

B15: Reserved

M SNR[14:0]: These two registers provide a indication of the signal to noise ratio of the channel being received by the MT312. It should not be taken as the absolute value of the SNR.

$$Eb/N0 = \sim \frac{13312 - M\ SNR[14:0]}{683}\ dB.$$

The equation given only holds for Es/No values in the range 3 to 15 dB, i.e. Eb/No values in the range 0 to 12 dB.

7.2.4 Viterbi Error Count at Viterbi Input. Registers 11 - 13 (R)

NAME	ADR	B7	B6	B5	B4	B3	B2	B1	B0		Def hex
VIT ERRCNT H	11	VIT ERRCNT[23:16] - Viterbi error count (high byte)								R	00
VIT ERRCNT M	12	VIT ERRCNT[15:8] - Viterbi error count (middle byte)								R	00
VIT ERRCNT L	13	VIT ERRCNT[7:0] - Viterbi error count (low byte)								R	00

This is effectively the QPSK Bit Error Rate.

VIT ERRCNT[23:0]: This is the count of bits corrected by the Viterbi decoder. This value is updated when the Viterbi error timer (VIT_ERRPER) expires (indicated by B2 in register FEC_INT) and is NOT reset by reading.

$$QPSK\ BER = \frac{VIT_ERRCNT[23:0]}{VIT_ERRPER[23:0] * 4}$$

7.2.5 Reed Solomon Bit Errors Corrected. Registers 14 - 16 (R)

NAME	ADR	B7	B6	B5	B4	B3	B2	B1	B0		Def hex
RS BERCNT H	14	RS BERCNT[23:16] - Reed Solomon bit errors corrected (high byte)								R	00
RS BERCNT M	15	RS BERCNT[15:8] - Reed Solomon bit errors corrected (middle byte)								R	00
RS BERCNT L	16	RS BERCNT[7:0] - Reed Solomon bit errors corrected (low byte)								R	00

This is effectively the Viterbi Bit Error Rate.

RS BERCNT[23:0]: These three registers provide a measurement of the number of bit errors corrected by the Reed Solomon decoder. Reading the high byte stops the count incrementing. Reading the low byte resets all three bytes and restarts the count incrementing again.

$$Viterbi\ BER = \frac{RS_BERCNT[23:0]}{dt * Rs * 2 * CR}$$

Where: dt = delta time between two readings in sec (recommend 20s for 20 - 30 MBaud signals)
Rs = Symbol rate in Baud
CR = Viterbi code rate
In denominator: the factor 2 is for QPSK, change it to 1 for BPSK

e.g. for Rs = 27.5Mbaud, CR = 3/4 and dt = 20 sec

$$Viterbi\ BER = \frac{RS_BERCNT[23:0] * 4}{20 * 27.5E6 * 2 * 3}$$

$$\text{Viterbi BER} = \frac{\text{RS_BERCNT[23:0]}}{8.25E8}$$

7.2.6 Reed Solomon Uncorrected block Errors. Registers 17 - 18 (R)

NAME	ADR	B7	B6	B5	B4	B3	B2	B1	B0		Def hex
RS UBC H	17	RS UBC[15:8] - Reed Solomon uncorrected block errors (high byte)								R	00
RS UBC L	18	RS UBC[7:0] - Reed Solomon uncorrected block errors (low byte)								R	00

RS UBC[15:0]: These two registers provide a measurement of the Reed Solomon uncorrected block errors. Reading the high byte resets the byte and stops the count incrementing. Reading the low byte resets the byte and restarts the count incrementing again.

$$\text{Block Error Rate} = \frac{\text{RS_UBC[15:0]} * \text{Blk_size}}{dt * Rs * CR}$$

Where: dt = delta time between two readings in sec
Rs = Symbol rate in Baud
CR = Viterbi code rate
Blk size = 1632 bits for DVB and 1096 bits for DSS
In denominator: the factor 2 is for QPSK, change it to 1 for BPSK

8 Automatic Gain Control

8.1 Automatic Gain Control Read/Write Registers

8.1.1 AGC Control. Register 39 (R/W)

NAME	ADR	B7	B6	B5	B4	B3	B2	B1	B0		Def hex
AGC CTRL	39	Reserved	Reserved	AGC SD[1:0]		AGC BW[2:0]			AGC SL	R/W	26

B7: Reserved. Must be set low.

B6: Reserved. Must be set low.

B5-4: AGC SD[1:0] Sigma Delta clock decimation ratio related to system clock.

AGC SD[1:0]	Decimation
00	2
01	4
10	8
11	16

Table 4 - Sigma Delta clock decimation ratio programming

AGC control output is a pulse density modulated output created by a sigma-delta modulator. To reduce power consumption this is not clocked at the full system clock rate. The frequency at which this is clocked is the system clock divided by the decimation factor in Table 6.

B3-1: AGC BW[2:0] Front End AGC bandwidth (retain default value of 3).

B0: AGC SL Analogue AGC slope
High = positive slope i.e. RF gain proportional to AGC voltage.
Low = negative slope i.e. RF gain inversely proportional to AGC voltage (default).

8.1.2 AGC REF Reference Value. Register 41 (R/W)

NAME	ADR	B7	B6	B5	B4	B3	B2	B1	B0		Def hex
AGC REF	41	AGC REF[7:0] AGC reference level								R/W	67

AGC REF[7:0] Front End AGC reference value.

The AGC loop control in MT312 is designed to bring the mean square value of the I signal (or the Q signal) at the ADC output (prior to any digital filtering) to the value set by the AGC REF register.

8.2 Automatic Gain Control Read Registers

8.2.1 Measured Signal Level at MT312 Input. Register 19 (R)

NAME	ADR	B7	B6	B5	B4	B3	B2	B1	B0		Def hex
SIG LEVEL	19	SIG LEVEL[11:4] - Signal level at MT312 input								R	00

B7-0: SIG LEVEL[11:4]: This register provides a measurement of the MT312 input signal level. It contains the 8 MSBs. The remaining 4 LSBs are contained in SIG LEV L register 107 together with the front end AGC lock status flag. In almost all conditions, it should only be necessary to read the high byte to determine the incoming signal level. If further accuracy is required, then the remaining bits of the lower byte should be read and the 12 bits combined into one number.

When AGC is controlling the signal level, there is a direct relationship between SIG LEVEL and AGC REF:

SIG LEVEL * 8 = AGC REF

NOTE: the signal level is measured at the output of the ADC before any digital filtering takes place. Hence the reading includes all noise and other signal channels passed by the SAW or baseband filter.

8.2.2 Measured AGC Feed Back Value. Registers 108 - 110 (R)

NAME	ADR	B7	B6	B5	B4	B3	B2	B1	B0		Def hex
AGC H	108	AGC[13:6] - Front end AGC (high byte)								R	00
AGC M	109	AGC[5:0] - Front end AGC (low byte)						ERR DB[9:8]		R	00
AGC L	110	ERR DB[7:0] - Error difference (low byte)								R	00

AGC[13:0]: These two registers provide a measurement of the AGC error feed back value by the MT312 to the front end. Reading the bytes does NOT reset the value.This measurement can be used to provide an indication of the signal level at the input to the tuner.

To avoid having too large a number, the following formula extracts a number less than 10000:

Tuner input signal level = AGC[13-6] * 4 + AGC[5-4] / 64.

ERR DB[9:0]: The ERR DB is the difference between the expected signal level defined by AGC REF and received signal level. This is in a non-linear logarithmic scale (hence the notation DB).

The way H/M/L registers work within the QPSK block is as follows. When you read the H register the 24-bit value is dumped into a shadow register. You don't have to read M and L after this. However, what you must NOT do is to read M and L (or just L of a 24 or 16-bit register) without reading H. The safest solution is to read H/M/L in that order.

9 MPEG Packet Data Ouput

9.1 MPEG Clock Modes

There are four MOCLK modes of operation, controlled by register bits.

MANUAL MOCLK register 96 bit 7	DIS SR register 97 bit 7	MOCLK generation mode
0	0	Use Symbol Rate for MOCLK generation.
0	1	Disable use of Symbol Rate for MOCLK generation.
1	0	Manually set MOCLK period from MOCLK RATIO (reg. 33).
1	1	Use external MICLK (pin 14) signal for MOCLK.

Table 5 - MPEG clock modes

9.1.1 MANUAL MOCLK = 0 and DIS SR = 0.

In this mode MOCLK is generated from the symbol clock . MOCLK will be a continuously running clock once symbol lock has been achieved in the QPSK block.

9.1.2 MANUAL MOCLK = 0 and DIS SR = 1.

In this mode MOCLK is not generated from the symbol clock but instead uses the data in the QPSK decimation ratio. This mode is not normally used but is available for engineering test purposes.

9.1.3 MANUAL MOCLK = 1 and DIS SR = 0.

This is the Programmable Clock Division Ratio mode of operation. MOCLK is generated by dividing the PLL clock frequency by the MOCLK RATIO + 6 see register 33 on 47.

$$\text{MOCLK frequency} = \frac{\text{PLLfrequency}}{(\text{MCLK_RATIO} + 6)}$$

PLL frequency	MOCLK RATIO + 6	MOCLK frequency	comment
60MHz	6	10.0MHz	maximum
60MHz	9	6.667 MHz	minimum
90MHz	6	15MHz	maximum
90MHz	9	10.0MHz	minimum

Table 6 - MOCLK input minimum and maximum frequencies

The range of values of 6 to 9 for (MOCLK RATIO + 6) will guarantee operation for 2 - 45 MSym/s. However, for a restricted range of symbol rates, higher (MOCLK RATIO + 6) values may be used with a lower MOCLK frequency. The equation in section 9.4 on 58 must be evaluated to ensure successful operation and avoid buffer overflow in the MT312.

9.1.4 MANUAL MOCLK = 1 and DIS SR = 1.

This is the External MPEG Clock mode of operation. The external MOCLK is input on the MICLK pin 14. The clock supplied must be a continuous clock, otherwise the data buffers in the MT312 would overflow and data would be lost. The maximum permitted MICLK frequency is:

$$\text{MICLK frequency maximum} = \frac{\text{PLLfrequency}}{6.3}$$

Where PLL frequency is 60MHz the MICLK frequency maximum = 9.524MHz.
Where PLL frequency is 90MHz the MICLK frequency maximum = 14.286MHz.

As in the Programmable Clock Division Ratio mode, the minimum MICLK frequency must be high enough to clock the complete MPEG packet out before the next one arrives. For this reason, the minimum MICLK frequency recommended is 6.7MHz at 60MHz and 10MHz at 90MHz.

The MCLKINV control bit in the Output Data Control register (96) will change the phase of the MICLK used to clock the data out. With MCLKINV = 0, data is clocked out on the positive edge of MICLK. If MCLKINV = 1, data is clocked out on the negative edge of MICLK.

9.2 Data Output Header Format - DVB only

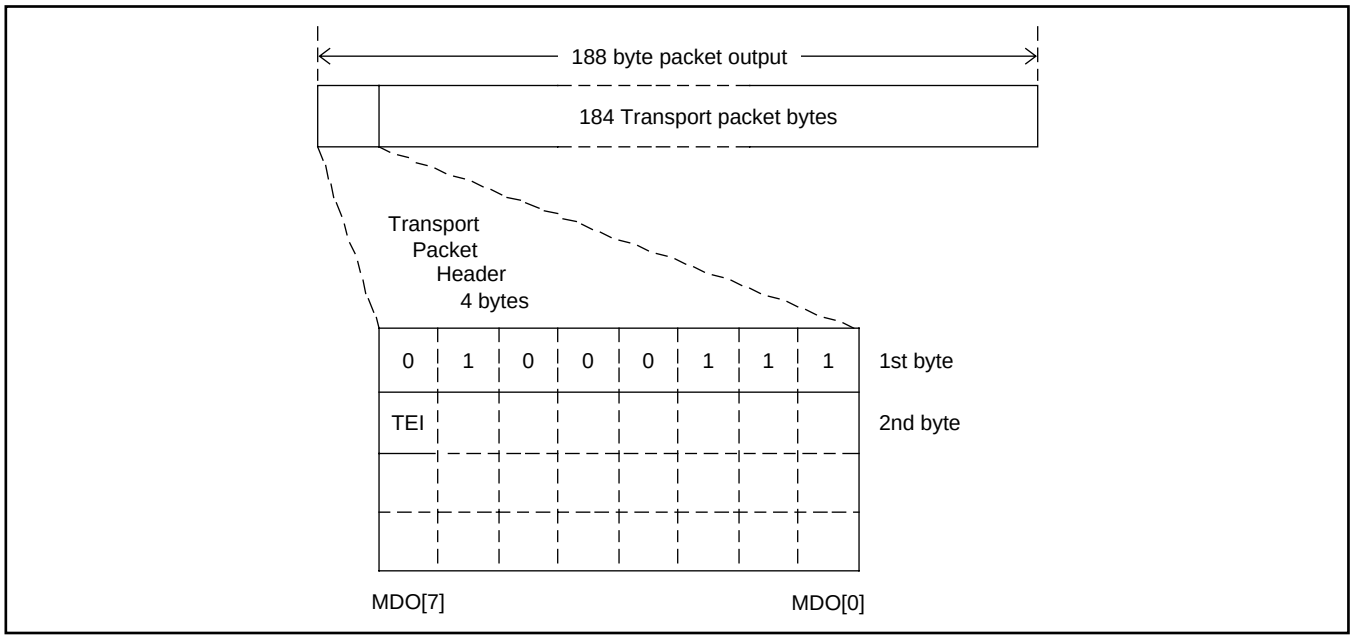


Figure 22 - DVB Transport Packet Header bytes

After decoding the 188 byte MPEG packet, it is output on the MDO pins in 188 consecutive clock cycles.

Additionally, in DVB mode, when the EN TEI bit in the OP CTRL register (96) is set high (default), the TEI bit of any uncorrectable packet will automatically be set to 1, see 52. If EN TEI bit is low then TEI bit will not be changed (but note that if this bit is already 1, for example, due to a channel error which has not been corrected, it will remain high at output).

9.3 MPEG/DSS Data Output Signals

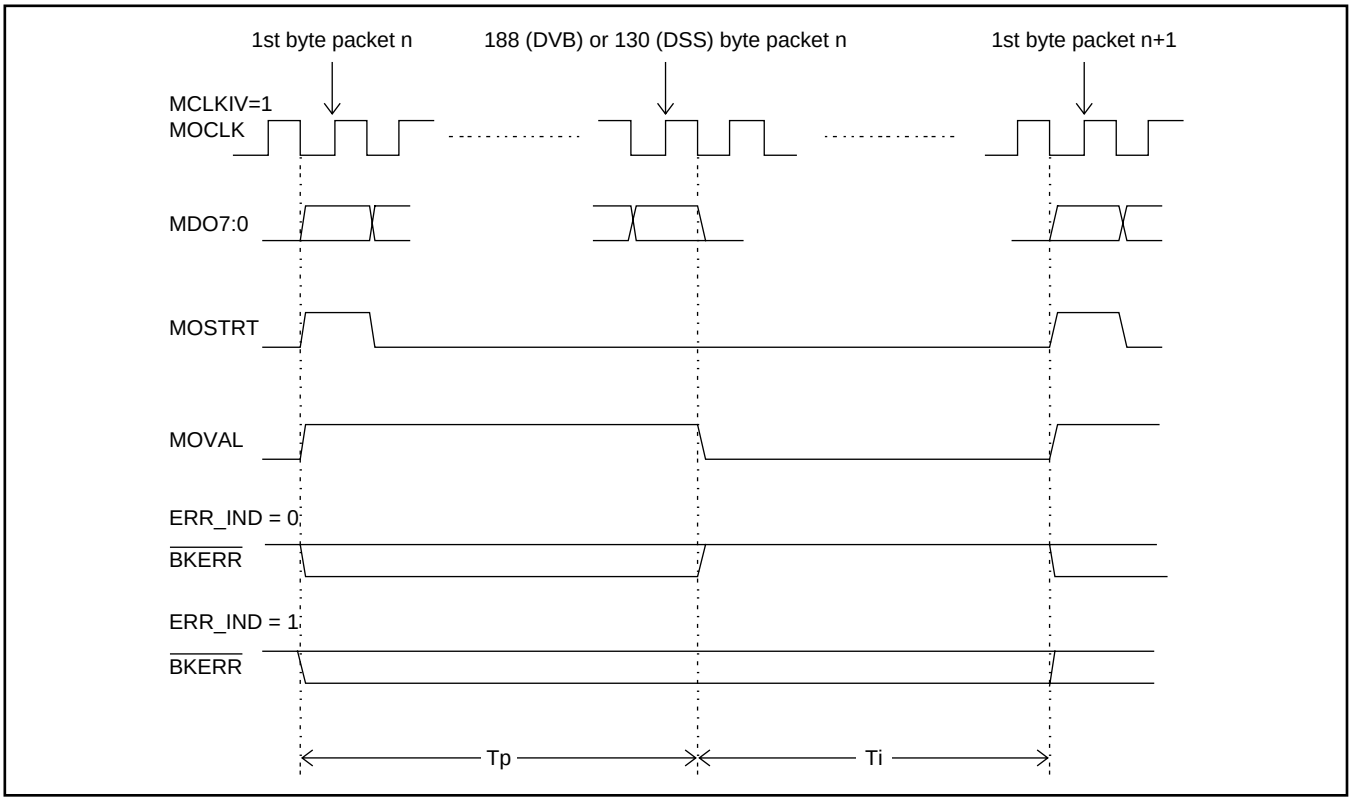


Figure 23 - MT312 output data wave form diagram

Figure 22 illustrates the case when ERR IND is set high and the De-scrambler lock remains high. If the first packet shown is good, $\overline{\text{BKERR}}$ would remain high at the first MOSTRT shown, going low at the second MOSTRT shown when that packet has uncorrected block errors. If the first packet shown is bad, $\overline{\text{BKERR}}$ will go low at the first MOSTRT shown and continue low until a good packed is received.

MOCLK will be a continuously running clock once symbol lock has been achieved in the QPSK block and is derived from either the system clock or MICLK if external clock is selected. MOCLK shown in Figure 24, Figure 25 and Figure 26 with MCLKINV = 1, the default state, see register 96 in 7.1.3 FEC Set Up. Register 97 (R/W) on page 51.

MOCLK is the MPEG data byte rate clock, the internal rate is calculated from the formulae in section 9.4. The maximum movement in the packet synchronisation byte position is limited to ± one output clock period.

All output data and signals (MDO[7:0], MOSTRT, MOVAL, $\overline{\text{BKERR}}$) change on the negative edge of MOCLK (MCLKINV = 1) to present stable data and signals on the positive edge of the clock.

A complete packet of data is output on MDO[7:0] on 188 (DVB) or 130 (DSS) consecutive clocks and the MDO[7:0] pins will remain low during the inter packet gaps.

MOSTRT goes high for the first byte clock of a packet.

MOVAL goes high on the first byte of a packet and remains high until the 188th byte (DVB) or 130th byte (DSS) has been clocked out.

$\overline{\text{BKERR}}$ has two modes of operation, selected by ERR IND bit 7 of MON CTRL register 103, see 59.

When ERR IND is High: $\overline{\text{BKERR}}$ remains high when error free MPEG packets are being output on the MDO[7:0] bus. $\overline{\text{BKERR}}$ goes low when there is no De-scrambler lock OR on the first byte of a packet where uncorrectable bytes are detected. $\overline{\text{BKERR}}$ remains low until error free MPEG packets are being output on the MDO[7:0] bus.

When ERR IND is Low: $\overline{\text{BKERR}}$ remains high when error free MPEG packets are being output on the MDO[7:0] bus. $\overline{\text{BKERR}}$ goes low on the first byte of a packet where uncorrectable bytes are detected and will remain low until the 188th byte (DVB) or 130th byte (DSS) has been clocked out.

Note: the signal on pin 75 can be inverted by setting the BKERIV bit 6 of OP CTRL register 96, see 48.

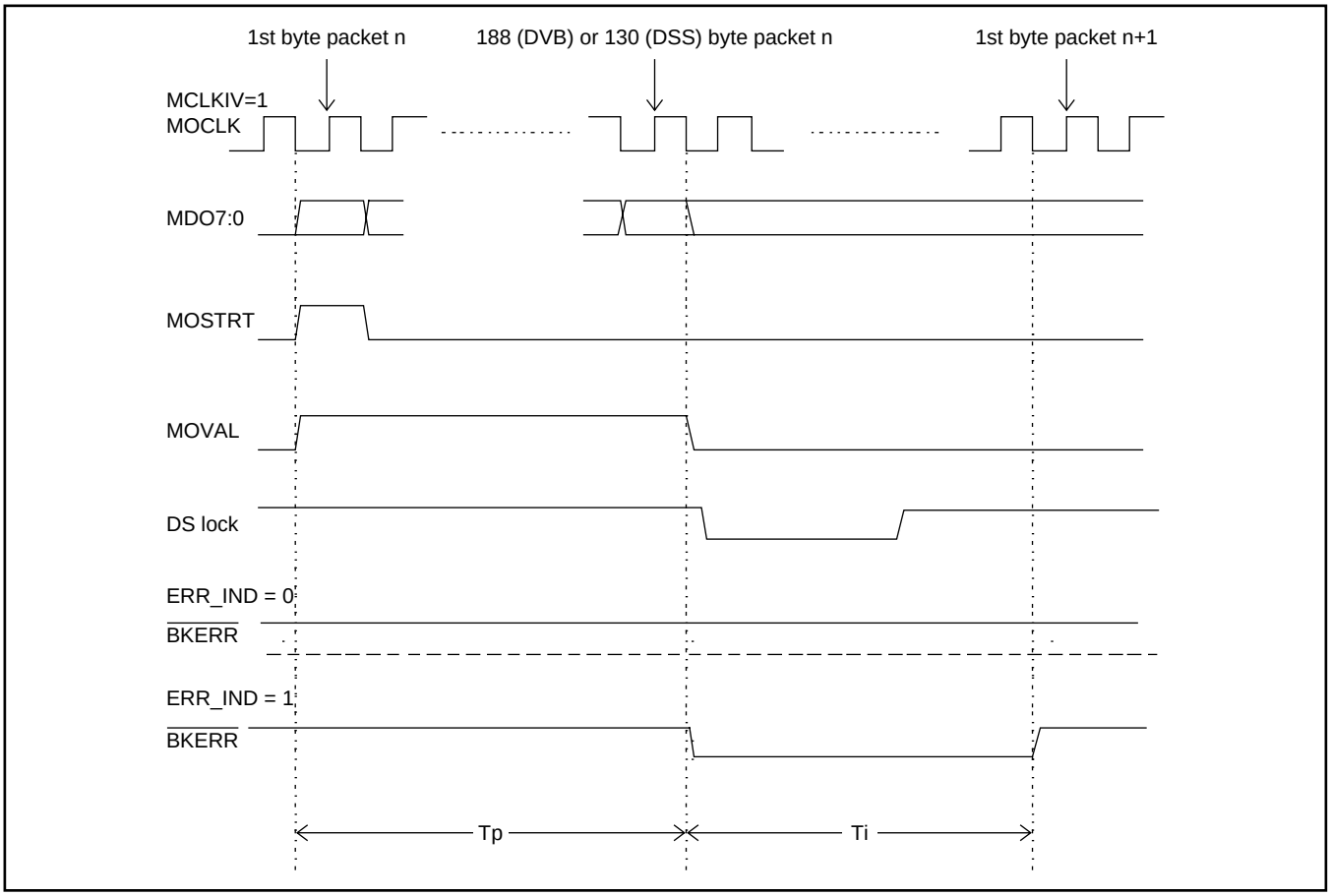


Figure 24 - MT312 output data wave form diagram 2

Figure 23 illustrates the case when ERR IND is set high and the De-scrambler lock is lost during output of the first packet. The first packet shown is good, in which case $\overline{\text{BKERR}}$ would remain high at the first MOSTRT shown, going low when De-scrambler lock goes low. Will go high at the next MOSTRT for a good packet.

9.4 Data output timing

The number of PLL clocks per Byte clock is: $N = \frac{Q*R*P}{2*V} * \frac{PLL}{RS}$ truncated to an integer

Where: Q = 1 for QPSK, 2 for BPSK
R = 204/193 for DVB, 147/135 for DSS
P = 8 for parallel byte output, 1 for serial byte output
V = Viterbi code rate, i.e. 3/4 for ASTRA
PLL = Sampling frequency MHz
RS = Symbol rate in MBaud, i.e. 27.5MBaud for ASTRA

e.g. For DVB ASTRA N = 1 * 204/193 * 8/2 * 4/3 *90E6/27.5E6
N = 18

The transport Stream clock rate = PLL / N
= 90E6 / 18
= 5E6Hz

The time to transmit a packet = 204 * 8/2 * 4/3 *1/RS
= 1088 / RS
= 3.9564E-5 sec

Time to output 188 bytes = 188/5E6
= 3.76E-5 sec

The gap between packets = 3.9564E-5 - 3.76E-5
= 1.936E-6 sec

The gap as number of byte clocks = 1.936E-6 * 5E6
= 9.82

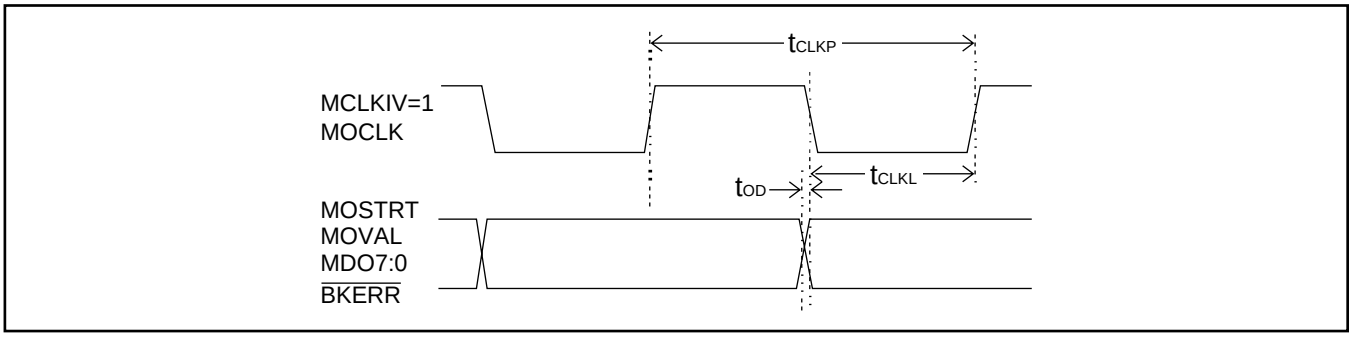


Figure 25 - MT312 output data wave form diagram 2

Parameter	Symbol	Min	Typ	Max	Units
Data output delay (when MCLKINV = 1)	tOD		±2	±4	ns

9.5 MPEG Packet Data Output Read/Write Registers

9.5.1 Output Data Control. Register 96 (R/W)

NAME	ADR	B7	B6	B5	B4	B3	B2	B1	B0		Def hex
OP CTRL	96	MANUAL MOCLK	BKE RIV	MCL KINV	EN TEI	BSO	BA LK[2:0]			R/W	33

B7: MANUAL MOCLK — Manual MOCLK mode selection, see register 97

B6: BKERIV — High = Inverted signal on $\overline{\text{BKERR}}$ output pin.
Low = Normal signal on $\overline{\text{BKERR}}$ output pin.

B5: MCLKINV — High = Normal signal on MOCLK output pin.
Low = Inverted signal on MOCLK output pin.

For a description of how to use these features, see section 9.1 MPEG Clock Modes on 55.

With MCLKINV = 0, data is clocked out on the positive edge of MOCLK. If MCLKINV = 1, data is clocked out on the negative edge of MOCLK.

B4: EN TEI — High = Enable automatic setting of transport error indicator (TEI) bit in MPEG packet header byte 2 when the block is flagged as uncorrectable by the Reed-Solomon decoder. See section 8.2 Data output header format - DVB only. (Not used in DSS).

B3: BSO — High = Bit serial output of the MPEG data on MDO0 pin.
Low = Parallel output of the MPEG data on MDO[7:0] pins.

B2 -0: BA LK[2:0] + 2 = Number of bytes for byte aligner to lock.
The default register value of 3 is equivalent to 5 good sync words.

9.5.2 Monitor Control. Register 103 (R/W)

NAME	ADR	B7	B6	B5	B4	B3	B2	B1	B0		Def hex
MON CTRL	103	ERR IND	Reserved			MON CTRL[3:0] Monitor control				R/W	00

B7: ERR IND — Error Indicator.

High — $\overline{\text{BKERR}}$ remains high when error free MPEG packets are being output on the MDO[7:0] bus. $\overline{\text{BKERR}}$ goes low when there is no De-scrambler lock OR on the first byte of a packet where uncorrectable bytes are detected. $\overline{\text{BKERR}}$ will remain low until error free MPEG packets are being output on the MDO[7:0] bus.

Low — $\overline{\text{BKERR}}$ remains high when error free MPEG packets are being output on the MDO[7:0] bus. $\overline{\text{BKERR}}$ goes low on the first byte of a packet where uncorrectable bytes are detected and will remain low until the 188th byte (DVB) or 130th byte (DSS) has been clocked out.

Note: the $\overline{\text{BKERR}}$ signal on pin 75 can be inverted by setting the BKERIV bit 6 of OP CTRL register 96, see page 37.

B6-4: Reserved, not used.

B3-0: MON CTRL[3:0] selects which pair of registers will be read from MONITOR H & L registers 123 and 124, (see section 6.10 on page 48).

MON CTRL[3:0]	MONITOR H (123)	MONITOR L (124)
0	CS SYM I	CS SYM Q
1	DC OFFSET I	DC OFFSET Q
2	Reserved	Reserved
3	MBAUD OP H	MBAUD OP L
4	Reserved	Reserved
5	DEC RATIO[15:13] and the rest reserved	Reserved
6	M FLD[7:0]	M FLD7:0]
7	M TLD H	M TLD L
8	M PLD H	M PLD L
15 - 9	Not used	Not used

I and Q input samples when MON CTRL[3:0] = 0.

DC offset in the I and Q inputs when MON CTRL[3:0] = 1.

Symbol Rate when MON CTRL[3:0] = 3, (see section 6.2.4 Monitor Registers. Registers 123 - 124 (R)).

Decimation ratio when MON CTRL[3:0] = 5, (see 6.2.4 Monitor Registers. Registers 123 - 124 (R)).

Timing synchroniser frequency lock detector value when MON CTRL[3:0] = 6, (see section 6.2.4 Monitor Registers. Registers 123 - 124 (R)).

Timing lock detector value when MON CTRL[3:0] = 7, (see section 6.2.4 Monitor Registers. Registers 123 - 124 (R)).

Phase lock detector value when MON CTRL[3:0] = 8, (see section 6.2.4 Monitor Registers. Registers 123 - 124 (R)).

The remaining settings of MON CTRL[3:0] are either reserved for diagnostic purposes or not used.

10 Secondary Registers for Test and De-Bugging

10.1 Read / Write Secondary Register Map

NAME	ADR	B7	B6	B5	B4	B3	B2	B1	B0		Def hex	Page
AGC INIT	40	AGC INIT[7:0] Front end AGC initial value								R/W	3B	63
AGC MAX	42	AGC MAX[7:0] Front end AGC maximum value								R/W	FF	63
AGC MIN	43	AGC MIN[7:0] Front end AGC minimum value								R/W	00	63
AGC LK TH	44	AGC LK TH[7:0] Front end AGC lock threshold value								R/W	0A	63
TS AGC LK TH	45	TS AGC LK TH[7:0] Fine AGC lock threshold value								R/W	1E	63
AGC PWR SET	46	AGC PWR SET[7:0] AGC power initial value								R/W	14	63
QPSK MISC	47	DAGC D	A OPEN	MIX D	CACC D	FOC D	TSLP D	CSLP D	ADC FM	R/W	00	63
SNR THS LOW	48	SNR THS LOW[7:0] SNR estimator low threshold								R/W	5A	63
SNR THS HIGH	49	SNR THS HIGH[7:0] SNR estimator high threshold								R/W	46	64
TS SW RATE	50	TS SW RATE[7:0] TS sweep rate								R/W	1E	64
TS SW LIM L	51	TS SW LIM L[7:0] TS sweep limit low								R/W	40	64
TS SW LIM H	52	TS SW LIM H[7:0] TS sweep limit high								R/W	84	64
CS SW RATE 1	53	CS SW RATE 1[7:0] CS sweep rate								R/W	20	64
CS SW RATE 2	54	CS-SW RATE 2[7:0] CS sweep rate								R/W	48	64
CS SW RATE 3	55	CS SW RATE 3[7:0] CS sweep rate								R/W	70	64
CS SW RATE 4	56	CS SW RATE 4[7:0] CS sweep rate								R/W	90	65
CS SW LIM	57	CS SW LIM[7:0] CS sweep limit								R/W	7C	65
TS LPK	58	TS KPROPE[11:4]								R/W	57	65
TS LPK M	59	TS KPROPE[3:0]				TS KINTE[11:8]				R/W	85	65
TS LPK L	60	TS KINTE[7:0]								R/W	9B	65
CS KPROP H	61	NONSNR	CS KP2[4:0]					CS KP1[4:3]		R/W	12	65
CS KPROP L	62	CS KP1[2:0]			CS KP0[4:0]					R/W	96	65
CS KINT H	63	Reserved	CS KI2[4:0]					CS KI1[4:3]		R/W	51	66
CS KINT L	64	CS KI1[2:0]			CS KI0[4:0]					R/W	3B	66
QPSK SCALE	65	QPSK SCALE[7:0] QPSK output scale factor for IOUT and QOUT outputs								R/W	27	66
TLD OUTLK TH	66	TLD OUTLK TH[7:0] TLD threshold when not in lock								R/W	82	66
TLD INLK TH	67	TLD INLK TH[7:0] TLD threshold when in lock								R/W	0A	66
FLD TH	68	FLD TH[7:0] Frequency lock threshold								R/W	20	66
PLD OUTLK3	69	SW R N MX[1:0]		PLD OUTLK3[9:4]						R/W	AE	66
PLD OUTLK2	70	PLD OUTLK3[3:0]				PLD OUTLK2[9:6]				R/W	E6	66
PLD OUTLK1	71	PLD OUTLK2[5:0]						PLD O LK1 [9:8]		R/W	40	66

Read/Write Secondary register map

NAME	ADR	B7	B6	B5	B4	B3	B2	B1	B0		Def hex	Page
PLD OUTLK0	72	PLD OUTLK1[7:0]								R/W	7E	66
PLD INLK3	73	Reserved		PLD INLK3[9:4]						R/W	01	67
PLD INLK2	74	PLD INLK3[3:0]				PLD INLK2[9:6]				R/W	A0	67
PLD INLK1	75	PLD INLK2[5:0]						PLD INLK1 [9:8]		R/W	68	67
PLD INLK0	76	PLD INLK1[7:0]								R/W	1A	67
PLD ACC TIME	77	CS PLD MPLEN[3:0]				LOSSLOCK INT SW[3:0]				R/W	48	67
SWEEP PAR	78	SW LIM SC[1:0]		TS NR SWEEP[2:0]			CS NR SWEEP[2:0]			R/W	49	68
STARTUP TIME	79	STARTUP INTERVAL[7:0]								R/W	30	68
LOSSLOCK TH	80	LOSSLOCK TH SPUR[3:0]				LOSSLOCK TH SW[3:0]				R/W	21	68
FEC LOCK TM	81	FEC LOCK TIME[7:0]								R/W	20	68
LOSSLOCK TM	82	LOSSLOCK TIME[7:0]								R/W	10	69
VIT ERRPER H	83	VIT ERRPER[23:16] Viterbi error period (high byte)								R/W	FF	69
VIT ERRPER M	84	VIT ERRPER[15:8] Viterbi error period (middle byte)								R/W	FF	69
VIT ERRPER L	85	VIT ERRPER[7:0] Viterbi error period (low byte)								R/W	FF	69
VIT SETUP	86	FR AL TM O[1:0]		SRCH CYC [1:0]		SEARCH START [2:0]			EX F LK	R/W	34	69
VIT REF0	87	VIT REF0[7:0] Viterbi reference byte 0								R/W	80	69
VIT REF1	88	VIT REF1[7:0] Viterbi reference byte 1								R/W	14	70
VIT REF2	89	VIT REF2[7:0] Viterbi reference byte 2								R/W	0A	70
VIT REF3	90	VIT REF3[7:0] Viterbi reference byte 3								R/W	06	70
VIT REF4	91	VIT REF4[7:0] Viterbi reference byte 4								R/W	04	70
VIT REF5	92	VIT REF5[7:0] Viterbi reference byte 5								R/W	02	70
VIT REF6	93	VIT REF6[7:0] Viterbi reference byte 6								R/W	01	70
VIT MAXERR	94	VIT MAXERR [7:0] Viterbi max. error bit count								R/W	FF	70
BA SETUPT	95	BA FSM[1:0]		BA MV [1:0]		BA UNLK[3:0]				R/W	D4	71
PROG SYNC	98	PROG SYNC BYTE[7:0] Enabled by FEC SETUP [2]								R/W	47	71
AFC SEAR TH	99	AFC SEAR TH[7:0]								R/W	23	71
CSACC DIF TH	100	ACC DIF TH[7:0]								R/W	20	71
QPSK LK CT	101	CS L LK	TS L LK	ACC CK	NUM PLD INT[4:0]					R/W	04	71
QPSK ST CT	102	HLD ST	AFC RS	M S RS	NXT FR	FCE ST	FORCED ST[2:0]			R/W	00	72
QPSK RESET	104	Reserved		REL QP	PR QP	PR CS	PR TS	PR FE	PR AGC	R/W	00	72
QPSK TST CT	105	QPSK TEST CTRL[7:0]								R/W	00	72
QPSK TST ST	106	QPSK TEST TS[7:0]								R/W	00	73
TEST MODE	125	Test mode								R/W	00	73

Read/Write Secondary register map (continued)

10.2 Secondary Registers for Test and De-Bugging Read/Write Registers

10.2.1 AGC Initial Value. Register 40 (R/W)

AGC INIT (40)	**Default value**	**59 dec.**	**3B hex.**

AGC INIT[7:0] Front End AGC initial value.

10.2.2 AGC Maximum Value. Register 42 (R/W)

AGC MAX (42)	**Default value**	**255 dec.**	**FF hex.**

AGC MAX[7:0] Front End AGC maximum value.

10.2.3 AGC Minimum Value. Register 43 (R/W)

AGC MIN (43)	**Default value**	**0 dec.**	**00 hex.**

AGC MIN[7:0] Front End AGC minimum value.

10.2.4 AGC Lock Threshold Value. Register 44 (R/W)

AGC LK TH (44)	**Default value**	**10 dec.**	**0A hex.**

AGC LK TH[7:0] Front End AGC lock threshold value.

10.2.5 AGC Lock Threshold Value. Register 45 (R/W)

TS AGC LK TH (45)	**Default value**	**30 dec.**	**1E hex.**

TS AGC LK TH[7:0] Timing synchroniser fine AGC lock threshold value.

10.2.6 AGC Power Setting Initial Value. Register 46 (R/W)

AGC PWR SET (46)	**Default value**	**20 dec.**	**14 hex.**

AGC PWR SET[7:0] AGC power setting initial value.

10.2.7 QPSK Miscellaneous. Register 47 (R/W)

QPSK MISC (47)	**Default value**	**0 dec.**	**00 hex.**

QPSK MISC[B7-0] Reserved, must be set low,

10.2.8 SNR Low Threshold Value. Register 48 (R/W)

SNR THS LOW (48)	**Default value**	**90 dec.**	**5A hex.**

SNR THS LOW[7:0]	SNR low threshold value.

10.2.9 SNR HIGH Threshold Value. Register 49 (R/W)

SNR THS HIGH (49)	**Default value**	**70 dec.**	**46 hex.**

SNR THS HIGH[7:0]	SNR high threshold value.	**Change to 50 dec. 32 hex. after a full reset.**

10.2.10 Timing Synchronisation Sweep Rate. Register 50 (R/W)

TS SW RATE (50)	**Default value**	**30 dec.**	**1E hex.**

TS SW RATE[7:0]	Timing Synchronisation sweep rate. For DSS set the value to 20 dec. 14 hex. after a full reset.

10.2.11 Timing Synchronisation Sweep Limit Low. Register 51 (R/W)

TS SW LIM L (51)	**Default value**	**64 dec.**	**40 hex.**

TS SW LIM L[7:0]	Timing Synchronisation sweep limit low.

10.2.12 Timing Synchronisation Sweep Limit High. Register 52 (R/W)

TS SW LIM H (52)	**Default value**	**132 dec.**	**84 hex.**

TS SW LIM H[7:0]	Timing Synchronisation sweep limit high.

10.2.13 Carrier Synchronisation Sweep Rate 1. Register 53 (R/W)

CS SW RATE 1 (53)	**Default value**	**32 dec.**	**20 hex.**

CS SW RATE 1[7:0]	Carrier Synchronisation sweep rate 1.

10.2.14 Carrier Synchronisation Sweep Rate 2. Register 54 (R/W)

CS SW RATE 2 (54)	**Default value**	**72 dec.**	**48 hex.**

CS SW RATE 2[7:0]	Carrier Synchronisation sweep rate 2.

10.2.15 Carrier Synchronisation Sweep Rate 3. Register 55 (R/W)

CS SW RATE 3 (55) **Default value** **112 dec.** **70 hex.**

CS SW RATE 3[7:0] Carrier Synchronisation sweep rate 3.

10.2.16 Carrier Synchronisation Sweep Rate 4. Register 56 (R/W)

CS SW RATE 4 (56) **Default value** **144 dec.** **90 hex.**

CS SW RATE 4[7:0] Carrier Synchronisation sweep rate 4.

10.2.17 Carrier Synchronisation Sweep Limit. Register 57 (R/W)

CS SW LIM (57) **Default value** **124 dec.** **7C hex.**

CS SW LIM[7:0] Carrier Synchronisation sweep limit.

10.2.18 Timing Synchronisation Coefficients. Registers 58 - 60 (R/W)

NAME	ADR	B7	B6	B5	B4	B3	B2	B1	B0		Def hex
TS LPK H	58	TS KPROPE[11:4]								R/W	57
TS LPK M	59	TS KPROPE93:0]				TS KINTE[11:8]				R/W	85
TS LPK L	60	TS KINTE[7:0]								R/W	9B

B23-12: TS KPROPE[11:0] Timing Synchronisation Proportional path coefficients.

B11-0: TS KINTE [11:0] Timing Synchronisation Integration path coefficients.

10.2.19 Carrier Synchronisation Proportional Part Coefficients. Registers 61 - 62 (R/W)

NAME	ADR	B7	B6	B5	B4	B3	B2	B1	B0		Def hex
CS KPROP H	61	NON SNR	CS KP2[4:0]					CS KP1[4:3]		R/W	12
CS KROP L	62	CS KP1 [2:-0]			CS KP0[p4:0]					R/W	3B

B15: NONSNR High = Non SNR sweep.

B14-10: CS KP2[4:0] Carrier proportional tracking coefficients.

B9-5: CS KP14:0] Carrier proportional transition coefficients.

B4-0: CS KP04:0] Carrier proportional acquire coefficients.

10.2.20 Carrier Synchronisation Integral Coefficients. Registers 63 - 64 (R/W)

NAME	ADR	B7	B6	B5	B4	B3	B2	B1	B0		Def hex
CS KINT H	63	Reserved	CS KI2[4:0]					CS KI1[4:3]		R/W	51
CS KINT L	64	CS KI1[2:0]			CS KI0[4:0]					R/W	3B

B15: Reserved

B14-10: CS KI2 [4:0] Carrier integer tracking coefficients.

B9-5: CS KI1 [4:0] Carrier integer transition coefficients.

B4-0: CS KI0[4:0] Carrier integer acquire coefficients.

10.2.21 QPSK Output Scale Factor. Register 65 (R/W)

QPSK SCALE (65) **Default value** **39 dec.** **27 hex.**

QPSK SCALE [7:0] QPSK output scale factor for IOUT and QOUT outputs.

10.2.22 Timing Lock Detect Threshold out of lock. Register 66 (R/W)

TLD OUTLK TH (66) **Default value** **130 dec.** **82 hex.**

TLD OUTLK TH [7:0] Timing Lock Detect threshold when not in lock.

10.2.23 Timing Lock Detect Threshold in lock. Register 67 (R/W)

TLD INLK TH (67) **Default value** **10 dec.** **0A hex.**

TLD INLK TH[7:0] Timing Lock Detect threshold when in lock.

10.2.24 Frequency Lock Detect Threshold. Register 68

FLD TH (68) **Default value** **32 dec.** **20 hex.**

FLD TH[7:0] Frequency lock detect threshold.

10.2.25 Phase Lock Detect Threshold out of lock. Registers 69 - 72 (R/W)

NAME	ADR	B7	B6	B5	B4	B3	B2	B1	B0		Def hex
PLD OUTLK3	69	SW R N MX[1:0]				PLD OUTLK3[9:4]				R/W	AE
PLD OUTLK2	70	PLD OUTLK3[3:0]				PLD OUTLK2[9:6]				R/W	E6
PLD OUTLK1	71	PLD OUTLK2[5:0]						PLD O LK1[9:8]		R/W	40
PLD OUTLK0	72	PLD OUTLK1[7:0]								R/W	7E

B31-30: SW R N MX[1:0] CS Sweep rate number max.

B29-20: PLD OUTLK TH3[9:0]

B19-10: PLD OUTLK TH2[9:0]

B9-0: PLD OUTLK TH1[9:0]

10.2.26 Phase Lock Detect Threshold in lock. Registers 73 - 76 (R/W)

NAME	ADR	B7	B6	B5	B4	B3	B2	B1	B0		Def hex
PLD INLK3	73	Reserved								R/W	01
PLD INLK2	74	PLD INLK3[3:0]				PLD INLK2[9:6]				R/W	A0
PLD INLK1	75	PLD INLK2[5:0]							PLD INLK1 [9:8]		68
PLD INLK0	76	PLD INLK1[7:0]								R/W	1A

B31-30: Reserved

B29-20: PLD INLK TH3[9:0]

B19-10: PLD INLK TH2[9:0]

B9-0: PLD INLK TH1[9:0]

10.2.27 Phase Lock Detect Accumulator Time. Register 77 (R/W)

NAME	ADR	B7	B6	B5	B4	B3	B2	B1	B0		Def hex
PLD ACC TIME	77	CS PLD MPLEN[3:0]				LOSSLOCK INT SW[3:0]				R/W	48

B7-4: CS PLDMPLEN[3:0] Maximum value allowed is 8.

B3-0: LOSSLOCK INT SW[3:0]

10.2.28 Sweep PAR. Register 78 (R/W)

NAME	ADR	B7	B6	B5	B4	B3	B2	B1	B0		Def hex
SWEEP PAR	78	SW LIM SC [1:0]		TS NR SWEEP[2:0]			CS NR SWEE{[2:0]			R/W	49

B7-6: SW LIM SC[1:0] Frequency sweep limit scale.

B5-3: TS NR SWEEP[2:0]

B2-0: CS NR SWEEP[2:0]

10.2.29 Start up Time. Register 79 (R/W)

NAME	ADR	B7	B6	B5	B4	B3	B2	B1	B0		Def hex
STARTUP TIME	79	STARTUP INTERVAL[7:0]								R/W	30

STARTUP INTERVAL[7:0]

10.2.30 Loss Lock Threshold. Register 80 (R/W)

NAME	ADR	B7	B6	B5	B4	B3	B2	B1	B0		Def hex
LOSSLOCK TH	80	LOSSLOCK TH SPUR[3:0]				LOSSLOCK TH SW[3:0]				R/W	21

B7-4: LOSSLOCK TH SPUR[3:0]

B3-0: LOSSLOCK TH SW[3:0]

10.2.31 FEC Lock Time. Register 81 (R/W)

FEC LOCK TM (81). **Default value** **32 dec.** **20 hex.**

FEC LOCK TM[7:0]

The number of symbol periods which the QPSK allows for the FEC to lock after achieving carrier and timing synchronisation is given by :

FEC LOCK TM * Search factor * 65536

The parameter Search Factor is 1 if there is no code rate search and is 8 if there is a code rate search, i.e. the QPSK allows more time for the FEC to lock in the presence of a code rate search.

If the FEC does not lock within the allotted number of symbol periods, then the QPSK resets the timing and carrier loops and resumes the search for a QPSK signal.

10.2.32 Loss Lock Time. Register 82 (R/W)

LOSSLOCK TM (82) **Default value** **16 dec.** **10 hex.**

LOSSLOCK TM[7:0]

After the FEC locks it can unlock due to a signal fade or a cycle slip. Then the QPSK allows the following number of symbol periods for the FEC to regain lock :

LOSSLOCK TM * 262144

If the FEC does not regain lock during this number of symbol periods, then QPSK will re-acquire lock.

10.2.33 Viterbi Error Period. Registers 83 - 85 (R/W)

VIT ERRPER (83, 84 & 85) Default value 16,777,215 dec.FF FF FF hex.

VIT ERRPER [23:0] Viterbi error period. This is the period over which the Viterbi error count is measured. See registers 11, 12 & 13 on page 53.

10.2.34 Viterbi Set up. Register 86 (R/W)

NAME	ADR	B7	B6	B5	B4	B3	B2	B1	B0		Def hex
VIT SETUP	86	FR AL TM O[1:0]		SRCH CYC [1:0]		SEARCH START [2:0]			EX F LK	R/W	34

B7-6: FR AL TM O [1:0] Frame (or byte) align time out.

B5-4: SRCH CYC[2:0] Viterbi BER based search cycles.

B3-1: SEARCH START[2:0] Code rate search start, only one code rate may be selected.

B6-4	Code rate search start at:
0	1/2
1	2/3
2	3/4
3	5/6
4	6/7
5	7/8

Table 7 - Viterbi code rate search start

B0: EX F LK Exit false lock.

10.2.35 Viterbi Reference Byte 0. Register 87 (R/W)

VIT REF0 (87)	Default value	128 dec.	80 hex.

VIT REF0[7:0] Viterbi reference byte 0.

10.2.36 Viterbi Reference Byte 1. Register 88 (R/W)

VIT REF1 (88)	Default value	20 dec.	14 hex.

VIT REF1[7:0] Viterbi reference byte 1.

10.2.37 Viterbi Reference Byte 2. Register 89 (R/W)

VIT REF2 (89)	Default value	10 dec.	0A hex.

VIT REF2[7:0] Viterbi reference byte 2.

10.2.38 Viterbi Reference Byte 3. Register 90 (R/W)

VIT REF3 (90)	Default value	6 dec.	06 hex.

VIT REF3[7:0] Viterbi reference byte 3.

10.2.39 Viterbi Reference Byte 4. Register 91 (R/W)

VIT REF4 (91)	Default value	4 dec.	04 hex.

VIT REF4[7:0] Viterbi reference byte 4.

10.2.40 Viterbi Reference Byte 5. Register 92 (R/W)

VIT REF5 (92)	Default value	2 dec.	02 hex.

VIT REF5[7:0] Viterbi reference byte 5.

10.2.41 Viterbi Reference Byte 6. Register 93 (R/W)

VIT REF6 (93)	Default value	1 dec.	01 hex.

VIT REF6[7:0] Viterbi reference byte 6.

10.2.42 Viterbi Maximum Error. Register 94 (R/W)

VIT MAXERR (94)	Default value	148 dec.	94 hex.

VIT MAXERR[7:0]Viterbi maximum error.

This register controls the frequency of the BER indication audio signal, output on the status pin when the FEC STAT EN register B0 is set high, see pages 11 and 50.

10.2.43 Byte Align Set up. Register 95 (R/W)

NAME	ADR	B7	B6	B5	B4	B3	B2	B1	B0		Def hex
BA SETUP	95	BA FSM[1:0]		BA MV[1:0]		BA UNLK[3:0]				R/W	D4

B7-6: BA FSM[1:0] Byte Align FSM mode.

B5-4: MA MV[2:0] + 5 = Byte Align majority voting.

B3-0: BA UNLK[3:0] +3 = Number of bad sync words to unlock the Byte Align. The default register value of 4 is equivalent to 7 bad sync words.

10.2.44 Program Synchronising Byte. Register 98 (R/W)

PROG SYNC (98) **Default value** **71 dec.** **47 hex.**

PROG SYNC[7:0] If FEC SETUP[2] is high, use the PROG SYNC value to synchronise MPEG data packets.

10.2.45 AFC Frequency Search Threshold. Register 99 (R/W)

AFC SEAR TH (99) **Default value** **35 dec.** **23 hex.**

AFC SEAR TH[7:0]

10.2.46 Accumulator Differential Threshold. Register 100 (R/W)

CSACC DIFF TH (100) **Default value** **32 dec.** **20 hex.**

CSACC DIFF TH[7:0]

10.2.47 QPSK Lock Control. Register 101 (R/W)

NAME	ADR	B7	B6	B5	B4	B3	B2	B1	B0		Def hex
QPSK LK CT	101	CS L LK	TS L LK	ACC CK	NUM PLD INT[4:0]					R/W	04

B7: CS L LK High = Use CS long lock.

B6: TS L LK High = Use TS long lock.

B5: ACC CK High = Disable Accumulator check option.

B4-0: NUM PLD INT[4:0] Maximum value allowed is 29.

10.2.48 QPSK State Control. Register 102 (R/W)

NAME	ADR	B7	B6	B5	B4	B3	B2	B1	B0		Def hex
QPSK ST CT	102	HLD ST	AFC RS	M S RS	NXT FR	FCE ST	FORCED ST[2:0]			R/W	00

B7: HLD ST — High = Hold state.

B6: AFC RS — High = AFC reset.

B5: M S RS — High = Mixer scan reset.

B4: NXT FR — High = Get next frequency.

B3: FCE ST — High = Force state.

B2-0: FORCED ST[2:0] — Forced state.

10.2.49 QPSK Reset. Register 104 (R/W)

NAME	ADR	B7	B6	B5	B4	B3	B2	B1	B0		Def hex
QPSK RESET	104	Reserved		REL QP	PR QP	PR CS	PR TS	PR FE	PR AGC	R/W	00

B7-6: Reserved Must be set low.

B5: REL QP — High = Release QPSK FSM.

B4: PR QP — High = Partial reset FSM (applies to QPSK control).

B3: PR CS — High = Partial reset carrier synchroniser

B2: PR TS — High = Partial reset timing synchroniser (includes fine AGC).

B1: PR FE — High = Partial reset front-end logic.

B0: PR AGC — High = Partial reset analogue AGC.

10.2.50 QPSK Test Control. Register 105 (R/W)

QPSK TST CT (105) **Default value** **0 dec.** **00 hex.**

QPSK TEST CTRL[7:0] — For factory test purposes only.

10.2.51 QPSK Test State. Register 106 (R/W)

QPSK TEST ST (106) **Default value** **0 dec.** **00 hex.**

QPSK TEST ST[7:0] For factory test purposes only.

10.2.52 Test Mode. Register 125 (R/W)

TEST MODE (125) **Default value** **0 dec.** **00 hex.**

TEST MODE[7:0]: This register is for testing purposes only.

10.3 Read only Secondary Register Map

Writing to these registers will have no effect.

NAME	ADR	B7	B6	B5	B4	B3	B2	B1	B0		Def hex
TEST R	107	TEST R[7:0] Test Read, for test purposes only.								R	00

10.4 Secondary Registers for Test and De-Bugging Read Register

10.4.1 Test Read. Register 107 (R)

TEST R (107) Default value0 dec.00 hex.

TEST R[7:0]For test purposes only.

11 Microprocessor Control

11.1 Primary 2-Wire Bus Address

The 2-wire bus Address is determined by applying VDD or VSS to the ADDR[7:1] pins. See 11.3 Primary 2-Wire Bus Interface.

11.2 RADD: 2-Wire Register Address (W)

RADD is the 2-wire register address. It is the first byte written after the MT312 2-wire chip address when in write mode.

To write to the chip, the microprocessor should send a START condition and the chip address with the write bit set, followed by the register address where subsequent data bytes are to be written. Finally, when the 'message' has been sent, a STOP condition is sent to free the bus.

To read from the chip from register address zero, the microprocessor should send a START condition and the chip address with the read bit set, followed by the requisite number of CLK1 clocks to read the bytes out. Finally a STOP condition is sent to free the bus. RADD is not sent in this case.

To read from the chip from an address other than zero, the microprocessor should send the chip address with the write bit set, followed by the register address where subsequent data bytes are to be read. Then the microprocessor should send a START condition and the chip address with the read bit set, followed by the requisite number of CLK1 clocks to read the bytes out. Finally a STOP condition is sent to free the bus

A STOP condition shall reset the RADD value to 00. For examples of use, see 74.

RADD (virtual register, address none)

NAME	ADR	B7	B6	B5	B4	B3	B2	B1	B0		Def hex
RADD	N/A	IAI	AD6	AD5	AD4	AD3	AD2	AD1	AD0	W	-

B7: IAI High = Inhibit auto increment.
Low = Increment addresses.

B6-0: AD[6:0] 2-wire register address, numbers in the range 0 to 127 are allowed.

When the register address is incremented to 127 it stops and the bus will continue to write to or read from register 127 until a STOP condition is sent.

11.3 Primary 2-Wire Bus Interface

The primary 2-wire bus serial interface uses pins:

DATA1 (pin 54) Serial data, the most significant bit is sent first.
CLK1 (pin 53) Serial clock.

The 2-wire bus Address is determined by applying VDD or VSS to the ADDR[7:1] pins.

For compatibility with VP310, the 2-wire bus Address should be 0001 110 R/ and the pins connected as follows:

ADDR[7]	ADDR[6]	ADDR[5]	ADDR[4]	ADDR[3]	ADDR[2]	ADDR[1]
VSS	VSS	VSS	VDD	VDD	VDD	VSS

When the MT312 is powered up, the $\overline{\text{RESET}}$ pin 49 should be maintained low for typically 250ms (minimum 100ms) after VDD has reached normal operation levels. This is to ensure that the crystal oscillator and internal PLL have become fully established and that the internal reset signal is fully clocked into all parts of the circuit. As the reset pin is pulled high, the logic levels on ADDR[7:1] are latched to become the 2-wire bus address ADDR[7:1]. ADDR[0] is the R/W bit.

IIN[5:1] are only used for test purposes and should be wired to VSS.

The circuit works as a slave transmitter with the eighth bit set high or as a slave receiver with the eighth bit set low. In receive mode, the first data byte is written to the RADD virtual register, which forms the register sub-address.

Bit 7 of the RADD register, IAI is an Inhibit Auto Increment function. When the IAI bit is set high, the automatic incrementing of register addresses is inhibited. IAI set low is the normal situation so that data bytes sent on the 2-wire bus after the RADD register data are loaded into successive registers. This automatic incrementing feature avoids the need to individually address each register.

Following a valid chip address, the 2-wire bus STOP command resets the RADD register to 00. If the chip address is not recognised, the MT312 will ignore all activity until a valid chip address is received. The 2-wire bus START command does NOT reset the RADD register to 00. This allows a combined 2-wire bus message, to point to a particular read register with a write command, followed immediately with a read data command. If required, this could next be followed with a write command to continue from the latest address. RADD would not be sent in this case. Finally a STOP command should be sent to free the bus.

When the 2-wire bus is addressed (after a recognised STOP command) with the read bit set, the first byte read out shall be the content of register 00.

11.4 Secondary 2-Wire Bus for Tuner Control

The MT312 has a General Purpose Port that can be configured to provide a secondary 2-wire bus with full bi-directional operation. When pass-through is enabled, a transparent connection is made to the tuner. This innovative design simplifies the software required to program the tuner to only five data bytes.

Pass-through mode is selected by setting register (20) GPP CTRL[B6] = 1.

The allocation of the pins is: GPP[0] pin 44 = CLK2, GPP[1] pin 45 = DATA2.

11.5 Examples of 2-Wire Bus Messages

KEY:	S	Start condition	W	Write (= 0)
	P	Stop condition	R	Read (= 1)
	A	Acknowledge	NA	NOT Acknowledge
ITALICS		MT312 output	RADD	Register Address

Write operation - as a slave receiver:

S	DEVICE ADDRESS	W	A	RADD (n)	A	DATA (reg n)	A	DATA (reg n+1)	A	P

Read operation - MT312 as a slave transmitter:

S	DEVICE ADDRESS	R	A	DATA (reg 0)	A	DATA (reg 1)	A	DATA (reg 2)	NA	P

Write/read operation with repeated start - MT312 as a slave transmitter:

S	DEVICE ADDRESS	W	A	RADD (n)	A	S	DEVICE ADDRESS	R	A	DATA (reg n)	A	DATA (reg n+1)	NA	P

Write / read / write operation with repeated start and auto increment off with IAI set high - MT312 as a slave transmitter. This example uses the GPP CTRL register where the register address is 20 + 128 (IAI). Data is first read from the GPP CTRL register, then following a restart, data is written to the GPP CTRL register.

S	DEVICE ADDRESS	W	A	RADD (148)	A	S	DEVICE ADDRESS	R	A	DATA (reg 20)	NA	S	DEVICE ADDRESS	W	A	DATA (reg 20)	A	P

To program the Tuner, use the following sequence of three messages:

Open secondary 2-wire port:

S	MT312 ADDRESS	W	A	GPP CTRL (20)	A	DATA (64)	A	P

Program Tuner:

S	TUNER ADDRESS	W	A	DATA (BYTE 2)	A	DATA (BYTE 3)	A	DATA (BYTE 4)	A	DATA (BYTE 5)	A	P

Close secondary 2-wire port:

S	MT312 ADDRESS	W	A	GPP CTRL (20)	A	DATA (0)	A	P

Always close the secondary 2-wire port after programming the Tuner, to avoid 2-wire bus clock interference in the Tuner.

11.6 Primary 2-Wire Bus Timing

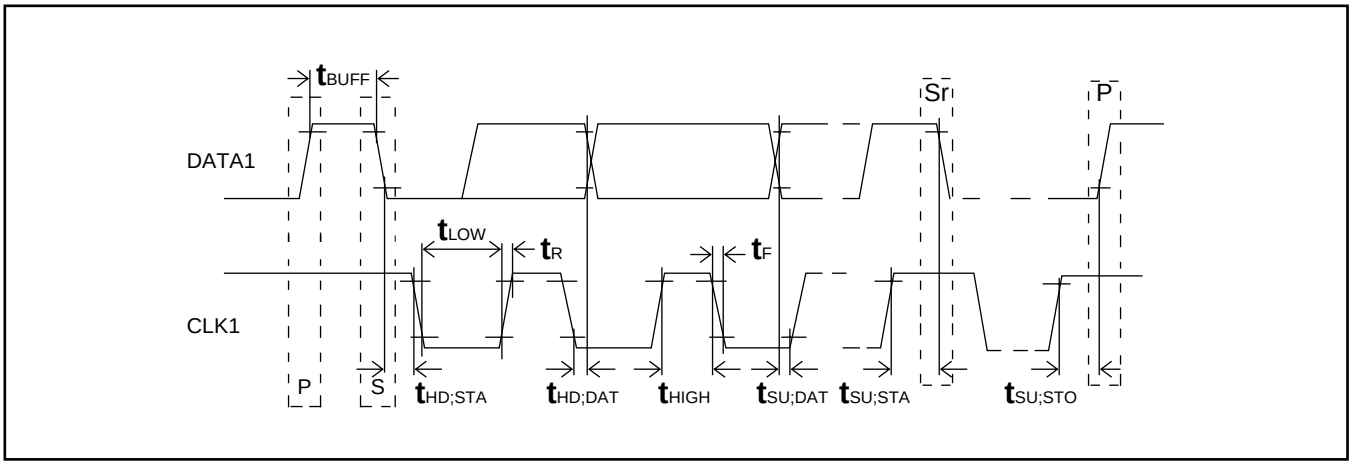


Figure 26 - One DiSEqC™ data byte - 0x11 (hex) plus parity bit

Where: S = Start
Sr = Restart, i.e. Start without stopping first.
P = Stop.

Parameter: Primary 2-wire bus only	Symbol	Value		Unit
		Min	Max	
CLK1 clock frequency	f_{CLK}	0	450	kHz
Bus free time between a STOP and START condition.	t_{BUFF}	200		ns
Hold time (repeated) START condition.	$t_{HD;STA}$	200		ns
LOW period of CLK1 clock.	t_{LOW}	450		ns
HIGH period of CLK1 clock.	t_{HIGH}	600		ns
Set-up time for a repeated START condition.	$t_{SU;STA}$	200		ns
Data hold time (when input).	$t_{HD;DAT}$	100		ns
Data set-up time	$t_{SU;DAT}$	100		ns
Rise time of both CLK1 and DATA1 signals.	t_R		note 1	ns
Rise time of both CLK1 and DATA1 signals, (100pF to ground)	t_F	20		ns
Set-up time for a STOP condition.	$t_{SU;STO}$	200		ns

Table 8 - Primary 2-wire bus timing

Note 1.The rise time depends on the external bus pull up resistor.

12 Electrical Characteristics

12.1 Recommended Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Units
Core power supply voltage	CVDD	1.62	1.8	1.98	V
Core power supply current	CIDD		130	150	mA
Power supply voltage	VDD	3.0	3.3	3.6	V
Power supply current	IDD		170	180	mA
Input clock frequency 1	$\overline{XTI}$	9.99		16.00	MHz
CLK1 clock frequency	FCLK1			450	kHz
Ambient operating temperature		0		70	°C

Table 9 - Recommended operating conditions

Note 1. When not using a crystal, $\overline{XTI}$ may be driven from an external source over the frequency range shown.

12.2 Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Unit
Power supply	VDD	-0.3	+3.6	V
Voltage on input pins (5 v rated)	VI	-0.3	5.5	V
Voltage on input pins (3.3v rated)	VI	-0.3	VDD + 0.3	V
Voltage on input pins (1.8v rated)	VI	-0.3	CVDD + 0.3	V
Voltage on output pins (5v rated)	VO	-0.3	5.5	V
Voltage on output pins (3.3v rated)	VO	-0.3	VDD + 0.3	V
Voltage on output pins (1.8v rated)	VO	-0.3	CVDD + 0.3	V
Storage temperature	TSTG	-55	150	°C
Operating ambient temperature	TOP	0	70	°C
Junction temperature	TJ		125	°C

Table 10 - Maximum operating conditions

Note: Stresses exceeding these listed under 'Absolute Ratings' may induce failure. Exposure to absolute maximum ratings for extended periods may reduce reliabilty. Functionality at or above these conditions is not implied.

12.3 Crystal Specification

Parallel resonant fundamental frequency (preferred)	9.99 to 16.00MHz.
Tolerance over operating temperature range	±25ppm.
Tolerance overall	±50ppm.
Nominal load capacitance	30pF.
Equivalent series resistance	<35Ω

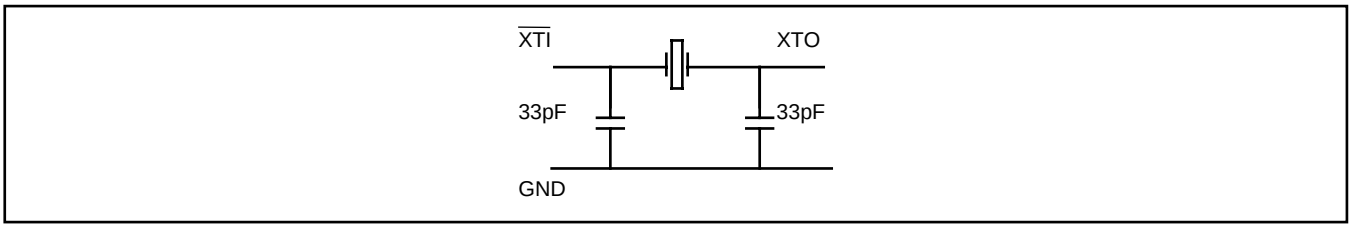


Figure 27 - Crystal oscillator circuit

NOTE: The crystal frequency should be chosen to ensure that the system clock would marginally exceed the maximum symbol rate required. See 59.

12.4 DC Electrical Characteristics

Parameter	Conditions / Pin	Symbol	Min.	Typ.	Max.	Unit
Core operating voltage		CVDD	1.62	1.8	1.98	V
Peripheral operating voltage		VDD	3.0	3.3	3.6	V
Average core power supply current		CIDD		130	150	mA
Average peripheral power supply current		IDD		170	180	mA
Average supply current Stand-by Mode				1	2	mA
Output levels VOH Tri-state push pull	1 mA drive current. IIN, QIN, TESTCLK, MDO, MOVAL, MOSTRT, MOCLK, $\overline{\text{BKERR}}$, DISECQ, STATUS	VOH	0.80 VDD	0.92 VDD		V
Output levels VOL Tri-state push pull	1 mA drive current, Pins as VOH.			0.2	0.4	V
Output level open drain	4 mA drive current. 6 mA drive current. AGC, DATA1, $\overline{\text{IRQ}}$, GPP<2:0>				0.4 0.6	V V
Input levels VIH CMOS	3.3V input	VIH	0.7VDD			V
Input levels VIH CMOS	5.0V input	VIH	0.7VDD			V
Input levels VIL CMOS		VIL			0.3VDD	V
Input leakage Current	VIN = 0 and VDD				10	µA

Table 11 - DC electrical characteristics

12.5 MT312 Pinout Description

Pin	Name	Description	I/O	Note	V	mA
4,5,6,7,8,11,12	ADDR[7:1]	Primary 2-wire bus address defining pins	I/O	CMOS	3.3	1
14	MICLK	MPEG clock input used to generate MOCLK. Enabled when both register 96 bit 7 and register 97 bit 7 are set high. In this mode, MICLK must be continuous.	I	CMOS	5 [1]	
16	TESTCLK	External ADC mode clock.	O	PECL	Tri-state	3.3
18	$\overline{\text{XTI}}$	Crystal clock input or external reference clock input.	I	CMOS	3.3	
19	XTO	Crystal output. An internal feedback resistor to $\overline{\text{XTI}}$ is included	O	CMOS	3.3	
23	PLL1	Phase Locked Loop test output	23			
26	VRT	ADC Voltage top reference level	26			
27	IREF	I channel de-coupling input	I			
28	ISINGP	I channel input	I			
29	NC	No connection	I			
32	VRM	ADC Voltage middle reference level				
33	QSINGP	Q channel input	I			
34	QREF	Q channel de-coupling input	I			
35	VRB	ADC Voltage bottom reference level				
38	RREF	Bias level				
39	TEST1	For factory test only. This pin must be connected to VSS in normal operation	I	CMOS	3.3	
40	TEST2	For factory test only. This pin must be connected to VSS in normal operation	I	CMOS	3.3	
43	AGC	AGC sigma-delta output	O	Open drain	5 [1]	6
46,45,44	GPP[2:0] (DISEQC2)	General Purpose Port for tuner control, register defined. GPP0 = secondary CLK2, GPP1 = secondary DATA2, GPP2 = DiSEqC™ v2.2 input signal.	I/O	Open drain	5 [1]	6
47	DISEQC1	DiSEqC™ Horizontal/Vertical control	O	CMOS	3.3	1
48	DISEQC0	DiSEqCTM 22kHz output	O	CMOS	3.3	1
49	$\overline{\text{RESET}}$	Active low reset input	I	CMOS	5 [1]	
52	STATUS	Audio BER or Status output, register defined	O	CMOS	3.3	1

Note 1.8V tolerant pins with thresholds related to 3.3V.

Pin	Name	Description	I/O	Note	V	mA
53	CLK1	2-wire serial bus clock	I	CMOS	5 [1]	
54	DATA1	2-wire serial bus data	I/O	Open drain	5 [1]	6
57	$\overline{IRQ}$	Active low interrupt output. A low output on this pin indicates an event has occurred and the microprocessor should read the interrupt registers. Reading all interrupt registers resets this pin.	O	Open drain	5 [1]	6
58	MOCLK	MPEG clock output at the data byte rate.	O	CMOS Tri-state	3.3	1
69,68,66,65, 64,63,61,59	MDO[7:0]	MPEG transport packet data output bus.	O	CMOS Tri-state	3.3	1
71	$\overline{MDOEN}$	Logic 1 = MPEG data and clock outputs disable - Tri-state. Logic 0 = MPEG data and clock outputs enable	I	CMOS	5 [1]	
72	MOVAL	MPEG data output valid. This pin is high during the MOCLK clock cycles when valid data bytes are being output.	O	CMOS Tri-state	3.3	1
75	$\overline{BKERR}$	Active low uncorrectable block indicator OR no signal indicator selected by ERR IND bit 7 of MON CTRL register.	O	CMOS Tri-state	3.3	1
76	MOSTRT	MPEG output start signal, high on the first byte of a packet.	O	CMOS Tri-state	3.3	1
2,9,17,42,50, 55,62,67	CVDD	Core Digital CVDD. All pins must be connected.			1.8	
13,73	VDD	Peripheral VDD. All pins must be connected.			3.3	
37	ADCAVDD	ADC core analogue VDD. All pins must be connected.			1.8	
30	ADCDVDD	ADC core digital VDD. All pins must be connected.			3.3	
25	ADCFVDD	ADC core front end VDD. All pins must be connected.			3.3	
21	PLLVDD	PLL VDD. All pins must be connected.			1.8	
1,10,20,41,51, 60,70	CVSS	Digital VSS. All pins must be connected.			0	
15,56,74	VSS	Peripheral VSS. All pins must be connected.			0	
36	ADCAGND	ADC core analogue VSS. Must be connected to analogue GND.			0	
31	ADCDGND	ADC core digital VSS. Must be connected to analogue GND.			0	

Pin	Name	Description	I/O	Note	V	mA
53	CLK1	2-wire serial bus clock	I	CMOS	5 [1]	
24	ADCFGND	ADC core front end VSS. Must be connected to analogue GND.			0	
22	PLLGND	PLL VSS. Must be connected to analogue GND.			0	
77,78,79,80,3	IIN[5:1]	Test bus, all inputs must be connected to VSS.	I/O	CMOS	3.3	1

Note 1. 8V tolerant pins with thresholds related to 3.3V.

12.6 Alphabetical Listing of Pin-Out

FUNCTION	PIN	FUNCTION	PIN	FUNCTION	PIN	FUNCTION	PIN
ADCAGND	36	CVDD	17	IIN[4]	78	PLLVDD	21
ADCAVDD	37	CVDD	42	IIN[5]	77	QREF	34
ADCDVDD	30	CVDD	50	IREF	27	QSINGP	33
ADCDGND	31	CVDD	62	$\overline{\text{IRQ}}$	57	$\overline{\text{RESET}}$	49
ADCFGND	24	CVDD	67	ISINGP	28	RREF	38
ADCFVDD	25	CVSS	1	MDO[0]	59	STATUS	52
ADDR[1]	12	CVSS	10	MDO[1]	61	TEST1	39
ADDR[2]	11	CVSS	20	MDO[2]	63	TEST2	40
ADDR[3]	8	CVSS	41	MDO[3]	64	TESTCLK	16
ADDR[4]	7	CVSS	51	MDO[4]	65	VRB	35
ADDR[5]	6	CVSS	60	MDO[5]	66	VRM	32
ADDR[6]	5	CVSS	70	MDO[6]	68	VRT	26
ADDR[7]	4	DATA1	54	MDO[7]	69	VDD	13
AGC	43	DATA2/GPP1	45	$\overline{\text{MDOEN}}$	71	CVDD	55
$\overline{\text{BKERR}}$	75	DISEQC0 22kHz	48	MICLK	14	VDD	73
CLK1	53	DISEQC1 HV	47	MOCLK	58	VSS	15
CLK2/GPP0	44	DISEQC2/ GPP2	46	MOSTRT	76	VSS	56
NC	29	IIN[1]	3	MOVAL	72	VSS	74
CVDD	2	IIN[2]	80	PLL1	23	XTI	18
CVDD	9	IIN[3]	79	PLLGND	22	XTO	19

Table 12 - Alphabetical listing of pin-out

13 Application Diagram

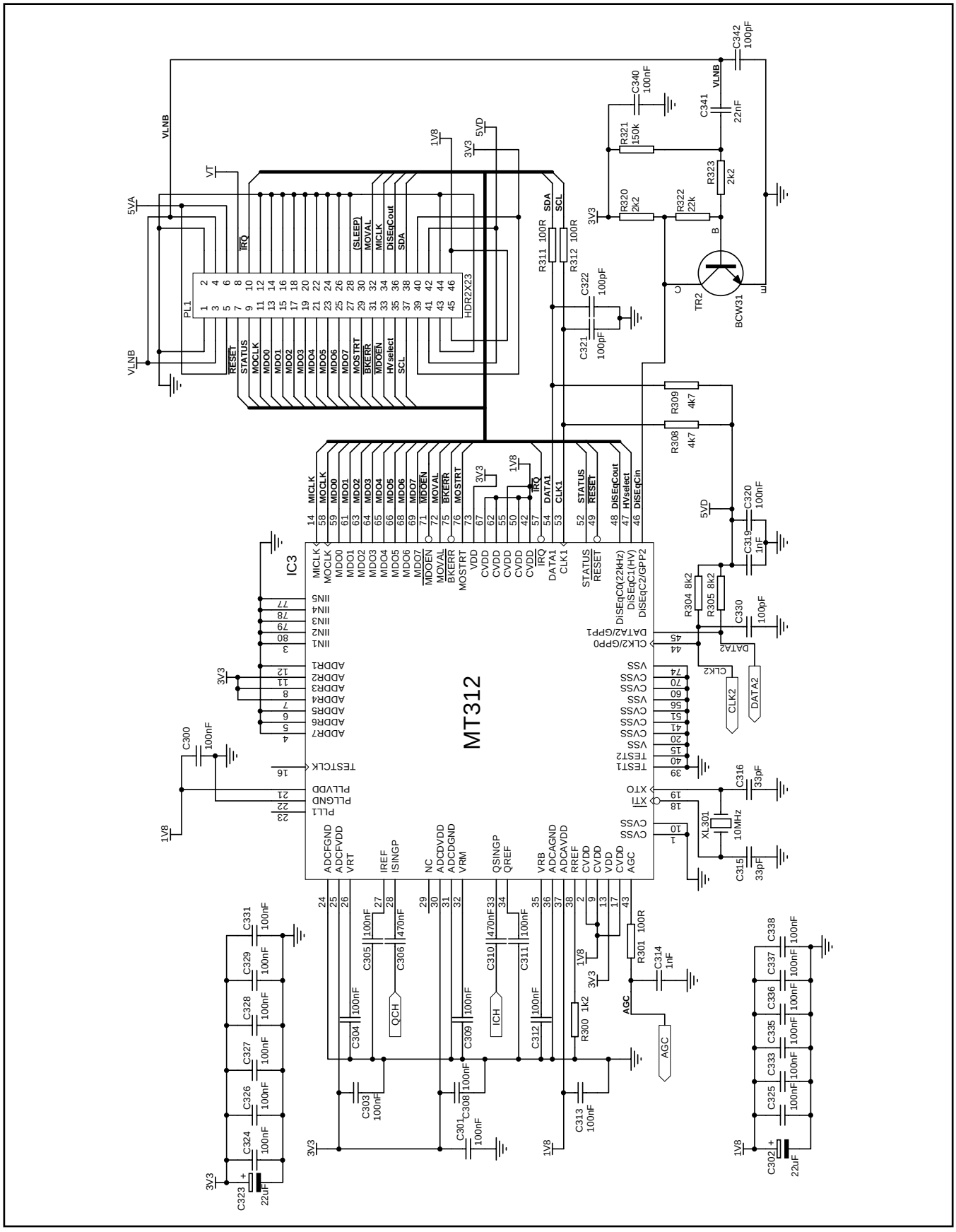


Figure 28 - Application Schematic

14 MT312 Register Map

RADD is a virtual register with no address containing the address of the register to be accessed. It is written immediately after the 2-wire write address.

NAME	ADR	B7	B6	B5	B4	B3	B2	B1	B0		Def hex
RADD	N/A	IAI	AD6	AD5	AD4	AD3	AD2	AD1	AD0	W	-

14.1 Read / Write Register Map

NAME	ADR	B7	B6	B5	B4	B3	B2	B1	B0		Def hex	Page
GPP CTRL	20	Reserved	2W PAS	GPP DIR[2:0]			GPP PIN[2:0]			R/W	20	25
RESET	21	FR 312	PR 312	FR QP	PR QP	FR VIT	PR VIT	PR BA	PR DS	R/W	00	21
DISEQC MODE	22	Reserved	HV	DISEQC instruction length			22kHz mode			R/W	00	30
SYM RATE H	23	SEARCH	Reserved	SYM RATE[13:8] in MBaud)high byte)						R/W	1B	36
SYM RATE L	24	SYM RATE[7:0] in MBaud (low byte)								R/W	80	36
VIT MODE	25	AUT IQ	V IQ SP	CR 7/8	CR 6/7	CR 5/6	CR 3/4	CR 2/3	CR 1/2	R/W	44	38
QPSK CTRL	26	Reserved	Q IQ SP	Reserved	Reserved	Reserved	AFC M	Reserved	ROLL 20	R/W	00	39
GO	27	Reserved							GO	R/W	00	40
IE QPSK H	28	IE QPSK[23:16] Interrupt enable QPSK (high byte)								R/W	00	40
IE QPSK M	29	IE QPSK[15:8] Interrupt enable QPSK (middle byte)								R/W	00	40
IE QPSK L	30	IE QPSK[7:0] Interrupt enable QPSK (low byte)								R/W	00	40
IE FEC	31	IE FEC[7:0] Interrupt enable FEC								R/W	00	47
QPSK STAT EN	32	QPSK STAT EN[7:0] Enable various QPSK outputs on STATUS pin								R/W	00	41
FEC STAT EN	33	MOCLK RATIO[3:0]				DS Lock	BA lock	VIT lock	BER tog	R/W	14	47
SYS CLK	34	SYS CLK[7:0] - System clock frequency x2 in MHz								R/W	00	23
DISEQC RATIO	35	DISEQC RATIO[7:0]								R/W	00	30
DISEQC INSTR	36	DISEQC Instruction[7:0]								R/W	00	31
FR LIM	37	Reserved	FR LIM[6:0] - Freq. Limit in MHz							R/W	00	26
FR OFF	38	FR OFF[7:0] - Freq. Offset in MHz								R/W	00	27
AGC CTRL	39	Reserved	Reserved	AGC SD[1:0]		AGC BW[2:0]			AGC SL	R/W	26	52
AGC REF	41	AGC REF[7:0] AGC reference level								R/W	67	52
OP CTRL	96	MANUAL MOCLK	BKERIV	MCLKINV	EN TEI	BSO	BA LK[2:0]			R/W	03	59
FEC SETUP	97	DIS SR	ENCLKO	DIS DS	DIS RS	DIS VIT	EN PRS	DS LK[1:0]		R/W	00	48
MON CTRL	103	ERR IND	Reserved			MON CTRL[3:0] Monitor control				R/W	00	59
DISEQC2 CTRL1	121	DISEQC2 CTRL1[7:8]								R/W	00	31

NAME	ADR	B7	B6	B5	B4	B3	B2	B1	B0		Def hex	Page
DISEQC2 CTRL2	122	MIN PULS PER			TONE EXT PER			MAX TONE PER		R/W	D4	32
CONFIG	127	312 EN	DSS B	DSS A	BPSK	PLL FACTOR[1:0]		CRYS15	ADC EXT	R/W	08	22

14.2 Read Only Register Map

Writing to these registers will have no effect

NAME	ADR	B7	B6	B5	B4	B3	B2	B1	B0		Def hex	Page
QPSK INT H	00	QPSK INT[23:16] Interrupt QPSK (high byte)								R	00	42
QPSK INT M	01	QPSK INT [15:8] Interrupt QPSK (middle byte)								R	00	42
QPSK INT L	02	QPSK INT [7:0] Interrupt QPSK (low byte)								R	00	42
FEC INT	03	FEC INT[7:0] Interrupt FEC								R	00	48
QPSK STAT H	04	QPSK STATUS[15:8] (high byte)								R	00	44
QPSK STAT L	05	QPSK STATUS[7:0] (low byte)								R	00	44
FEC STATUS	06	FEC STATUS[7:0]								R	00	49
LNB FREQ H	07	LNB FREQ[15:8] Measured LNB frequency error (high byte)								R	00	27
LNB FREQ L	08	Reserved	LNB FREQ [7:0] Measured LNB frequency error (low byte)							R	00	27
M SNR H	09	M SNR[14:8] Measured SNR (high byte)								R	00	49
M SNR L	10	M SNR [7:0] Measured SNR (low byte)								R	00	49
VIT ERRCNT H	11	VIT ERRCNT[23:16] - Viterbi error count (high byte)								R	00	50
VIT ERRCNT M	12	VIT ERRCNT[15:8] - Viterbi error count (middle byte)								R	00	50
VIT ERRCNT L	13	VIT ERRCNT[7:0] - Viterbi error count (low byte)								R	00	50
RS BERCNT H	14	RS BERCNT[23:16] - Reed Solomon bit errors corrected (high byte)								R	00	50
RS BERCNT M	15	RS BERCNT[15:8] - Reed Solomon bit errors corrected (middle byte)								R	00	50
RS BERCNT L	16	RS BERCNT[7:0] - Reed Solomon bit errors corrected (low byte)								R	00	50
RS UBC H	17	RS UBC[15:8] - Reed Solomon uncorrected block errors (high byte)								R	00	51
RS UBC L	18	RS UBC[7:0] - Reed Solomon uncorrected block errors (low byte)								R	00	51
SIG LEVEL	19	SIG LEVEL[11:4] - Signal level at MT312 input								R	00	53
AGC H	108	AGC (23:16] - Front end AGC (high byte)								R	00	85
AGC M	109	AGC[15:8] - Front end AGC (middle byte)								R	00	85
AGC L	110	AGC[7:0] - Front end AGC (low byte)								R	00	85
FREQ ERR1 H	111	FREQ ERR1[23:16] Input frequency error course (high byte)								R	00	28
FREQ ERR1 M	112	FREQ ERR1[15:8] Input frequency error course (middle byte)								R	00	28
FREQ ERR1 L	113	FREQ ERR1[7:0] Input frequency error course (low byte)								R	00	28
FREQ ERR2 H	114	FREQ ERR2[15:8] Input frequency error fine (high byte)								R	00	28
FREQ ERR2 L	115	FREQ ERR2[7:0] Input frequency error fine (low byte)								R	00	28
SYM RAT OP H	116	SYM RAT OP[15:8] Symbol Rate Output (high byte)								R	00	44
SYM RAT OP L	117	SYM RAT OP[7:0] Symbol Rate Output (low byte)								R	00	44
DISEQC2 INT	118	DISEQC2 INT[7:0]								R	00	33

NAME	ADR	B7	B6	B5	B4	B3	B2	B1	B0		Def hex	Page
DISEQC2 STAT	119	DISEQC2 STATUS[7:0]								R	00	34
DISEQC2 FIFO	120	DISEQC2 FIFO[7:0]								R	00	34
MONITOR H	123	MONITOR[15:8] Monitor (high byte)								R	00	45
MONITOR L	124	MONITOR[7:0] Monitor (low byte)								R	00	45
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15 INDEX

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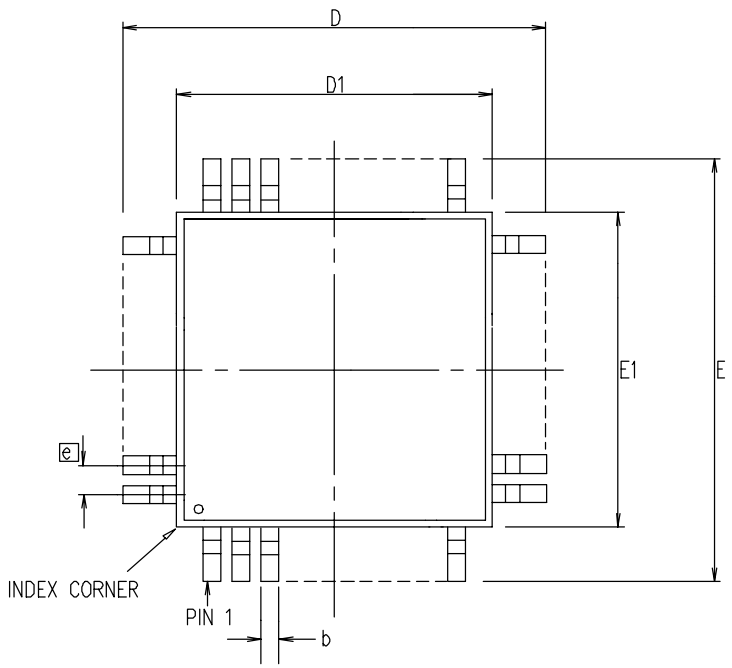
V

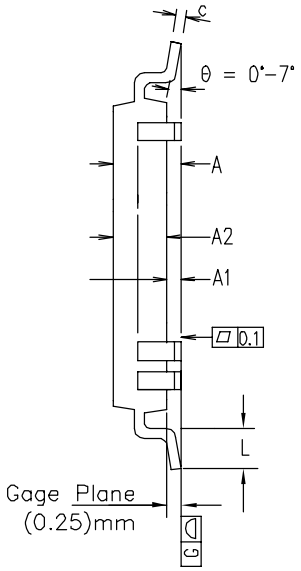
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VIT MAXERR 12, 62, 70
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06921 Sophia Antipolis Cedex
France.

2. Digital Satellite Equipment Control (DiSEqC™)
EUTELSAT
European Telecommunications Satellite Organisation
70, rue Balard - 75502 PARIS Cedex 15
France.





Symbol	Control Dimensions in millimetres			Altern. Dimensions in inches	
	MIN	MAX		MIN	MAX
A	–	2.45		–	0.096
A1	0.00	0.25		0.000	0.010
A2	1.80	2.20		0.071	0.087
D	17.20 BSC			0.677 BSC	
D1	14.00 BSC			0.551 BSC	
E	17.20 BSC			0.677 BSC	
E1	14.00 BSC			0.551 BSC	
L	0.73	1.03		0.029	0.041
e	0.65 BSC.			0.026 BSC.	
b	0.22	0.40		0.009	0.016
c	0.11	0.23		0.004	0.009
	Pin features				
N	80				
ND	20				
NE	20				
NOTE	SQUARE				

Conforms to JEDEC MS–022 BC Iss. B

Notes:

1. Pin 1 indicator may be a corner chamfer, dot or both.
2. Controlling dimensions are in millimeters.
3. The top package body size may be smaller than the bottom package body size by a max. of 0.15 mm.
4. Dimension D1 and E1 do not include mould protusion.
5. Dimension b does not include dambar protusion.
6. Coplanarity, measured at seating plane G, to be 0.010 mm max.

This drawing supersedes 418/ED/51210/016 (Swindon)

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ACN	202049	204612	205120	207056	
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APPD.					

ORIGINATING SITE: SWINDON

Title: Package Outline Drawing for
80L MQFP (GP)
(14x14x2.0) mm, Body+3.2 mm

Drawing Number

GPD00232