4.5V TO 18V INPUT 10 PIN SYNCHRONOUS BUCK CONTROLLER WITH POWER GOOD

FEATURES

- **Input Operating Voltage Range: 4.5 V to 18 V**
- **Up to 20 A Output Currents**
- **Supports Pre-Biased Outputs**
- **0.5% 0.591 V Reference**
- **600 kHz (TPS40192) and 300 kHz (TPS40193) Switching Frequencies**
- **Three Selectable Thermally Compensated Short Circuit Protection Levels**
- **Hiccup Restart from Faults**
- **Internal 5-V Regulator**
- **High and Low side FET RDS_{ON} Current Sensing**
- **10-Pin 3 mm × 3 mm SON Package**
- **Internal 4-ms Soft-Start Time**
- **Thermal Shutdown Protection at 145°C**

APPLICATIONS

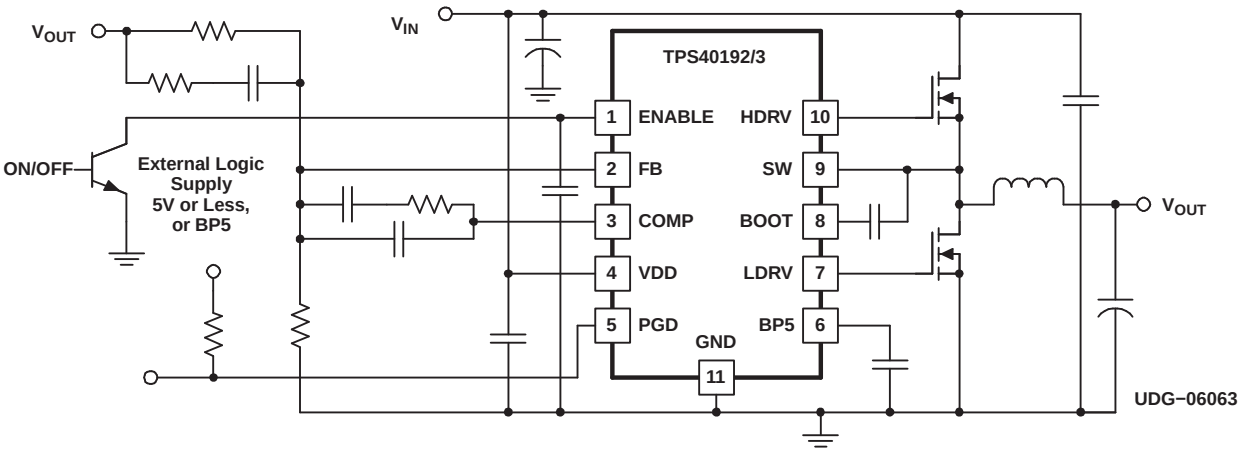
- **Cable Modem CPE**
- **Digital Set Top Box**
- **Graphics/Audio Cards**
- **Entry Level and Mid-Range Servers**

CONTENTS

DESCRIPTION

TPS40192 and TPS40193 are cost-optimized synchronous buck controllers that operate from 4.5 V to 18 V input. These controllers implement a voltage-mode control architecture with the switching frequency fixed at either 600 kHz (TPS40192) or 300 kHz (TPS40193). The higher switching frequency facilitates the use of smaller inductor and output capacitors, thereby providing a compact power-supply solution. An adaptive anti-cross conduction scheme is used to prevent shoot through current in the power FETs.

SIMPLIFIED APPLICATION DIAGRAM



DESCRIPTION (continued)

Short circuit detection is done by sensing the voltage drop across the low-side MOSFET when it is on and comparing it with a user selected threshold of 100 mV, 200 mV or 280 mV. The threshold is set with a single external resistor connected from COMP to GND. This resistor is sensed at startup and the selected threshold is latched. Pulse by pulse limiting (to prevent current runaway) is provided by sensing the voltage across the high-side MOSFET when it is on and terminating the cycle when the voltage drop rises above a fixed threshold of 550 mV. When the controller senses an output short circuit, both MOSFETs are turned off and a timeout period is observed before attempting to restart. This provides limited power dissipation in the event of a sustained fault.

ORDERING INFORMATION

T_J	PACKAGE	FREQUENCY (kHz)	TAPE AND REEL QUANTITY	PART NUMBER
-40°C to 85°C	Plastic 10-Pin SON (DRC)	300	250	TPS40193DRCT
			3000	TPS40193DRCR
		600	250	TPS40192DRCT
			3000	TPS40192DRCR

DEVICE RATINGS

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted(1)

		TPS40192/TPS40193	UNIT
Input voltage range	VDD, ENABLE	–0.3 to 20	V
	SW	–5 to 25	
	BOOT, HDRV	–0.3 to 30	
	BOOT-SW, HDRV-SW (differential from BOOT or HDRV to SW)	-0.3 to 6	
	COMP, FB, BP5, LDRV, PGD	–0.3 to 6	
T_J	Operating junction temperature range	–40 to 150	°C
T_{stg}	Storage temperature	–55 to 150	

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
V_{VDD}	Input voltage	4.5		18	V
T_J	Operating Junction temperature	-40		125	°C

PACKAGE DISSIPATION RATINGS

PACKAGE	AIRFLOW (LFM)	$R_{\theta JA}$ High-K Board(1) (°C/W)	Power Rating (W) T_A = 25°C	Power Rating (W) T_A = 85°C
DRC	0 (Natural Convection)	47.9	2.08	0.835
	200	40.5	2.46	0.987
	400	38.2	2.61	1.04

(1) Ratings based on JEDEC High Thermal Conductivity (High K) Board. For more information on the test method, see TI Technical Brief SZZA017.

ELECTROSTATIC DISCHARGE (ESD) PROTECTION

	MIN	TYP	MAX	UNIT
Human Body Model (HBM)		2500		V
Charged Device Model (CDM)		1500		

ELECTRICAL CHARACTERISTICS

T_J = –40°C to 85°C, V_{VDD}= 12 V_{dc}, all parameters at zero power dissipation (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
REFERENCE							
V_{FB}	Feedback voltage range		0°C ≤ T_J ≤ 85°C	588	591	594	mV
			-40°C ≤ T_J ≤ 85°C	585	591	594	
INPUT SUPPLY							
V_{VDD}	Input voltage range			4.5		18.0	V
I_{VDD}	Operating current		V_{ENABLE} = 3 V		2.5	4.0	mA
			V_{ENABLE} = 0.6 V		45	70	µA
ON BOARD REGULATOR							
V_{5VBP}	Output voltage		V_{VDD} > 6 V, I_{5VBP} ≤ 10 mA	5.1	5.3	5.5	V
V_{DO}	Regulator dropout voltage		V_{VDD} - V_{BP5} , V_{VDD} = 5 V, I_{BP5} ≤ 25 mA		350	550	mV
I_{SC}	Regulator current limit threshold			50			mA
I_{BP5}	Average current					50	
OSCILLATOR							
f_{SW}	Switching frequency	TPS40193		240	300	360	kHz
		TPS40192		500	600	700	
V_{RMP}	Ramp amplitude(1)				1		V
PWM							
D_{MAX}	Maximum duty cycle(1)			85%			
$t_{ON(min)}$	Minimum controlled pulse(1)					110	ns
t_{DEAD}	Output driver dead time		HDRV off to LDRV on		50		
			LDRV off to HDRV on		25		
SOFT-START							
t_{SS}	Soft-start time			3	4	6	ms
t_{SSDLY}	Soft-start delay time				2		
t_{REG}	Time to regulation				6		
ERROR AMPLIFIER							
GBWP	Gain bandwidth product(1)			7	10		MHz
A_{OL}	DC gain(1)			60			dB
I_{IB}	Input bias current (current out of FB pin)					100	nA
I_{EAOP}	Output source current		V_{FB} = 0 V	1			mA
I_{EAOM}	Output sink current		V_{FB} = 2 V	1			
SHORT CIRCUIT PROTECTION							
$t_{PSS(min)}$	Minimum pulse during short circuit(1)				250		ns
t_{BLNK}	Blanking time(1)			60	90	120	
t_{OFF}	Off-time between restart attempts			30	50		ms
V_{ILIM}	Short circuit comparator threshold voltage		$R_{COMP(GND)}$ = OPEN, T_J = 25°C	160	200	240	mV
			$R_{COMP(GND)}$ = 4 kΩ, T_J = 25°C	80	100	120	
			$R_{COMP(GND)}$ = 12 kΩ, T_J = 25°C	228	280	342	
V_{ILIMH}	Short circuit threshold voltage on high-side MOSFET		T_J = 25°C	400	550	650	

(1) Ensured by design. Not production tested.

ELECTRICAL CHARACTERISTICS (continued)

T_J = –40°C to 85°C, V_{VDD}= 12 V_{dc}, all parameters at zero power dissipation (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OUTPUT DRIVERS						
R_{HDHI}	High-side driver pull-up resistance	V_{BOOT} - V_{SW} = 4.5 V, I_{HDRV} = -100 mA		3	6	Ω
R_{HDLO}	High-side driver pull-down resistance	V_{BOOT} - V_{SW} = 4.5 V, I_{HDRV} = 100 mA		1.5	3.0	
R_{LDHI}	Low-side driver pull-up resistance	I_{LDRV} = -100 mA		2.5	5.0	
R_{LDLO}	Low-side driver pull-down resistance	I_{LDRV} = 100 mA		0.8	1.5	
t_{HRISE}	High-side driver rise time(2)	C_{LOAD} = 1 nF		15	35	ns
t_{HFALL}	High-side driver fall time(2)			10	25	
t_{LRISE}	Low-side driver rise time(2)			15	35	
t_{LFALL}	Low-side driver fall time(2)			10	25	
UVLO						
V_{UVLO}	Turn-on voltage		3.9	4.2	4.4	V
$UVLO_{HYST}$	Hysteresis		700	800	900	mV
SHUTDOWN						
V_{IH}	High-level input voltage, ENABLE			1.9	3.0	V
V_{IL}	Low-level input votlage, ENABLE		0.6			
POWER GOOD						
V_{OV}	Feedback voltage limit for powergood			650		mV
V_{UV}	Feedback voltage limit for powergood			525		
V_{PG_HYST}	Powergood hysteresis voltage at FB pin			30		
R_{PGD}	Pulldown resistance of PGD pin	V_{FB} = 0 V		7	50	Ω
I_{PDGLK}	Leakage current	V_{FB} = 0 V		7	12	µA
BOOT DIODE						
V_{DFWD}	Bootstrap diode forward voltage	I_{BOOT} = 5 mA	0.5	0.8	1.2	V
THERMAL SHUTDOWN						
T_{JSD}	Junction shutdown temperature(2)			145		°C
T_{JSDH}	Hysteresis(2)			20		

(2) Ensured by design. Not production tested.

TYPICAL CHARACTERISTICS

RELATIVE REFERENCE FEEDBACK VOLTAGE
vs
JUNCTION TEMPERATURE

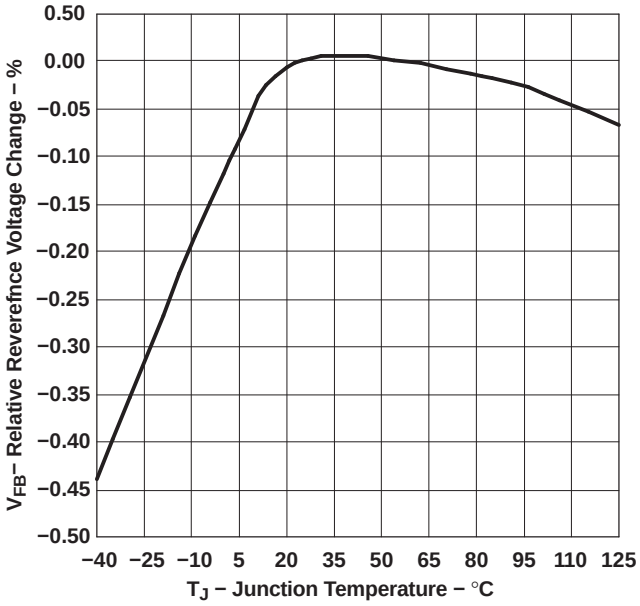


Figure 1.

RELATIVE OSCILLATOR FREQUENCY CHANGE
vs
JUNCTION TEMPERATURE

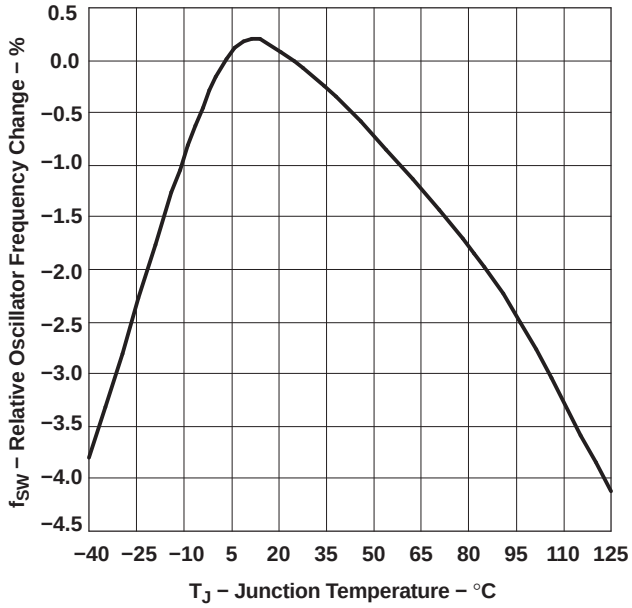


Figure 2.

SHUTDOWN INPUT CURRENT
vs
JUNCTION TEMPERATURE

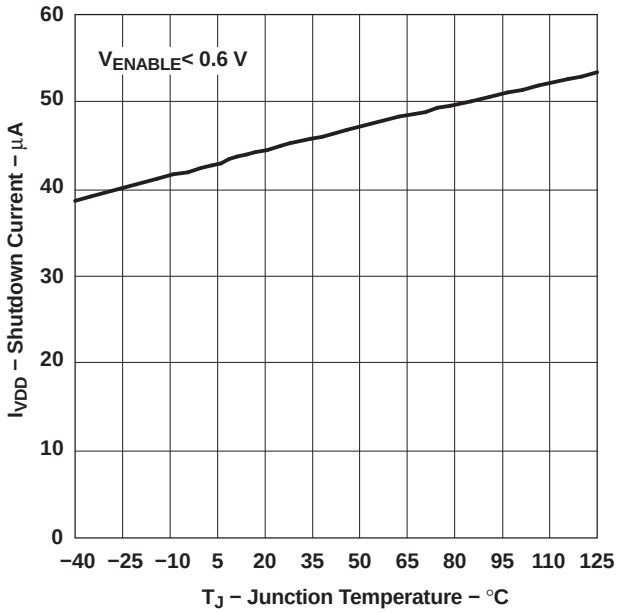


Figure 3.

ENABLE THRESHOLD VOLTAGE
vs
JUNCTION TEMPERATURE

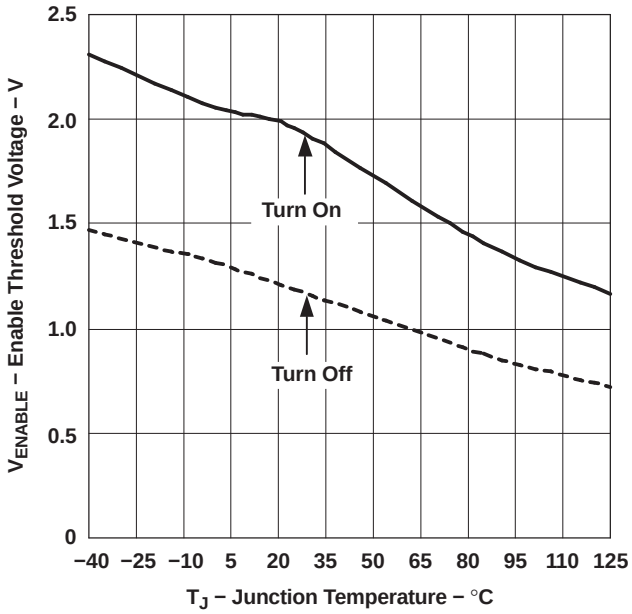


Figure 4.

TYPICAL CHARACTERISTICS (continued)

SOFT START TIME vs JUNCTION TEMPERATURE

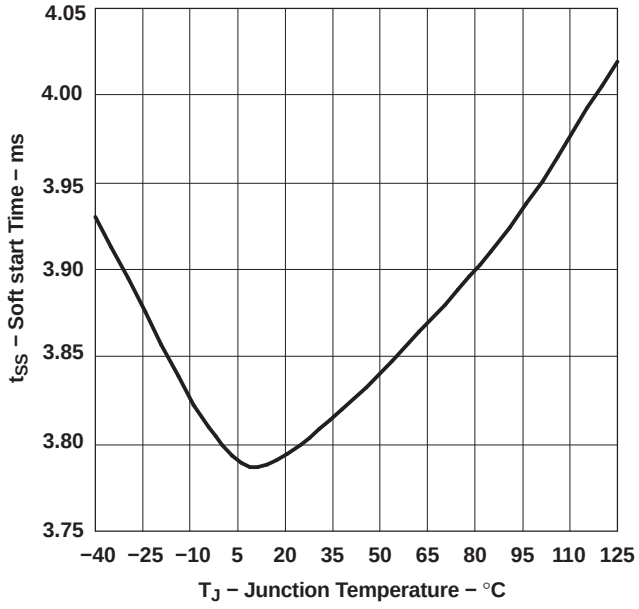


Figure 5.

LOW-SIDE MOSFET CURRENT LIMIT THRESHOLD vs JUNCTION TEMPERATURE

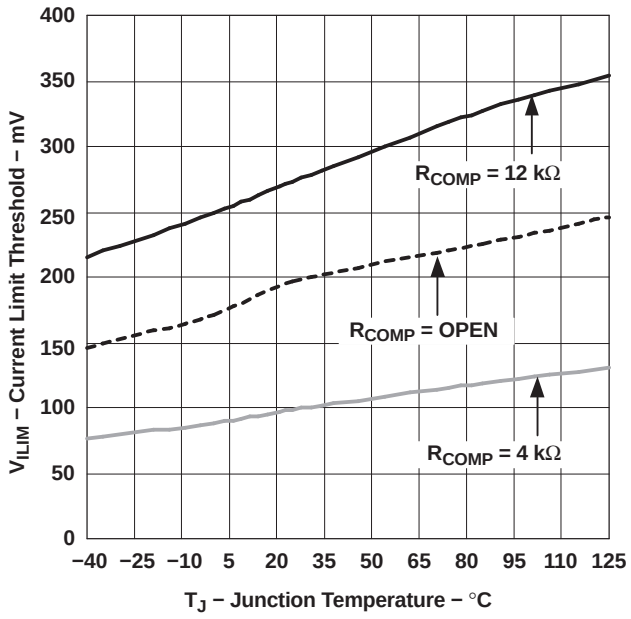


Figure 6.

HIGH-SIDE MOSFET CURRENT LIMIT THRESHOLD vs JUNCTION TEMPERATURE

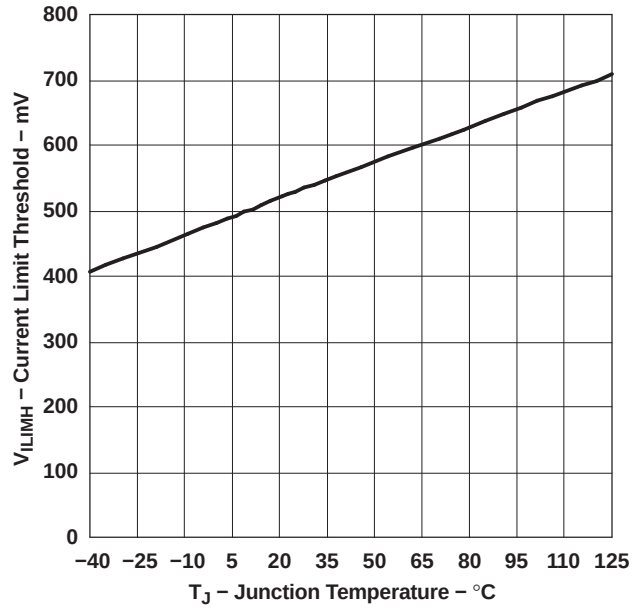


Figure 7.

TOTAL TIME TO REGULATION vs JUNCTION TEMPERATURE

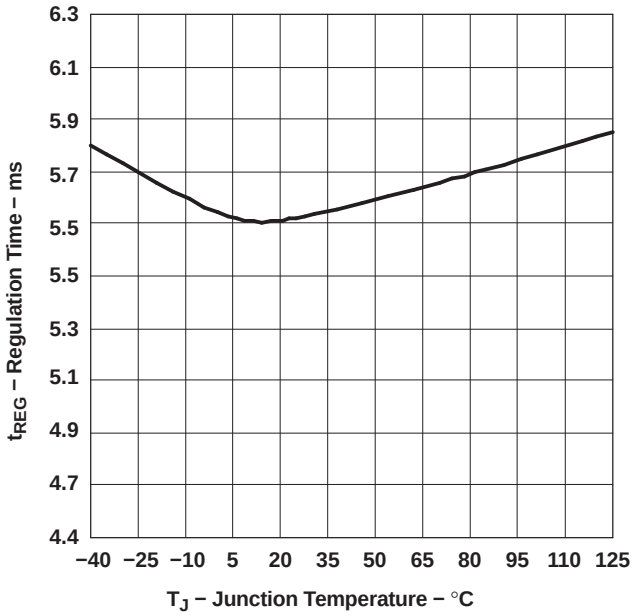


Figure 8.

TYPICAL CHARACTERISTICS (continued)

POWERGOOD THRESHOLD VOLTAGE vs JUNCTION TEMPERATURE

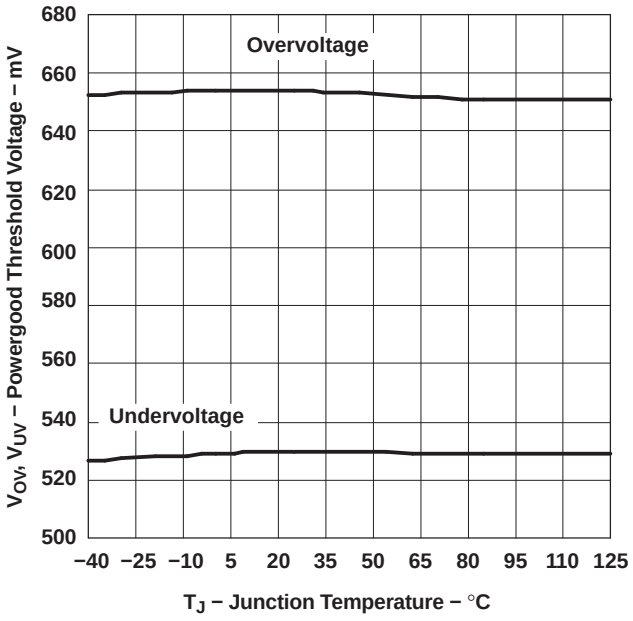


Figure 9.

SHUTDOWN CURRENT vs INPUT VOLTAGE

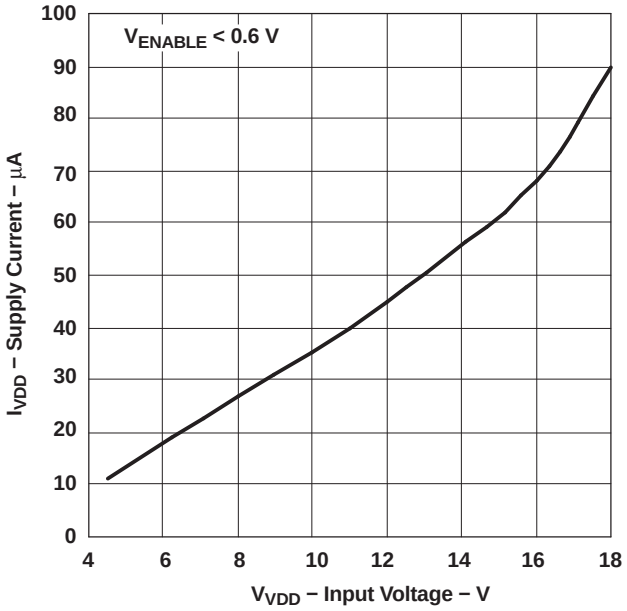


Figure 10.

RELATIVE OVERCURRENT TRIP POINT vs FREEWHEEL TIME

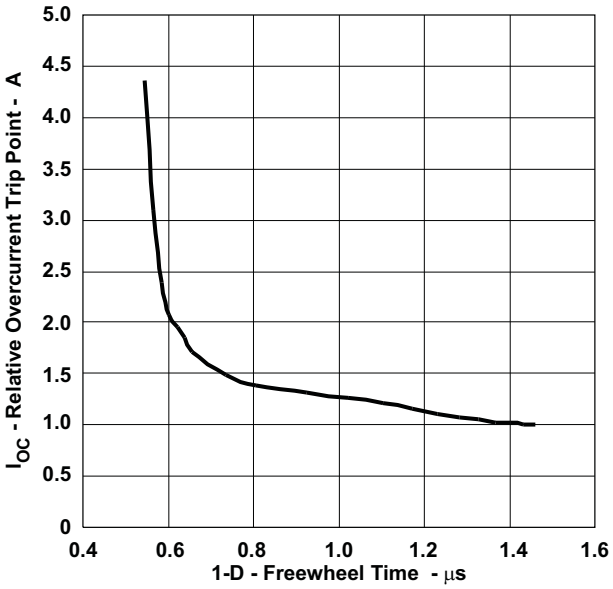


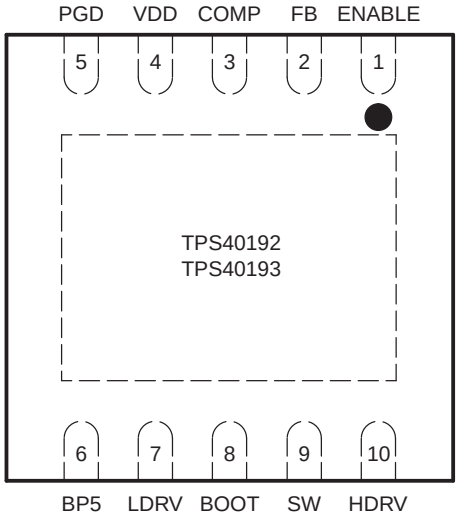
Figure 11.

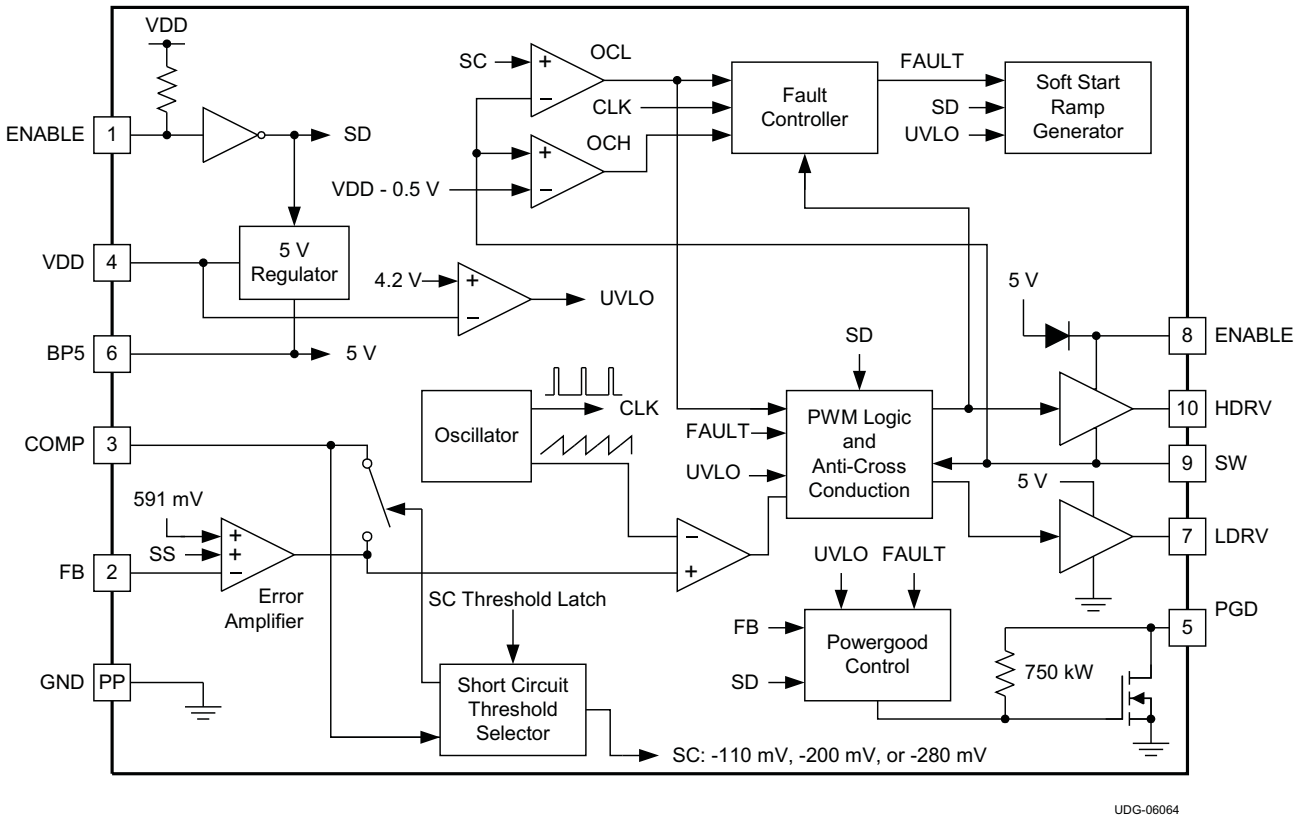
DEVICE INFORMATION

TERMINAL FUNCTIONS

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
BOOT	8	I	Gate drive voltage for the high-side N-channel MOSFET. A capacitor 100 nF typical must be connected between this pin and SW.
BP5	6	O	Output bypass for the internal regulator. Connect at least 1µF capacitor from this pin to GND. Larger capacitors, up to 4.7µF will improve noise performance when using a low side FET with a gate charge of 25nC or greater. Low power, low noise loads may be connected here if desired. The sum of the external load and the gate drive requirements must not exceed 50 mA. This regulator is turned off when ENABLE is pulled low.
COMP	3	O	Output of the error amplifier.
ENABLE	1	I	Logic level input which starts or stops the controller from an external user command. A high-level turns the controller on. A weak internal pull-up holds this pin high so that the pin may be left floating if this function is not used.
FB	2	I	Inverting input to the error amplifier. In normal operation the voltage on this pin is equal to the internal reference voltage (591 mV typical)
GND	(11)	-	Thermal pad ground connection. Common reference for the device. Connect to the system GND.
HDRV	10	O	Bootstrapped output for driving the gate of the high side N channel FET.
LDRV	7	O	Output to the rectifier MOSFET gate
PGD	5	O	Open drain power good output
SW	9	I	Sense line for the adaptive anti-cross conduction circuitry. Serves as common connection for the flying high side MOSFET driver
VDD	4	I	Power input to the controller

DRC PACKAGE
(TOP VIEW)




VDD
ENABLE
1
SD
SC
OCL
CLK
OCH
VDD - 0.5 V
Fault Controller
FAULT
SD
UVLO
Soft Start Ramp Generator
VDD
4
5 V Regulator
4.2 V
UVLO
BP5
6
5 V
5 V
8
ENABLE
SD
Oscillator
CLK
FAULT
UVLO
PWM Logic and Anti-Cross Conduction
10
HDRV
9
SW
5 V
COMP
3
591 mV
SS
FB
2
Error Amplifier
7
LDRV
UVLO FAULT
SC Threshold Latch
FB
SD
Powergood Control
PGD
5
750 kW
GND
PP
Short Circuit Threshold Selector
SC: -110 mV, -200 mV, or -280 mV

UDG-06064

APPLICATION INFORMATION

Introduction

The TPS40192 and TPS40193 are cost optimized controllers providing all the necessary features to construct a high performance DC/DC converter while keeping costs to a minimum. Support for pre-biased outputs eliminates concerns about damaging sensitive loads during startup. Strong gate drivers for the high side and rectifier N-channel MOSFETs decrease switching losses for increased efficiency. Adaptive gate drive timing prevents shoot through and minimizes body diode conduction in the rectifier MOSFET, also increasing efficiency. Selectable short circuit protection thresholds and hiccup recovery from a short circuit increase design flexibility and minimize power dissipation in the event of a prolonged output fault. A dedicated enable pin (ENABLE) allows the converter to be placed in a very low quiescent current shutdown mode. Internally fixed switching frequency and soft-start time reduce external component count, simplifying design and layout, as well as reducing footprint and cost. The 3 mm $\times$ 3 mm package size also contributes to a reduced overall converter footprint.

Voltage Reference

The band gap cell is designed with a trimmed 591 mV output. The 0.5% tolerance on the reference voltage allows the user to design a very accurate power-supply.

Oscillator

The TPS40192 has a fixed internal switching frequency of 600 kHz while the TPS40193 operates at 300 kHz.

UVLO

When the input voltage is below the UVLO threshold, the device holds all gate drive outputs in the low (OFF) state. When the input rises above the UVLO threshold, and the ENABLE pin is above the turn ON threshold, the oscillator begins to operate and the start-up sequence is allowed to begin. The UVLO level is internally fixed at 4.2 V.

APPLICATION INFORMATION (continued)

Enable Functionality

The TPS40192 and TPS40193 have a dedicated ENABLE pin. This simplifies user level interface design since no multiplexed functions exist. Another benefit is a true low power shutdown mode of operation. When the ENABLE pin is pulled to GND, all unnecessary functions, including the BP5 regulator, are turned off, reducing the device IDD current to 45-uA. A functionally equivalent circuit of the enable circuitry shown in Figure 12.

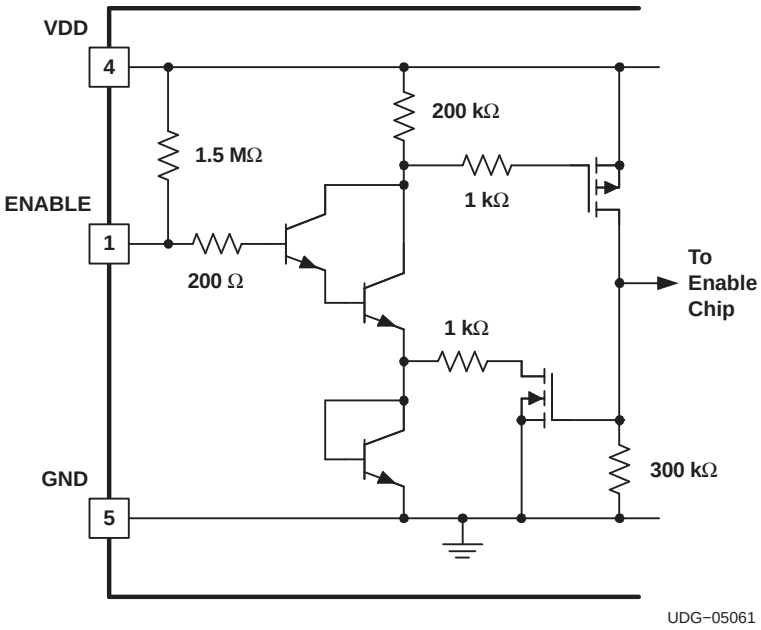


Figure 12. TPS40192 ENABLE Pin Internal Circuitry

If the ENABLE pin is left floating, the chip starts automatically. The pin must be pulled to less than 600 mV to guarantee that the TPS40192/3 is in shutdown mode. Note that the ENABLE pin is relatively high impedance. In some situations, there could be enough noise nearby to cause the ENABLE pin to swing below the 600 mV threshold and give erroneous shutdown commands to the rest of the device. There are two solutions to this problem should it arise.

1. Place a capacitor from ENABLE to GND. A side effect of this is to delay the start of the converter while the capacitor charges past the enable threshold
2. Place a resistor from VDD to ENABLE. This causes more current to flow in the shutdown mode, but does not delay converter startup. If a resistor is used, the total current into the ENABLE pin should be limited to no more than 500 µA.

Startup Sequence and Timing

The TPS40192/3 startup sequence is as follows. After input power is applied, the 5-V onboard regulator comes up. Once this regulator comes up, the device goes through a period where it samples the impedance at the COMP pin and determines the short circuit protection threshold voltage, by placing 400 mV on the COMP pin for approximately 1 ms. During this time, the current is measured and compared against internal thresholds to select the short circuit protection threshold. After this, the COMP pin is brought low for 1 ms. This ensures that the feedback loop is preconditioned at startup and no sudden output rise occurs at the output of the converter when the converter is allowed to start switching. After these initial two milliseconds, the internal soft-start circuitry is engaged and the converter is allowed to start. See Figure 13.

APPLICATION INFORMATION (continued)

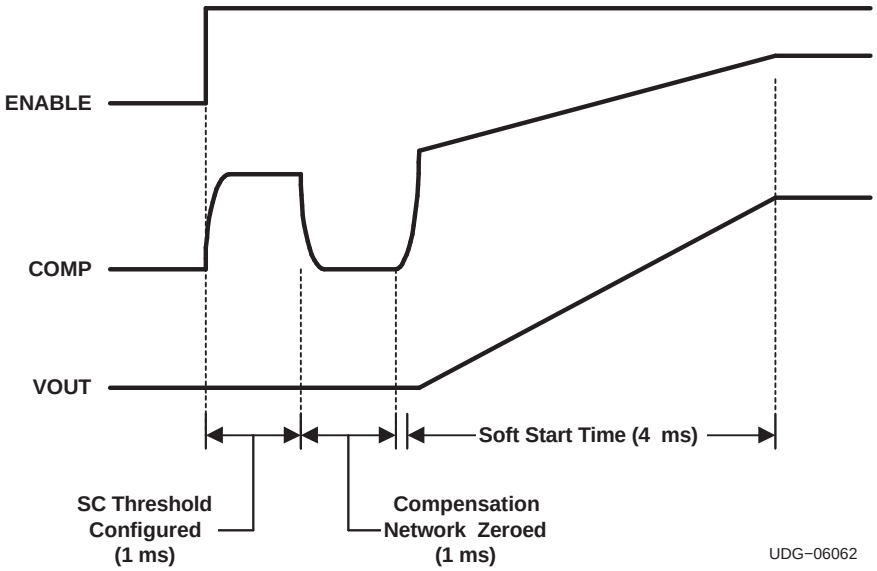


Figure 13. Startup Sequence

Selecting the Short Circuit Current

A short circuit in the TPS40192/3 is detected by sensing the voltage drop across the low-side FET when it is on, and across the high-side FET when it is on. If the voltage drop across either FET exceeds the short circuit threshold in any given switching cycle, a counter increments one count. If the voltage across the high-side FET was higher that the short circuit threshold, that FET is turned off early. If the voltage drop across either FET does not exceed the short circuit threshold during a cycle, the counter is decremented for that cycle. If the counter fills up (a count of 7) a fault condition is declared and the drivers turn off both MOSFETs. After a timeout of approximately 50 ms, the controller attempts to restart. If a short circuit is still present at the output, the current quickly ramps up to the short circuit threshold and another fault condition is declared and the process of waiting for the 50 ms an attempting to restart repeats. The low side threshold will increase as the low side on time decreases due to blanking time and comparator response time. See Figure 11 for changes in the threshold as the low side FET conduction time decreases.

The TPS40192/3 provides three selectable short circuit protection thresholds for the low side FET: 100 mV, 200 mV and 280 mV. The particular threshold is selected by connecting a resistor from COMP to GND. Table 1 shows the short circuit thresholds for corresponding resistors from COMP to GND. When designing the compensation for the feedback loop, remember that a low impedance compensation network combined with a long network time constant can cause the short circuit threshold setting to not be as expected. The time constant and impedance of the network connected from COMP to FB should be as in Equation 1 to guarantee no interaction with the short circuit threshold setting.

$$\frac{0.4\ \text{V}}{\text{R1}} \times e^{\left(\frac{-t}{\text{R1} \times \text{C1}}\right)} < 10\ \mu\text{A} \tag{1}$$

where

- t is 1 ms, the sampling time of the short circuit threshold setting circuit
- R1 and C1 are the values of the components in Figure 14

APPLICATION INFORMATION (continued)

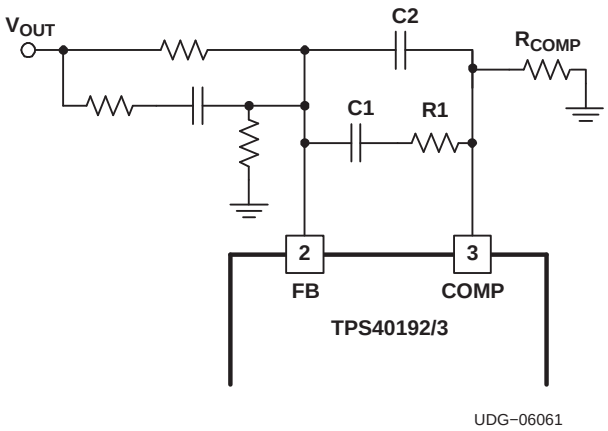


Figure 14. Short Circuit Threshold Feedback Network

Table 1. Short Circuit Threshold Voltage Selection

COMPARATOR RESISTANCE R_{COMP} (kΩ)	CURRENT LIMIT THRESHOLD VOLTAGE (mV) V_{ILIM}(V)
12 ±10%	280
Open	200
4 ±10%	100

The range of short circuit current thresholds that can be expected is shown in Equation 2 and Equation 3.

$$I_{SCP(max)} = \frac{V_{ILIM(max)}}{R_{DS(on)min}} \quad (2)$$

$$I_{SCP(min)} = \frac{V_{ILIM(min)}}{R_{DS(on)max}} \quad (3)$$

where

- I_{SCP} is the short circuit current
- V_{ILIM} is the short circuit threshold for the low-side MOSFET
- $R_{DS(on)}$ is the channel resistance of the low-side MOSFET

Note that due to blanking time considerations, overcurrent threshold accuracy may fall off for duty cycle greater than 75% with the TPS40192, or 88% with the TPS40193. The reason for this is that the over current comparator will have only a very short time to sample the SW pin voltage under these conditions and may not have time to respond to voltages very near the threshold.

The short circuit protection threshold for the high-side MOSFET is fixed at 550 mV typical, 400 mV minimum. This threshold is in place to provide a maximum current output using pulse by pulse current limit in the case of a fault. The pulse will be terminated when the voltage drop acros the high side FET exceeds the short circuit threshold. The maximum amount of current that can be guaranteed to be sourced from a converter can be found by Equation 4.

$$I_{OUT(max)} = \frac{V_{ILIM(min)}}{R_{DS(on)max}} \quad (4)$$

where

- $I_{OUT(max)}$ is the maximum current that the converter is guaranteed to source
- $V_{ILIMH(min)}$ is the short circuit threshold for the high-side MOSFET (400 mV)

- $R_{DS(on)max}$ is the maximum resistance of the high-side MOSFET

If the required current from the converter is greater than the calculated $I_{OUT(max)}$, a lower resistance high-side MOSFET must be chosen. Both the high side and low side thresholds use temperature compensation to approximate the change in resistance for a typical power MOSFET. This will help couneract shifts in overcurrent thresholds as temperature increases. For this to be effective, the MOSFETs and the IC must be well coupled thermally.

5-V Regulator

These devices have an on board 5-V regulator that allows the parts to operate from a single voltage feed. No separate 5-V feed to the part is required. This regulator needs to have a minimum of 1-µF of capacitance on the BP5 pin to guarantee stability. A ceramic capacitor is suggested for this purpose.

This regulator can also be used to supply power to nearby circuitry, eliminating the need for a separate LDO in some cases. If this pin is used for external loads, be aware that this is the power supply for the internals of the TPS40192/3. While efforts have been made to reduce sensitivity, any noise induced on this line has an adverse effect on the overall performance of the internal circuitry and shows up as increased pulse jitter, or skewed reference voltage. Also, when the device is disabled by pulling the EN pin low, this regulator is turned off and will not be available to supply power.

The amount of power available from this pin varies with the size of the power MOSFETs that the drivers must operate. Larger MOSFETs require more gate drive current and reduce the amount of power available on this pin for other tasks. The total current that can be drwan from this pin by both the gate drive and external loads cannot exceed 50mA. The IC itself will use up to 4mA from the regulator and the total gate drive current can be found from Equation 5.

For regulator stability, a 1-µF capacitor is required to be connected from BP5 to GND. In some applications using higher gate charge MOSFETs, a larger capacitor is required for noise suppression. For a total gate charge of both the high and low side MOSFETs greater than 20 nC, a 2.2-µF or larger capacitor is recommended.

$$I_G = f_{SW} \times \left(Q_{G\ (high)} + Q_{G\ (low)}\right) \tag{5}$$

where

- I_G is the required gate drive current
- f_{SW} is the switching frequency (600 kHz for TPS40192, and 300 kHz for TPS40193)
- $Q_{G(high)}$ is the gate charge requirement for the high-side FET when V_{GS}=5 V
- $Q_{G(low)}$ is the gate charge requirement for the low-side FET when V_{GS}=5 V

Pre-Bias Startup

The TPS40192/3 contains a unique circuit to prevent current from being *pulled* from the output during startup in the condition the output is pre-biased. When the soft-start commands a voltage higher than the pre-bias level (internal soft-start becomes greater than feedback voltage [V_{FB}]), the controller slowly activates synchronous rectification by starting the first LDRV pulses with a narrow on-time. It then increments that on-time on a cycle-by-cycle basis until it coincides with the time dictated by (1-D), where D is the duty cycle of the converter. This scheme prevents the initial sinking of the pre-bias output, and ensures that the out voltage (V_{OUT}) starts and ramps up smoothly into regulation and the control loop is given time to transition from pre-biased startup to normal mode operation with minimal disturbance to the output voltage. The amount of time from the start of switching until the low-side MOSFET is turned on for the full (1-D) interval is defined by 32 clock cycles.

Drivers

The drivers for the external HDRV and LDRV MOSFETs are capable of driving a gate-to-source voltage of 5 V. The LDRV driver switches between VDD and GND, while HDRV driver is referenced to SW and switches between BOOT and SW. The drivers have non-overlapping timing that is governed by an adaptive delay circuit to minimize body diode conduction in the synchronous rectifier. The drivers are capable of driving MOSFETS that are appropriate for a 15-A (TPS40192) or 20A (TPS40193) converter.

Power Good

The TPS40192/3 provides an indication that output power is good for the converter. This is an open drain signal and pulls low when any condition exists that would indicate that the output of the supply might be out of regulation. These conditions include:

- V_{FB} is more than ±10% from nominal
- soft-start is active
- an undervoltage condition exists for the device
- a short circuit condition has been detected
- die temperature is over (145°C)

NOTE:

When there is no power to the device, PGOOD is not able to pull close to GND if an auxiliary supply is used for the power good indication. In this case, a built in resistor connected from drain to gate on the PGOOD pull down device makes the PGOOD pin look approximately like a diode to GND.

Thermal Shutdown

If the junction temperature of the device reaches the thermal shutdown limit of 145°C, the PWM and the oscillator are turned off and HDRV and LDRV are driven low, turning off both FETs. When the junction cools to the required level (125°C nominal), the PWM inititates soft start as during a normal power up cycle.

DESIGN EXAMPLE

INTRODUCTION

This example illustrates the design process and component selection for a 12 V to 1.8 V point-of-load synchronous buck regulator using the TPS40192. A definition of symbols used can be found in Table 7 of this datasheet.

Table 2. Design Example Electrical Characteristics

PARAMETER		TEST CONDITION	MIN	NOM	MAX	UNIT
V_{IN}	Input voltage		8		14	V
$V_{IN(ripple)}$	Input ripple	I_{OUT} = 10 A			0.6	
V_{OUT}	Output voltage	0 A ≤ I_{OUT} ≤ 10 A	1.764	1.800	1.836	
	Line regulation	8.0 V ≤ V_{IN} ≤ 14 V			0.5%	
	Load regulation	0 A ≤ I_{OUT} ≤ 10 A			0.5%	
V_{RIPPLE}	Output ripple	I_{OUT} = 10 A			36	mV
V_{OVER}	Output overshoot	3 A ≤ I_{OUT} ≤ 7 A		50		
V_{UNDER}	Output undershoot			50		
I_{OUT}	Output current		0		10	A
I_{SCP}	Short circuit current trip point					
η	Efficiency	V_{IN} =12 V, I_{OUT} = 5 A			90%	
f_{SW}	Switching frequency			600		kHz
	Size					

The bill of materials for this application is shown Table 6. The efficiency, line and load regulation from boards built using this design are shown in Figure 15 and Table 2. Gerber Files and additional application information are available from the factory.

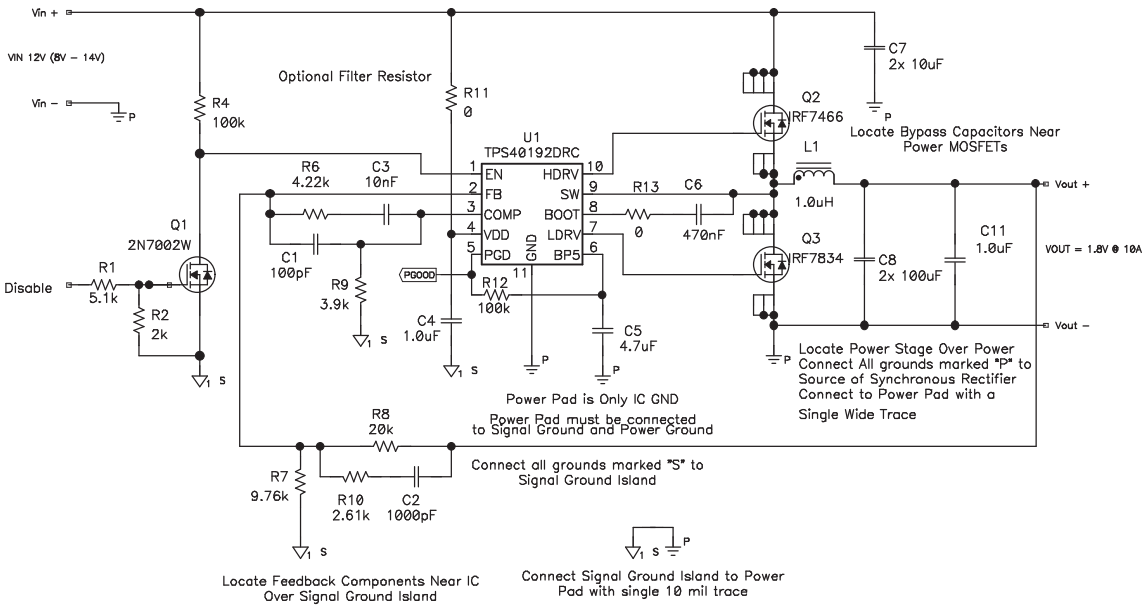


Figure 15. TPS40192 Sample Schematic

Design Procedure

Selecting the Switching Frequency

For this design the TPS40192, with f_{SW} = 600 kHz, is selected to reduce inductor and capacitor sizes.

Inductor Selection

The inductor is typically sized for approximately 30% peak-to-peak ripple current (I_{RIPPLE}). Given this target ripple current, the required inductor size can be calculated by Equation 6.

$$L \approx \frac{V_{IN(max)} - V_{OUT}}{0.3 \times I_{OUT}} \times \frac{V_{OUT}}{V_{IN(max)}} \times \frac{1}{f_{SW}} \tag{6}$$

Solving this for

- $V_{IN(max)}$ = 14 V
- V_{OUT} = 1.8 V
- I_{OUT} = 10A
- f_{SW} = 600 kHz

an inductor value of 0.87 µH is obtained.

A standard value of 1.0 µH is selected. Solving for I_{RIPPLE} with 1.0 µH results in 2.6-A peak-to-peak ripple.

The RMS current through the inductor is approximated by Equation 7.

$$I_{L(rms)} = \sqrt{\left(I_{L(avg)}\right)^2 + \frac{1}{12}\left(I_{RIPPLE}\right)^2} = \sqrt{\left(I_{OUT}\right)^2 + \frac{1}{12}\left(I_{RIPPLE}\right)^2} \tag{7}$$

Using Equation 7, the maximum RMS current in the inductor is approximately 10.03 A

Output Capacitor Selection (C8)

The selection of the output capacitor is typically driven by the output transient response. The Equation 8 and Equation 9 overestimate the voltage deviation to account for delays in the loop bandwidth and can be used to determine the required output capacitance.

$$V_{OVER} < \frac{I_{TRAN}}{C_{OUT}} \times \Delta T = \frac{I_{TRAN}}{C_{OUT}} \times \frac{I_{TRAN} \times L}{V_{OUT}} = \frac{\left(I_{TRAN}\right)^2 \times L}{V_{OUT} \times C_{OUT}} \tag{8}$$

$$V_{UNDER} < \frac{I_{TRAN}}{C_{OUT}} \times \Delta T = \frac{I_{TRAN}}{C_{OUT}} \times \frac{I_{TRAN} \times L}{V_{IN} - V_{OUT}} = \frac{\left(I_{TRAN}\right)^2 \times L}{\left(V_{IN} - V_{OUT}\right) \times C_{OUT}} \tag{9}$$

If

- $V_{IN(min)} > 2 \times V_{OUT}$, use overshoot to calculate minimum output capacitance.
- $V_{IN(min)} < 2 \times V_{OUT}$, use undershoot to calculate minimum output capacitance.

$$C_{OUT(min)} = \frac{\left(I_{TRAN(max)}\right)^2 \times L}{V_{OUT} \times V_{OVER}} \tag{10}$$

Based on a 4-A load transient with a maximum 50 mV overshoot at 8.0 V input, calculate a minimum 178-µF output capacitance.

With a minimum capacitance, the maximum allowable ESR is determined by the maximum ripple voltage and is approximated by Equation 11.

$$ESR_{MAX} < \frac{V_{RIPPLE(tot)} - V_{RIPPLE(cap)}}{C_{OUT}} = \frac{V_{RIPPLE(tot)} - \left(\frac{I_{RIPPLE}}{C_{OUT} \times f_{SW}}\right)}{I_{RIPPLE}} \tag{11}$$

Based on 178 µF of capacitance, 2.6-A ripple current, 600-kHz switching frequency and 36-mV ripple voltage, calculate a capacitive ripple of 24.3 mV and a maximum ESR of 4.4 mΩ.

Two 1206 100-µF, 6.3-V X5R ceramic capacitors are selected to provide more than 178-µF of minimum capacitance and less than 4.4 mΩ of ESR (2.5 mΩ each).

Peak Current Rating of the Inductor

With output capacitance, it is possible to calculate the charge current during start-up and determine the minimum saturation current rating for the inductor. The start-up charging current is approximated by Equation 12.

$$I_{CHARGE} = \frac{V_{OUT} \times C_{OUT}}{T_{SS}} \tag{12}$$

Using the TPS40192's minimum soft-start time of 3.0 ms, C_{OUT} = 240 µF and V_{OUT} = 1.8 V, I_{CHARGE} = 144 mA.

$$I_{L(peak)} = I_{OUT(max)} + \frac{1}{2} I_{RIPPLE} + I_{CHARGE} \tag{13}$$

Table 3. Inductor Requirements

PARAMETER	SYMBOL	VALUE	UNITS
Inductance	L	1.0	µH
RMS current (thermal rating)	$I_{L(rms)}$	10.03	A
Peak current (saturation rating)	$I_{L(peak)}$	11.3	

A PG0083.102 1.0-µH is selected for its small size, low DCR (6.6 mΩ) and high current handling capability (12 A thermal, 17 A saturation)

Input Capacitor Selection (C7)

The input voltage ripple is divided between capacitance and ESR. For this design $V_{RIPPLE(cap)}$ = 400 mV and $V_{RIPPLE(ESR)}$ = 200 mV. The minimum capacitance and maximum ESR are estimated by Equation 14.

$$C_{IN(min)} = \frac{I_{LOAD} \times V_{OUT}}{V_{RIPPLE(cap)} \times V_{IN} \times f_{SW}} \tag{14}$$

$$ESR_{MAX} = \frac{V_{RIPPLE(esr)}}{I_{LOAD} + \frac{1}{2} I_{RIPPLE}} \tag{15}$$

For this design C_{IN} > 9.375 µF and ESR < 17.7 mΩ . The RMS current in the input capacitors is estimated by Equation 16.

$$I_{RMS(Cin)} = I_{IN(rms)} - I_{IN(avg)} = \left(I_{OUT} + \frac{1}{12} I_{RIPPLE}\right) \sqrt{\frac{V_{OUT}}{V_{IN}}} - \frac{V_{OUT} \times I_{OUT}}{V_{IN}} \tag{16}$$

For this design V_{IN} = 14 V, V_{OUT} = 1.8 V, I_{OUT}=10 A and I_{RIPPLE} = 2.6 A calculate an RMS of 2.37 A, so the total of our input capacitors must support 2.37 A of RMS ripple current.

Two 1210 10-µF 25V X5R ceramic capacitors with about 2 mΩ ESR and a 2-A_{RMS} current rating are selected. Higher voltage capacitors are selected to minimize capacitance loss at the DC bias voltage to ensure the capacitors have sufficient capacitance at the working voltage.

MOSFET Switch Selection (Q1, Q2)

The switching losses for the high-side FET are estimated by Equation 17.

$$P_{G1\_SW} = \frac{1}{2} V_{IN} \times I_{OUT} \times T_{SW} \times f_{SW} = \frac{1}{2} V_{IN} \times I_{OUT} \times \frac{Q_{GD1}}{\frac{V_{DD} - V_{TH}}{R_{DRV}}} \times f_{SW} \tag{17}$$

For this design switching losses will be highest at high-line Designing for 1 W of total losses in each MOSFETS and 60% of the total high-side FET losses in switching losses, we can estimate our maximum gate-drain charge for the design by using Equation 18.

$$Q_{GD1} < \frac{P_{G1SW}}{V_{IN} \times I_{OUT}} \times \frac{V_{DD} - V_T}{RDRV} \times \frac{1}{f_{SW}} \tag{18}$$

For a 2-V gate threshold MOSFET, the TPS40192's 5-V gate drive, and the TPS40192's 2.5-Ω drive resistance, we estimate a maximum gate-to-drain charge of 8.5 nC. The switching losses of the synchronous rectifier are lower than the switching losses of the main FET because the voltage across the FET at the point of switching is reduced to the forward voltage drop across the body diode of the SR FET and are estimated by using Equation 19.

The conduction losses in the main FET are estimated by the RMS current through the FET times its $R_{DS(on)}$.

$$P_{G1COM} = \left(I_{OUT} \times \frac{1}{12} I_{RIPPLE}\right)^2 \times R_{DS(on)} \times D = I_{L(rms)} \times R_{DS(on)Q1} \times \frac{V_{OUT}}{V_{IN}} \tag{19}$$

Estimating about 40% of total MOSFET losses to be high-side conduction losses, the maximum $R_{DS(on)}$ of the high-side FET can be estimated by using Equation 20.

$$R_{DS(on)Q1} = \frac{P_{Q1C(on)}}{\left(I_{L(rms)}\right)^2 \times \frac{V_{OUT}}{V_{IN}}} \tag{20}$$

For this design with I_{L_RMS} = 11.22 A_{RMS} and 8 V to 1.8 V design, calculate $R_{DS(on)Q1}$ < 17.3 mΩ for our main switching FET.

Estimating 80% of total low-side MOSFET losses in conduction losses, repeat the calculation for the synchronous rectifier, whose losses are dominated by the conduction losses. Calculate the maximum $R_{DS(on)}$ of the synchronous rectifier by Equation 21.

$$R_{DS(on)Q2} = \frac{P_{Q2C(on)}}{\left(I_{L(rms)}\right)^2 \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)} \tag{21}$$

For this design $I_{L(RMS)}$ = 10.22 A at V_{IN} = 14 V to 1.8 V $R_{DS(on)Q2(max)}$ = 8.8 mΩ.

Table 4. Inductor Requirements V_{IN} = 4.5 V

PARAMETER	SYMBOL	VALUE	UNITS
High-side MOSFET on-resistance	$R_{DS(on)}$	17.3	mΩ
High-side MOSFET gate-to-drain charge	Q_{GD1}	8.5	nC
Low-side MOSFET on-resistance	$R_{DS(on)Q2}$	8.8	mΩ

The IRF7466 has an $R_{DS(on)MAX}$ of 17 mΩ at 4.5-V gate drive and only 8.0-nC V_{GD} "Miller" charge with a 4.5-V gate drive, and is chosen as a high-side FET. The IRF7834 has an $R_{DS(on)MAX}$ of 5.5 mΩ at 4.5-V gate drive and 44 nC of total gate charge. These two FETs have maximum total gate charges of 23 nC and 44 nC respectively, which draws 40.2-mA from the 5-V regulator, less than its 50-mA minimum rating.

Boot Strap Capacitor

To ensure proper charging of the high-side FET gate, limit the ripple voltage on the boost capacitor to less than 50 mV.

$$C_{BOOST} = 20 \times Q_{G1} \tag{22}$$

Based on the IRF7466 MOSFET with a gate charge of 23 nC, we calculate minimum of 460 nF of capacitance. The next higher standard value of 470 nF is selected for the bootstrap capacitor.

Input Bypass Capacitor (C6)

As suggested the TPS40192/93 datasheet, select a 1.0-µF ceramic bypass capacitor for VDD.

BP5 Bypass Capacitor (C5)

The TPS40192 recommends a minimum 1.0-µF ceramic capacitance to stabilize the 5-V regulator. To limit regulator noise to less than 10 mV, the bypass capacitor is sized by using Equation 23.

$$C_{BP5} = 100 \times MAX\left(Q_{G1}, Q_{G2}\right) \tag{23}$$

Since Q2 is larger than Q1 and Q2's total gate charge is 44 nC, a BP5 capacitor of 4.4-µF is calculated, and the next larger standard value of 4.7 µF is selected to limit noise on the BP5 regulator.

Input Voltage Filter Resistor (R11)

$V_{IN(min)}$ > 6.0 V so a 0 Ω resistor is placed in the VDD resistor location. If $V_{IN(min)}$ was < 6.0 V, an optional 1Ω to 2 Ω series VDD resistor could be used to filter switching noise from the device. Limit the voltage drop across this resistor to less than 50 mV.

$$R_{VDD} < \frac{V_{RVDD(max)}}{I_{DD}} = \frac{50\ mV}{3\ mA + \left(Q_{G1}, Q_{G2}\right) \times f_{SW}} \tag{24}$$

Driving the two FETs with 23 nC and 44 nC respectively, we calculate a maximum I_{VDD} current of 43 mA and would select a 1-Ωresistor.

Short Circuit Protection (R9)

The TPS40192/93 use the negative drop across the low-side FET during the OFF time to measure the inductor current. The voltage drop across the low-side FET is given by Equation 25.

$$V_{CS} = I_{L(peak)} \times R_{DS(on)} \tag{25}$$

When 8 V ≤ V_{IN} ≤14 V, $I_{L(peak)}$ = 11.5 A Using the IRF7834 MOSFET, we calculate a peak voltage drop of 63.3 mV.

The TPS40192's internal temperature coefficient helps compensate for the MOSFET's $R_{DS(on)}$ temperature coefficient. For this design select the short circuit protection voltage threshold of 110 mV by selecting R9 = 3.9 kΩ.

Feedback Compensation

Modeling the Power Stage

The DC gain of the modulator is given by Equation 26.

$$A_{MOD} = \frac{dV_{OUT}}{dV_{COMP}} = \frac{dD}{V_{COMP}} \times V_{IN} = \frac{dt}{dV_{RAMP}} \times \frac{1}{T_{SW}} \times V_{IN} \tag{26}$$

Since the peak-to-peak ramp voltage given in the Electrical Characteristics Table is projected from the ramp slope over a full switching period, the modulator gain can be calculated as Equation 27.

$$A_{MOD} = \frac{V_{IN}}{V_{RAMP(p-p)}} \tag{27}$$

This design finds a maximum modulator gain of 14 (23.0 dB). The L-C filter applies a double pole at the resonance frequency described in Equation 28.

$$f_{RES} = \frac{1}{2\pi \times \sqrt{L \times C}} \tag{28}$$

For this design with a 1.0-µH inductor and 2 100-µF capacitors, the resonance frequency is approximately 11.3 kHz. At any lower frequency, the power stage has a DC gain of 23 dB and at any higher frequency the power stage gain drops off at -40 dB per decade. The ESR zero is approximated in Equation 29.

$$f_{ESR} = \frac{1}{2\pi \times C_{OUT} \times R_{ESR}} \quad (29)$$

For C_{OUT} = 2, 100-µF and R_{ESR} = 2.5 mΩ each, f_{ESR} = 636 kHz, greater than 1/5th the switching frequency and outside the scope of the error amplifier design. The gain of the power stage would change to -20 dB per decade above f_{ESR}. The straight line approximation the power stage gain is described in Figure 16.

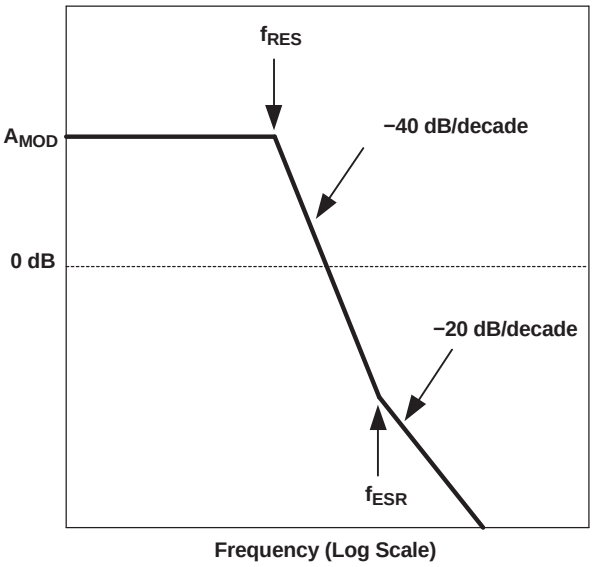


Figure 16. Approximation of Power Stage Gain

The following compensation design procedure assumes $f_{ESR} > f_{RES}$. For designs using large high-ESR bulk capacitors on the output where $f_{ESR} < f_{RES}$. Type-II compensation can be used but is not addressed in this document.

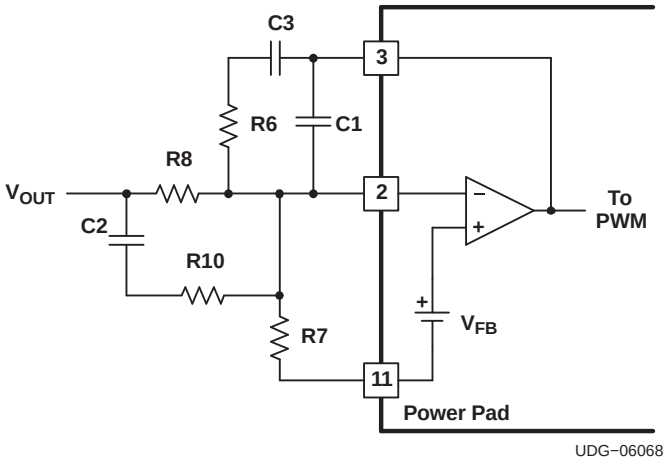


Figure 17. Type-III Compensator Used with TPS40040/41

Feedback Divider (R7, R8)

Select R8 to be between 10 kΩ and 100 kΩ. For this design, select 20 kΩ. R7 is then selected to produce the desired output voltage when V_{FB} = 0.591 V using Equation 30.

$$R7 = \frac{V_{FB} \times R8}{V_{OUT} - V_{FB}} \quad (30)$$

V_{FB} = 0.591 V and R8 = 20 kΩ for V_{OUT} = 1.8 V, R7 = 9.78 kΩ, so the value of 9.76 kΩ is selected as the closest standard value. A slightly lower nominal value increases the nominal output voltage slightly to compensate for some trace impedance at load.

Error Amplifier Compensation (R6, R10, C1, C2, C3)

Place two zeros at 50% and 100% of the resonance frequency to boost the phase margin before resonance frequency generates -180° of phase shift. For f_{RES} = 11.7 kHz, F_{Z1} = 5.8 kHz and F_{Z2} = 11 kHz. Selecting the crossover frequency (f_{CO}) of the control loop between 3 times the LC filter resonance and 1/5th the switching frequency. For most applications 1/10th the switching frequency provides a good balance between ease of design and fast transient response.

- If $f_{ESR} < f_{CO}$ $F_{P1} = f_{ESR}$ and $F_{P2} = 4 \times f_{CO}$.
- If $f_{ESR} > 2 \times f_{CO}$; $F_{P1} = f_{CO}$ and $F_{P2} = 8 \times f_{CO}$.

For this design

- f_{SW} = 600 kHz,
- f_{RES} = 11.7 kHz
- f_{ESR} = 636 kHz
- f_{CO} = 60 kHz and since
- $f_{ESR} > 2 \times f_{CO}$, $F_{P1} = f_{CO}$ = 60 kHz and $F_{P2} = 4 \times f_{CO}$ = 500 kHz.

Since $f_{CO} < f_{ESR}$ the power stage gain at the desired crossover can be approximated in Equation 31.

$$A_{PS(fco)} = A_{MOD(dc)} - 40 \times LOG\left(\frac{f_{CO}}{f_{RES}}\right) \quad (31)$$

$A_{PS(FCC)}$ = -5.4 dB, and the error amplifier gain between the poles should be should be $10^{5.4\ dB/20}$ = 1.86.

Table 5. Error Amplifier Design Parameters

PARAMETER	SYMBOL	VALUE	UNITS
First zero frequency	F_{Z1}	5.8	kHz
Second zero frequency	F_{Z2}	11.0	
First pole frequency	F_{P1}	60	
Second pole frequency	F_{P2}	500	
Midband gain	$A_{MID(band)}$	1.86	V/V

Approximate C2 with the formula described in Equation 32.

$$C2 = \frac{1}{2\pi \times R8 \times f_{Z2}} \quad (32)$$

C2 = 1000 pf (A standard capacitor value to calculated 723 pF) and approximate R6 with the formula described in Equation 33.

$$R10 = \frac{1}{2\pi \times C2 \times f_{P1}} \quad (33)$$

R10 = 2.61 kΩ (Closest standard resistor value to calculated 2.65 kΩ) Calculate R3 with Equation 34.

$$R6 = \frac{A_{MID(band)} \times (R10 \times R8)}{R10 + R8} \quad (34)$$

With $A_{MID(band)}$ = 1.86, R10 = 2.61 kΩ and R8 = 20 kΩ , R6 = 4.22 kΩ (Closest standard resistor value to calculated 4.29 kΩ).

Calculate C1 and C3 using Equation 35 and Equation 36.

$$C3 = \frac{1}{2\pi \times R6 \times f_{Z1}} \quad (35)$$

$$C1 = \frac{1}{2\pi \times R6 \times f_{P1}} \quad (36)$$

For R6 = 4.22kΩ , C1 = 100 pF (a standard value close to 75 pF) C3 = 1000 pF (the closest standard value to 7.5 nF) error amplifier straight line approximation transfer function is described in Figure 18.

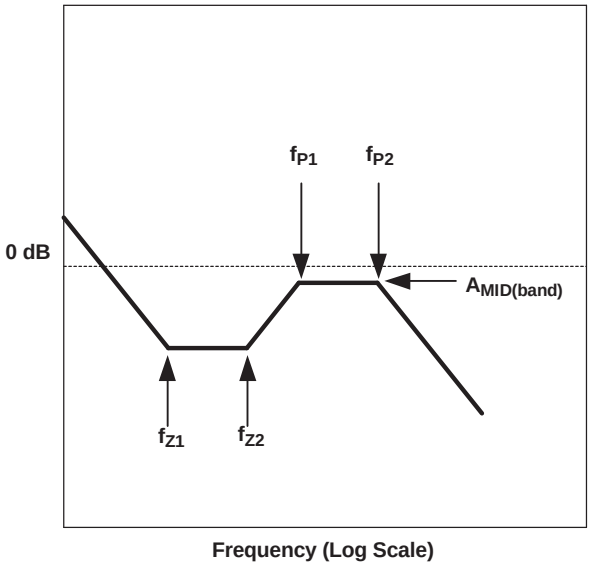


Figure 18. Error Amplifier Transfer Function Approximation

Bill of Materials

Table 6. Bill of Materials

QTY	RefDes	Value	Description	Size	Part Number	MFR
1	C1	100 pF	Capacitor, Ceramic, 10V, C0G, 10%	0603	STD	STD
1	C2	1000 pF	Capacitor, Ceramic, 10V, C0G, 10%	0603	STD	STD
1	C3	10 nF	Capacitor, Ceramic, 10V, C0G, 10%	0603	STD	STD
1	C4	1.0 µF	Capacitor, Ceramic, 25V, X5R, 20%	0805	STD	STD
1	C5	4.7 µF	Capacitor, Ceramic, 10V, X5R, 20%	0805	STD	STD
1	C6	470 nF	Capacitor, Ceramic, 10V, X5R, 20%	0603	Std	Std
2	C7	10 µF	Capacitor, Ceramic, 25V, X5R, 20%	1210	C3225X7R1E106M	TDK
2	C8	100 µF	Capacitor, Ceramic, 6.3V, X5R, 20%	1210	C3225X5R0J107M	TDK
1	C11	1.0 µF	Capacitor, Ceramic, 6.3V, X5R, 20%	0603	STD	STD
1	L1	1.0 µH	Inductor, SMT, 1.0-µF, 6.6 mΩ, 12 A / 17 A	0.268 x 0.268 inch	PG0083.102	Pulse
1	Q1	2N7002W	Mosfet, N-Ch, V_{DS} 60 V, $R_{DS(on)}$ 2 Ω, I_{DD} 115 mA	SOT-323 (SC-70)	2N7002W-7	Diodes Inc
1	Q2	IRF7466	Transistor, MOSFET, N-channel, 30 V, $R_{DS(on)}$ 17 mΩ, 9 A	SO8	IRF7466	IR
1	Q3	IRF7834	Transistor, MOSFET, N-channel, 30 V, $R_{DS(on)}$ 5.5 mΩ, 9 A	SO8	IRF7834	IR
1	R1	5.1 kΩ	Resistor, Chip, 1/16W, 5%	0603	Std	Std
1	R2	2 kΩ	Resistor, Chip, 1/16W, 5%	0603	Std	Std
1	R4	100 kΩ	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	R6	4.22 kΩ	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	R7	9.76 kΩ	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	R8	20 kΩ	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	R9	3.9 kΩ	Resistor, Chip, 1/16W, 5%	0603	Std	Std
1	R10	2.61 kΩ	Resistor, Chip, 1/16W, 1%	0603	Std	Std
2	R11, R13	0	Resistor, Chip, 1/16W, 5%	0603	Std	Std
1	R12	100 kΩ	Resistor, Chip, 1/16W, 5%	0603	Std	Std
1	U1	TPS40192DRC	Cost Optimized Midrange Input Votlage High-Frequancy Synchronous Buck Controller	DRC10	TPS40192DRC	TI

DEFINITION OF SYMBOLS

Table 7. Definition of Symbols

SYMBOL	DESCRIPTION
$V_{IN(max)}$	Maximum Operating Input Voltage
$V_{IN(min)}$	Minimum Operating Input Voltage
$V_{IN(ripple)}$	Peak to Peak AC ripple voltage on V_{IN}
V_{OUT}	Target Output Voltage
$V_{OUT(ripple)}$	Peak to Peak AC ripple voltage on V_{OUT}
$I_{OUT(max)}$	Maximum Operating Load Current
I_{RIPPLE}	Peak-to-Peak ripple current through Inductor
$I_{L(peak)}$	Peak Current through Inductor
$I_{L(rms)}$	Root Mean Squared Current through Inductor
$I_{RMS(Cin)}$	Root Mean Squared Current through Input Capacitor
f_{SW}	Switching Frequency
f_{CO}	Desired Control Loop Crossover frequency
A_{MOD}	Low Frequency Gain of the PWM Modulator (V_{OUT} / $V_{CONTROL}$)
$V_{CONTROL}$	PWM Control Voltage (Error Amplifier Output Voltage V_{COMP})
f_{RES}	L-C Filter Resonant Frequency
f_{ESR}	Output Capacitors' ESR zero Frequency
F_{P1}	First Pole Frequency in Error Amplifier Compensation
F_{P2}	Second Pole Frequency in Error Amplifier Compensation
F_{Z1}	First Zero Frequency in Error Amplifier Compensation
F_{Z2}	Second Pole Frequency in Error Amplifier Compensation
Q_{G1}	Total Gate Charge of Main MOSFET
Q_{G2}	Total Gate Charge of SR MOSFET
$R_{DS(on)Q1}$	"ON" Drain to Source Resistance of Main MOSFET
$R_{DS(on)Q2}$	"ON" Drain to Source Resistance of SR MOSEFT
$P_{Q1C(on)}$	Conduction Losses in Main Switching MOSFET
P_{Q1SW}	Switching Losses in Main Switching MOSFET
$P_{Q2C(on)}$	Conduction Losses in Synchronous Rectifier MOSFET
Q_{GD}	Gate to Drain Charge of Synchronous Rectifier MOSFET
Q_{GS}	Gate to Source Charge of Synchronous Rectifier MOSFET

ADDITIONAL REFERENCES

Related Parts

The following parts have characteristics similar to the TPS40192/3 and may be of interest.

Related Parts

DEVICE	DESCRIPTION
TPS40100	Midrange Input Synchronous Controller with Advanced Sequencing and Output Margining
TPS40075	Wide Input Synchronous Controller with Voltage Feed Forward
TPS40190	Low Pin Count Synchronous Buck Controller

References

These references may be found on the web at www.power.ti.com under Technical Documents. Many design tools and links to additional references, including design software, may also be found at www.power.ti.com

1. *Under The Hood Of Low Voltage DC/DC Converters*, SEM1500 Topdevice 5, 2002 Seminar Series
2. *Understanding Buck Power Stages in Switchmode Power Supplies*, SLVA057, March 1999
3. *Design and Application Guide for High Speed MOSFET Gate Drive Circuits*, SEM 1400, 2001 Seminar Series
4. *Designing Stable Control Loops*, SEM 1400, 2001 Seminar Series
5. Additional PowerPAD™ information may be found in Applications Briefs SLMA002 and SLMA004
6. QFN/SON PCB Attachment, Texas Instruments Literature Number SLUA271, June 2002

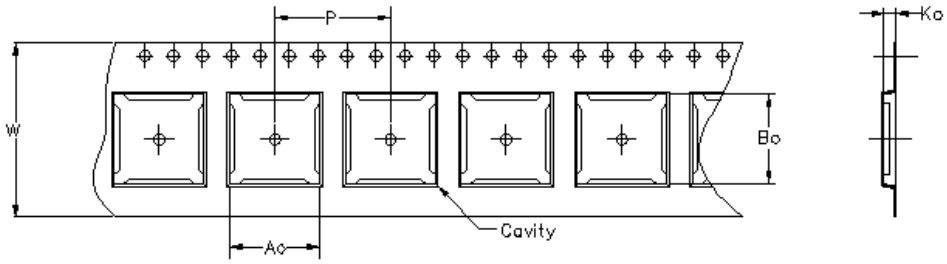
PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
TPS40192DRCR	ACTIVE	SON	DRC	10	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS40192DRCRG4	ACTIVE	SON	DRC	10	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS40192DRCT	ACTIVE	SON	DRC	10	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS40192DRCTG4	ACTIVE	SON	DRC	10	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS40193DRCR	ACTIVE	SON	DRC	10	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS40193DRCRG4	ACTIVE	SON	DRC	10	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS40193DRCT	ACTIVE	SON	DRC	10	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS40193DRCTG4	ACTIVE	SON	DRC	10	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

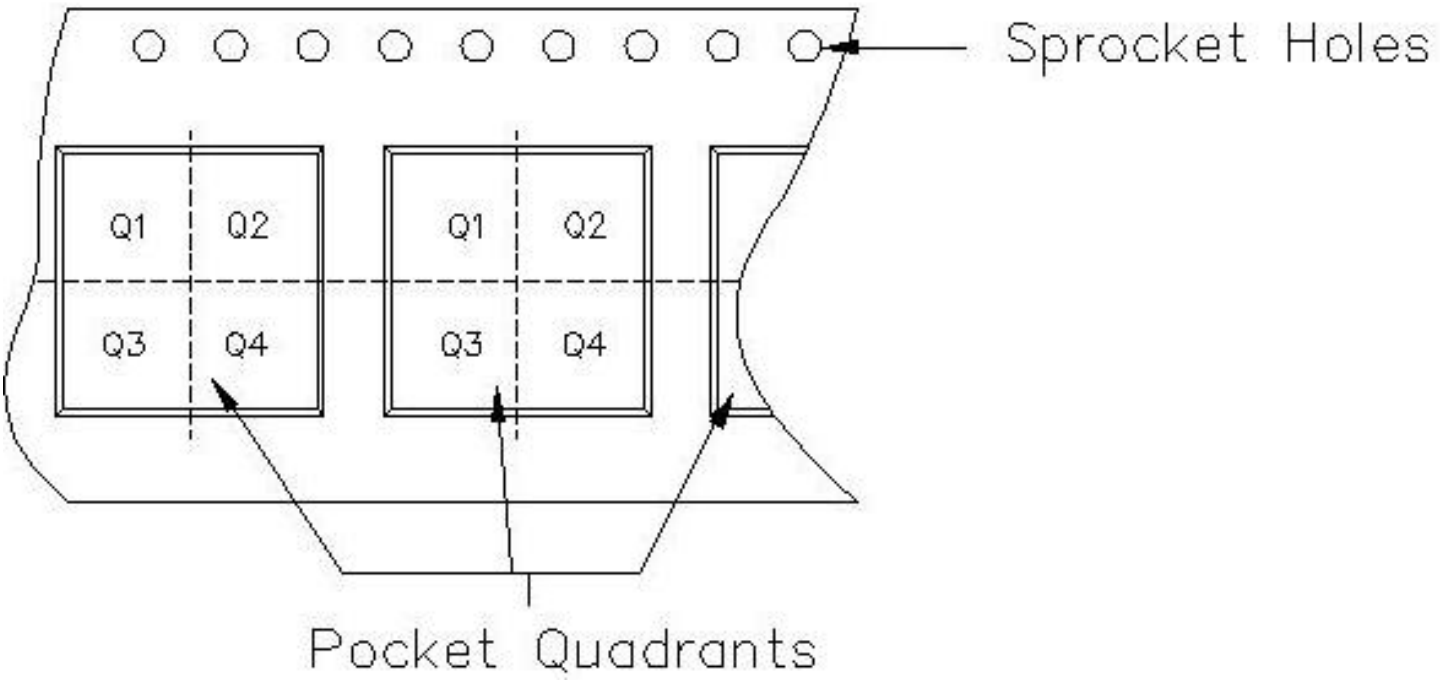
(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.



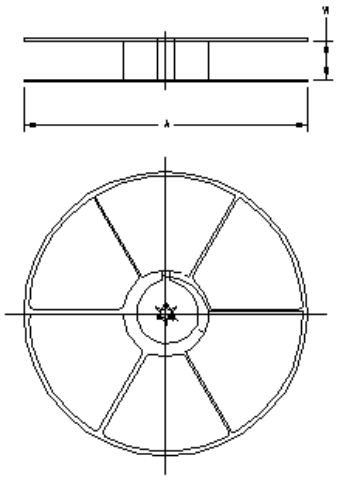
Carrier tape design is defined largely by the component lentgh, width, and thickness.

Ao = Dimension designed to accommodate the component width.
Bo = Dimension designed to accommodate the component length.
Ko = Dimension designed to accommodate the component thickness.
W = Overall width of the carrier tape.
P = Pitch between successive cavity centers.



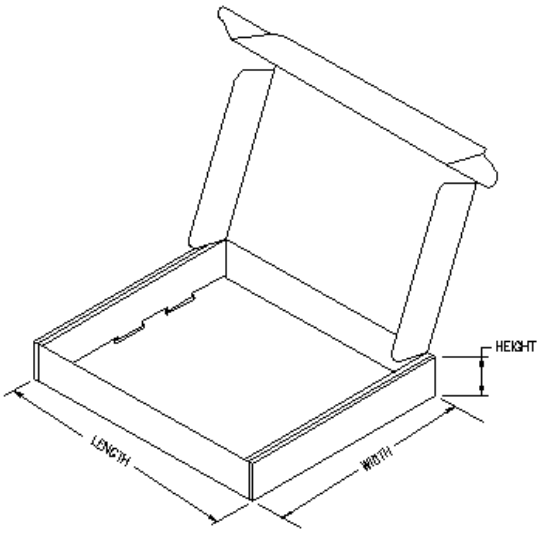
TAPE AND REEL INFORMATION

Device	Package	Pins	Site	Reel Diameter (mm)	Reel Width (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS40192DRCR	DRC	10	MLA	330	12	3.3	3.3	1.1	8	12	Q2
TPS40192DRCT	DRC	10	MLA	180	12	3.3	3.3	1.1	8	12	Q2
TPS40193DRCR	DRC	10	MLA	330	12	3.3	3.3	1.1	8	12	Q2
TPS40193DRCT	DRC	10	MLA	180	12	3.3	3.3	1.1	8	12	Q2

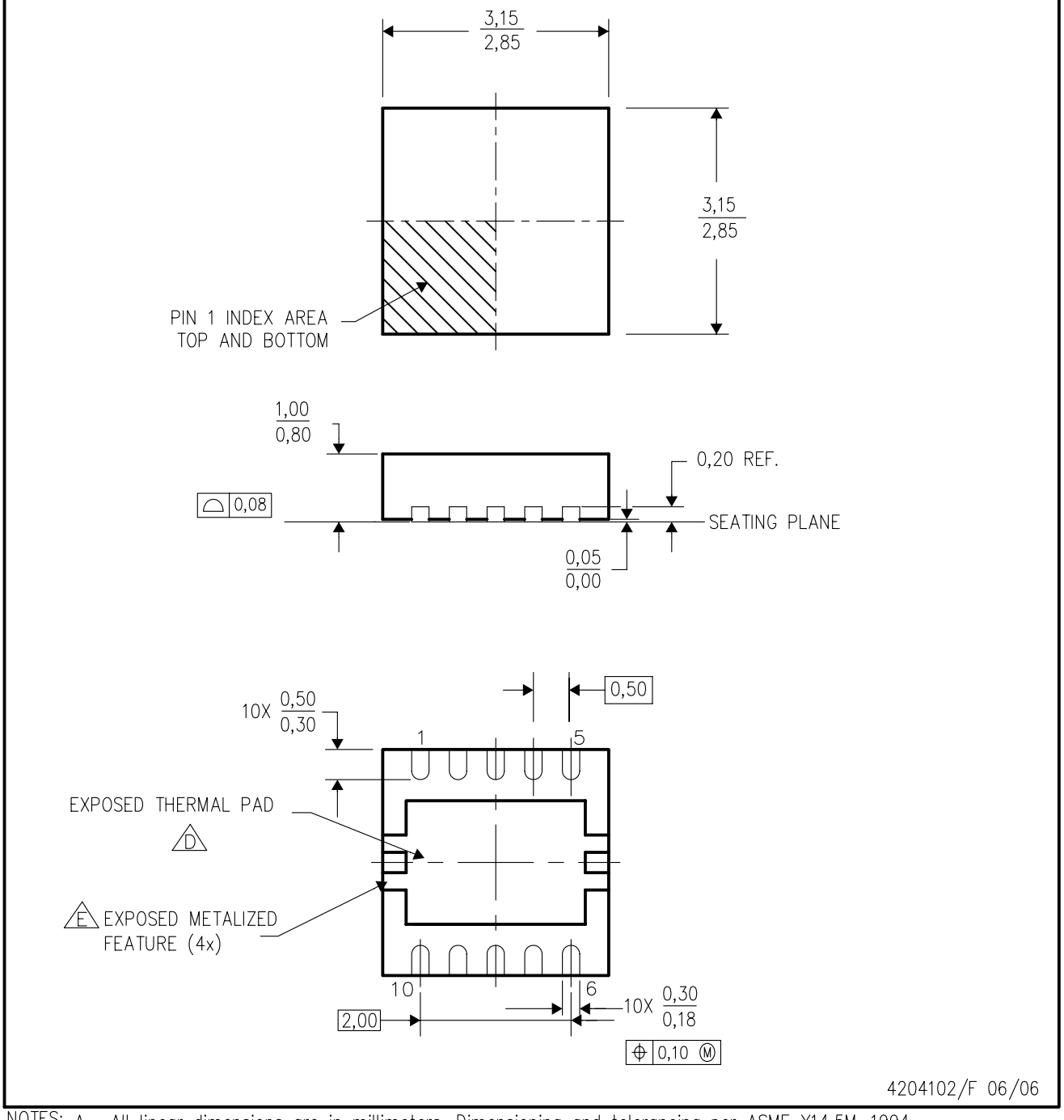


TAPE AND REEL BOX INFORMATION

Device	Package	Pins	Site	Length (mm)	Width (mm)	Height (mm)
TPS40192DRCR	DRC	10	MLA	346.0	346.0	29.0
TPS40192DRCT	DRC	10	MLA	190.0	212.7	31.75
TPS40193DRCR	DRC	10	MLA	346.0	346.0	29.0
TPS40193DRCT	DRC	10	MLA	190.0	212.7	31.75


HEIGHT
LENGTH
WIDTH

DRC (S–PDSO–N10) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Small Outline No–Lead (SON) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
E. Metalized features are supplier options and may not be on the package.

THERMAL PAD MECHANICAL DATA

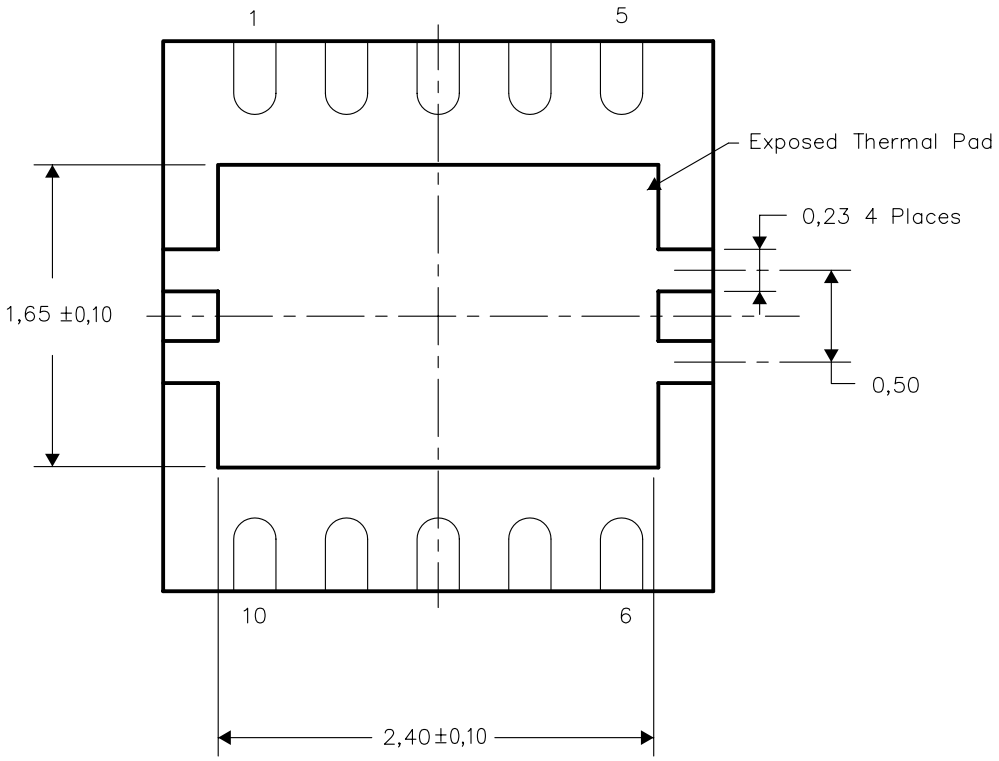
DRC (S–PDSO–N10)

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to a ground or power plane (whichever is applicable), or alternatively, a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, Quad Flatpack No–Lead Logic Packages, Texas Instruments Literature No. SCBA017. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

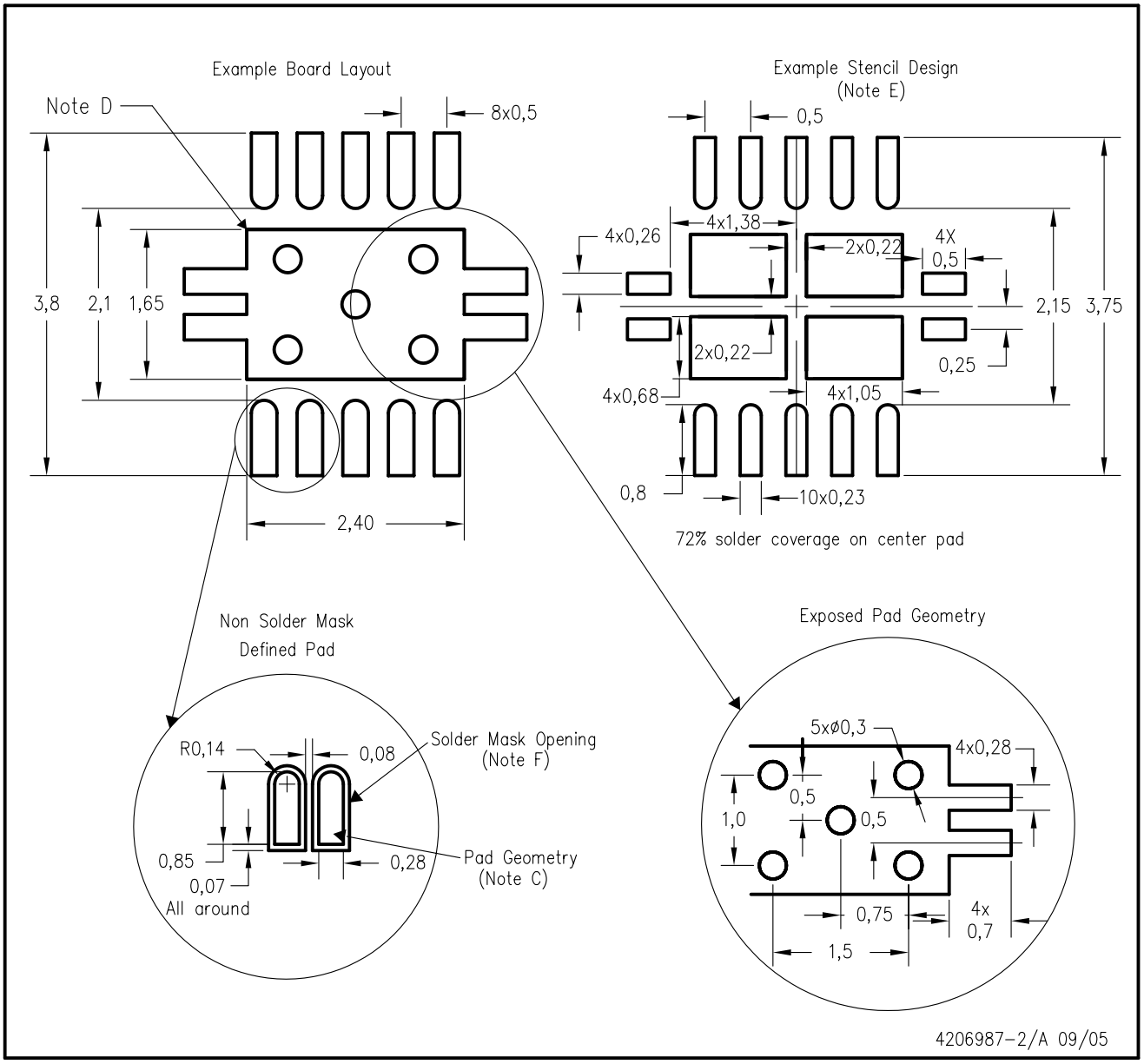


Bottom View

NOTE: All linear dimensions are in millimeters

Exposed Thermal Pad Dimensions

DRC (S–PDSO–N10)



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SCBA017, SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

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