QUARTZ CRYSTAL OSCILLATOR

■ GENERAL DESCRIPTION

The NJU6319 series is a C-MOS quartz crystal oscillator which contains of an oscillation amplifier, 3-stage divider and 3-state output buffer.

The oscillation frequency is as wide as up to 50MHz and the symmetry of 45-55% is realized over full oscillation frequency range.

The oscillation amplifier incorporates feed-back resistance and oscillation capacitors (Cg, Cd), therefore, it requires no external component expect quartz crystal and operating voltage is correspondence of 3V.

The 3-stage divider generates f_o, $f_o/2$, $f_o/4$ and $f_o/8$ and only one frequency selected by internal circuits is output.

The 3-state output buffer is C-MOS compatible and capable of 10 LSTTL driving.

■ PACKAGE OUTLINE




NJU6319XC NJU6319XE



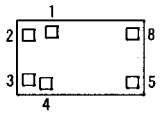
NJU6319XR

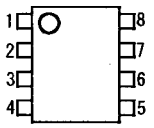
■ FEATURES

- Operating Voltage -- 2.7~6.0V
- Maximum Oscillation Frequency -- 50MHz
- Low Operating Current
- High Fan-out -- LSTTL 10
- 3-state Output Buffer
- Selected Frequency Output (mask option)
  Only one frequency out of f_o, $f_o/2$, $f_o/4$ and $f_o/8$ output
- Oscillation Capacitors Cg and Cd on-chip
- Oscillation Output Stand-by Function
- Package Outline -- Chip/EMP/VSP 8
- C-MOS Technology

■ PAD LOCATION/PIN CONFIGURATION

Chip EMP/VSP8





■ LINE-UP TABLE

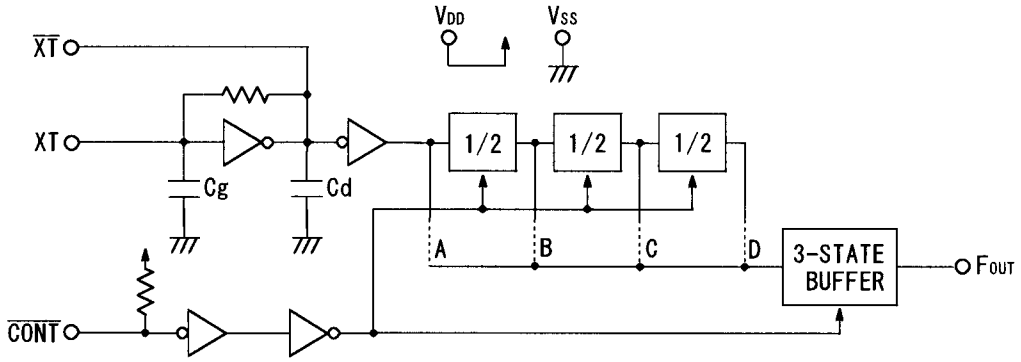
Type No.	Output Frequency	Cg	Cd
NJU6319A	f_o	23pF	23pF
NJU6319B	$f_o/2$	23pF	23pF
NJU6319C	$f_o/4$	23pF	23pF
NJU6319D	$f_o/8$	23pF	23pF
NJU6319P	f_o	No	No

■ COORDINATES Unit:um

No.	PAD	X	Y
1	$\overline{CONT}$	350	655
2	XT	130	630
3	$\overline{XT}$	140	175
4	V_{SS}	300	130
5	F_{OUT}	1185	145
6	NC	-	-
7	NC	-	-
8	V_{DD}	1185	650

Chip Size : 1.33 X 0.8mm
Chip Thickness : 400±30um
Note1) No.6 and 7 terminals are only for package type information. There are no PAD on the chip.

■ BLOCK DIAGRAM



■ TERMINAL DESCRIPTION

No.	SYMBOL	F U N C T I O N
1	$\overline{CONT}$	3-State Output Control and Divider Reset $\overline{CONT}$ / F_{OUT} H or Open: Output either one frequency from f_o, $f_o/2$, $f_o/4$ and $f_o/8$ (Note2) L: Output High Impedance and Divider Reset
2 3	XT $\overline{XT}$	Quartz Crystal Connecting terminals
4	V_{SS}	GND
5	F_{OUT}	Output either one frequency from f_o, $f_o/2$, $f_o/4$ and $f_o/8$
8	V_{DD}	+3V/+5V

Note2) Refer to Line-Up Table.

■ ABSOLUTE MAXIMUM RATINGS

(Ta=25°C)

P A R A M E T E R	SYMBOL	R A T I N G S	UNIT
Supply Voltage	V_{DD}	-0.5 ~ +7.0	V
Input Voltage	V_{IN}	V_{SS}-0.5 ~ V_{DD}+0.5	V
Output Voltage	V_O	-0.5 ~ V_{DD}+0.5	V
Input Current	I_{IN}	±10	mA
Output Current	I_O	±25	mA
Power Dissipation	P_D	200 (EMP) 320 (VSP)	mW
Operating Temperature Range	Topr	-40 ~ + 85	°C
Storage Temperature Range	Tstg	-65 ~ +150	°C

Note) Decoupling capacitor should be connected between V_{DD} and V_{SS} due to the stabilized operation for the circuit.

■ ELECTRICAL CHARACTERISTICS

(Ta=25°C)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Operating Voltage	V_{DD}		2.7		6.0	V

(V_{DD}=3V, Ta=25°C)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Operating Current	I_{DD}	fosc=16MHz, No load Note3			8	mA
Stand-by Current	Ist	$\overline{CONT}$, XT=V_{SS}, No load Note4			1	uA
Input Voltage	V_{IH}		2.7		3.0	V
	V_{IL}		0		0.3	
Output Current	I_{OH}	V_{OH}=2.7V	1			mA
	I_{OL}	V_{OL}=0.3V	1			
Input Current	I_{IN}	$\overline{CONT}$=V_{SS}			400	uA
3-st. Offleakage Current	I_{OZ}	$\overline{CONT}$=V_{SS}, F_{OUT}=V_{DD} or V_{SS}			±0.1	uA
Internal Capacitor	Cg, Cd	Note5		23		pF
Max. Oscillation Freq.	f_{MAX}	Note3	50			MHz
Output Signal Symmetry	SYM	C_L=15pF at 1/2V_{DD}	45	50	55	%
Output Signal Rise Time	t_r	C_L=15pF, 20%-80%			8	ns
Output Signal Fall Time	t_f	C_L=15pF, 80%-20%			8	ns

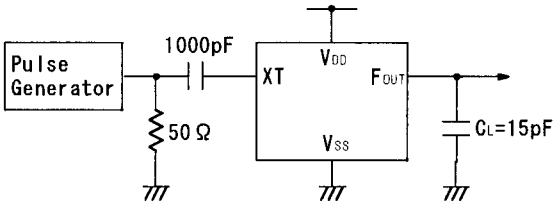
(V_{DD}=5V, Ta=25°C)

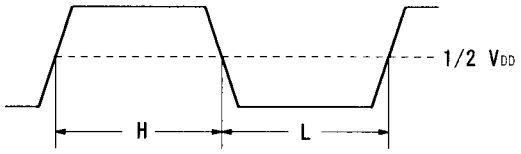
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Operating Current	I_{DD}	fosc=16MHz, No load Note3			15	mA
Stand-by Current	Ist	$\overline{CONT}$=XT=V_{SS}, No load Note4			1	uA
Input Voltage	V_{IH}		2.0		5.0	V
	V_{IL}		0		0.8	
Output Current	I_{OH}	V_{OH}=4.5V	4			mA
	I_{OL}	V_{OL}=0.5V	4			
Input Current	I_{IN}	$\overline{CONT}$=V_{SS}			400	uA
3-st. Offleakage Current	I_{OZ}	$\overline{CONT}$=V_{SS}, F_{OUT}=V_{DD} or V_{SS}			±0.1	uA
Internal Capacitor	Cg, Cd	Note5		23		pF
Max. Oscillation Freq.	f_{MAX}	Note3	50			MHz
Output Signal Symmetry	SYM	C_L=15pF at 1/2V_{DD}	45	50	55	%
Output Signal Rise Time	t_r	C_L=15pF, 20% - 80%			8	ns
Output Signal Fall Time	t_f	C_L=15pF, 80% - 20%			8	ns

Note3) Only P version is measured with external capacitors contained 18pF for Cg and 16pF for Cd.
Note4) Excluding input current on $\overline{CONT}$ terminal.
Note5) P version is not mentioned due to internal oscillation capacitors Cg and Cd separated.

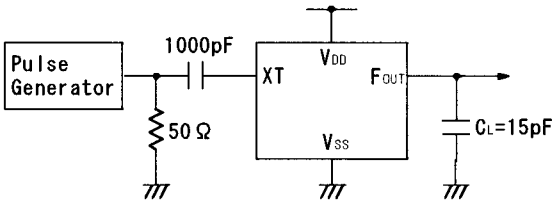
■ MEASUREMENT CIRCUITS

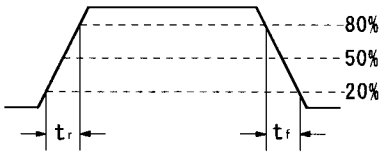
(1) Output Signal Symmetry (C_L=15pF)





(2) Output Signal Rise/Fall Time (C_L=15pF)





MEMO

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