DATA SHEET

Generalplus

GPCD9002A

Multi-Channel Sound Controller

Apr. 11, 2017

Version 1.2

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MULTI-CHANNEL SOUND CONTROLLER

1.GENERAL DESCRIPTION

GPCD9002A is ROMless and workable up to 4M bytes external ROM, 512 bytes working SRAM, three sets of 12-bit timers, 32 general I/Os, one 10-bit ADC with 8 channels input and one 14-bit DAC with push-pull amplifier. The microprocessor can implement software based on audio processing, function control and others. For audio processing, melody and speech can be mixed into one output. GPCD9002A is implemented with a high performance SPU voice engine to play maximum 8-channel voice with ADPCM/PCM data. It operates over a wide voltage range of 2.4V - 5.5V and includes Low Voltage Reset function. In addition, GPCD9002A provides sleep mode for power savings. It can be awaked from sleep mode by interrupt sources or by IO's state change. There is a Serial Peripheral Interface (SPI) controller built-in GPCD9002A to facilitate communicating with other devices and components.

2.FEATURES

- Working Voltage: 2.4V - 5.5V
- CPU speed: Max. 8MHz.
- F_{OSC} = Max. 16MHz (2 x CPU clock)
- External ROM Max. 4M bytes
- RAM size: Max. 512 bytes
- Three 12-bit timer/counter, TMA with capture and comparison function, TMB/TMC with comparison function (Programmable and auto reload)
- Sleep mode to reduce power
- Key change wakeup function
- 16 IRQs & 7 NMI interrupts
- Watchdog function
- 5.5V to 3.3V regulator

- Low Voltage Reset and Low Voltage Detection
- 32 general I/Os (bit programmable)
- 8 I/O with high sink current for LED application
- All IOs with 1M pull low function to prevent current leakage from error key touch
- One 14-bit DAC with push-pull amplifier for direct drive speaker
- SPU (Sound Processing Unit) engine can output audio data with 14-bit resolution to perform high quality voice/melody
- IR PWM Output
- Hardware PWMIO supports 4 LED outputs(IOB[3:0]) with brightness control of 256-level
- Real-time clock
- 8-channel SPU engine with ADPCM/PCM wave table
- Two sets of 14-bit software channel with noise filter to play high quality sound.
- Generalplus ICE_CORE embedded, new Application can be developed using G+Midiar® Development tools
- Interface to speed up flash program and read
- Tone color (Speech) with ADPCM algorithm to save memory usage
- 10-bit ADC with 8 channels line-in
- SPI master interface

3.APPLICATION FIELD

- Talking instrument controller
- General music synthesizer
- General purpose controller
- High end toy controller
- Intelligent education toys
- And more

4.BLOCK DIAGRAM
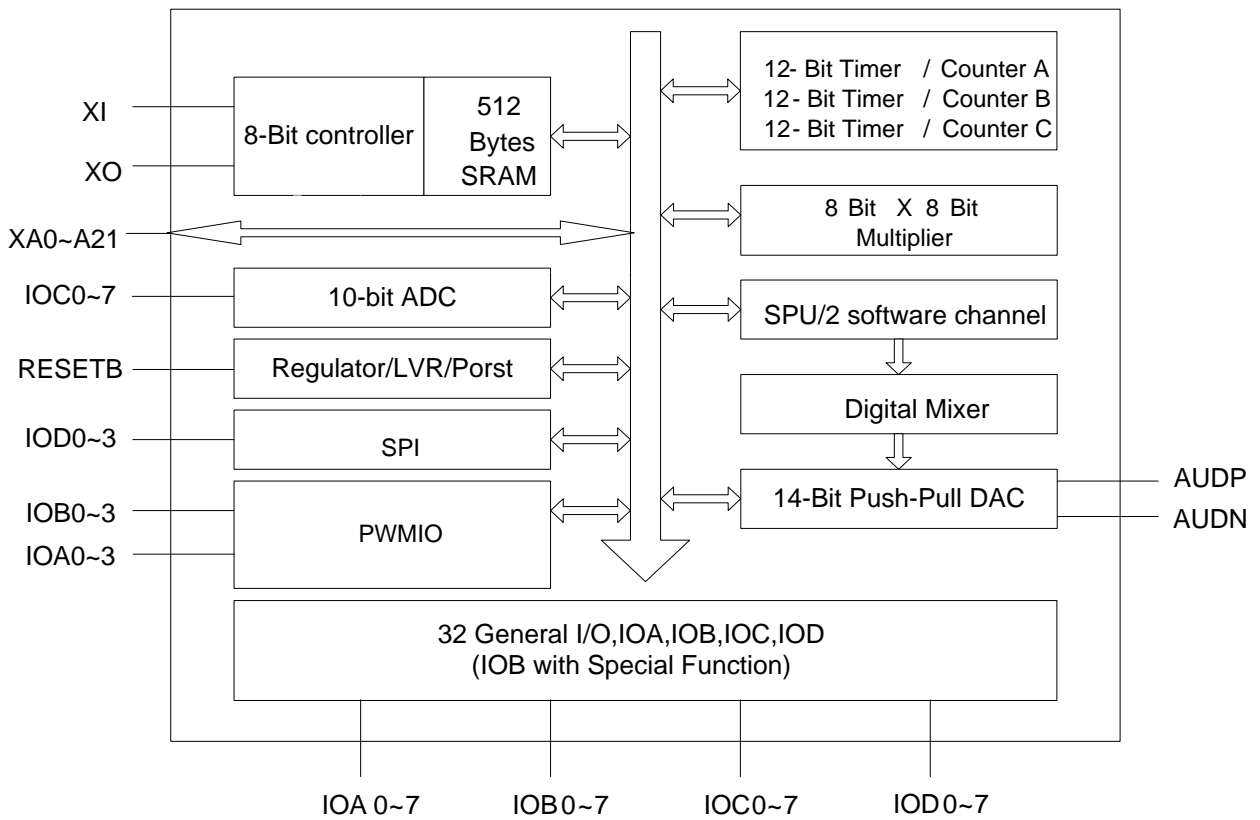
5. SIGNAL DESCRIPTION

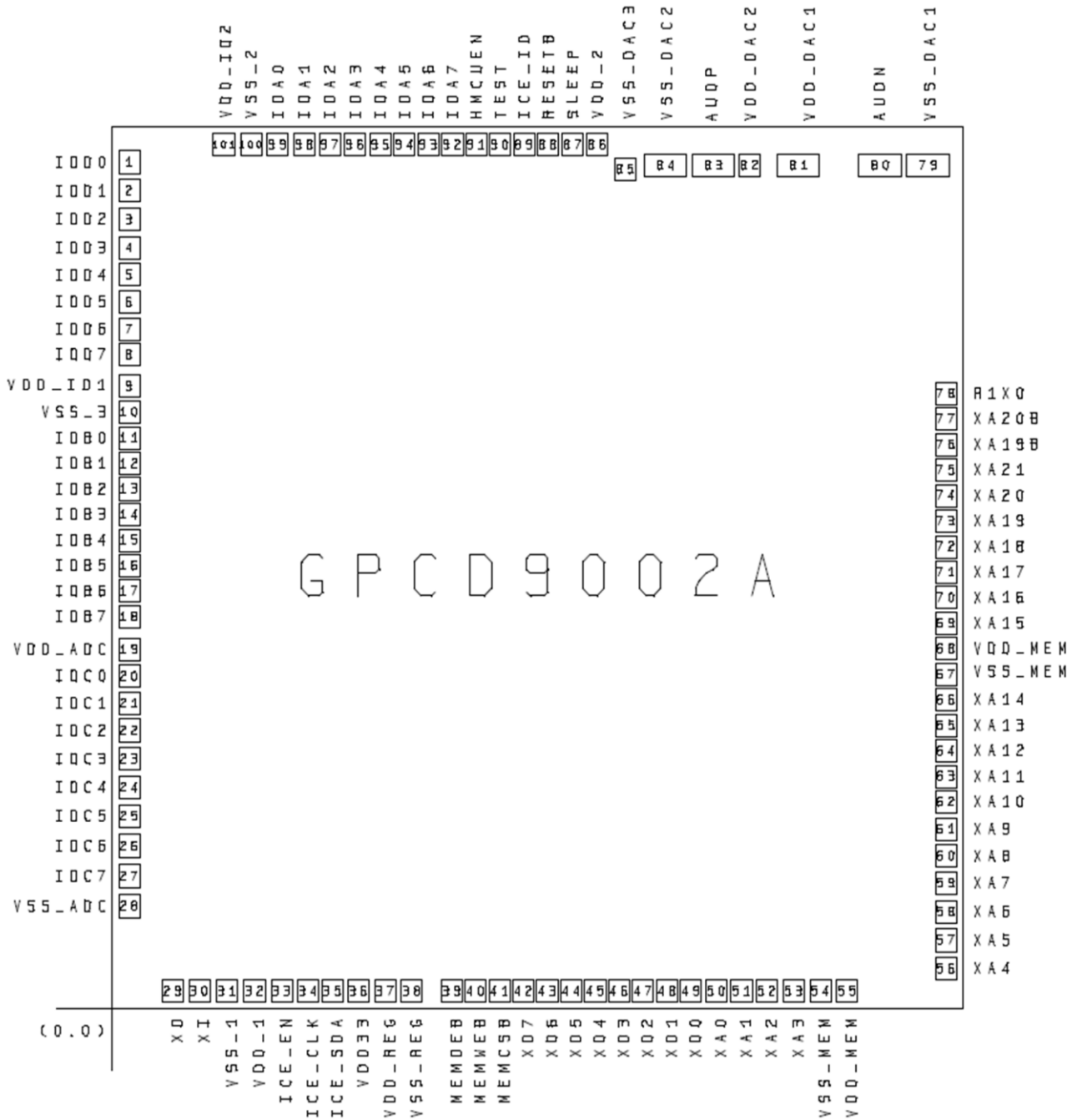| Name	Pin No.	LQFP 128Pin No.	Type	Description	Power Domain	Note
IO PORT						
IOA0~IOA7	99~92	92~85	I/O	Bi-directional IO ports, can be wakeup pins	VDD_IO1	
IOB0~IOB7	11~18	109~116	I/O	Bi-directional IO ports, can be wakeup pins	VDD_IO2	
IOC0~IOC7	20~27	118~125	I/O	Bi-directional IO ports, can be wakeup pins	VDD_ADC	
IOD0~IOD7	1~8	99~106	I/O	Bi-directional IO ports, can be wakeup pins	VDD_IO1	
ROM/OTP Address & Data Bus Interface						
XA0~XA21, XA19B~XA20B	50~53, 56~66, 69~77	24~27, 35~45, 48~56	O	Address of 4M byte external ROM(XA19B and XA20B are the reverse state of XA19 and XA20)	VDD_MEM	
XD0~XD7	49~42	23~16	I/O	Data bus of 4M byte external ROM	VDD_MEM	
MEMCSB	41	15	O	Memory chip select enable(active low)	VDD_MEM	
MEMWEB	40	14	O	Memory write enable(active low)	VDD_MEM	
MEMOEB	39	13	O	Memory output enable(active low)	VDD_MEM	
ICE Related						
ICE_EN	33	7	I	ICE enable	VDD33	Pull-low
ICE_CLK	34	8	I	ICE clock	VDD33	Pull-low
ICE_SDA	35	9	I/O	ICE serial data bus	VDD33	
Clock Related						
XO	29	3	O	Oscillator Crystal output	VDD33	
XI	30	4	I	Oscillator crystal input./R_{OSC} input	VDD33	Floating
POWER PAD						
VDD_ADC	19	117	P	Positive supply for ADC/IOC (2.4V~5.5V)	-	
VDD_REG	37	11	P	Positive supply for regulator (2.4V~5.5V)	-	
VDD_MEM	55, 68	29, 47	P	Positive supply for memory AD bus and its control pin (2.4V~5.5V)	-	X2
VDD_DAC1	81	73	P	Positive supply for amplifier (2.4V~5.5V)	-	
VDD_DAC2	82	74	P	Positive supply for DAC (2.4~5.5V)	-	
VDD_IO2	101	94	P	Positive supply for IOA/IOD (2.4V~5.5V)	-	
VDD_IO1	9	107	P	Positive supply for IOB (2.4V~5.5V)	-	
VDD_1~2	32, 86	6, 79	P	Core power from regulator and strongly recommended connect to VDD33 via PCB	-	X2
VDD33	36	10	O	Core power output from regulator	-	
VSS_REG	38	12	G	Ground reference for regulator	-	
VSS_MEM	54, 67	28, 46	G	Ground reference for memory	-	X2
VSS_1~3	31, 100, 10	5, 93, 108	G	Ground reference for IOA/IOB/IOC, ICE, core etc.	-	X3
VSS_ADC	28	126	G	Ground reference for ADC	-	
VSS_DAC1~2	79, 84	69, 77	G	Ground reference for amplifier	-	X2

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Name	Pin No.	LQFP 128Pin No.	Type	Description	Power Domain	Note
VSS_DAC3	85	78	G	Ground reference for DAC	-	
Others						
ICE_ID	89	82	I	ICE ID for flash identification	VDD_IO1	Pull-low
R1X0	78	57	I	ROSC/XTAL selection pin.	VDD_MEM	Floating
HMCUEN	91	84	I	Select HARDMACRO 6502(1) or RTL 6502 (0)	VDD_IO1	Pull-high
RESETB	88	81	I	External reset pin(active low)	VDD_IO1	Pull-high
TEST	90	83	I	For test mode, NC for normal application.	VDD_IO1	Pull-low
AUDP	83	75	O	Audio output of push pull DAC	-	
AUDN	80	71	O	Audio output of push pull DAC	-	
SLEEP	87	80	O	Sleep indicator	VDD_IO1	

Total 101 pads

5.1. PAD Assignment

The IC substrate should be floating or connected to VSS.

Top pins (left to right): VDD_IO2 (101), VSS_2 (100), IOA0 (99), IOA1 (98), IOA2 (97), IOA3 (96), IOA4 (95), IOA5 (94), IOA6 (93), IOA7 (92), HMCUEN (91), TEST (90), ICE_ID (89), RESETB (88), SLEEP (87), VDD_2 (86), VSS_DAC3 (85), VSS_DAC2 (84), AUOP (83), VDD_DAC2 (82), VDD_DAC1 (81), AUDN (80), VSS_DAC1 (79)

Left pins (top to bottom):
IOD0 1
IOD1 2
IOD2 3
IOD3 4
IOD4 5
IOD5 6
IOD6 7
IOD7 8
VDD_ID1 9
VSS_3 10
IOB0 11
IOB1 12
IOB2 13
IOB3 14
IOB4 15
IOB5 16
IOB6 17
IOB7 18
VDD_ADC 19
IOC0 20
IOC1 21
IOC2 22
IOC3 23
IOC4 24
IOC5 25
IOC6 26
IOC7 27
VSS_ADC 28

Right pins (top to bottom):
78 R1X0
77 XA20B
76 XA19B
75 XA21
74 XA20
73 XA19
72 XA18
71 XA17
70 XA16
69 XA15
68 VDD_MEM
67 VSS_MEM
66 XA14
65 XA13
64 XA12
63 XA11
62 XA10
61 XA9
60 XA8
59 XA7
58 XA6
57 XA5
56 XA4

(0.0)

Bottom pins (left to right): XO (29), XI (30), VSS_1 (31), VDD_1 (32), ICE_EN (33), ICE_CLK (34), ICE_SDA (35), VDD3 (36), VDD_REG (37), VSS_REG (38), MEMOEB (39), MEMWEB (40), MEMCSB (41), XD7 (42), XD6 (43), XD5 (44), XD4 (45), XD3 (46), XD2 (47), XD1 (48), XD0 (49), XA0 (50), XA1 (51), XA2 (52), XA3 (53), VSS_MEM (54), VDD_MEM (55)

5.2. Pin Map – LQFP 128

GPCD9002A
LQFP 128

6. FUNCTIONAL DESCRIPTIONS

6.1. SRAM

The 512-byte SRAM (including Stack) area is located in $000000~$0002FF.

6.2. ROM

GPCD9002A can be selected external ROM with maximum 4M bytes.

6.3. Low Voltage Reset

GPCD9002A provides another important feature, Low Voltage Reset (LVR). With the LVR function, a reset signal is generated to reset system when the operating voltage drops under LVR. Without LVR, the CPU becomes unstable and abnormal when working voltage is too low.

6.4. Interrupt

GPCD9002A has two interrupt (INT) modes: IRQ (interrupt Request) and NMI (Non-Mask Interrupt Request). The interrupt controller controls 16 IRQs and 7 NMIs. A NMI cannot be interrupted by any other IRQs.

Interrupt Source	Interrupt Name	Priority
Timer A	NMI_TIMER_A	NMI
Timer B	NMI_TIMER_B	NMI
Timer C	NMI_TIMER_C	NMI
CPU_CLOCK/1024	NMI_D1024	NMI
CPU_CLOCK/4096	NMI_D4096	NMI
KEY	NMI_KEY	NMI
EXT	NMI_EXT	NMI
TIMER A	IRQ_TIMER_A	IRQ1
TIMER B	IRQ_TIMER_B	IRQ2
TIMER C	IRQ_TIMER_C	IRQ3
CPU_CLOCK/1024	IRQ_D1024	IRQ4
CPU_CLOCK/4096	IRQ_D4096	IRQ5
16 Hz	IRQ_16Hz	IRQ6
2 Hz	IRQ_2 Hz	IRQ7
KEY	IRQ_KEY	IRQ8
EXT	IRQ_EXT	IRQ9
SPU	IRQ_SPU	IRQ10
SPI	IRQ_SPI	IRQ11
ADC	IRQ_ADC	IRQ12
QD1_F	IRQ_QD1_F	IRQ13
QD1_B	IRQ_QD1_B	IRQ14
QD2_F	IRQ_QD2_F	IRQ15
QD2_B	IRQ_QD2_B	IRQ16

6.5. Hardware PWMIO

Hardware PWMIO supports 4 LED outputs (IOB[3:0]) with 256-level brightness control. The clock source of PWMIO can be selected by user's request.

6.6. I/O

The purpose of input and output ports is to communicate with other devices. Four programmable I/O ports are built-in, including Port A, B, C, and D. All Ports are general I/O with programmable wake-up capability and 1M pull low function. In addition to general I/O function, PortB also provides some special functions in certain pins. The PortA0 ~ 3 and PortB0 ~ 3 feature large sink current for LED application. The Port C and Port D are sharing other module's function such as ADC, SPI etc. Refer to following figure for *IO Sharing*.

6.6.1. I/O Configuration

The following diagram represents the I/O schematic.

I/O A, B, C, D Schematic:
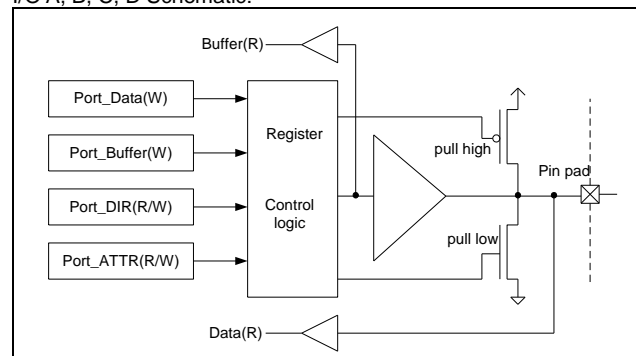
Port_Data and Port_Buffer are written into the same register but read from different nodes. To activate key wakeup function, first latch data on IOX_Data and enable the key wakeup function. Wakeup is triggered when the port's state is different from the first latched data.

A summary of IO sharing is listed as follows.

IO Sharing

	IOA								IOB							
	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Auto Wake up								V								
Wake up	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V
High Sink					V	V	V	V					V	V	V	V
PWMIO													V	V	V	V
IR(Output)									V							
External INT										V						
External Clock		V(TMC)	V(TMB)	V(TMA)												
RTC											V	V				
IIS Out/In	V(in)	V(in)	V(in)			V(out)	V(out)	V(out)								
QD					V(qd2)	V(qd2)	V(qd1)	V(qd1)								
CC		TMC	TMB	TMA						TMC	TMB	TMA				
1M Pull Low	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V

Note: QD means quadrature decoder; CC means Capture/Comparison.

	IOC								IOD							
	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Wake up	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V
ADC	V	V	V	V	V	V	V	V								
SPI													V(rx)	V(tx)	V(ck)	V(cs)
1M pull low	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V

6.7. Timer/Counter (Timer A/Timer B/Timer C)

Three 12-bit timers are embedded in GPCD9002A: TimerA, TimerB, and TimerC. These three timers all have 12-bit up counter and a preload register and programmable clock source. Timer A/B can also be the clock source of the software channel 1/2 respectively. The clock source of each timer can be set individually. Two clock sources, including CPU clock and external clock, can be selected individually or their combination to be timer's clock source. Besides, capture and comparison function are supported by TMA. Comparison is supported by TMB and TMC.
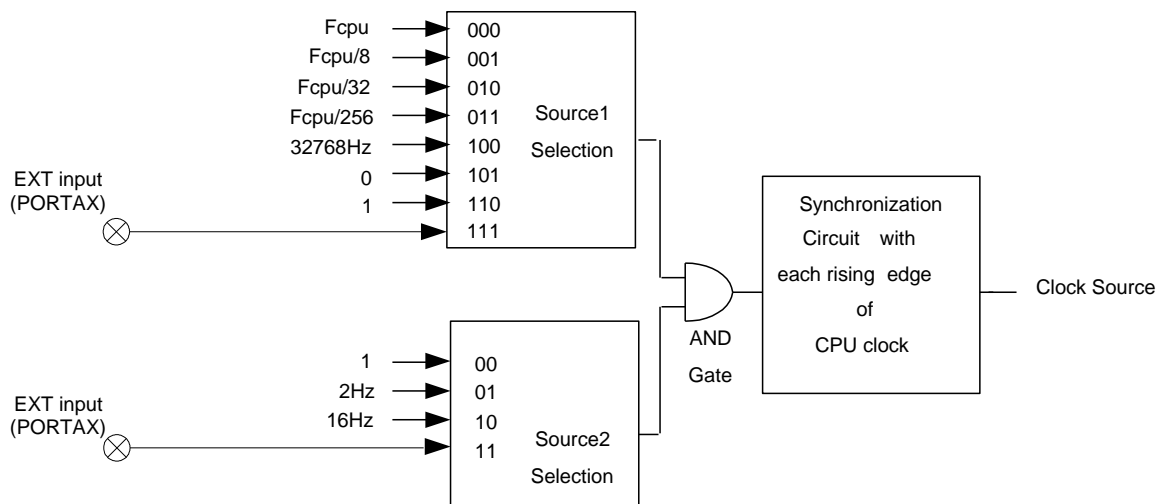
6.8. Sleep, Wakeup and Watchdog

6.8.1. Sleep and Wakeup

Sleep mode is to save power by stopping clock while device is not in use.   When sleep acts, the device runs from operating mode to standby mode.   Wake-up from sleep mode means turn the system from standby mode back to operating mode.

1). Sleep: After power on reset, IC starts working until a sleep command is given.   When a sleep signal is accepted, IC will turn off system clock and enter sleep mode.

2). Wake-up: When an IRQ/NMI interrupt signal is generated, GPCD9002A wakes up from sleep mode.   While wake-up is completed, program counter will continue to execute the next command.

6.8.2. Watchdog

The purpose of watchdog is to monitor system's operation normally.   Within a certain period, watchdog must be cleared. It protects the system from incorrect code execution by generating a system reset when software fails to clear watchdog flag within 0.75 seconds.   Watchdog function can be removed by option.

6.9. Speech and DAC

GPCD9002A features a high performance SPU voice engine to achieve maximum 8-channel voice with ADPCM/PCM.   The SPU also supports automatic zero-crossing concatenate function.   A hardware multiplier is also embedded in this SPU for software usage.   The fixed address of RAM area $0000 - $007F is designed as address pointers and a data buffer for the 8 channel speech/melody generation.   Moreover, two sets of 14-bit software channel with noise filter are supported.   There is one 14-bit DAC with push-pull amplifier for direct audio output.

6.10. Analog/Digital Converter

The 10-bit general purpose analog/digital converter (ADC) is embedded in GPCD9002A.   The ADC with 8 channels input can be selected by software programming with maximum 64KHz sampling rate.   Key press interrupt generation is supported.

6.11. SPI Controller

A Serial Peripheral Interface (SPI) controller is built-in GPCD9002A to facilitate communicating with other devices and components.   There are four control signals on SPI including SPICSN, SPICLK (SCK), SPITX (SDO), and SPIRX (SDI); the four signals are shared with PortD0, PortD1, PortD2 and PortD3. While SPI module is enabled by corresponding control bit.   These four pins cannot be GPIOs and any setting on corresponding GPIO control register will have no effect.   Four types of timing are

supported as follows:
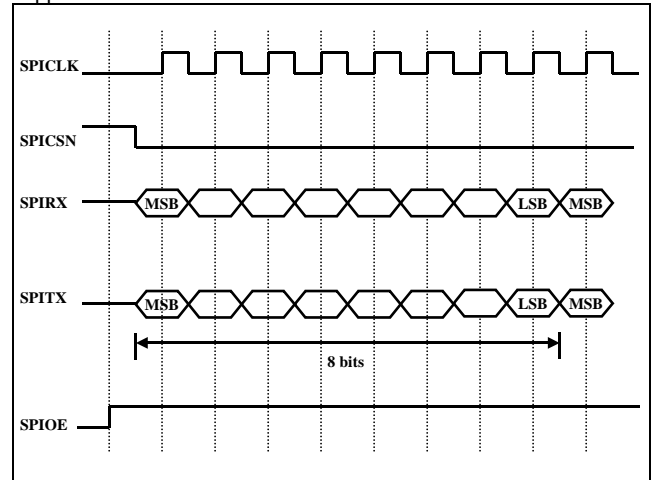
Master Mode, SPO = 0, SPH=0
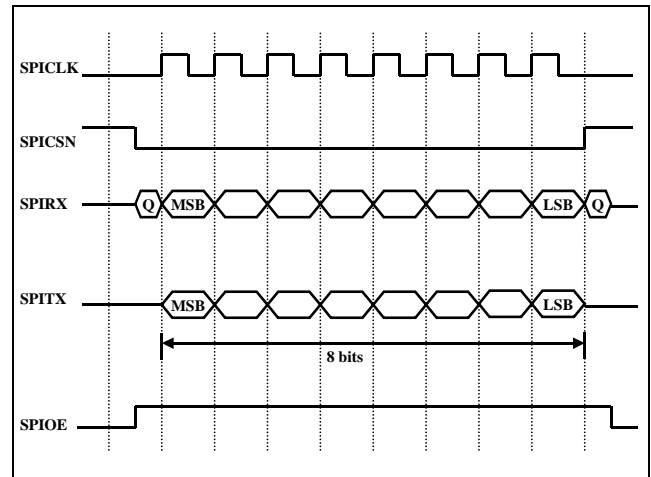
Master Mode, SPO = 0, SPH=1

Master Mode, SPO = 1, SPH=0

Master Mode, SPO = 1, SPH=1
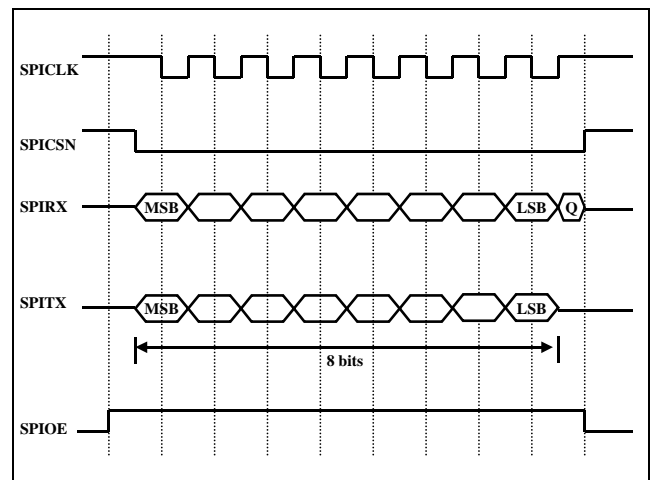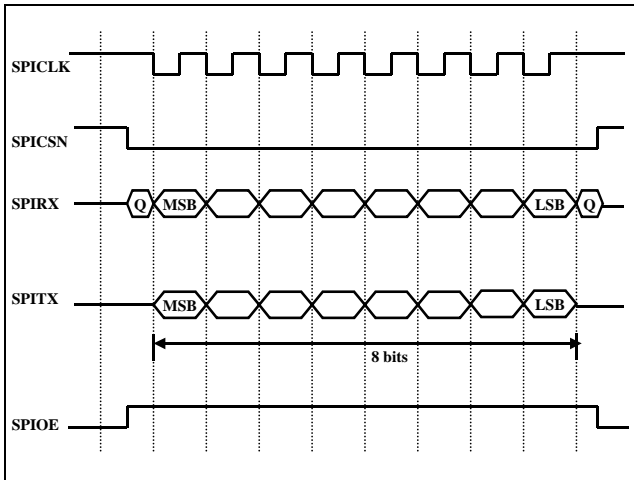
7. ELECTRICAL SPECIFICATIONS

7.1. Absolute Maximum Ratings

Characteristics	Symbol	Ratings
DC Supply Voltage	V_+	< 7.0V
Input Voltage Range	V_{IN}	-0.5V to V_+ + 0.5V
Operating Temperature	T_A	0℃ to +60℃
Storage Temperature	T_{STO}	-50℃ to +150℃

Note: Stresses beyond those given in the Absolute Maximum Rating table may cause permanent damage to the device. For normal operational conditions see DC Electrical Characteristics.

7.2. DC Characteristics (VDD_IO/VDD_ADC/VDD_REG=3.0V, TA=25℃)

Characteristics	Symbol	Min.	Typ.	Max.	Unit	Test Condition
Operating Voltage	VDD	2.4	-	3.6	V	For 2-battery
Operating Current	I_{OP}	-	9	-	mA	VDD_IO/VDD_ADC/VDD_REG=3.0V F_{CPU} = 8MHz , DAC on, no load
Standby Current	I_{STBY}	-	-	3	µA	VDD_IO/VDD_ADC/VDD_REG=3.0V
OSC Frequency	F_{OSC}	-	-	16	MHz	VDD_IO/VDD_ADC/VDD_REG=3.0V
Input High Level	V_{IH}	0.7*VDD	-	-	V	-
Input Low Level	V_{IL}	-	-	0.3*VDD	V	-
Output High Current (IOA/B/C/D[7:0])	I_{OH}	-	5	-	mA	VDD_IO/VDD_ADC/VDD_REG=3.0V, V_{OH} =2.1V
Output Sink Current (IOA/B[7:4], IOC/D[7:0])	I_{OL1}	-	9	-	mA	VDD_IO/VDD_ADC/VDD_REG=3.0V, V_{OL} =0.9V
Output High Sink Current (IOA/B[3:0])	I_{OL2}	-	18	-	mA	VDD_IO/VDD_ADC/VDD_REG=3.0V, V_{OL} =0.9V
Input Pull-Low Resistor (IOA/B/C/D[7:0])	R_{PL}	-	1330	-	Kohm	VDD_IO/VDD_ADC/VDD_REG=3.0V, Vin=3.0V
Input Pull-High Resistor (IOA/B/C/D[7:0])	R_{PH}	-	155	-	Kohm	VDD_IO/VDD_ADC/VDD_REG=3.0V, Vin=VSS

7.3. DC Characteristics (VDD_IO/VDD_ADC/VDD_REG=4.5V, TA=25℃)

Characteristics	Symbol	Min.	Typ.	Max.	Unit	Test Condition
Operating Voltage	VDD	3.6	-	5.5	V	For 3-battery
Operating Current	I_{OP}	-	12	-	mA	VDD_IO/VDD_ADC/VDD_REG=4.5V F_{CPU} = 8MHz , DAC on, no load
Standby Current	I_{STBY}	-	-	5	µA	VDD_IO/VDD_ADC/VDD_REG=4.5V
OSC Frequency	F_{OSC}	-	-	16	MHz	VDD_IO/VDD_ADC/VDD_REG=4.5V
Input High Level	V_{IH}	0.7*VDD	-	-	V	-
Input Low Level	V_{IL}	-	-	0.3*VDD	V	-
Output High Current (IOA/B/C/D[7:0])	I_{OH}	-	10	-	mA	VDD_IO/VDD_ADC/VDD_REG=4.5V, V_{OH} =3.15V
Output Sink Current (IOA/B[7:4], IOC/D[7:0])	I_{OL1}	-	18	-	mA	VDD_IO/VDD_ADC/VDD_REG=4.5V, V_{OL} =3.15V

Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
Output High Sink Current (IOA/B[3:0])	I_{OL2}	-	34	-	mA	VDD_IO/VDD_ADC/VDD_REG=4.5V, V_{OL} =3.15V
Input Pull-Low Resistor (IOA/B/C/D[7:0])	R_{PL}	-	821	-	Kohm	VDD_IO/VDD_ADC/VDD_REG=4.5V, Vin=4.5V
Input Pull-High Resistor (IOA/B/C/D[7:0])	R_{PH}	-	95	-	Kohm	VDD_IO/VDD_ADC/VDD_REG=4.5V, Vin=VSS

7.4. DAC Characteristics (VDD_IO/VDD_ADC/VDD_REG/VDD_DAC=4.5V, R_L=8Ω, f=1KHz, TA=25℃)

Characteristics	Symbol	Limit			Unit
		Min.	Typ.	Max.	
DAC Resolution	RESO	-	-	14	bit
THD+n (4.5V@0.45W)	-	-	0.4	-	%
Noise at No Signal	-	-	-97	-	dBr A
Dynamic Range(-60dB)	-	-	-80	-	dBr A

7.5. Regulator Characteristics (TA=25℃)

Characteristics	Symbol	Limit			Unit
		Min.	Typ.	Max.	
Input Voltage	VREGI	2.4	4.5	5.5	V
Maximum Current Output	IREGO	-	-	30	mA
Output Voltage	VREGO	2.4	3.3	3.6	V
Standby Current	IREGS	-	-	2.0	uA

7.6. ADC Characteristics (VDD_IO/VDD_ADC/VDD_REG/VDD_DAC=3.0V, TA=25℃)

Characteristics	Symbol	Limit			Unit
		Min.	Typ.	Max.	
ADC Resolution	RESO	-	-	10	bits
Signal-to-Noise Plus Distortion of ADC from Line-in	SINAD	-	-60	-	dB
Effective Number of Bit	ENOB	-	9.7	-	bits
Integral Non-linearity of ADC	INL	-	±1.0	-	LSB
Differential Non-linearity of ADC	DNL	-	±0.6	-	LSB
No Missing Code	-	-	9	-	bits
AD Conversion Rate	F_{CONV}	-	-	100K	Hz
Supply Voltage	VADC	2.4	4.5	5.5	V

7.7. F$_{OSC}$ vs. I$_{OP}$ (TA=25℃)
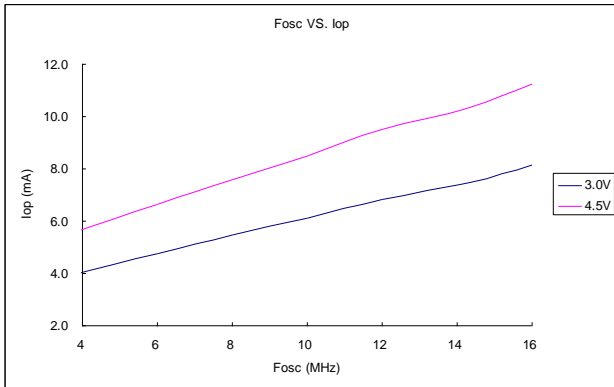
7.8. R$_{OSC}$ vs. F$_{OSC}$ (TA=25℃)
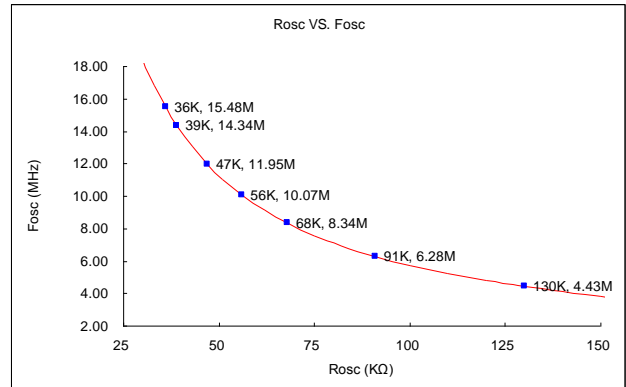
8. APPLICATION CIRCUITS

8.1. GPCD9002A Application Circuit with 32K crystal mode and without IO Output Driving Application (R_{OSC}-mode)

Note:
1. 4Ω speaker application is not allowed in GPCD9002A.
2. Above illustration only suggested for no IO heavy driving output, such as only key input trigger and no LED or motor driver output.
3. C1/C2 value may vary with system application.
4. VDD could be not bonded due to internally connect to VDD33.
5. If system is not stable, it is suggested to refer to following 8.3~8.6 circuits.
6. C4/C5 values are for design guidance only. The recommended 32K XTAL features are ESR=11.2~60K and CL1=CL2 =26~36pF (including PCB parasitic loading, for example, user should apply additional 20~30pF on X32I and X32O if PCB parasitic loading is 6pF)

8.2. GPCD9002A Application Circuit without IO Output Driving Application (XTAL-mode)

Note:

1. 4Ω speaker application is not allowed in GPCD9002A.

2. Above illustration only suggested for no IO heavy driving output, such as only key input trigger and no LED or motor driver output.

3. C1/C2 value may vary with system application.

4. VDD could be not bonded due to internally connect to VDD33.

5. If system is not stable, it is suggested to refer to following 8.3~8.6 circuits.

6. The values of C4/C5 are for design guidance only, different values may be needed for different crystal/resonator used.

8.3. GPCD9002A Application Circuit with R_OSC Option

Note: 4Ω speaker application is not allowed in GPCD9002A.
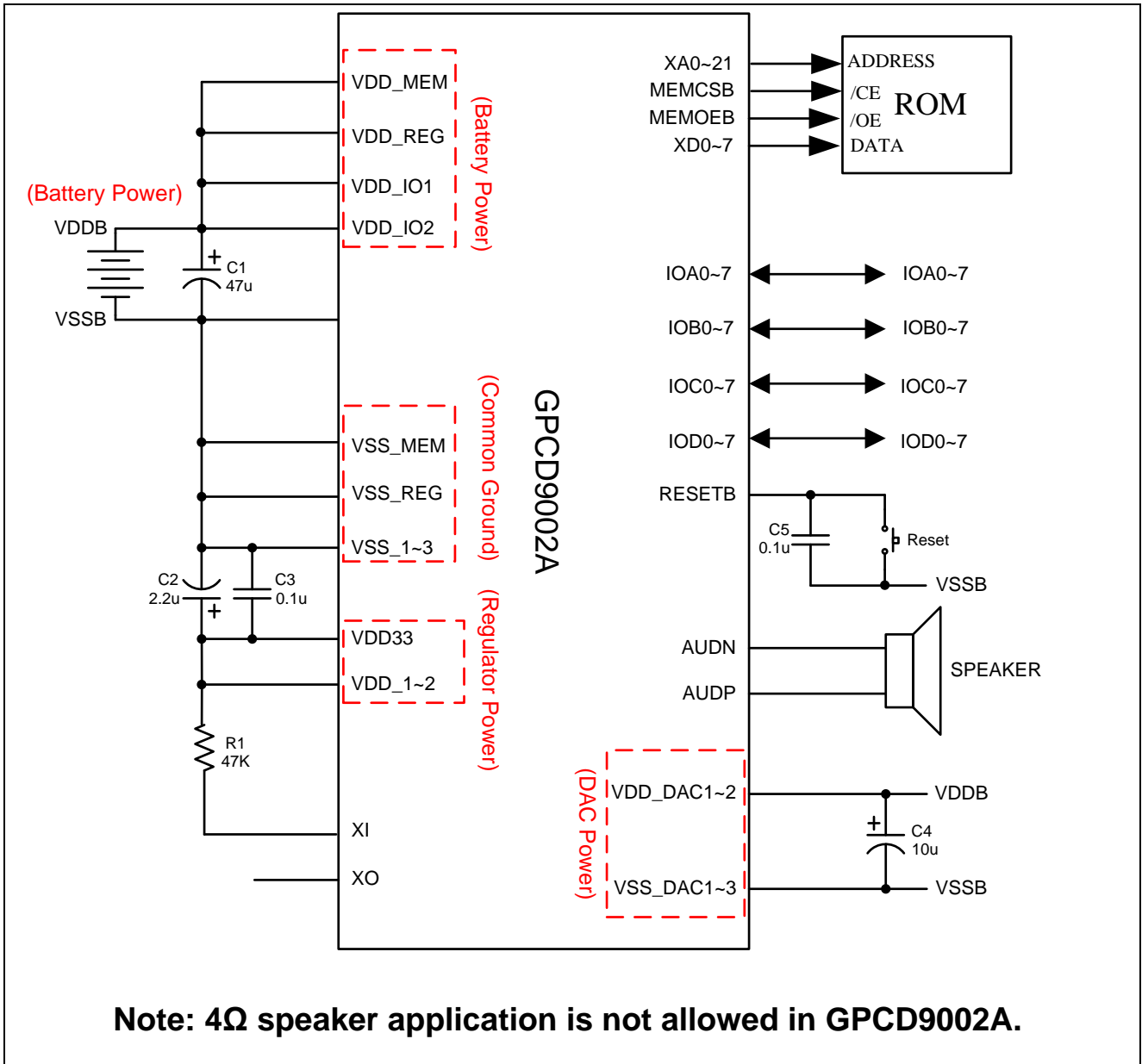
8.4. GPCD9002A Application Circuit with Crystal Option

Note:

1. 4Ω speaker application is not allowed in GPCD9002A.

2. The values of C6/C7 are for design guidance only, different values may be needed for different crystal/resonator used.
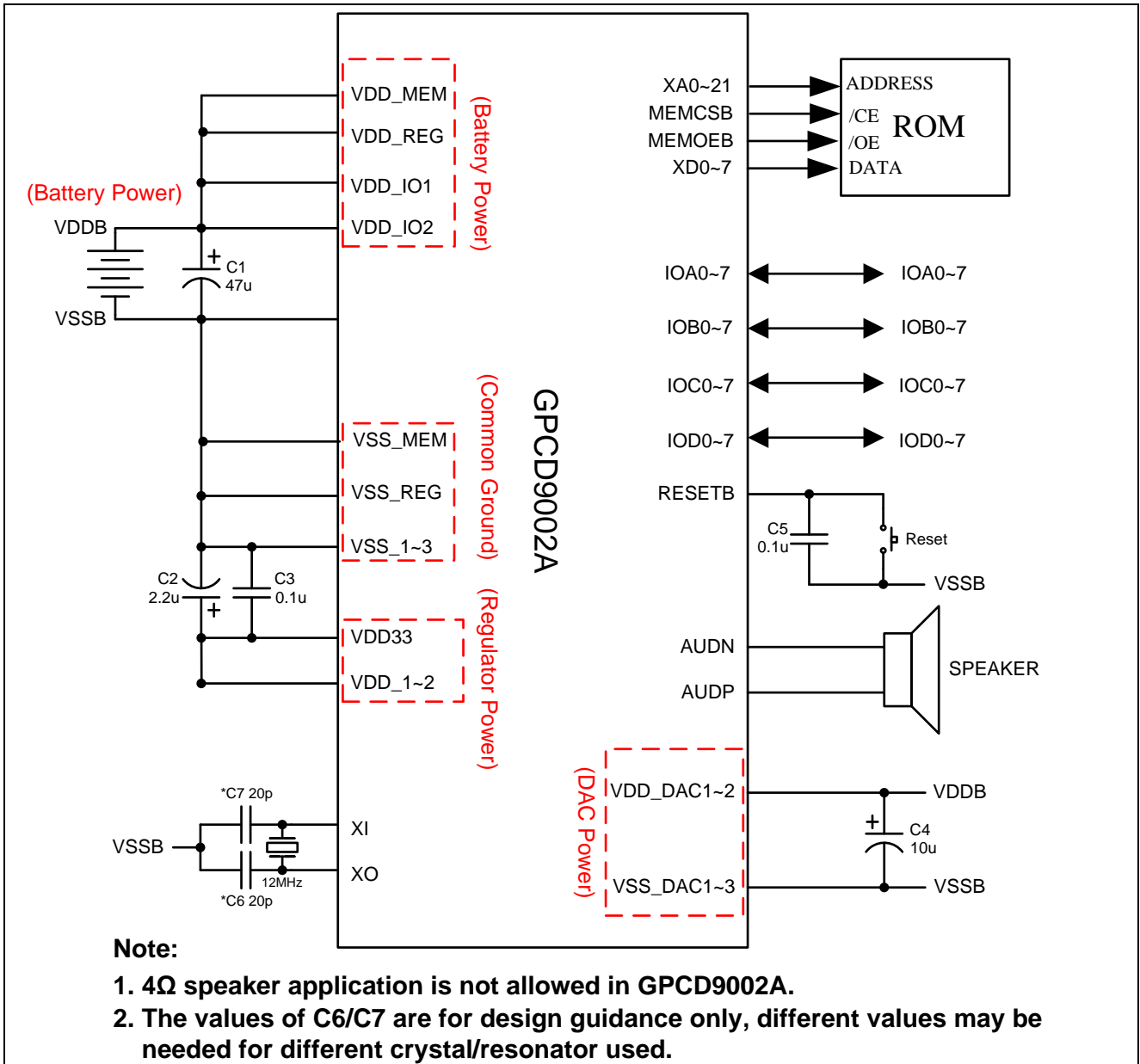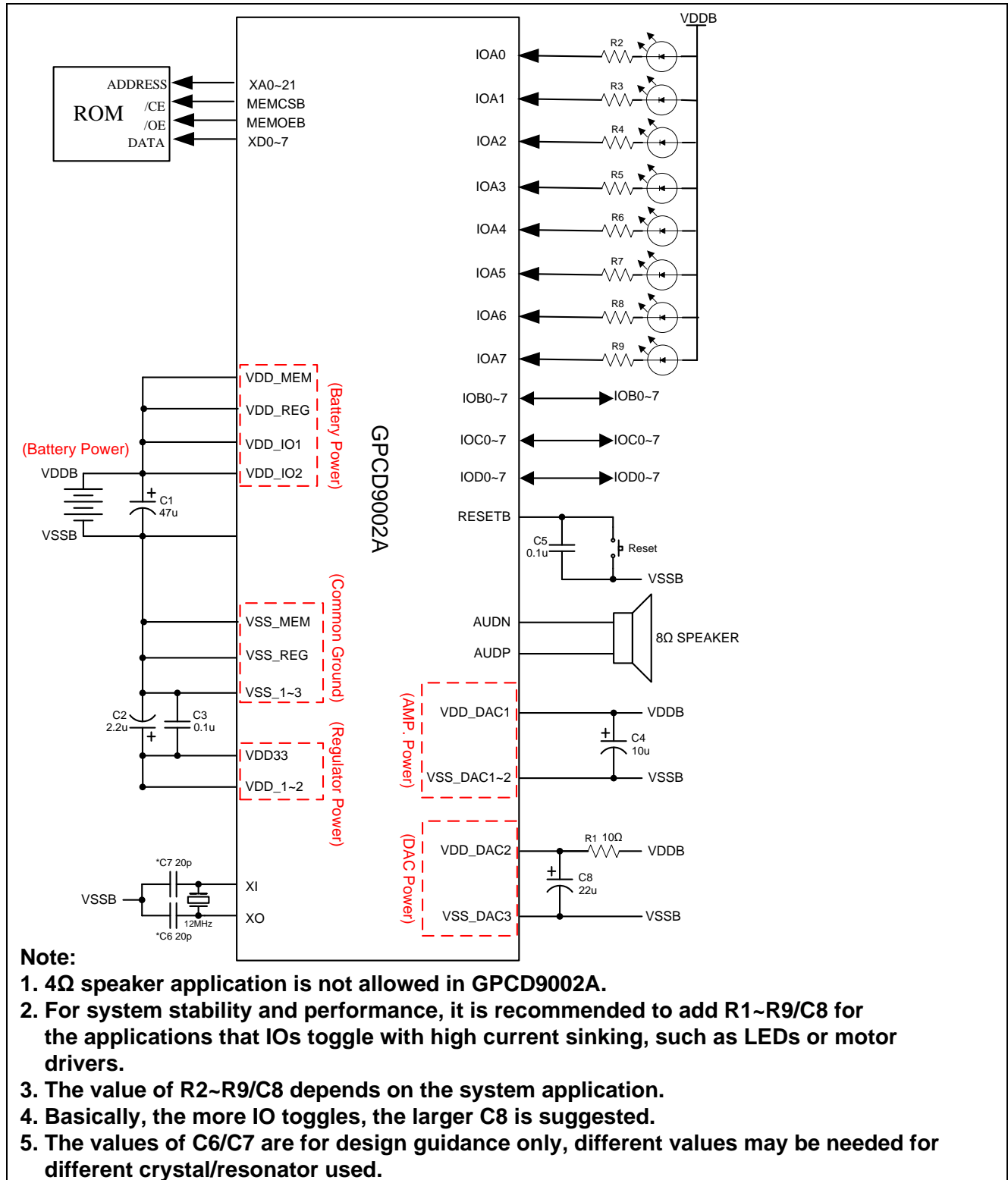
8.5. GPCD9002A Application Circuit with IO Heavy Loading(1): High Sourcing
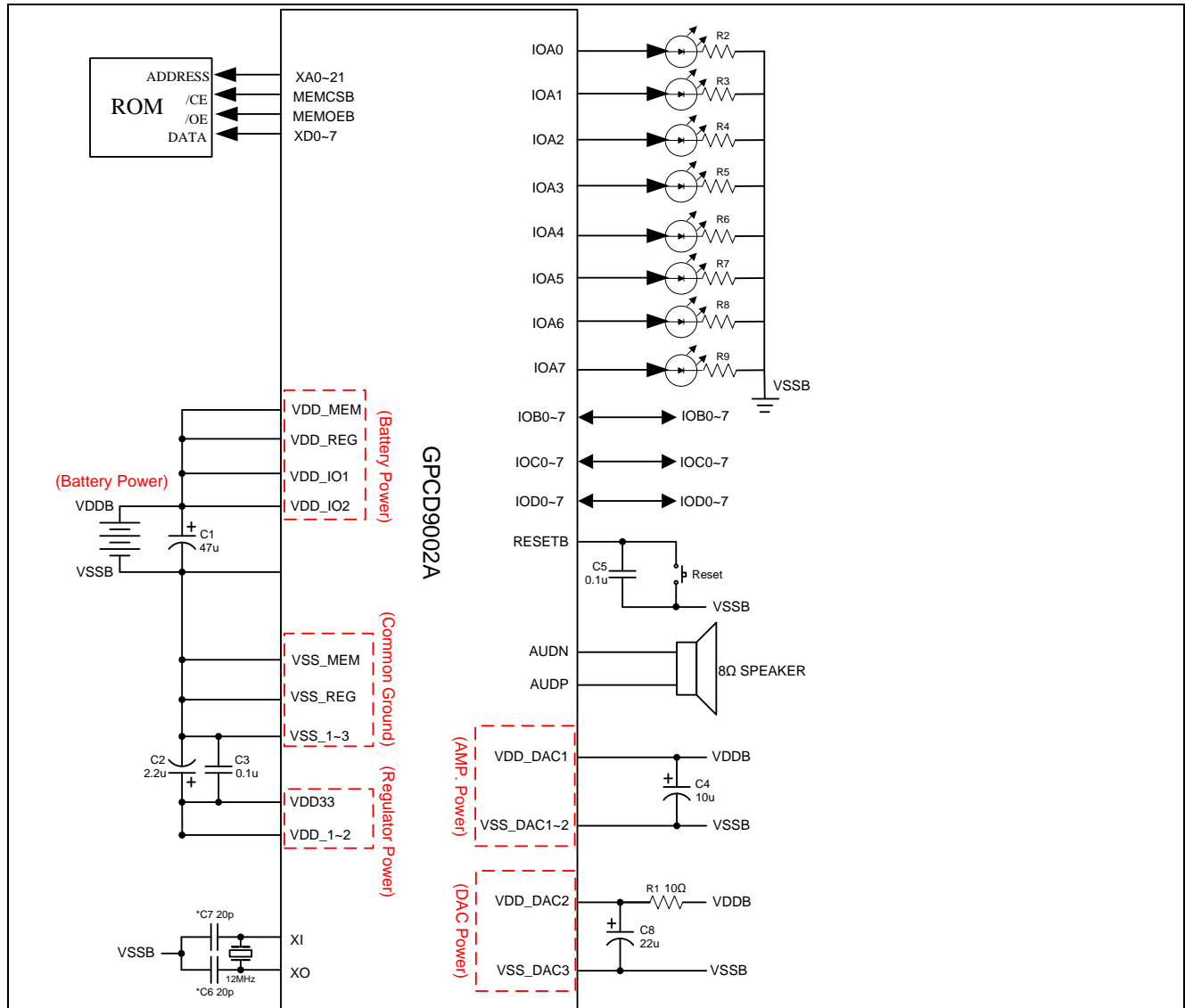
Note:

1. 4Ω speaker application is not allowed in GPCD9002A.
2. For system stability and performance, it is recommended to add R1/C8 for the applications that IOs toggle with high current sourcing, such as LEDs or motor drivers.
3. The value of R2~R9/C8 depends on applications. Basically, the more IO toggles, the larger C8 is suggested.
4. The values of C6/C7 are for design guidance only, different values may be needed for different crystal/resonator used.

8.6. GPCD9002A Application Circuit with IO Heavy Loading(2): High Sinking

Note:
1. **4Ω speaker application is not allowed in GPCD9002A.**
2. **For system stability and performance, it is recommended to add R1~R9/C8 for the applications that IOs toggle with high current sinking, such as LEDs or motor drivers.**
3. **The value of R2~R9/C8 depends on the system application.**
4. **Basically, the more IO toggles, the larger C8 is suggested.**
5. **The values of C6/C7 are for design guidance only, different values may be needed for different crystal/resonator used.**

9. PACKAGE/PAD LOCATIONS

9.1. Ordering Information

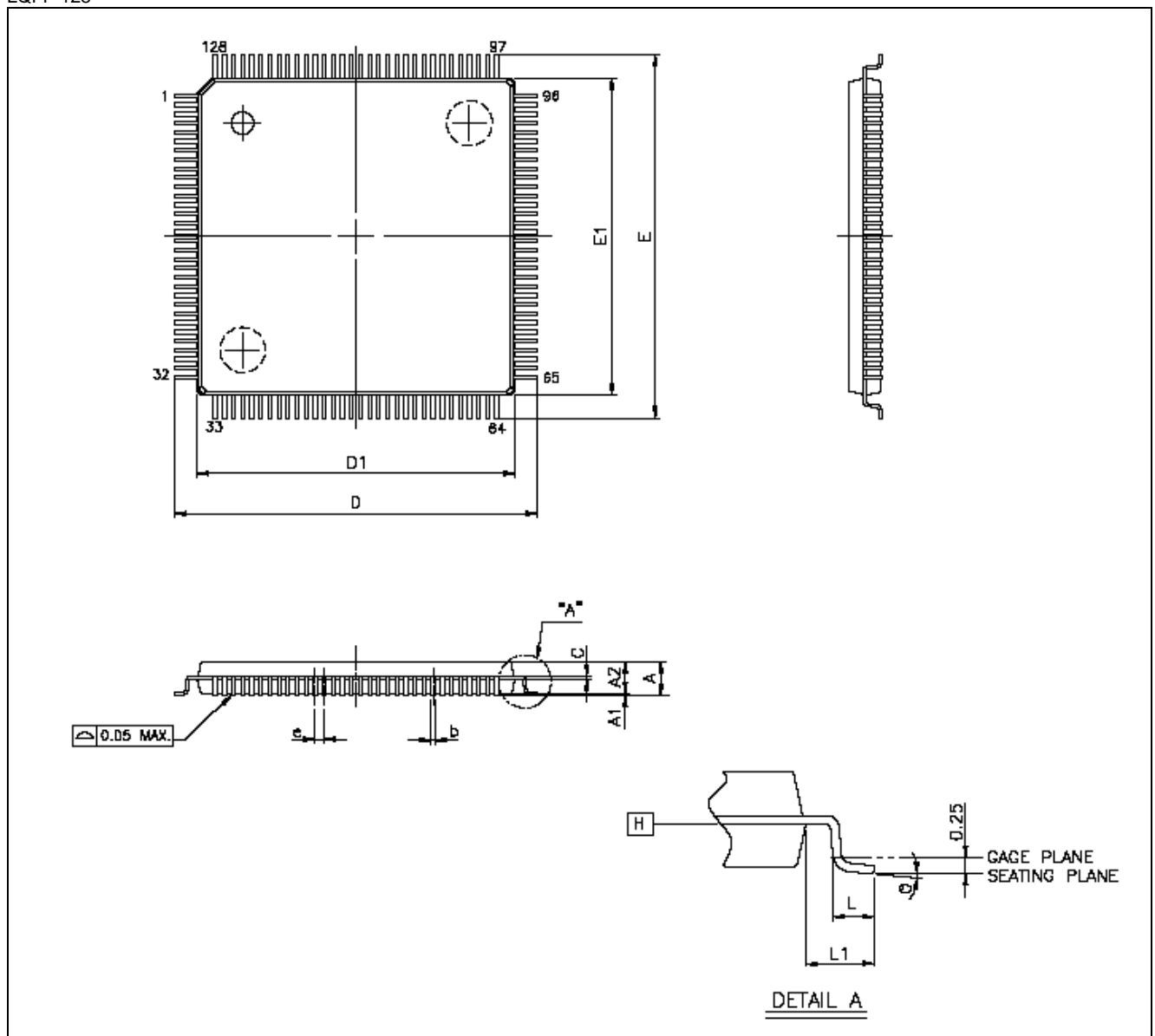| Product Number	Package Type
GPCD9002A-NnnV-C	Chip form
GPCD9002A-NnnV-HL09x	Green Package - LQFP128

Note1: Code number is assigned for customer.

Note2: Code number (N = A - Z or 0 - 9, nn = 00 - 99); version (V = A - Z).

Note3: Package form number (x = 1 - 9, serial number).

9.2. Package Information

LQFP 128

Symbol	Millimeter		
	Min.	Nom.	Max.
A	-	-	1.60
A1	0.05	-	0.15

Symbol	Millimeter		
	Min.	Nom.	Max.
A2	1.35	1.40	1.45
D	16.00 BCS.		
D1	14.00 BCS.		
E	16.00 BCS.		
E1	14.00 BCS.		
e	0.40 BCS.		
θ	0˚	3.5˚	7˚
b	0.13	0.16	0.23
c	0.09	-	0.20
L	0.45	0.60	0.75
L1	1.00 REF		

10. DISCLAIMER

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11. REVISION HISTORY

Date	Revision #	Description	Page
APR. 11, 2017	1.2	Rename PADs name : VDD_IO1 → VDD_IO2 VDD_IO2 → VDD_IO1	6,8,9
OCT. 08, 2013	1.1	Modify 8.1 Application circuit	17
JUL. 26, 2013	1.0	Add item "power domain" in section 5.SIGNAL DESCRIPTION.	5 - 6
JUN. 29, 2011	0.1	Original	24

     Version: 1.2