V437464C24V
3.3 VOLT 64M x 72 HIGH PERFORMANCE PC133 REGISTERED PLL ECC SDRAM MODULE

Features

- 168 Pin Registered ECC 67,108,864 x 72 bit Oganization SDRAM Modules
- Utilizes High Performance 64M x 4 SDRAM in TSOPII-54 Packages
- Fully PC Board Layout Compatible to INTEL'S Rev 1.2 Module Specification
- Single +3.3V (± 0.3V) Power Supply
- Programmable $\overline{\text{CAS}}$ Latency, Burst Length, and Wrap Sequence (Sequential & Interleave)
- Auto Refresh (CBR) and Self Refresh
- All Inputs, Outputs are LVTTL Compatible
- 8192 Refresh Cycles every 64 ms
- Serial Present Detect (SPD)
- SDRAM Performance

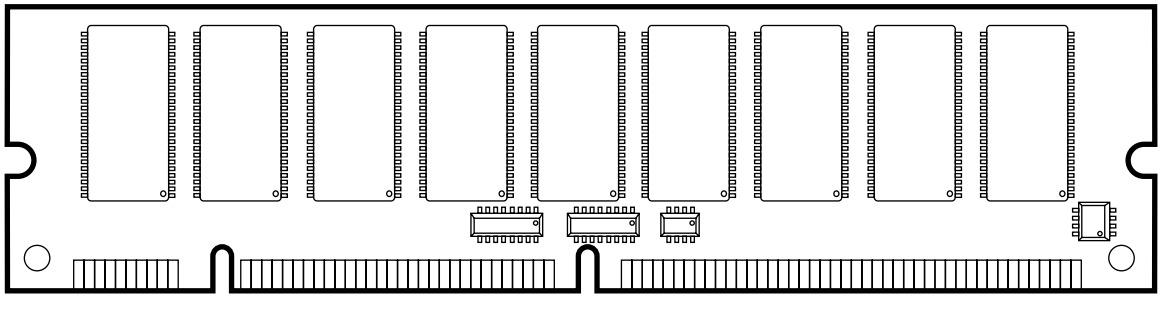
Description

The V437464C24V memory module is organized 67,108,864 x 72 bits in a 168 pin dual in line memory module (DIMM). The 64M x 72 registered DIMM uses 18 Mosel-Vitelic 64M x 4 ECC SDRAM. The x72 registered modules are ideal for use in high performance computer systems where increased memory density and fast access times are required.

	Key Component Timing Parameters	-7PC	-7	-8PC	Units
t_{CK}	Clock Frequency (max.)	143	143	125	MHz
t_{AC}	Clock Access Time $\overline{\text{CAS}}$ Latency = 3	5.4	5.4	6	ns
t_{AC}	Clock Access Time $\overline{\text{CAS}}$ Latency = 2	5.4	6	6	ns

- Module Frequency vs AC Parameter

Frequency	$\overline{\text{CL}}$ (CAS Latency)	t_{RCD}	t_{RP}	t_{RC}	Unit
V437464C24V 133 MHz (PC)	2	2	2	8	CLK
V437464C24V 133 MHz	3	3	3	8	CLK
V437464C24V 100 MHz (PC)	2	2	2	7	CLK



Pin Configurations (Front Side/Back Side)

Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back
1	VSS	29	DQM1	57	I/O19	85	VSS	113	DQM5	141	I/O51
2	I/O1	30	$\overline{CS0}$	58	I/O20	86	I/O33	114	$\overline{CS1}$	142	I/O52
3	I/O2	31	DU	59	VCC	87	I/O34	115	RAS	143	VCC
4	I/O3	32	VSS	60	I/O21	88	I/O35	116	VSS	144	I/O53
5	I/O4	33	A0	61	NC	89	I/O36	117	A1	145	NC
6	VCC	34	A2	62	DU	90	VCC	118	A3	146	DU
7	I/O5	35	A4	63	CKE1*	91	I/O37	119	A5	147	REGE
8	I/O6	36	A6	64	VSS	92	I/O38	120	A7	148	VSS
9	I/O7	37	A8	65	I/O22	93	I/O39	121	A9	149	I/O54
10	I/O8	38	A10(AP)	66	I/O23	94	I/O40	122	BA0	150	I/O55
11	I/O9	39	BA1	67	I/O24	95	I/O41	123	A11	151	I/O56
12	VSS	40	VCC	68	VSS	96	VSS	124	VCC	152	VSS
13	I/O10	41	VCC	69	I/O25	97	I/O42	125	CLK1*	153	I/O57
14	I/O11	42	CLK0	70	I/O26	98	I/O43	126	A12	154	I/O58
15	I/O12	43	VSS	71	I/O27	99	I/O44	127	VSS	155	I/O59
16	I/O13	44	DU	72	I/O28	100	I/O45	128	CKE0	156	I/O60
17	I/O14	45	$\overline{CS2}$	73	VCC	101	I/O46	129	$\overline{CS3}$	157	VCC
18	VCC	46	DQM2	74	I/O29	102	VCC	130	DQM6	158	I/O61
19	I/O15	47	DQM3	75	I/O30	103	I/O47	131	DQM7	159	I/O62
20	I/O16	48	DU	76	I/O31	104	I/O48	132	DU	160	I/O63
21	CBO	49	VCC	77	I/O32	105	CB4	133	VCC	161	I/O64
22	CB1	50	NC	78	VSS	106	CB5	134	NC	162	VSS
23	VSS	51	NC	79	CLK2*	107	VSS	135	NC	163	CLK3*
24	NC	52	CB2	80	NC	108	NC	136	CB6	164	NC
25	NC	53	CB3	81	WP	109	NC	137	CB7	165	SA0
26	VCC	54	VSS	82	SDA	110	VCC	138	VSS	166	SA1
27	$\overline{WE}$	55	I/O17	83	SCL	111	CAS	139	I/O49	167	SA2
28	DQM0	56	I/O18	84	VCC	112	DQM4	140	I/O50	168	VCC

Notes:

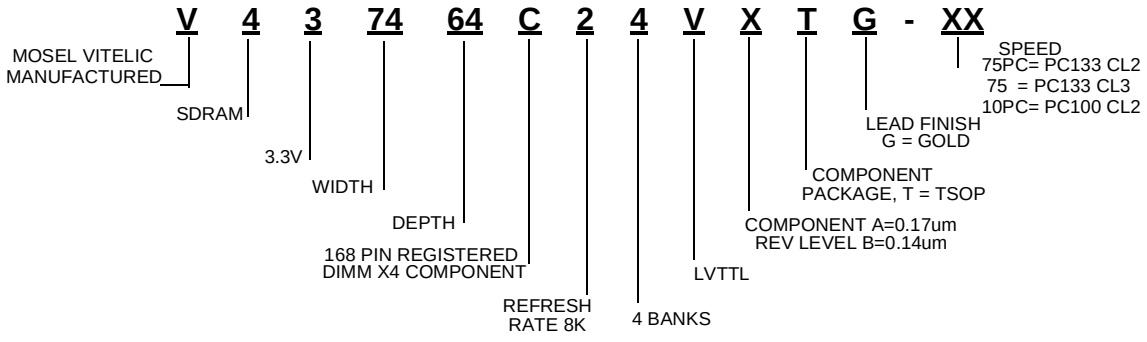
* These pins are not used in this module.

Pin Names

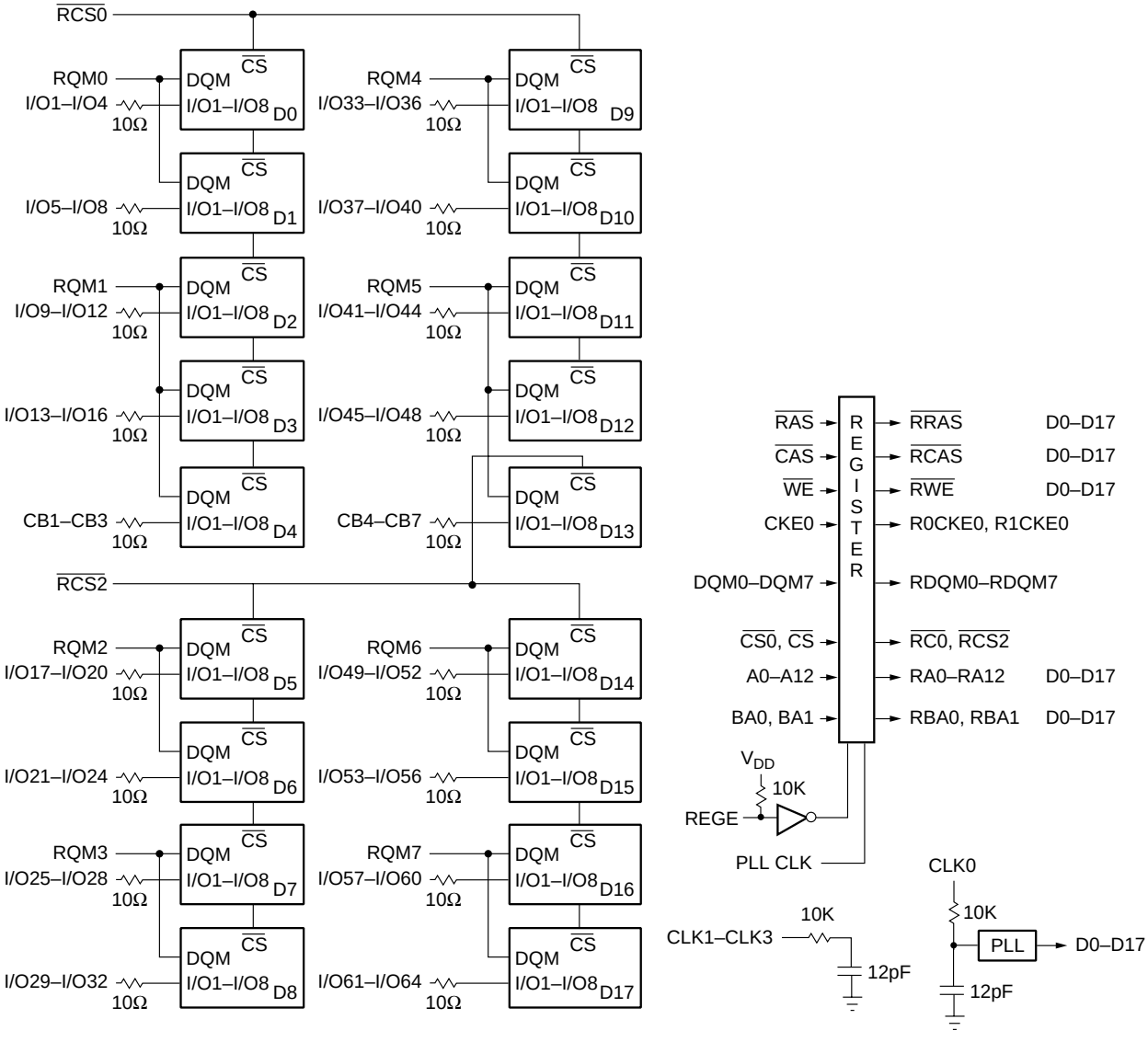
A0–A12	Address Inputs
I/O1–I/O64	Data Inputs/Outputs
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WE}$	Read/Write Input
BA0, BA1	Bank Selects
$\overline{CKE0}$	Clock Enable
$\overline{CS0}$, $\overline{CS2}$	Chip Select
CLK0–CLK3	Clock Input
DQM0–DQM7	Data Mask
VCC	Power (+3.3 Volts)
VSS	Ground
SCL	Clock for Presence Detect

SDA	Serial Data OUT for Presence Detect
SA0–A2	Serial Data IN for Presence Detect
CB0–CB4	Check Bits (x72 Organization)
NC	No Connection
REGE	Register Enable
DU	Don't Use

Module Part Number Information



Block Diagram



Serial Presence Detect Information

A serial presence detect storage device – E^2PROM – is assembled onto the module. Information about the module configuration, speed, etc. is written into the E^2PROM device during module production using a serial presence detect protocol (I^2C synchronous 2-wire bus)

SPD-Table

Byte Number	Function Described	SPD Entry Value	Hex Value		
			-75PC	-75	-10PC
0	Number of SPD bytes	128	80	80	80
1	Total bytes in Serial PD	256	08	08	08
2	Memory Type	SDRAM	04	04	04
3	Number of Row Addresses (without BS bits)	13	0D	0D	0D
4	Number of Column Addresses (for x4 SDRAM)	11	0B	0B	0B
5	Number of DIMM Banks	1	01	01	01
6	Module Data Width	72	48	48	48
7	Module Data Width (continued)	0	00	00	00
8	Module Interface Levels	LVTTL	01	01	01
9	SDRAM Cycle Time at CL=3	7.5 ns/10.0 ns	75	75	A0
10	SDRAM Access Time from Clock at CL=3	5.4 ns/6.0 ns	54	54	60
11	Dimm Config (Error Det/Corr.)	ECC	02	02	02
12	Refresh Rate/Type	Self-Refresh, 7.8µs	82	82	82
13	SDRAM width, Primary	x4	04	04	04
14	Error Checking SDRAM Data Width	n/a / x4	04	04	04
15	Minimum Clock Delay from Back to Back Random Column Address	t_{ccd} = 1 CLK	01	01	01
16	Burst Length Supported	1, 2, 4, 8	0F	0F	0F
17	Number of SDRAM Banks	4	04	04	04
18	Supported $\overline{CAS}$ Latencies	CL = 2/3	06	06	06
19	$\overline{CS}$ Latencies	$\overline{CS}$ Latency = 0	01	01	01
20	$\overline{WE}$ Latencies	WL = 0	01	01	01
21	SDRAM DIMM Module Attributes	Registered/Buffered	1F	1F	1F
22	SDRAM Device Attributes: General	Vcc tol ± 10%	0E	0E	0E
23	Minimum Clock Cycle Time at $\overline{CAS}$ Latency = 2	7.5ns/10.0ns	75	A0	A0
24	Maximum Data Access Time from Clock for CL = 2	5.4ns/6.0ns	54	54	60
25	Minimum Clock Cycle Time at CL = 1	Not Supported	00	00	00
26	Maximum Data Access Time from Clock at CL = 1	Not Supported	00	00	00
27	Minimum Row Precharge Time	15 ns/20 ns	0F	14	14

SPD-Table

Byte Number	Function Described	SPD Entry Value	Hex Value		
			-75PC	-75	-10PC
28	Minimum Row Active to Row Active Delay t_{RRD}	14 ns/15 ns/16 ns	0E	0F	10
29	Minimum RAS to $\overline{CAS}$ Delay t_{RCD}	15 ns/20 ns	0F	14	14
30	Minimum RAS Pulse Width t_{RAS}	42 ns/45 ns	2A	2D	2D
31	Module Bank Density (Per Bank)	512 MByte	80	80	80
32	SDRAM Input Setup Time	1.5 ns/2.0 ns	15	15	20
33	SDRAM Input Hold Time	0.8 ns/1.0 ns	08	08	10
34	SDRAM Data Input Setup Time	1.5 ns/2.0 ns	15	15	20
35	SDRAM Data Input Hold Time	0.8 ns/1.0 ns	08	08	10
62-61	Superset Information (May be used in Future)		00	00	00
62	SPD Revision	Revision 2/1.2	02	02	12
63	Checksum for Bytes 0 - 62		67	AE	1A
64	Manufacturer's JEDEC ID Code	Mosel Vitelic	40	40	40
65-71	Manufacturer's JEDEC ID Code (cont.)		00	00	00
72	Manufacturing Location				
73-90	Module Part Number (ASCII)				
91-92	PCB Identification Code				
93	Assembly Manufacturing Date (Year)				
94	Assembly Manufacturing Date (Week)				
95-98	Assembly Serial Number				
99-125	Reserved		00	00	00
126	Intel Specification for Frequency		64	64	64
127	Supported Frequency				
128+	Unused Storage Location		00	00	00

DC Characteristics

T_A = 0°C to 70°C; V_{SS} = 0 V; V_{DD}, V_{DDQ} = 3.3V ± 0.3V

Symbol	Parameter	Limit Values		Unit
		Min.	Max.	
V_{IH}	Input High Voltage	2.0	V_{CC}+0.3	V
V_{IL}	Input Low Voltage	–0.3	0.8	V
V_{OH}	Output High Voltage (I_{OUT} = –4.0 mA)	2.4	—	V
V_{OL}	Output Low Voltage (I_{OUT} = 4.0 mA)	—	0.4	V
$I_{I(L)}$	Input Leakage Current, any input (0 V < V_{IN} < 3.6 V, all other inputs = 0V)	–10	10	µA
$I_{O(L)}$	Output leakage current (DQ is disabled, 0V < V_{OUT} < V_{CC})	–10	10	µA

Capacitance

T_A = 0°C to 70°C; V_{DD} = 3.3V ± 0.3V, f = 1 MHz

Symbol	Parameter	Limit Values	Unit
C_{I1}	Input Capacitance (A0 to A11, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$)	15	pF
C_{I2}	Input Capacitance ($\overline{CS0}$-$\overline{CS3}$)	15	pF
C_{ICL}	Input Capacitance (CLK0)	20	pF
C_{I3}	Input Capacitance (CKE0)	15	pF
C_{I4}	Input Capacitance (DQM0-DQM7)	15	pF
C_{IO}	Input/Output Capacitance (I/O1-I/064)	16	pF
C_{SC}	Input Capacitance (SCL, SA0-2)	8	pF
C_{SD}	Input/Output Capacitance	18	pF

Absolute Maximum Ratings

Parameter	Max.	Units
Voltage on VDD Supply Relative to V_{SS}	-1 to 4.6	V
Voltage on Input Relative to V_{SS}	-1 to 4.6	V
Operating Temperature	0 to +70	°C
Storage Temperature	-55 to 125	°C
Power Dissipation		W

Standby and Refresh Currents[1]

T_A = 0°C to 70°C, V_{CC} = 3.3V ± 0.3V

Symbol	Parameter	Test Conditions		75PC/75	10PC	Unit	Note
$I_{CC}1$	Operating Current	Burst length = 4, CL = 3 t_{RC}> = t_{RC}(min), t_{CK}> = t_{CK}(min), IO = 0 mA 2 Bank Interleave Operation		4140	3060	mA	1,2
$I_{CC}2P$	Precharged Standby Current in Power Down Mode	CKE< = V_{IL}(max), t_{CK}> = t_{CK}(min)		36	36	mA	
$I_{CC}2N$	Precharged Standby Current in Non-Power Down Mode	CKE> = V_{IH}(min), t_{CK}> = t_{CK}(min)		720	540	mA	$\overline{CS}$ = High
$I_{CC}3P$	Active Standby Current in Power Down Mode	CKE< = V_{IL}(max), t_{CK}> = t_{CK}(min)		180	180	mA	
$I_{CC}3N$	Active Standby Current in Non-Power Down Mode	CKE> = V_{IH}(min), t_{CK}> = t_{CK}(min), Input changed one time		900	810	mA	$\overline{CS}$ = High
$I_{CC}4$	Burst Operating Current	t_{RC} = Infinite, CL = 3, t_{CK}> = t_{CK}(min), IO = 0 mA 2 Banks Activated		2700	1800	mA	1, 2
$I_{CC}5$	Auto Refresh Current	t_{RC}>= t_{RC}(min)		4300	3960	mA	1,2
$I_{CC}6$	Self Refresh Current	CKE = <0,2 V	Standard	54	54	mA	1,2
			L-version	32	32		

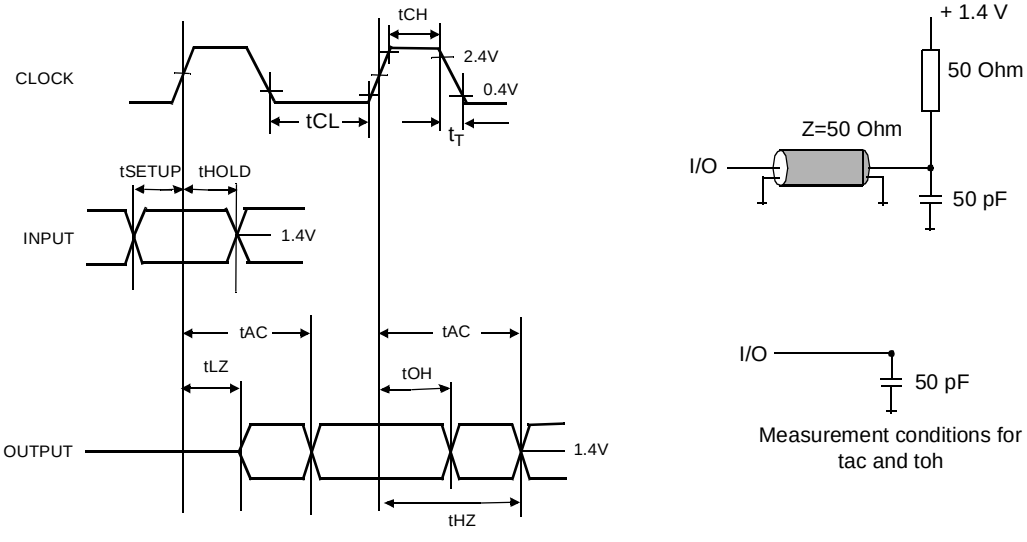
AC Characteristics [3,4]

T_A = 0° to 70°C; V_{SS} = 0V; V_{CC} = 3.3V ± 0.3V, t_T = 1 ns

			Limit Values							
			-75PC		-75		-10PC			
#	Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Unit	Note
Clock and Clock Enable										
1	t_{CK}	Clock Cycle Time								
		$\overline{CAS}$ Latency = 3	7.5		7.5		10		ns	
		$\overline{CAS}$ Latency = 2	7.5		10		10		ns	
2	f_{CK}	System frequency								
		$\overline{CAS}$ Latency = 3	–	133	–	133	–	100	MHz	
		$\overline{CAS}$ Latency = 2	–	133	–	100	–	100	MHz	
3	t_{AC}	Clock Access Time								4,5
		$\overline{CAS}$ Latency = 3	–	5.4	–	5.4	–	6	ns	
		$\overline{CAS}$ Latency = 2	–	6	–	6	–	6	ns	
4	t_{CH}	Clock High Pulse Width	2.5	–	2.5	–	3	–	ns	6
5	t_{CL}	Clock Low Pulse Width	2.5	–	2.5	–	3	–	ns	6
6	t_{CS}	Input Setup time	1.5	–	1.5	–	2	–	ns	7
7	t_{CH}	Input Hold Time	0.8	–	0.8	–	1	–	ns	7
8	t_{CKSP}	CKE Setup Time (Power down mode)	2	–	2	–	2	–	ns	8
9	t_{CKSR}	CKE Setup Time (Self Refresh Exit)	8	–	8	–	8	–	ns	9
10	t_T	Transition time (rise and fall)	0.3	1.2	0.3	1.2	0.3	1.2	ns	
Common Parameters										
11	t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ delay	15	–	20	–	20	–	ns	6
12	t_{RC}	Cycle Time	60	–	60	–	70	–	ns	6
13	t_{RAS}	Active Command Period	42	100K	45	100K	45	100K	ns	6
14	t_{RP}	Precharge Time	15	–	20	–	20	–	ns	6
15	t_{RRD}	Bank to Bank Delay Time	14	–	15	–	20	–	ns	6
16	t_{CCD}	$\overline{CAS}$ to $\overline{CAS}$ delay time (same bank)	1	–	1	–	1	–	CLK	
Refresh Cycle										
17	t_{SREX}	Self Refresh Exit Time	10	–	10	–	10	–	ns	
18	t_{REF}	Refresh Period (8192 cycles)	64	–	64	–	64	–	ms	
Read Cycle										
19	t_{OH}	Data Out Hold Time	3	–	3	–	3	–	ns	2
20	t_{LZ}	Data Out to Low Impedance Time	1	–	1	–	1	–	ns	
21	t_{HZ}	Data Out to High Impedance Time	3	7.5	3	7.5	3	8	ns	7
22	t_{DQZ}	DQM Data Out Disable Latency	–	2	–	2	–	2	CLK	
Write Cycle										
23	t_{DPL}	Data input to Precharge (write recovery)	10	–	10	–	10	–	ns	
24	t_{DQW}	DQM Write Mask Latency	0	–	0	–	0	–	CLK	

Notes:

1. The specified values are valid when addresses are changed no more than once during t_{CK}(min.) and when No Operation commands are registered on every rising clock edge during t_{RC}(min). Values are shown per module bank.
2. The specified values are valid when data inputs (DQ's) are stable during t_{RC}(min.).
3. All AC characteristics are shown for device level.
   An initial pause of 100 µs is required after power-up, then a Precharge All Banks command must be given followed by 8 Auto Refresh (CBR) cycles before the Mode Register Set Operation can begin.
4. AC timing tests have V_{IL} = 0.4V and V_{IH} = 2.4V with the timing referenced to the 1.4V crossover point. The transition time is measured between V_{IH} and V_{IL}. All AC measurements assume t_T = 1 ns with the AC output load circuit shown. Specific tac and toh parameters are measured with a 50 pF only, without any resistive termination and with a input signal of 1V / ns edge rate between 0.8V and 2.0V.



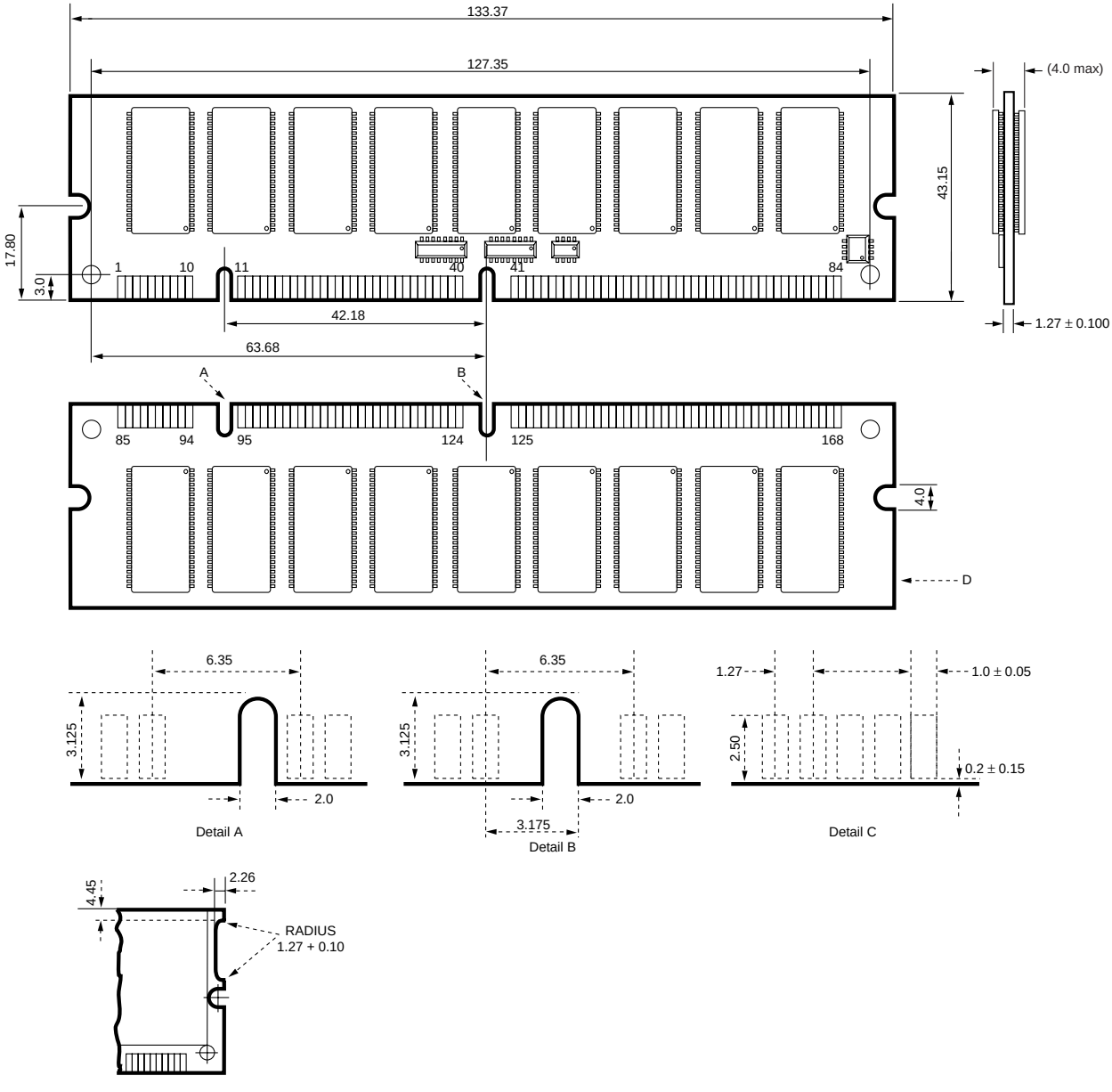
5. If clock rising time is longer than 1 ns, a time (t_T/2 -0.5) ns has to be added to this parameter.
6. Rated at 1.5V
7. If t_T is longer than 1 ns, a time (t_T -1) ns has to be added to this parameter.
8. Any time that the refresh Period has been exceeded, a minimum of two Auto (CBR) Refresh commands must be given to "wake-up" the device.
9. Self Refresh Exit is a synchronous operation and begins on the 2nd positive clock edge after CKE returns high. Self Refresh Exit is not complete until a time period equal to t_{RC} is satisfied once the Self Refresh Exit command is registered.
10. Referenced to the time which the output achieves the open circuit condition, not to output voltage levels.
11. t_{DAL} is equivalent to t_{DPL} + t_{RP}.

Package Diagram

L-DIM-168-30

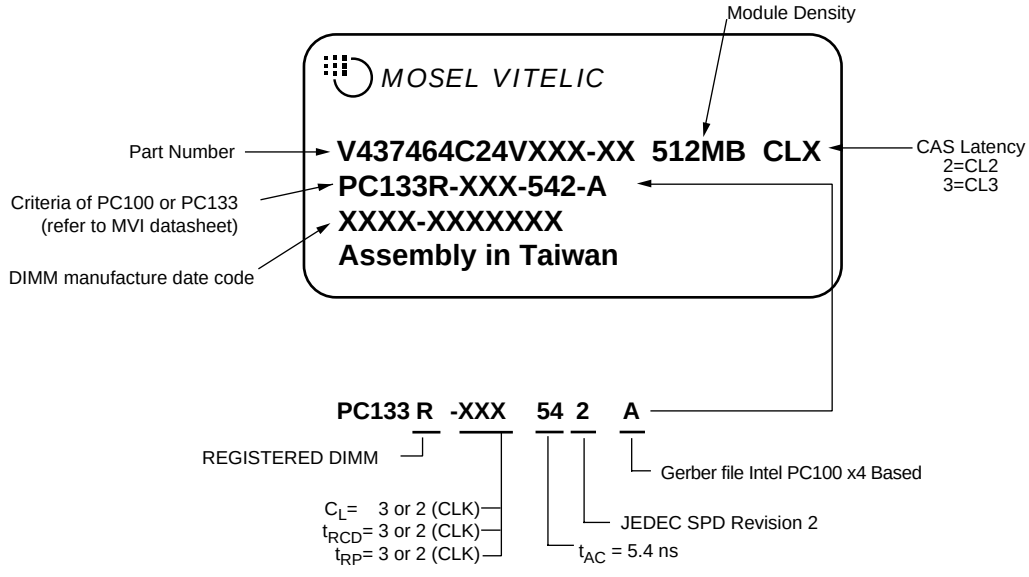
SDRAM DIMM Module Package

All measurements in mm



Tolerances: ± (0.13) unless otherwise specified.

Label Information



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