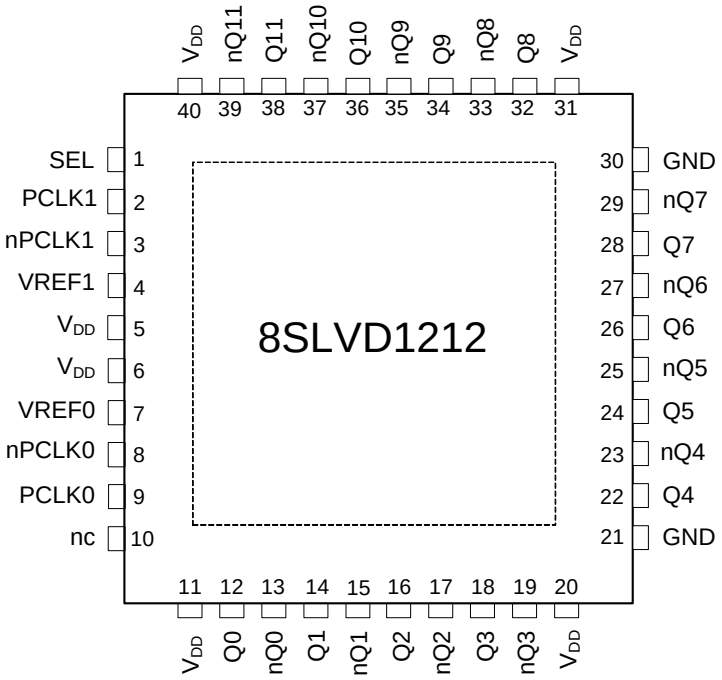
General Description

The 8SLVD1212 is a high-performance differential LVDS fanout buffer. The device is designed for the fanout of high-frequency, very low additive phase-noise clock and data signals. The 8SLVD1212 is characterized to operate from a 2.5V power supply. Guaranteed output-to-output and part-to-part skew characteristics make the 8SLVD1212 ideal for those clock distribution applications demanding well-defined performance and repeatability. Two selectable differential inputs and twelve low skew outputs are available. The integrated bias voltage reference enables easy interfacing of single-ended signals to the device inputs. The device is optimized for low power consumption and low additive phase noise.

Features

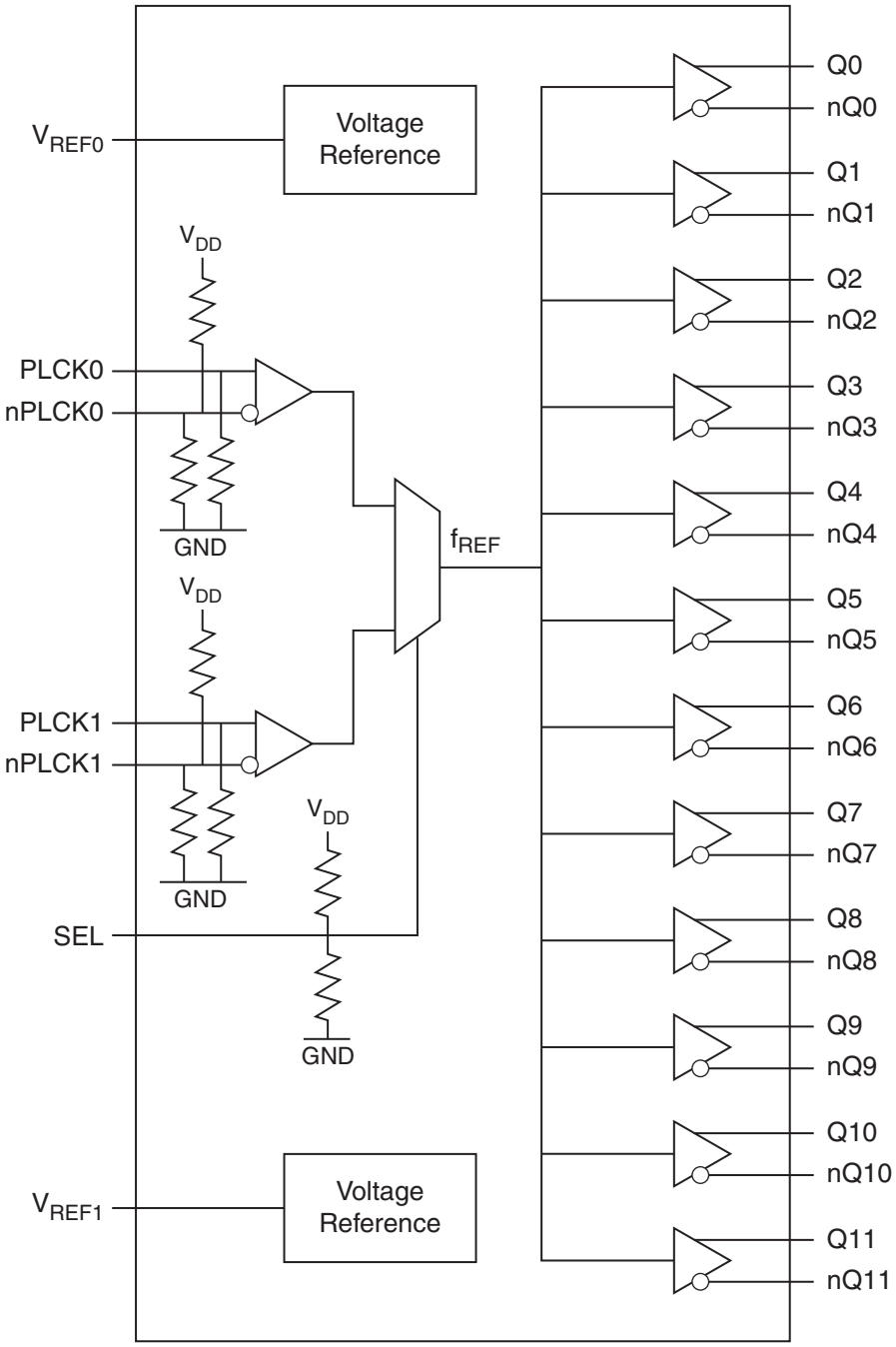
- Twelve low skew, low additive jitter LVDS output pairs
- Two selectable, differential clock input pairs
- Differential PCLK, nPCLK pairs can accept the following differential input levels: LVDS, LVPECL, CML
- Maximum input clock frequency: 2GHz (maximum)
- LVCMOS/LVTTL interface levels for the control input select pins
- Output skew: 45ps (max)
- Propagation delay: 310ps (typical)
- Low additive phase jitter, RMS; f_{REF} = 156.25MHz, 10kHz - 20MHz: 77fs (typical)
- Maximum device current consumption (I_{DD}): 213mA
- 2.5V supply voltage
- Lead-free (RoHS 6), 40-Lead VFQFN packaging
- -40°C to 85°C ambient operating temperature

Pin Assignment



40-Lead VFQFN
6.0mm x 6.0mm x 0.9mm package body

Block Diagram



Pin Descriptions and Characteristics

Table 1. Pin Descriptions[1]

Number	Name	Type		Description
1	SEL	Input	Pullup/ Pulldown	Reference select control pin. See *Table 3* for function. LVCMOS/LVTTL interface levels.
2	PCLK1	Input	Pulldown	Non-inverting differential clock/data input.
3	nPCLK1	Input	Pullup/ Pulldown	Inverting differential clock/data input. $V_{DD}/2$ default when left floating.
4	V_{REF1}	Output		Bias voltage reference for the PCLK1, nPCLK1 inputs.
5	V_{DD}	Power		Power supply pins.
6	V_{DD}	Power		Power supply pins.
7	V_{REF0}	Output		Bias voltage reference for the PCLK0, nPCLK0 inputs.
8	nPCLK0	Input	Pullup/ Pulldown	Inverting differential clock/data input. $V_{DD}/2$ default when left floating.
9	PCLK0	Input	Pulldown	Non-inverting differential clock/data input.
10	nc	Unused		Do not connect.
11	V_{DD}	Power		Power supply pins.
12	Q0	Output		Differential output pair. LVDS interface levels.
13	nQ0	Output		
14	Q1	Output		Differential output pair. LVDS interface levels.
15	nQ1	Output		
16	Q2	Output		Differential output pair. LVDS interface levels.
17	nQ2	Output		
18	Q3	Output		Differential output pair. LVDS interface levels.
19	nQ3	Output		
20	V_{DD}	Power		Power supply pins.
21	GND	Power		Power supply ground.
22	Q4	Output		Differential output pair. LVDS interface levels.
23	nQ4	Output		
24	Q5	Output		Differential output pair. LVDS interface levels.
25	nQ5	Output		
26	Q6	Output		Differential output pair. LVDS interface levels.
27	nQ6	Output		
28	Q7	Output		Differential output pair. LVDS interface levels.
29	nQ7	Output		
30	GND	Power		Power supply ground.
31	V_{DD}	Power		Power supply pins.
32	Q8	Output		Differential output pair. LVDS interface levels.
33	nQ8	Output		

Table 1. Pin Descriptions[1]

Number	Name	Type		Description
34	Q9	Output		Differential output pair. LVDS interface levels.
35	nQ9	Output		
36	Q10	Output		Differential output pair. LVDS interface levels.
37	nQ10	Output		
38,	Q11	Output		Differential output pair. LVDS interface levels.
39	nQ11	Output		
40	V_{DD}	Power		Power supply pins.
	GND_EP	Power		Exposed pad of package. Connect to GND.

NOTE 1: *Pulldown* and *Pullup* refer to internal input resistors. See *Table 2*, *Pin Characteristics,* for typical values.

Table 2. Pin Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			2		pF
$R_{PULLDOWN}$	Input Pulldown Resistor			50		kΩ
R_{PULLUP}	Input Pullup Resistor			50		kΩ

Function Table

Table 3. SEL Input Function Table[1]

SEL	Operation
0	PCLK0, nPCLK0 is the selected differential clock input.
1	PCLK1, nPCLK1 is the selected differential clock input.
Open	Input buffers are disabled and outputs are static.

NOTE 1: SEL is an asynchronous control.

Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Electrical Characteristics* or *AC Electrical Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, V_{DD}	4.6V
Inputs, V_I	-0.5V to V_{DD} + 0.5V
Outputs, I_O Continuous Current Surge Current	 10mA 15mA
Input Sink/Source, I_{REF}	±2mA
Maximum Junction Temperature, $T_{J,MAX}$	125°C
Storage Temperature, T_{STG}	-65°C to 150°C
ESD - Human Body Model[1]	2000V
ESD - Charged Device Mode[1]	500V

NOTE 1: According to JEDEC/JS-001-2012/ 22-C101E.

DC Electrical Characteristics

Table 4A. Power Supply DC Characteristics, V_{DD} = 2.5V ± 5%, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Power Supply Voltage		2.375	2.5V	2.625	V
I_{DD}	Power Supply Current	Q0 to Q11 terminated 100Ω between nQx, Qx		184	213	mA

Table 4B. LVCMOS/LVTTL DC Characteristics, V_{DD} = 2.5V ± 5%, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{MID}	Input voltage		Floating		V_{DD} / 2		V
V_{IH}	Input High Voltage			0.7 * V_{DD}		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage			-0.3		0.2 * V_{DD}	V
I_{IH}	Input High Current	SEL	V_{DD} = V_{IN} = 2.625V			150	µA
I_{IL}	Input Low Current	SEL	V_{DD} = 2.625V, V_{IN} = 0V	-150			µA

Table 4C. Differential Inputs Characteristics, V_{DD} = 2.5V ± 5%, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
I_{IH}	Input High Current	PCLK0, nPCLK0 PCLK1, nPCLK1	$V_{IN} = V_{DD} = 2.625V$			150	µA
I_{IL}	Input Low Current	PCLK0, PCLK1	$V_{IN} = 0V, V_{DD} = 2.625V$	-10			µA
		nPCLK0, nPCLK1	$V_{IN} = 0V, V_{DD} = 2.625V$	-150			µA
V_{REF0}, V_{REF1}	Reference Voltage for Input Bias		I_{REFx} = ±0.5mA	$(V_{DD}/2) – 0.15$	$V_{DD}/2$	$(V_{DD}/2) + 0.15$	V
V_{PP}	Peak-to-Peak Voltage[1]		f_{REF} < 1.5GHz	0.1		1.5	V
			f_{REF} > 1.5GHz	0.2		1.5	V
V_{CMR}	Common Mode Input Voltage[1, 2]			1.0		$V_{DD} – (V_{PP}/2)$	V

NOTE 1: V_{IL} should not be less than -0.3V. V_{IH} should not be greater than V_{DD}.
NOTE 2: Common mode input voltage is defined at the crosspoint.

Table 4D. LVDS DC Characteristics, V_{DD} = 2.5V ± 5%, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OD}	Differential Output Voltage	Outputs Loaded with 100Ω	247		454	mV
ΔV_{OD}	V_{OD} Magnitude Change				50	mV
V_{OS}	Offset Voltage		1.125		1.375	V
ΔV_{OS}	V_{OS} Magnitude Change				50	mV

AC Electrical Characteristics

Table 5. AC Electrical Characteristics, V_{DD} = 2.5V ± 5%, T_A = -40°C to 85°C[1]

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
f_{REF}	Input Frequency	PCLK[0:1], nPCLK[0:1]				2	GHz
ΔV/Δt	Input Edge Rate	PCLK[0:1], nPCLK[0:1]		1.5			V/ns
t_{PD}	Propagation Delay[2]		PCKx, nPCLKx to any Qx, nQx for V_{PP} = 0.1V or 0.3V	200	310	500	ps
*t*sk(o)	Output Skew[3, 4]					45	ps
*t*sk(p)	Pulse Skew[5, 6]		f_{REF} = 100MHz, 500MHz, 1GHz, 1.5GHz			80	ps
*t*sk(pp)	Part-to-Part Skew[4, 7]					300	ps
t_{JIT}	Buffer Additive Phase Jitter, RMS; refer to Additive Phase Jitter Section		f_{REF} = 156.25MHz, V_{PP} = 1.0V, V_{CMR} = 1V Integration Range: 10kHz – 20MHz		77	90	fs
t_R / t_F	Output Rise/ Fall Time		20% to 80% Outputs Loaded with 100Ω		100	200	ps
$MUX_{ISOLATION}$	Mux Isolation[8]		f_{REF} = 100MHz		75		dB

NOTE 1: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

NOTE 2: Measured from the differential input crosspoint to the differential output crosspoint.

NOTE 3: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the differential crosspoint.

NOTE 4: This parameter is defined in accordance with JEDEC Standard 65.

NOTE 5: Output pulse skew tsk(p) is absolute difference of the propagation delay times: $|t_{PLH} - t_{PHL}|$.

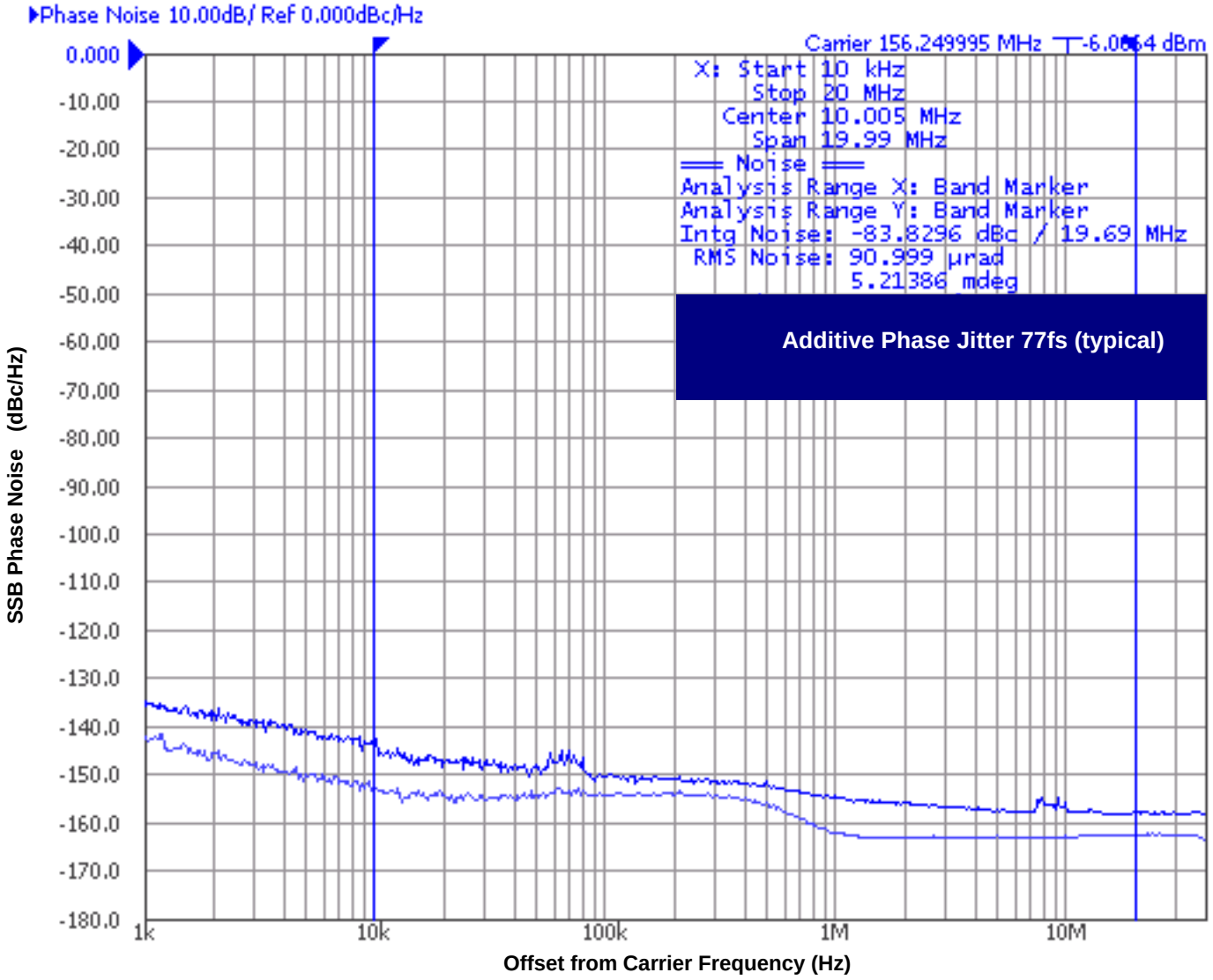
NOTE 6: Output duty cycle is frequency dependent: odc= input duty cycle +/- ((tsk(p)/2)*(1/output period))*100.

NOTE 7: Defined as skew between outputs on different devices operating at the same supply voltage, same frequency, same temperature and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential cross point.

NOTE 8: Qx, nQx outputs measured differentially. See *MUX Isolation diagram* in the *Parameter Measurement Information section.*

Additive Phase Jitter

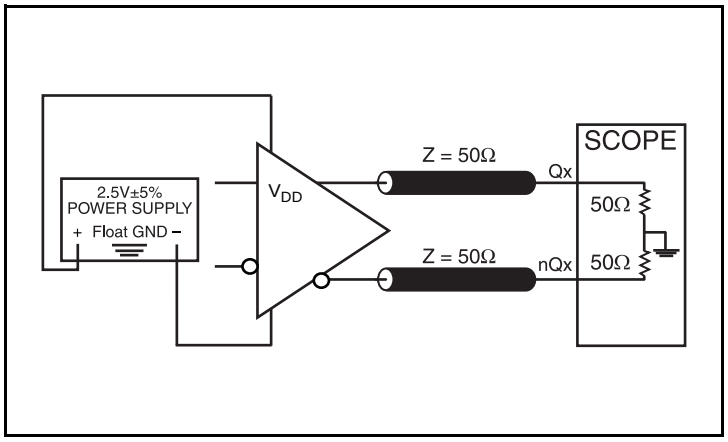
The spectral purity in a band at a specific offset from the fundamental compared to the power of the fundamental is called the ***dBc Phase Noise.*** This value is normally expressed using a Phase noise plot and is most often the specified plot in many applications. Phase noise is defined as the ratio of the noise power present in a 1Hz band at a specified offset from the fundamental frequency to the power value of the fundamental. This ratio is expressed in decibels (dBm) or a ratio of the power in the 1Hz band to the power in the fundamental. When the required offset is specified, the phase noise is called a ***dBc*** value, which simply means dBm at a specified offset from the fundamental. By investigating jitter in the frequency domain, we get a better understanding of its effects on the desired application over the entire time record of the signal. It is mathematically possible to calculate an expected bit error rate given a phase noise plot.



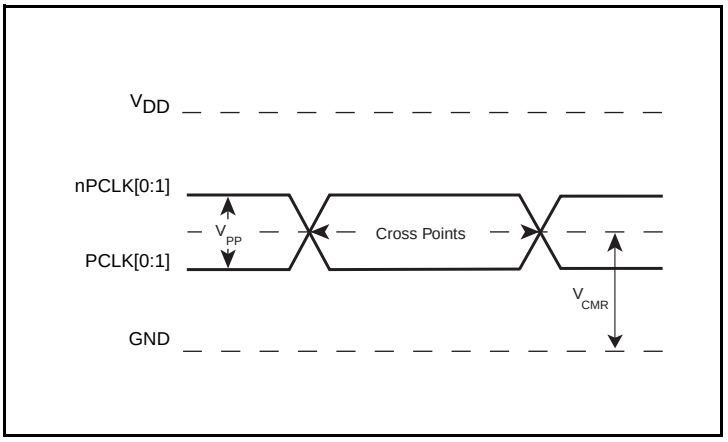
As with most timing specifications, phase noise measurements have issues relating to the limitations of the measurement equipment. The noise floor of the equipment can be higher or lower than the noise floor of the device. Additive phase noise is dependent on both the noise floor of the input source and measurement equipment.

Measured using a Wenzel 156.25MHz Oscillator as the input source.

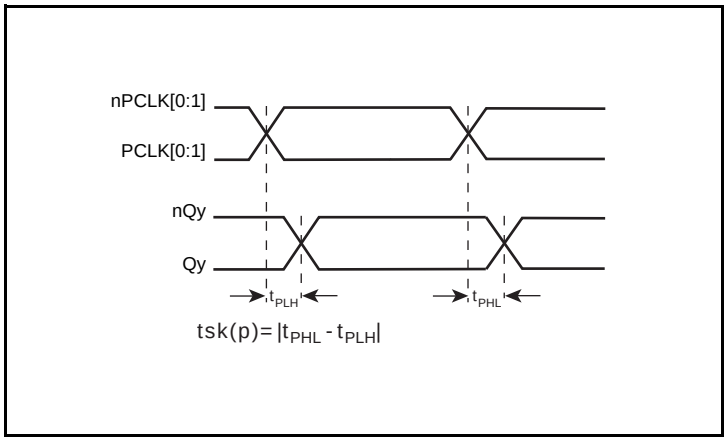
Parameter Measurement Information



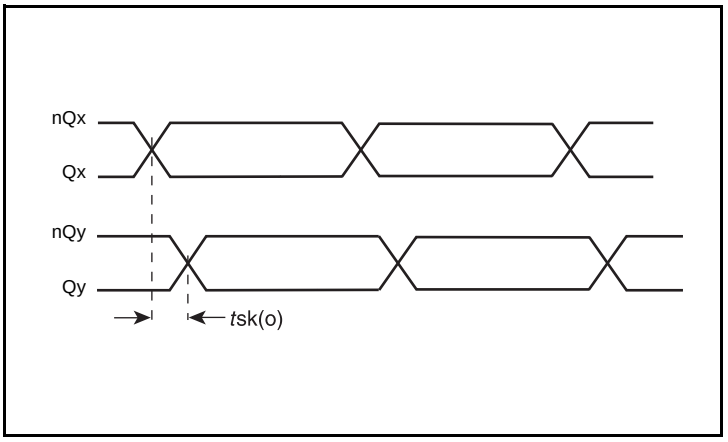
2.5V LVDS Output Load Test Circuit



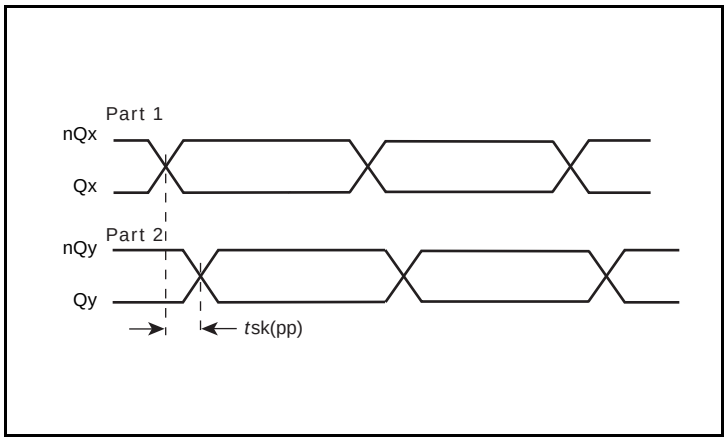
Differential Input Level



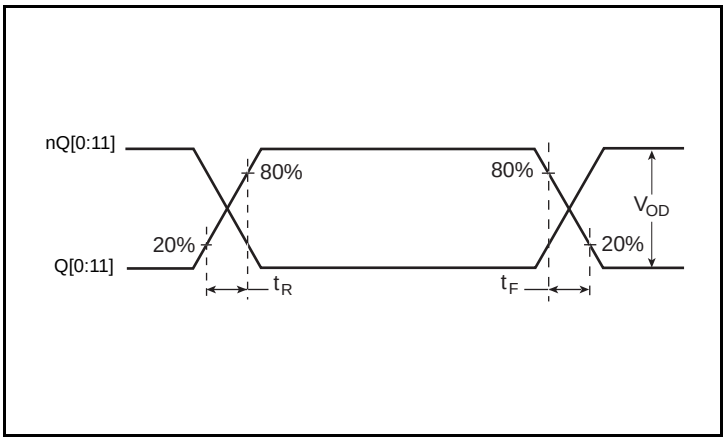
Pulse Skew



Output Skew

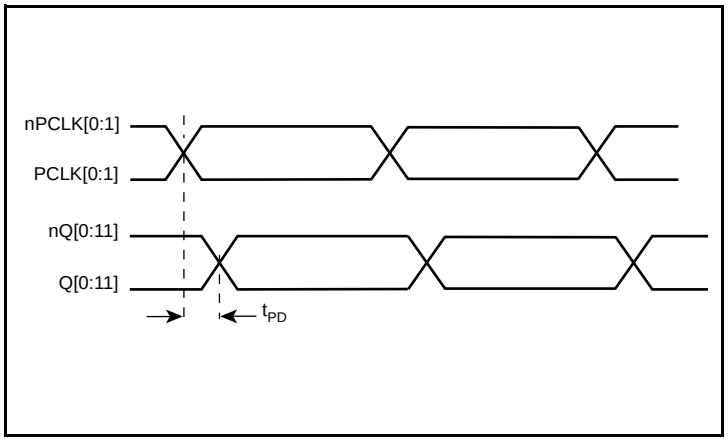


Part-to-Part Skew

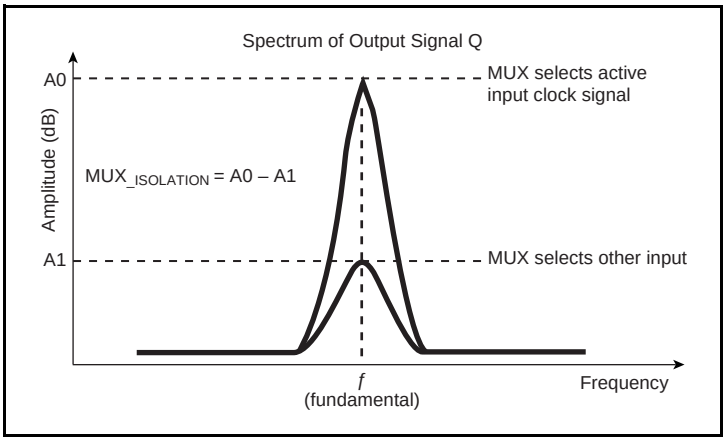


Output Rise/Fall Time

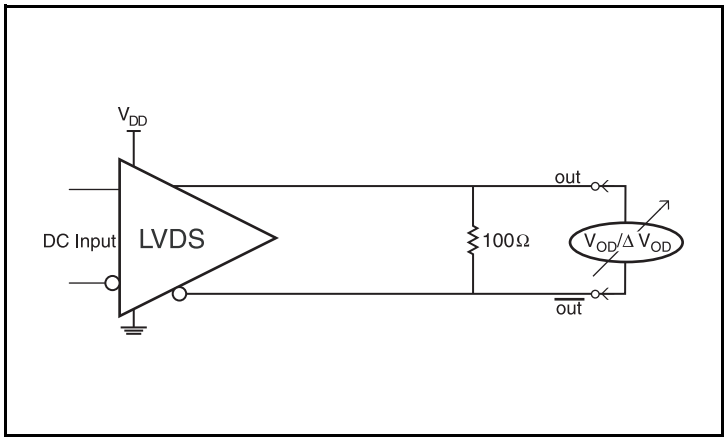
Parameter Measurement Information, continued



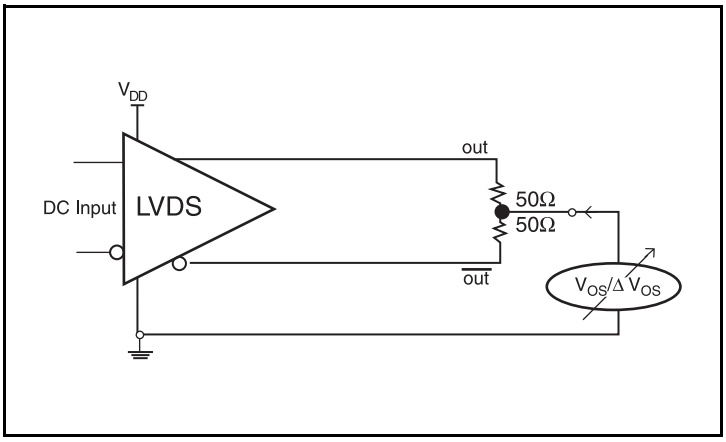
Propagation Delay



MUX Isolation



Differential Output Voltage Setup



Offset Voltage Setup

Applications Information

Recommendations for Unused Input and Output Pins

Inputs:

PCLK/nPCLK Inputs

For applications not requiring the use of a differential input, both the PCLK and nPCLK pins can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from PCLK to ground.

Outputs:

LVDS Outputs

All unused LVDS output pairs can be either left floating or terminated with 100Ω across. If they are left floating, there should be no trace attached.

Wiring the Differential Input to Accept Single-Ended Levels

Figure 1 shows how a differential input can be wired to accept single ended levels. The reference voltage V1 = V_{DD}/2 is generated by the bias resistors R1 and R2. The bypass capacitor (C1) is used to help filter noise on the DC bias. This bias circuit should be located as close to the input pin as possible. The ratio of R1 and R2 might need to be adjusted to position the V1 in the center of the input voltage swing. For example, if the input clock swing is 2.5V and V_{DD} = 2.5V, R1 and R2 value should be adjusted to set V1 at 1.25V. The values below are for when both the single ended swing and V_{DD} are at the same voltage. This configuration requires that the sum of the output impedance of the driver (Ro) and the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the input will attenuate the signal in half. This can be done in one of two ways. First, R3 and R4 in parallel should equal the transmission line impedance. For most 50Ω applications, R3 and R4 can be 100Ω.

The values of the resistors can be increased to reduce the loading for slower and weaker LVCMOS driver. When using single-ended signaling, the noise rejection benefits of differential signaling are reduced. Even though the differential input can handle full rail LVCMOS signaling, it is recommended that the amplitude be reduced. The datasheet specifies a lower differential amplitude, however this only applies to differential signals. For single-ended applications, the swing can be larger, however V_{IL} cannot be less than -0.3V and V_{IH} cannot be more than V_{DD} + 0.3V. Suggested edge rate faster than 1V/ns. Though some of the recommended components might not be used, the pads should be placed in the layout. They can be utilized for debugging purposes. The datasheet specifications are characterized and guaranteed by using a differential signal.

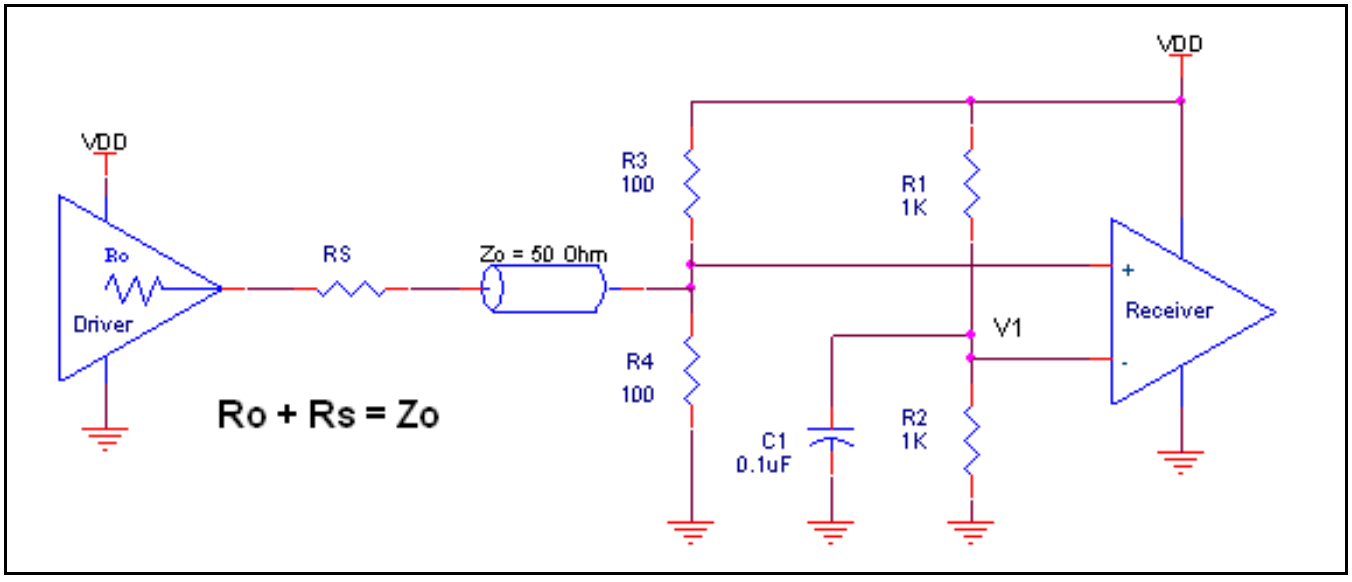


Figure 1. Recommended Schematic for Wiring a Differential Input to Accept Single-ended Levels

2.5V LVPECL Clock Input Interface

The PCLK /nPCLK accepts LVPECL, LVDS, CML and other differential signals. Both signals must meet the V_{PP} and V_{CMR} input requirements. *Figure 2A to Figure 2E* show interface examples for the PCLK/ nPCLK input driven by the most common driver types. The input interfaces suggested here are examples only. If the driver is from another vendor, use their termination recommendation. Please consult with the vendor of the driver component to confirm the driver termination requirements.

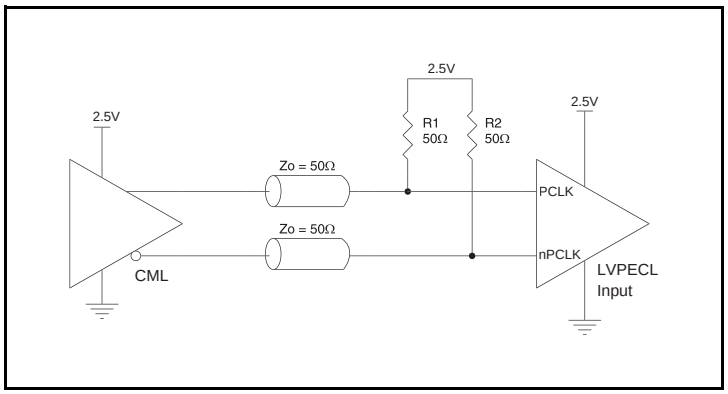


Figure 2A. PCLK/nPCLK Input Driven by a CML Driver

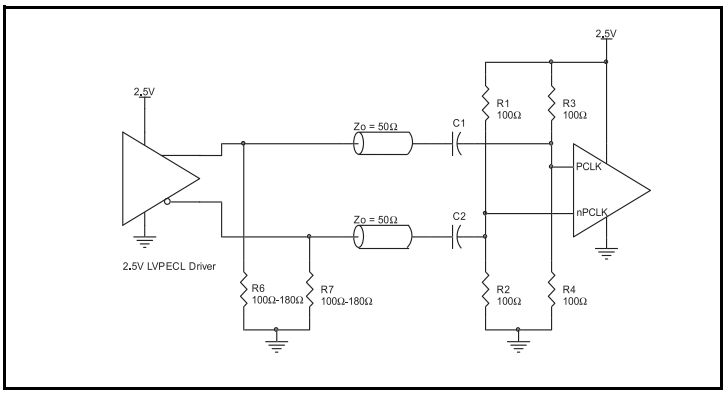


Figure 2D. PCLK/nPCLK Input Driven by a 2.5V LVPECL Driver with AC Couple

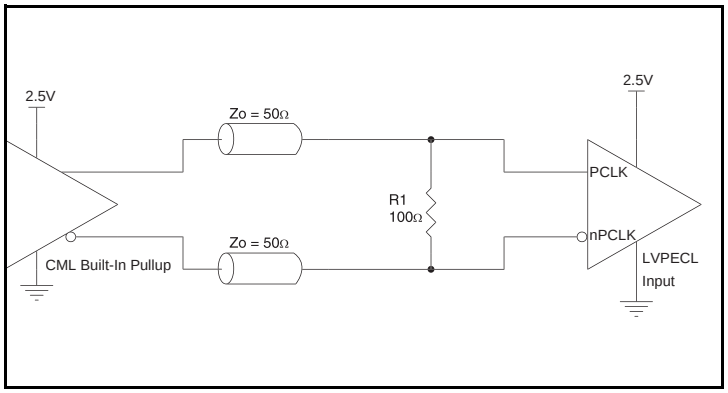


Figure 2B. Figure 2C.PCLK/nPCLK Input Driven by a Built-In Pullup CML Driver

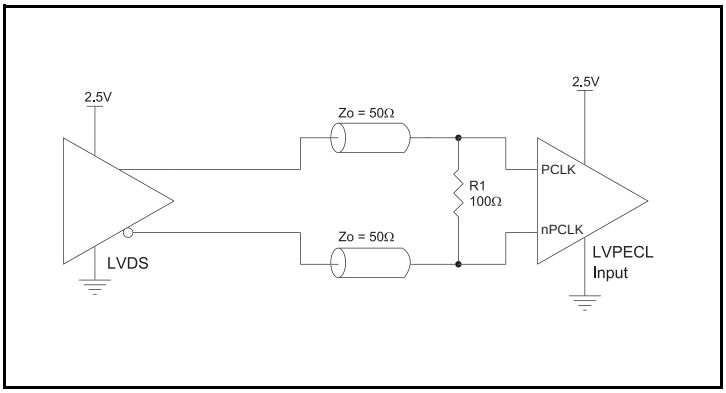


Figure 2E. PCLK/nPCLK Input Driven by a 2.5V LVDS Driver

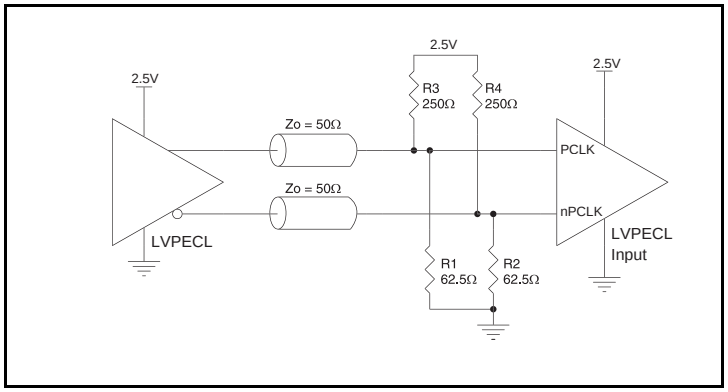


Figure 2C. PCLK/nPCLK Input Driven by a 2.5V LVPECL Driver

LVDS Driver Termination

For a general LVDS interface, the recommended value for the termination impedance (Z_T) is between 90Ω and 132Ω. The actual value should be selected to match the differential impedance (Z_0) of your transmission line. A typical point-to-point LVDS design uses a 100Ω parallel resistor at the receiver and a 100Ω differential transmission-line environment. In order to avoid any transmission-line reflection issues, the components should be surface mounted and must be placed as close to the receiver as possible. IDT offers a full line of LVDS compliant devices with two types of output structures: current source and voltage source. The standard termination schematic as shown in *Figure 3A* can be used with either type of output structure. *Figure 3B*, which can also be used with both output types, is an optional termination with center tap capacitance to help filter common mode noise. The capacitor value should be approximately 50pF. If using a non-standard termination, it is recommended to contact IDT and confirm if the output structure is current source or voltage source type. In addition, since these outputs are LVDS compatible, the input receiver's amplitude and common-mode input range should be verified for compatibility with the output.

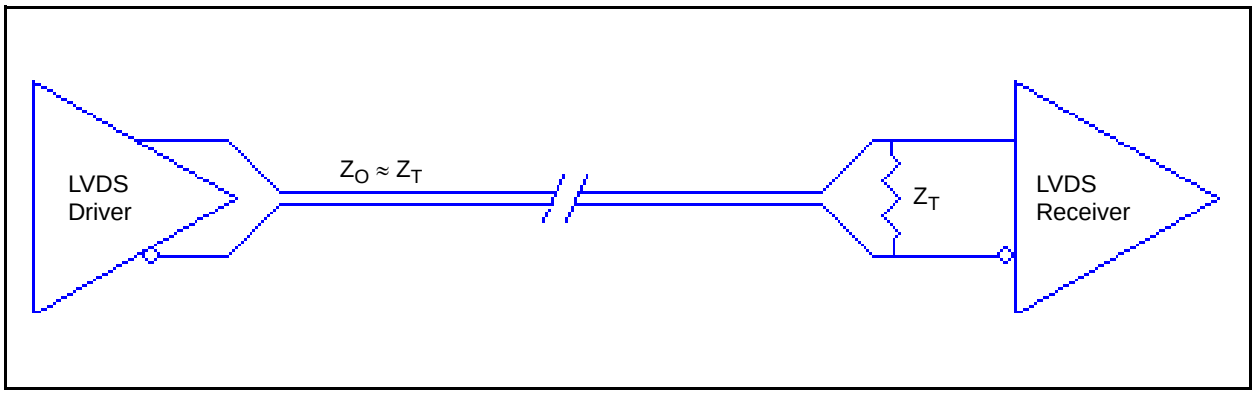


Figure 3A. Standard LVDS Termination

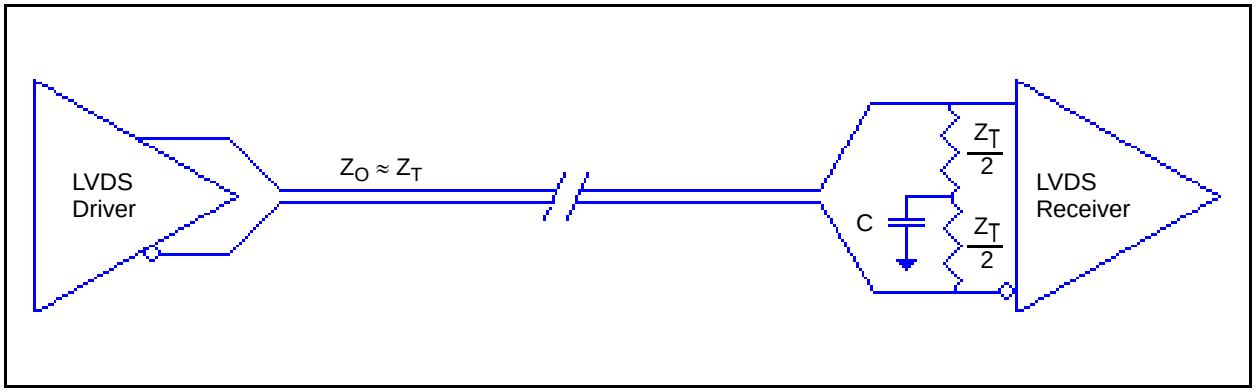


Figure 3B. Optional LVDS Termination

VFQFN EPAD Thermal Release Path

In order to maximize both the removal of heat from the package and the electrical performance, a land pattern must be incorporated on the Printed Circuit Board (PCB) within the footprint of the package corresponding to the exposed metal pad or exposed heat slug on the package, as shown in *Figure 4.* The solderable area on the PCB, as defined by the solder mask, should be at least the same size/shape as the exposed pad/slug area on the package to maximize the thermal/electrical performance. Sufficient clearance should be designed on the PCB between the outer edges of the land pattern and the inner edges of pad pattern for the leads to avoid any shorts.

While the land pattern on the PCB provides a means of heat transfer and electrical grounding from the package to the board through a solder joint, thermal vias are necessary to effectively conduct from the surface of the PCB to the ground plane(s). The land pattern must be connected to ground through these vias. The vias act as “heat pipes”. The number of vias (i.e. “heat pipes”) are application specific and dependent upon the package power dissipation as well as electrical conductivity requirements. Thus, thermal and electrical analysis and/or testing are recommended to determine the minimum number needed. Maximum thermal and electrical performance is achieved when an array of vias is incorporated in the land pattern. It is recommended to use as many vias connected to ground as possible. It is also recommended that the via diameter should be 12 to 13mils (0.30 to 0.33mm) with 1oz copper via barrel plating. This is desirable to avoid any solder wicking inside the via during the soldering process which may result in voids in solder between the exposed pad/slug and the thermal land. Precautions should be taken to eliminate any solder voids between the exposed heat slug and the land pattern. Note: These recommendations are to be used as a guideline only. For further information, please refer to the Application Note on the Surface Mount Assembly of Amkor’s Thermally/ Electrically Enhance Leadframe Base Package, Amkor Technology.

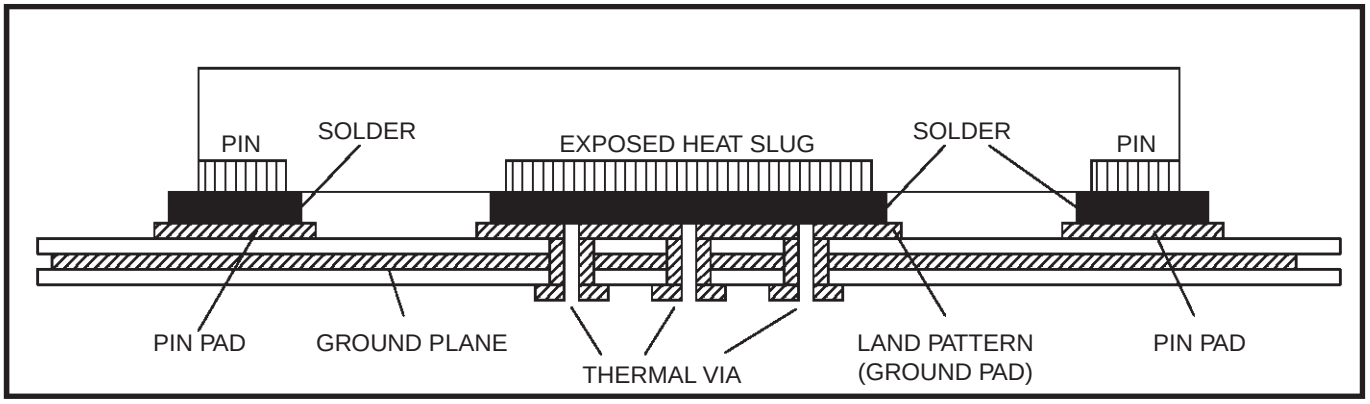


Figure 4. P.C. Assembly for Exposed Pad Thermal Release Path – Side View (drawing not to scale)

Power Considerations

This section provides information on power dissipation and junction temperature for the 8SLVD1212I. Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the 8SLVD1212I is the sum of the core power plus the output power dissipation due to the load. The following is the power dissipation for V_{DD} = 2.5V + 5% = 2.625V, which gives worst case results.

The maximum current at 85°C is as follows:

I_{DD_MAX} = 213mA

- Power $_{(core)MAX}$ = V_{DD_MAX} * I_{DD_MAX} = 2.625V * 213mA = **559.125mW**

Total Power$_{_MAX}$ = 559.125mW

2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature, Tj, to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for Tj is as follows: Tj = θ_{JA} * Pd_total + TA

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 33°C/W per *Table 6* below.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:

85°C + 0.559W * 33°C/W = 103.5°C. This is below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

Table 6. Thermal Resistance θ_{JA} for 40-Lead VFQFN, Forced Convection

θ_{JA} (°C/W) vs. Air Flow (m/s)			
Meters per Second	**0**	**1**	**2**
Multi-Layer PCB, JEDEC Standard Test Boards	33°C/W	26.3°C/W	24°C/W

Reliability Information

Table 7. θ_{JA} vs. Air Flow Table for a 40-Lead VFQFN, Forced Convection

θ_{JA} (°C/W) vs. Air Flow (m/s)			
Meters per Second	**0**	**1**	**2**
Multi-Layer PCB, JEDEC Standard Test Boards	33°C/W	26.3°C/W	24°C/W

Transistor Count

The transistor count for the 8SLVD1212 is: 8301

40-Lead VFQFN Package Outline and Package Dimensions

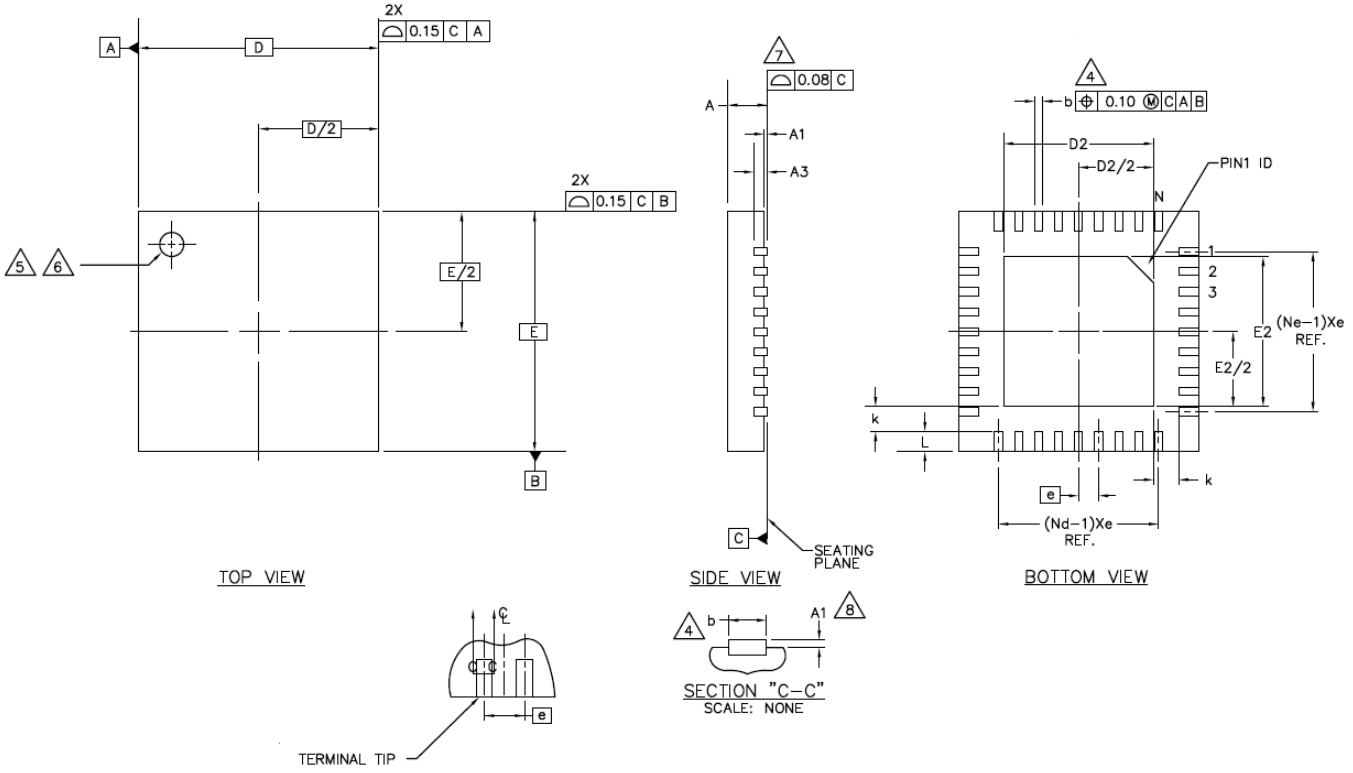


Table 8. Package Dimensions for 40-Lead Package

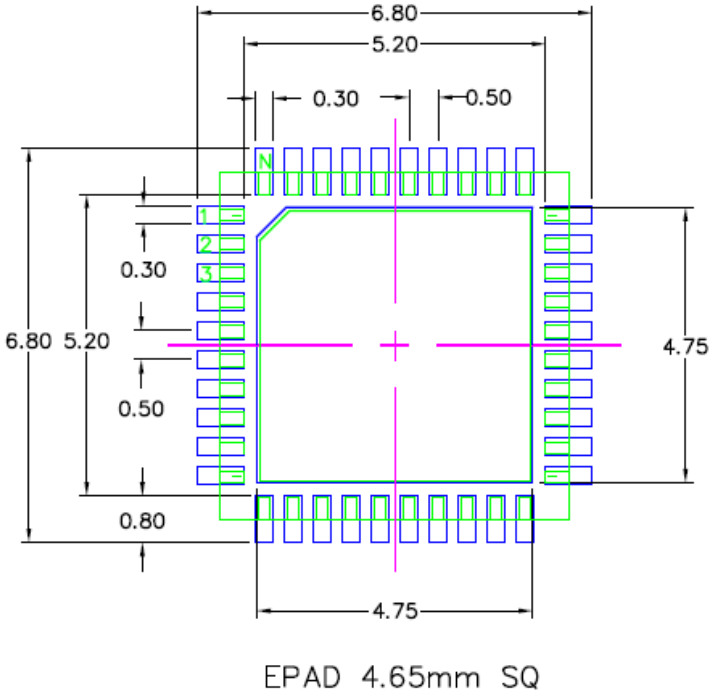
SYMBOL	DIMENSIONS			
	MIN	NOM	MAX	NOTE
b	0.18	0.25	0.3	4
D		6.00 BSC		
E		6.00 BSC		
D2	4.50	4.65	4.75	
E2	4.50	4.65	4.75	
L	0.30	0.40	0.50	
e		0.50 BSC		
N		40		2
A	0.80	0.90	1.00	
A1	0.00	0.02	0.05	7
A3		0.2 REF		
Nd and Ne		10		2

NOTES:

The drawing and dimension data originates from IDT Package Outline Drawing PSC-4115, Rev 07.

1. Dimensions and tolerances conform to ASME Y14.5M-1994.
2. N is the number of terminals.
   Nd is the number of terminals in X-direction.
   Ne is the number of terminals in Y-direction.
3. All dimensions are in millimeters.
4. Dimension b applies to plated terminal and is measured between 0.20 and 0.30mm from terminal tip.
5. The Pin #1 identifier must exist on the top surface of the package by using indentation mark or other feature of package body.
6. Exact shape and size of this feature is optional.
7. Applied to exposed pad and terminals. Exclude embedded part of exposed pad from measuring.
8. Applied only for terminals.
9. This outline conforms to JEDEC Publication 95, Registration MO-220, Variation VJJD-5 with exception of D2 & E2.

Recommended Land Pattern



NOTES:

The Recommended Land Pattern originates from IDT Package Outline Drawing PSC-4115, Rev 07.

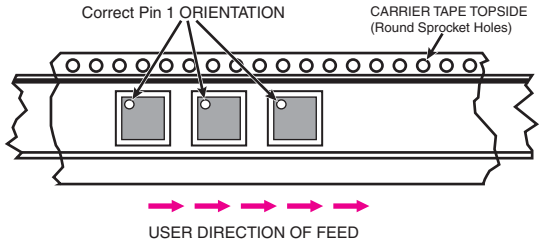
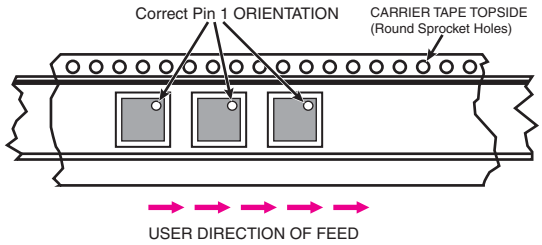
1. All dimensions are in millimeters. Angles in degrees.
2. Top down view, as viewed on PCB.
3. Component outline shows for reference in green.
4. Land pattern in blue, NSMD pattern assumed.
5. Land pattern recommendation per IPC-7351B generic requirement for surface mount design and land pattern.

Ordering Information

Table 9. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
8SLVD1212NLGI	IDT8SLVD1212NLGI	40-Lead VFQFN, Lead-Free	Tray	-40°C to 85°C
8SLVD1212NLGI8	IDT8SLVD1212NLGI	40-Lead VFQFN, Lead-Free	Tape & Reel, pin 1 orientation: EIA-481-C	-40°C to 85°C
8SLVD1212NLGI/W	IDT8SLVD1212NLGI	40-Lead VFQFN, Lead-Free	Tape & Reel, pin 1 orientation: EIA-481-D	-40°C to 85°C

Table 10. Pin 1 Orientation in Tape and Reel Packaging

Part Number Suffix	Pin 1 Orientation	Illustration
8	Quadrant 1 (EIA-481-C)	
/W	Quadrant 2 (EIA-481-D)	

Revision History Sheet

Rev	Table	Page	Description of Change	Date
2		17 - 18	Corrected package drawings.	08/21/15
3	T6 T7	15 16	Thermal Resistance table description, corrected the word “Convection”, updated table header. Reliability table description, added “Forced Convection”, updated table header. Updated datasheet header/footer.	7/5/16

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