

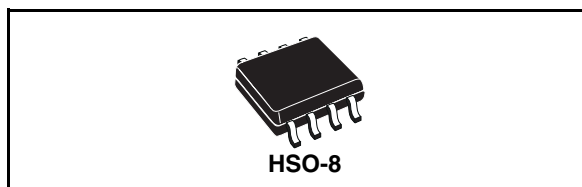
High performance 2A ULDO linear regulator

Features

- 2V to 14V input voltage range
- 200mΩ $r_{DS(on)}$ max
- 200μA quiescent current at any load
- Excellent load and line regulation
- Adjustable from 1.2V to 5V
- 1% voltage regulation accuracy
- Short circuit protection
- Thermal shut down
- HSOP8 package

Applications

- Motherboards
- Mobile PC
- Hand-held instruments
- PCMCIA Cards
- Processors I/O
- Chipset and RAM supply



Description

The L6932 Ultra Low Drop Output linear regulator operates from 2V to 14V and is able to support output current up to 2A. Designed with an internal 50mΩ N-channel Mosfet, it can be used for onboard DC-DC conversions saving in real estate, list of components, low noise generation and power dissipation.

L6932H1.2 is available as adjustable version from 1.2V to 5V with a voltage regulation accuracy of 1%.

The upper current limit is fixed at 2.5A to control the current in short circuit condition within ±8%. The current is sensed in the power mos in order to limit the power dissipation.

The device is also provided with a thermal shut down that limits the internal temperature at 150°C with a hysteresis of 20°C. L6932H1.2 provides the Enable and the Power good functions.

Figure 1. Typical operating circuit

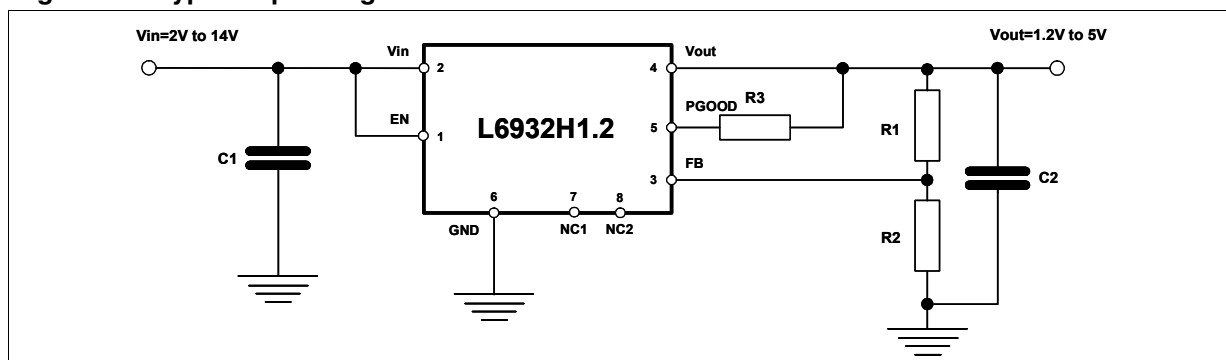


Table 1. Device summary

Part number	Package	Packaging
L6932H1.2	HSO-8	Tube
L6932H1.2TR	HSO-8	Tape and reel

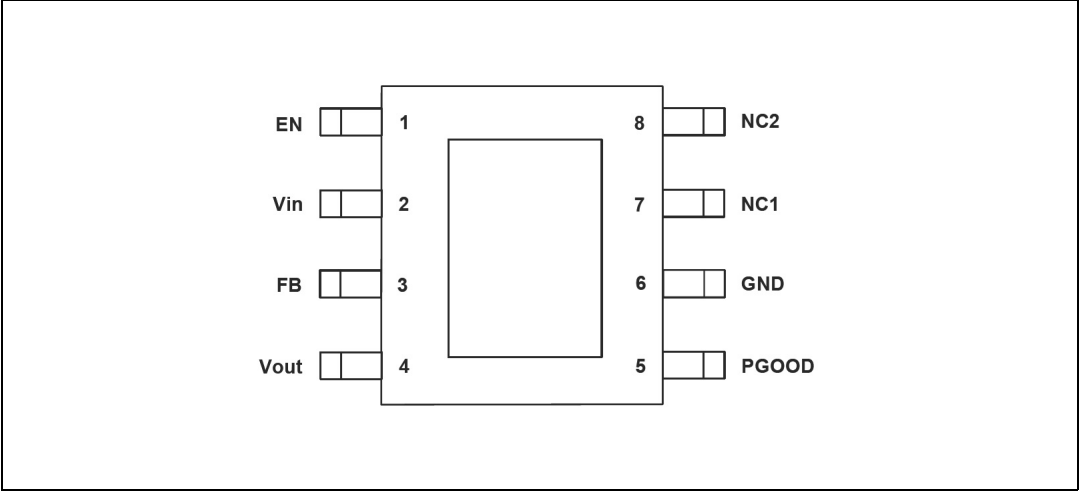
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1 Pin settings

1.1 Pin connection

Figure 2. Pin connection (top view)



1.2 Pin description

Table 2. Pin description

Name	Pin N°	Description
1	EN	Enables the device when connected to Vin and disables it when forced to GND.
2	VIN	Supply voltage. This pin is connected to the drain of the internal N-mos. Connect this pin to a capacitor larger than 10μF.
3	FB	Connecting this pin to a voltage divider it is possible to program the output voltage between 1.2V and 5V.
4	VOOUT	Regulated output voltage. This pin is connected to the source of the internal N-mos. Connect this pin to a capacitor of 10μF.
5	PGOOD	Power good output. The pin is open drain and detects the output voltage. It is forced low if the output voltage is lower than 90% of the programmed voltage.
6	GND	Ground pin
7, 8	NC1-NC2	Internally not connected.

2 Maximum ratings

2.1 Absolute maximum ratings

Table 3. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{IN}	VIN and PGOOD	14.5	V
	EN, OUT and ADJ	-0.3 to (Vin +0.3)	V

2.2 Thermal data

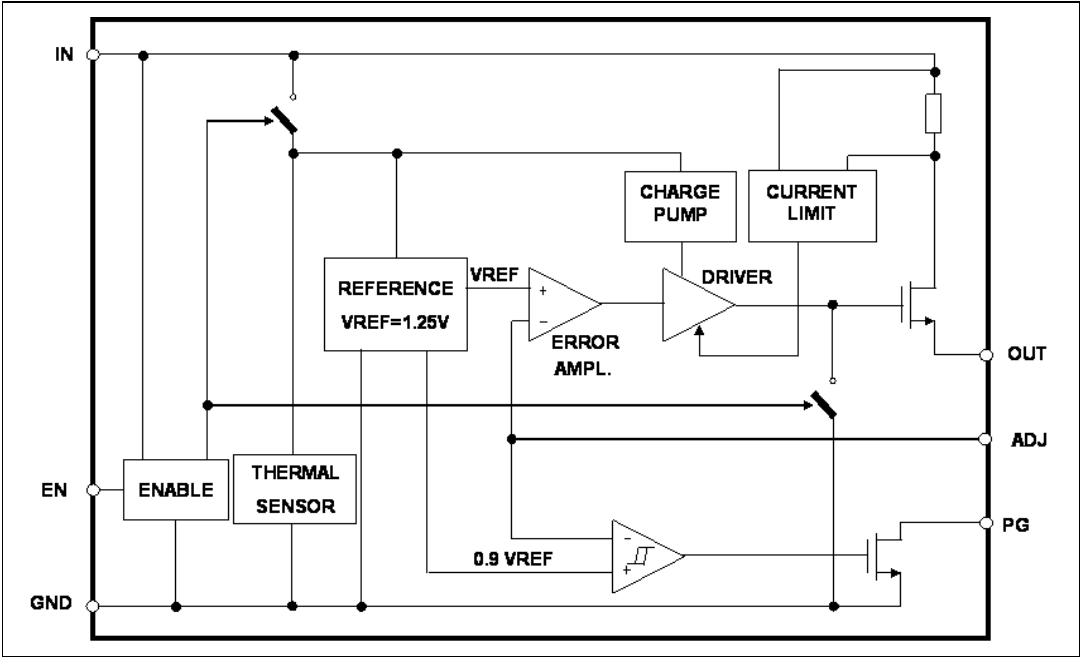
Table 4. Thermal data

Symbol	Parameter	Value	Unit
R_{thJA}	Maximum thermal resistance junction-ambient	34 ⁽¹⁾	°C/W
T_{MAX}	Maximum junction temperature	150	°C
T_{STG}	Storage temperature range	-65 to 150	°C

1. Package mounted on board

3 Block diagram

Figure 3. Internal block diagram



4 Electrical characteristics

Table 5. Electrical characteristics ($T_J = 25^\circ\text{C}$, $V_{IN} = 5\text{V}$ unless otherwise specified)

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
V_{IN}	Operating Supply Voltage		2		14	V
V_O	Output voltage	$I_O = 0.1\text{A}$; $V_{IN} = 3.3\text{V}$	1.188	1.2	1.212	V
	Line Regulation	$V_{IN} = 2.5\text{V} \pm 10\%$; $I_O = 10\text{mA}$			5	mV
		$V_{IN} = 3.3\text{V} \pm 10\%$; $I_O = 10\text{mA}$			5	mV
		$V_{IN} = 5\text{V} \pm 10\%$; $I_O = 10\text{mA}$			5	mV
	Load Regulation	$V_{IN} = 3.3\text{V}$; $0.1\text{A} < I_O < 2\text{A}$			15	mV
$r_{DS(on)}$	Drain Source ON resistance				200	$\text{m}\Omega$
I_{OCC}	Current limiting		2.3	2.5	2.7	A
I_q	Quiescent current			0.2	0.4	mA
I_{sh}	Shutdown current	$2\text{V} < V_{IN} < 14\text{V}^{(1)}$			25	μA
	Ripple Rejection	$f = 120\text{Hz}$, $I_O = 1\text{A}$, $V_{IN} = 5\text{V}$, $\Delta V_{IN} = 2\text{V}_{pp}$	60	75		dB
V_{en}	EN Input Threshold		0.5	0.65	0.8	V
	Pgood threshold	V_O rise		90		% V_O
	Pgood Hysteresis			10		% V_O
	Pgood saturation	$I_{pgood} = 1\text{mA}$		0.2	0.4	V

1. Specification referred to T from -25°C to 125°C .

5 Typical electrical performance

Figure 4. Output voltage vs junction temperature

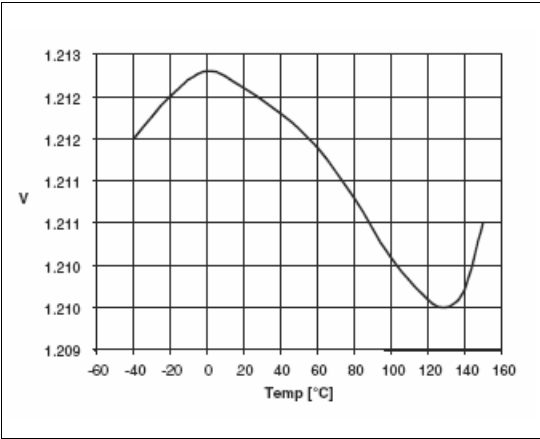


Figure 5. Quiescent current vs junction temperature

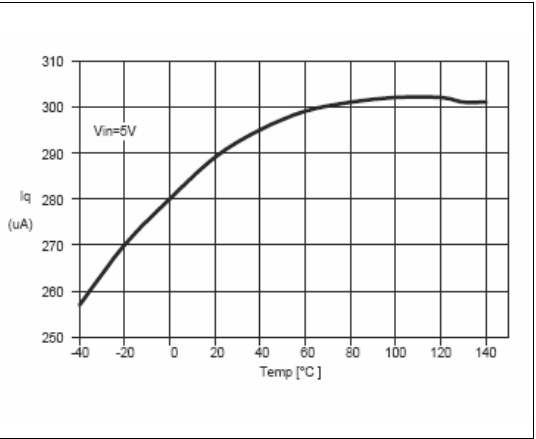


Figure 6. Shutdown current vs junction temperature

