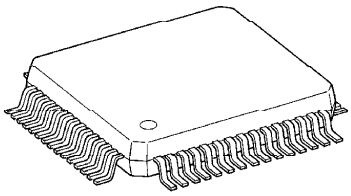
TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

TC9297F, TC9297FB

LCD DRIVER WITH ON-CHIP KEY INPUT

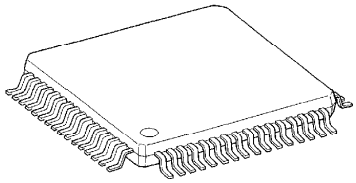
TC9297F/FB are an LCD driver IC with on-chip key input, which is serial data controlled.

TC9297F



QFP60-P-1414-0.80D

TC9297FB



QFP64-P-1212-0.65

Weight
QFP60-P-1414-0.80D : 1.10g (Typ.)
QFP64-P-1212-0.65 : 0.45g (Typ.)

FEATURES

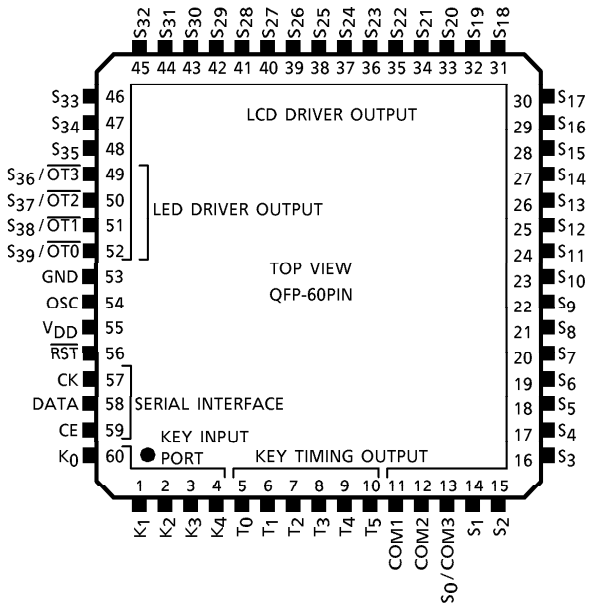
- Supports switching between 1/2 and 1/3 duty, and between 1/2 and 1/3 bias.
- Displays up to 80 segments in 1/2-duty mode and up to 117 segments in 1/3-duty mode.
- All display segments can be either off or on. Outputs of pins S_{36}-S_{39} can be switched between segment output and LED driver output.
- Supports key input from up to 30 keys.
- 3-wire configuration for controller connection.

961001EBA1

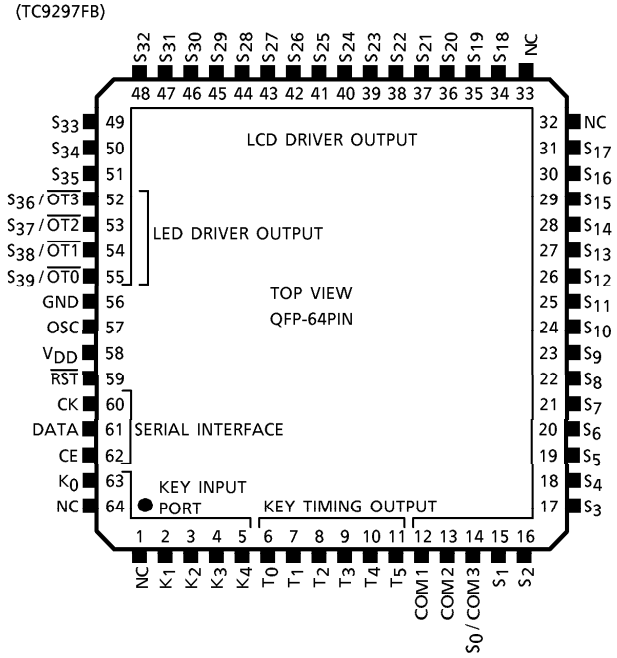
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PIN CONNECTION

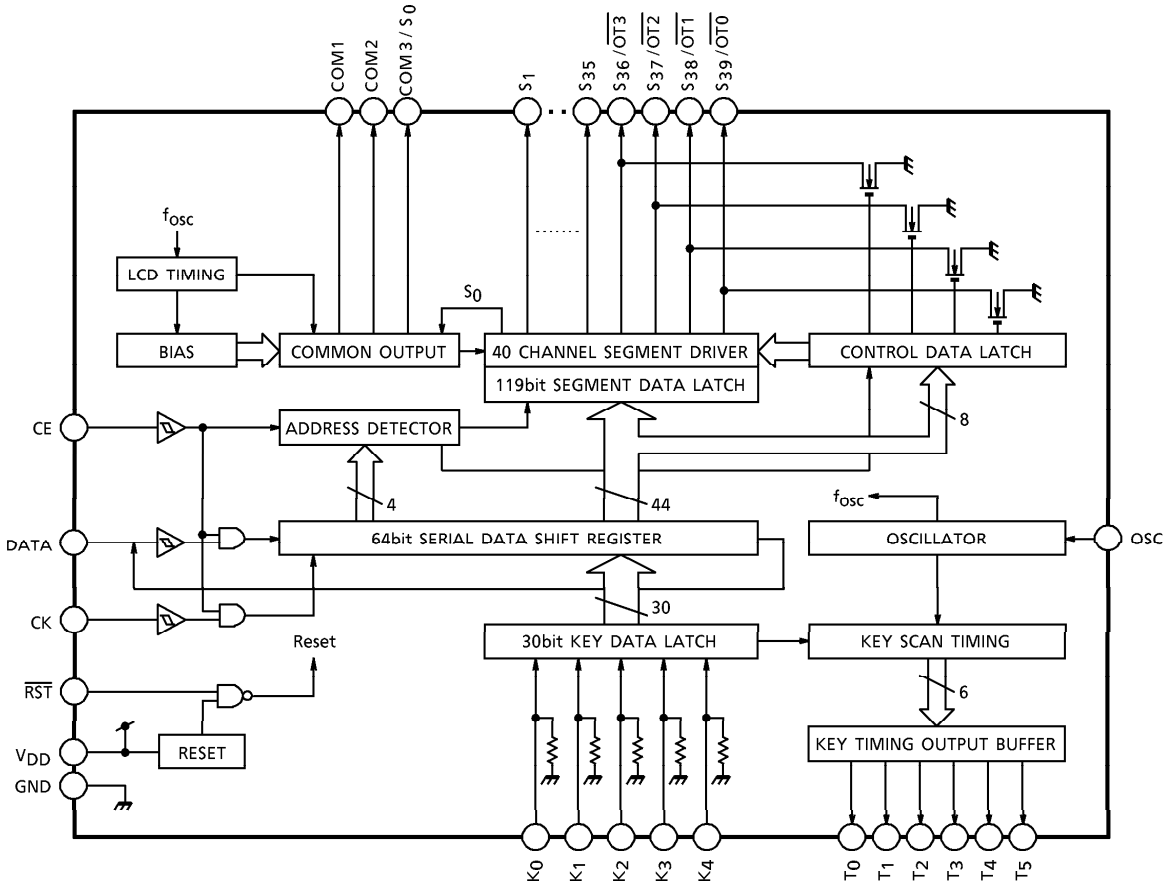
(TC9297F)



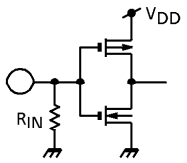
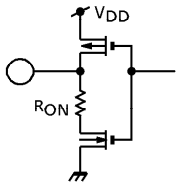
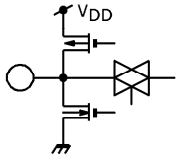
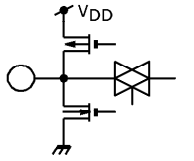
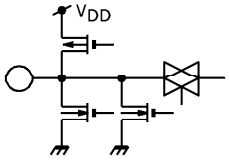
(TC9297FB)

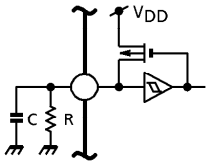
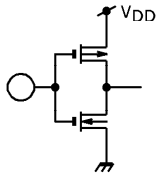
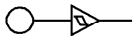
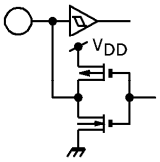
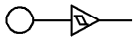


BLOCK DIAGRAM



PIN FUNCTIONS (Data in parenthesizes are for TC9297FB)

PIN No.	SYMBOL	PIN NAME	FUNCTION AND OPERATION	REMARKS
55 (58)	V_{DD}	Power supply input pin	Power supply input pin. Normally supplied with VRST-5.5V. Power-on reset function resets system when powered up and when V_{DD} drops below 3V (Typ.).	—
53 (56)	GND	Ground pin		
60 (63) 1 (2) ~ 4 (5)	K_0 K_1 ~ K_4	Key-scan input pin	Key-scan input pins. Data from up to $6 \times 5 = 30$ keys can be input by a key matrix with key scan output pins T_0-T_5. When high is input to pins, key scan begins. These are I/O pins with built-in pull-down resistors.	
5 (6) ~ 10 (11)	T_0 ~ T_5	Key scan timing output pin	Key scan timing output pins. Due to key matrix configured using load resistor RON on the N-channel, no diodes are required. Output is normally high. When high is input to key scan input pins K_0-K_4, key scan begins.	
11 (12) 12 (13)	COM1 COM2	LCD common output pin	LCD segment output/common output pins. When set to 1/2-duty, can display up to 80 segments in a matrix of pins COM1, 2 and S_0-S_{39}; when set to 1/3-duty, up to 117 segments in a matrix of COM1-3 and S_1-S_{39}. In 1/3-duty mode, pin S_0 is used as COM3.	
13 (14)	S_0/ COM3	LCD segment output /common output pin		
14 (15~31) ~ 48 (34~51)	S_1 ~ S_{35}	LCD segment output pin	LCD segment output/LED driver output pins. When set to 1/2-duty, can display up to 80 segments in a matrix of pins COM1, 2 and S_0-S_{39}; when set to 1/3-duty, up to 117 segments in a matrix of COM1-3 and S_1-S_{39}. Pins S_{36}-S_{39} also serve as LED driver pins. The LED driver output becomes N-ch open driver output, and large-current drive allows direct LED display.	
49 (52) ~ 52 (55)	S_{36}/$\overline{OT3}$ ~ S_{39}/$\overline{OT0}$	LCD segment output /LED driver output pin		

PIN No.	SYMBOL	PIN NAME	FUNCTION AND OPERATION	REMARKS
54 (57)	OSC	Crystal oscillator output pin	Oscillates when connected to an external crystal. The oscillation frequency is expressed by the frequency expression : $f_{OSC} \simeq 1.5 / (C.R)$ [Hz] For instance, when C = 0.01μF, R = 30kΩ : $f_{OSC} \simeq 5$kHz	
56 (59)	$\overline{RST}$	System reset input pin	System reset input pin. While RST input is low, the oscillator stops, all internal data are reset, and the LCD output and key scan output pins are fixed to high. There is a built-in power-on reset circuit, so this pin should normally be connected to V_{DD}.	
57 (60)	CK	Clock input pin	Serial interface pins that send to and receive from the controller display data and key input data, and the data to control these. Data send / receive is not performed while pin CE is low, but when CE goes high, begins at the DATA pins in sync with the clock input of the CK input pin. All these pins have built-in Schmitt input circuits.	
58 (61)	DATA	Data I / O pin		
59 (62)	CE	Chip enable input pin		

○ CONTENT OF ADDRESS DATA

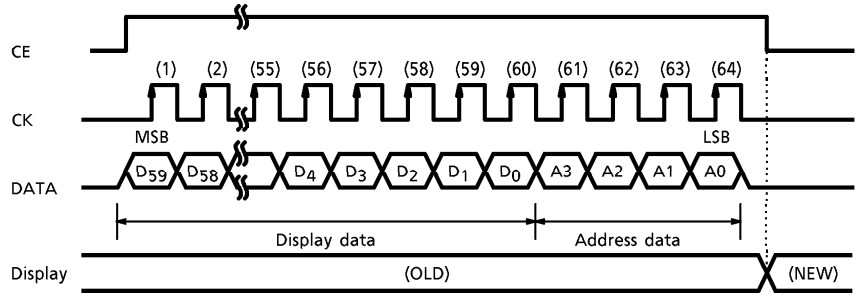
DUTY	A3	A2	A1	A0	ADDRESS (HEX)	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7	D_8~D_{32}	D_{33}~D_{39}	D_{40}~D_{59}
1/2	0	*	*	1	1, 3, 5, 7	S_0~S_{19} Display Data										
						S_0		S_1		S_2		S_3		S_4~S_{19}		—
						COM2 System	COM1 System	COM2 System	COM1 System	COM2 System	COM1 System	COM2 System	COM1 System	COM2, 1 System		
	0	*	1	*	2, 3, 6, 7	S_{20}~S_{39} Display Data										
						S_{20}		S_{21}		S_{22}		S_{23}		S_{24}~S_{39}		—
						COM2 System	COM1 System	COM2 System	COM1 System	COM2 System	COM1 System	COM2 System	COM1 System	COM2, 1 System		
1/3	0	*	*	1	1, 3, 5, 7	S_0~S_{19} Display Data										
						S_0			S_1			S_2~S_{19}				
						—			COM3 System	COM2 System	COM1 System	COM3, 2, 1 System				
	0	*	1	*	2, 3, 6, 7	S_{20}~S_{39} Display Data										
						S_{20}			S_{21}			S_{22}~S_{39}				
						COM3 System	COM2 System	COM1 System	COM3 System	COM2 System	COM1 System	COM3, 2, 1 System				
*	1	0	0	0	8	SET SEGMENT OUTPUT/LED DRIVER				LCD CONTROL		"0"	"0"	—		
						S_{39}/OT0	S_{38}/OT1	S_{37}/OT2	S_{36}/OT3	Duty	Bias					
	1	0	0	1	9	LED DRIVER CONTROL				DISPLAY CONTROL			"0"	—		
						OT0	OT1	OT2	OT3	OP	BL	LT				
	1	0	1	0	A	KEY DATA (OUTPUT)										"0"
						K_{ON}	K_{WK}	K_{01}	K_{02}	K_{03}	K_{04}	K_{05}	K_{06}	K_{07}~K_{30}		

* : Don't care
— : Invalid data

OPERATING INSTRUCTIONS

1. Input format for display data and mode data

- Display data input timing is as shown below (when set to 1/3-duty) :



For rise and fall times, see Electrical Characteristics.

- The last 4 bits of data are the address data.
- For segment data and control data corresponding to the segment data output being used, set all bits used.
- Segment data corresponding to the unused segment outputs of the MSB may be omitted.
- Segment data may be set to either address 1H or 2H.
- Do not set segment data until the data at address 8H have been set. Otherwise, it may be impossible to set segment data correctly.
- Data input is synchronized with the clock rising edge.

(1) 1/2-duty (80-segment) data format

The format for display data in 1/2-duty mode is as shown below:

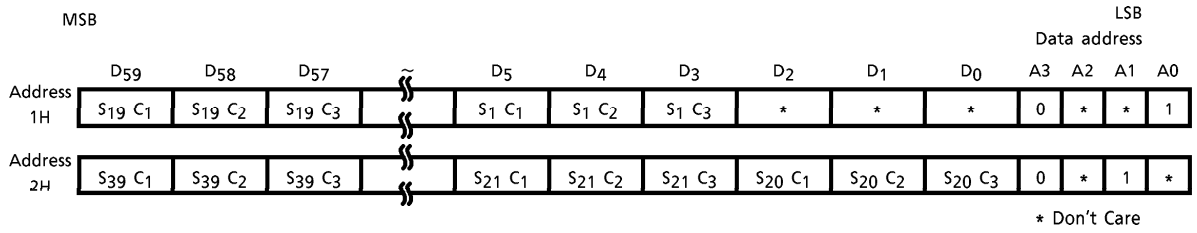
	MSB										LSB			
	D_{39}	D_{38}	D_{37}	D_{36}	D_{35}	D_{34}	~	D_3	D_2	D_1	D_0	Data address A3	A2	A1	A0
Address 1H	S_{19} C_1	S_{19} C_2	S_{18} C_1	S_{18} C_2	S_{17} C_1	S_{17} C_2		S_1 C_1	S_1 C_2	S_0 C_1	S_0 C_2	0	*	*	1
Address 2H	S_{39} C_1	S_{39} C_2	S_{38} C_1	S_{38} C_2	S_{37} C_1	S_{37} C_2		S_{21} C_1	S_{21} C_2	S_{20} C_1	S_{20} C_2	0	*	1	*

* Don't Care

- In this case, segment data controlled by COM3 are invalid, and data need not be set.
- Pins S_0-S_{39} can be used for segment output.

(2) 1 / 3-duty (80-segment) data format

The format for display data in 1 / 3-duty mode is as shown below:



- In this case, the pin is used as COM3, but set data as for the S_0 pin. (Note that the set data are non-functional.)
- Pins S_1-S_{39} can be used for segment output.

These data bits control on / off switching of the display corresponding to the common outputs. A waveform corresponding to display on / off is output to the segment output corresponding to common / segment data. Set "1" for display on and "0" for off.
To set data for pins S_0-S_{19} and S_{20}-S_{39} independently, specify the address to 1H and 2H respectively.
When data for pins S_0-S_{19} and S_{20}-S_{39} overlap, identical data can be transferred simultaneously with a single serial data transfer by specifying 3H as the address.
When there are unused segments of the MSB, the data setting for unused segments of the MSB omit and it can possible to set from used segment data of the MSB.

(Example) When up to 24 segments are used in 1 / 3-duty mode.



(3) Duty and bias bits

	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	A3	A2	A1	A0
Address 8H	0	0	Bias	Duty					1	0	0	0

	BIAS	DUTY	BIAS	DUTY
*	0	0	1/2	1/2
	0	1		1/3
	1	0	1/3	1/2
	1	1		1/3

* (Note) These data are reset to "0" at reset.

(4) BL and LT bits

	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	A3	A2	A1	A0
Address 9H	0	LT	BL						1	0	0	1

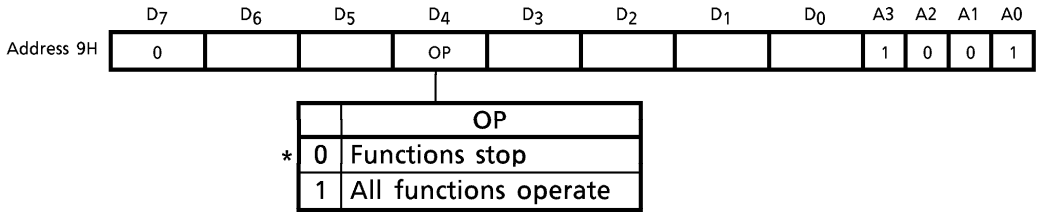
	LT	BL	DISPLAY
*	0	0	Normal display
	1		All on
	0	1	All off**
	1		

Even when the display is set to all on or all off, the display data prior to setting is retained and no resetting of display data is required.
It is also possible to set new data while all on or all off.

* (Note) These data are reset to "0" at reset.

** (Note) When both BL and LT are "1", BL takes priority.

(5) OP bit

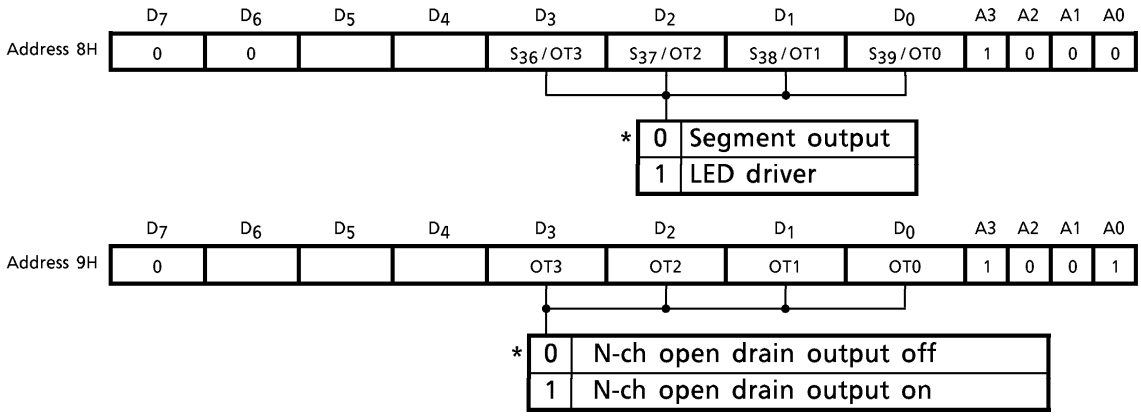


		OP
*	0	Functions stop
	1	All functions operate

The OP bit controls the operating and stopping of the LCD driver, key scan and other functions. When it is reset to "0", all operations stop, the LCD driver output and key scan output pins are fixed to high, and the oscillator stops.
The data of control bits prior to setting is retained, and new data can be set.
When this pin is set to "1", the oscillator, LCD driver and key scan operate.
At reset, this bit is reset to "0". Initialize control data and display data in this state.

* (Note) These data are reset to "0" at reset.

(6) Segment output / LED driver switching bits and LED driver control bits



		Segment output / LED driver
*	0	Segment output
	1	LED driver

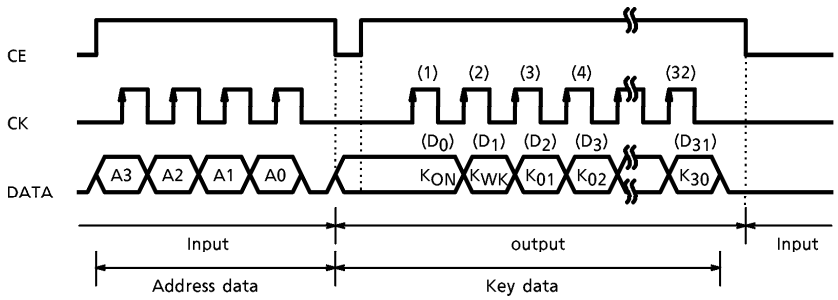
		N-ch open drain output
*	0	N-ch open drain output off
	1	N-ch open drain output on

The segment output / LED driver switching bits switch between segment output and the LED driver output. Resetting these bits to "0" selects segment output; setting to "1" selects LED driver output. When set to segment output, display data are output and the LCD display is turned on and off; when set to LED driver output, output is turned on and off by the LED driver control bit.
The LED driver is of N-ch open-drain structure. Setting the LED driver control bit to "0" turns off N-ch open output; setting to "1" turns off N-ch open output.
When set to segment output, the corresponding LED driver control data are invalid; conversely, when set to LED driver, the corresponding segment output display data are invalid.
When S_{36}-S_{39} are used for LED driver output, data must not be set to address 9H until the segment / LED switching bit of the corresponding address 8H has been set to "1".

* (Note) These data are reset to "0" at reset.

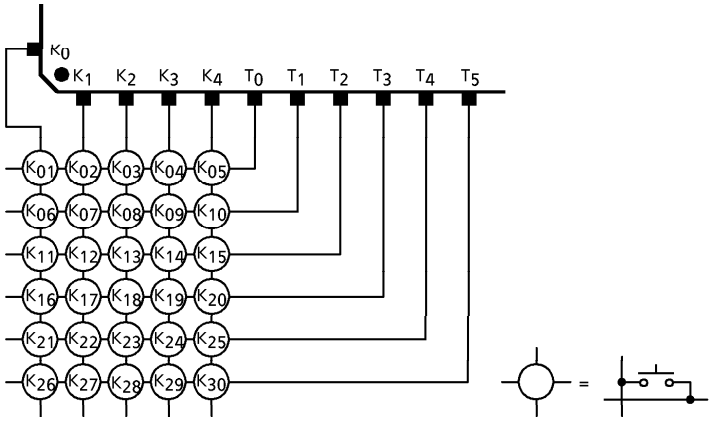
2. Key data output format

(1) Key data output timing is as shown below:



For rise and fall times, see Electrical Characteristics.

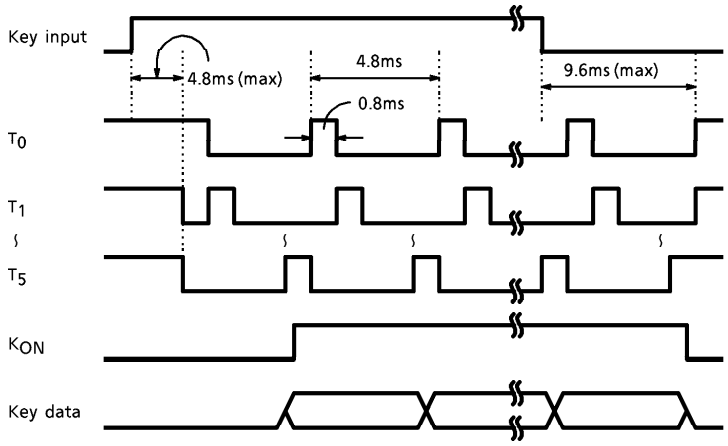
(2) Structure of key matrix



(Structure of key matrix)

- At key input, K_{ON} = "1"; when multiple strikes occur, K_{WK} = "1".
- After address input, the data pin is set to output at CE = " L", and key requests (K_{ON} = "1") can be accepted.
- Setting the CE pin from high to low returns the data pin to input; key data detection can be suspended.

(3) Key scan timing is as shown below:

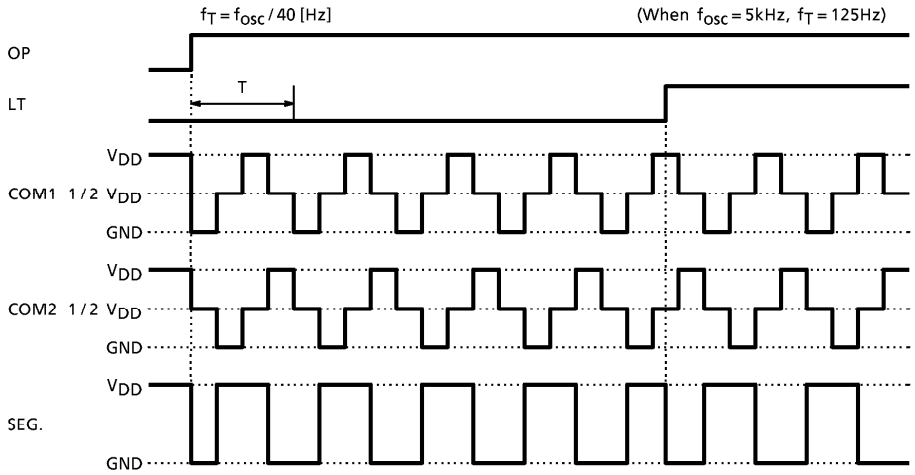


(Note) When f_{OSC} is 5kHz.

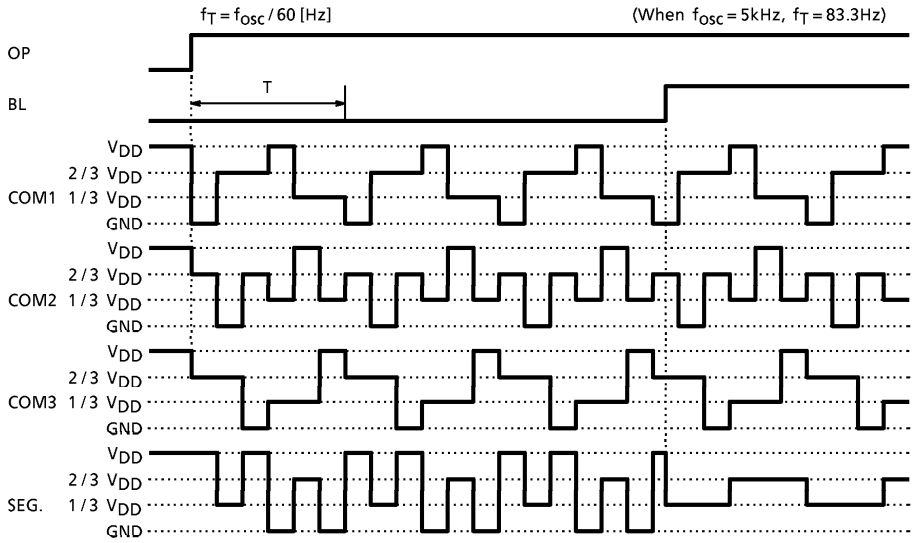
When high is input to the key input pin, key scanning begins within not more than one cycle (4.8ms when f_{OSC} is 5kHz), and the key data corresponding to the key timing is input. After one more cycle of key scanning, K_{ON} is set to "1" and key data are entered and upgraded every cycle. When the key is released, key scanning stops within not more than two cycles (9.6ms when f_{OSC} is 5kHz), and all key data are reset to "0".
Thus, key data must be accessed during key scanning.
To access key data, pin CE may be held low after input of address data.
The result is standby until key input occurs. In this state, the K_{ON} bit is output to the data pin as-is, so that it is "1" when there is key input and "0" when there is not.
If key data are continuously accessed based on the state of K_{ON}, key data can be effectively fetched.

3. The output waveforms of the LCD driver are as shown below.

- 1 / 2 duty, 1 / 2 bias (COM1 system off, COM2 system on)



- 1 / 3 duty, 1 / 3 bias (COM1 system on, COM2 system off, COM3 system on)



MAXIMUM RATINGS (Ta = 25°C)

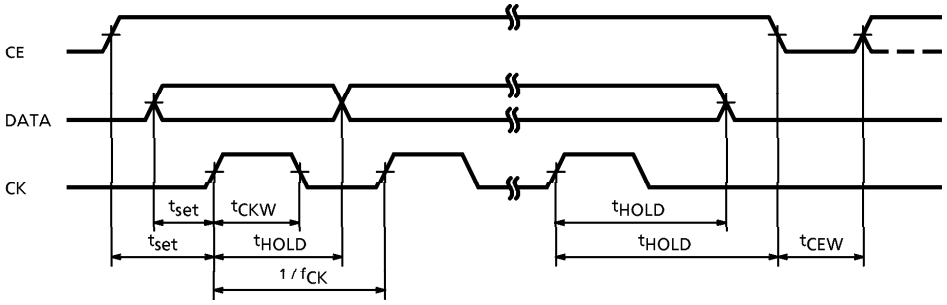
CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage	V_{DD}	−0.3~7.0	V
Input Voltage	V_{IN}	−0.3~V_{DD} + 0.3	V
Power Dissipation	P_D	300	mW
Operating Temperature	T_{opr}	−40~85	°C
Storage Temperature	T_{stg}	−65~150	°C

ELECTRICAL CHARACTERISTICS (Unless otherwise specified, V_{DD} = 4.5~5.5V, Ta = −40~85°C)

CHARACTERISTIC		SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Operating Supply Voltage		V_{DD}	—	—	V_{RST}	5.0	5.5	V
Power On Reset Voltage		V_{RST}	—	—	2.5	3.0	3.5	V
Operating Supply Current		I_{DD1}	—	V_{DD} = 5V, f_{osc} = 5kHz, No load	—	0.4	1.0	mA
Stand-by Current		I_{DD2}	—	OP = "0", V_{DD} = 5V	—	120	250	μA
Input Voltage	"H" Level	V_{IH}	—	K_0~K_3, CE, DATA, CK, $\overline{RST}$	V_{DD} × 0.8	~	V_{DD}	V
	"L" Level	V_{IL}	—	K_0~K_3, CE, DATA, CK, $\overline{RST}$	0	~	V_{DD} × 0.2	V
SCHMITT Voltage Width		V_{SCH}	—	V_{DD} = 5V, CE, DATA, CK	—	1.0	—	V
Input Leak Current	"H" Level	I_{IH}	—	V_{IN} = V_{DD}, CE, DATA, CK, $\overline{RST}$	—	~	±1.0	μA
	"L" Level	I_{IL}	—	V_{IN} = 0V, CE, DATA, CK, $\overline{RST}$	—	~	±1.0	μA
Output Voltage	1/2 Level	$V_{1/2}$	—	V_{DD} = 5V COM1, COM2	1/2V_{DD} − 0.5	1/2V_{DD}	1/2V_{DD} + 0.5	V
	1/3 Level	$V_{1/3}$	—	V_{DD} = 5V COM1~COM3, S_0~S_{39}	1/3V_{DD} − 0.5	1/3V_{DD}	1/3V_{DD} + 0.5	V
	2/3 Level	$V_{2/3}$	—	V_{DD} = 5V COM1~COM3, S_0~S_{39}	2/3V_{DD} − 0.5	2/3V_{DD}	2/3V_{DD} + 0.5	V
Output Current	"H" Level	I_{OH1}	—	V_{DD} = 5V, V_{OH} = 4.5V, T_0~T_5 COM1 ~COM3, S_0~S_{39}, DATA	−0.5	−3.0	—	mA
	"L" Level 1	I_{OL1}	—	V_{DD} = 5V, V_{OL} = 0.5V COM1~ COM3, S_0~S_{39}, DATA	0.5	3.0	—	mA
	"L" Level 2	I_{OL2}	—	V_{DD} = 5V, V_{OL} = 1.0V, $\overline{OT0}$~$\overline{OT3}$	10	20	—	mA
OFF-LEAK Current		I_{LO}	—	$\overline{OT0}$~$\overline{OT3}$	—	~	±1.0	μA
N-ch Output Load Resistor		R_{ON}	—	Ta = 25°C, T_0~T_5	75	150	300	kΩ
Pull-Down Resistor		R_{IN}	—	Ta = 25°C, K_0~K3				

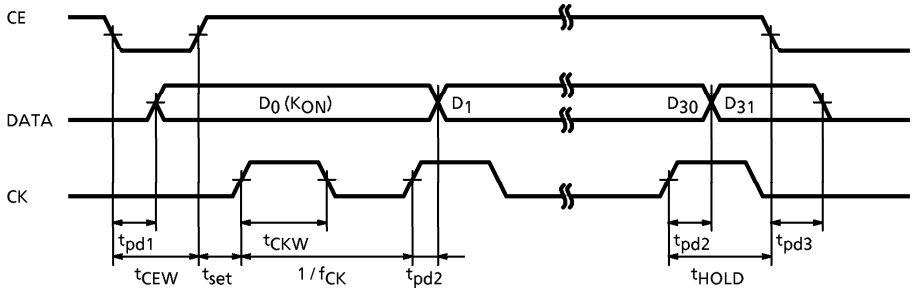
CHARACTERISTIC	SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Oscillation Frequency	f_{OSC}	—	—	—	5	20	kHz
Operating Clock Frequency Range	f_{CK}	—	Refer to timing chart as below	—	~	2.0	MHz
Clock Pulse Width	t_{CKW}			250	~	—	ns
Data Set Time	t_{set}			250	~	—	
Data Hold Time	t_{HOLD}			250	~	—	
CE Pulse Width	t_{CEW}			250	~	—	

CE, CK, DATA-IN TIMING



CHARACTERISTIC	SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Operating Clock Frequency Range	f_{CK}	—	Refer to timing chart as below	—	~	2.0	MHz
Clock Pulse Width	t_{CKW}			250	~	—	ns
Data Delay Time	t_{pd1}			—	~	250	
	t_{pd2}			—	~	250	
	t_{pd3}			—	~	250	
CE Pulse Width	t_{CEW}			250	~	—	
Data Set Time	t_{set}			250	~	—	
Data Hold Time	t_{HOLD}			250	~	—	

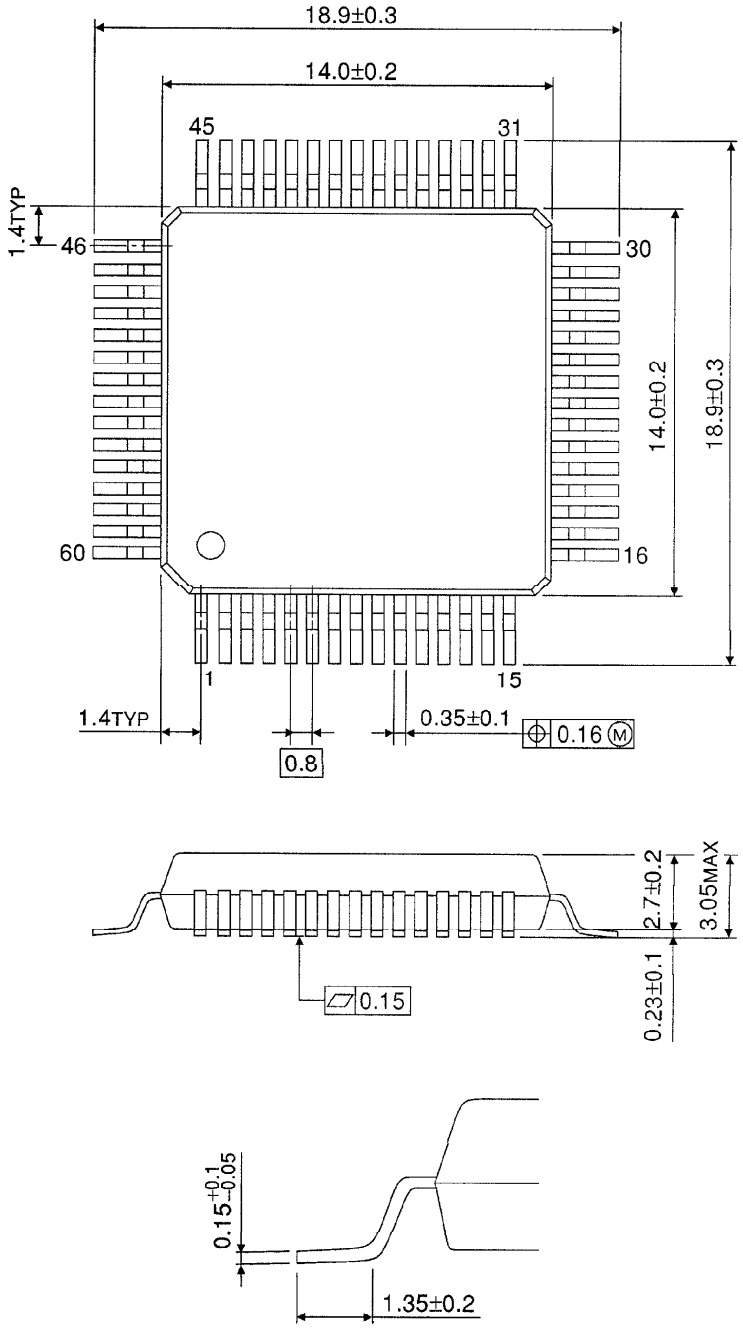
CE, CK, DATA-OUT TIMING



OUTLINE DRAWING

QFP60-P-1414-0.80D

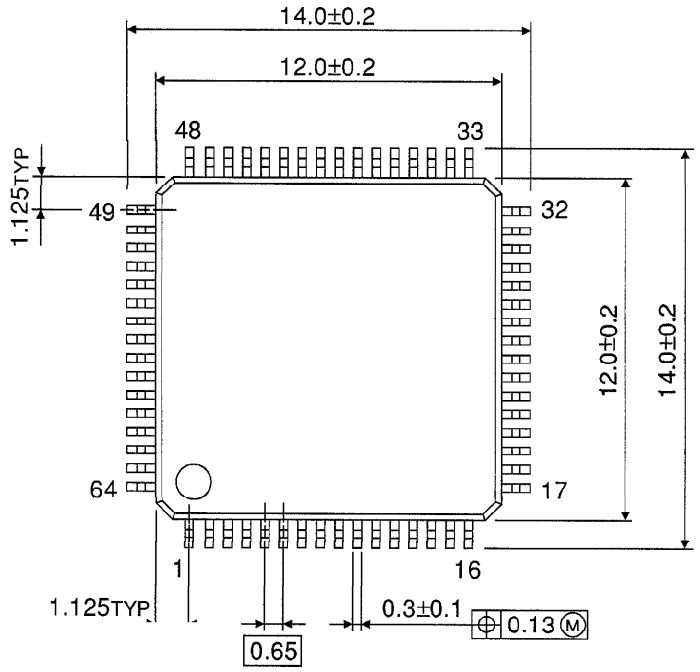
Unit : mm

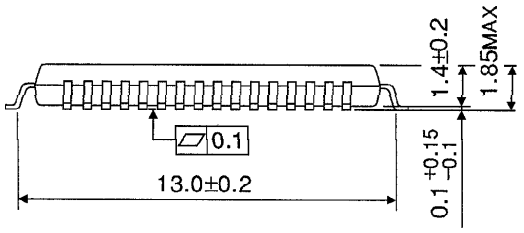


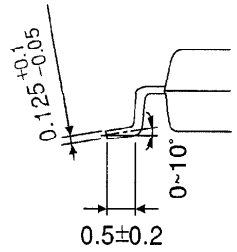
Weight : 1.10g (Typ.)

OUTLINE DRAWING

QFP64-P-1212-0.65 Unit : mm







Weight : 0.45g (Typ.)