# N-Channel 650V (D-S) Power MOSFET

| PRODUCT SUMMARY | | |
|---|---|---|
| $V_{DS}$ (V) at $T_J$ max. | 670 | |
| $R_{DS(on)}$ max. at 25 °C (Ω) | $V_{GS}$ = 10 V | 0.86 |
| $Q_g$ max. (nC) | 43 | |
| $Q_{gs}$ (nC) | 5 | |
| $Q_{gd}$ (nC) | 22 | |
| Configuration | Single | |

Available
RoHS

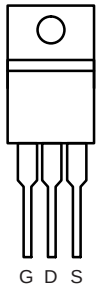
## FEATURES

- Low figure-of-merit (FOM) $R_{on}$ x $Q_g$
- Low input capacitance ($C_{iss}$)
- Reduced switching and conduction losses
- Ultra low gate charge ($Q_g$)
- Avalanche energy rated (UIS)

## APPLICATIONS

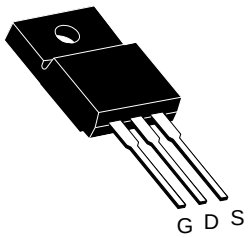
- Server and telecom power supplies
- Switch mode power supplies (SMPS)
- Power factor correction power supplies (PFC)
- Lighting
  - High-intensity discharge (HID)
  - Fluorescent ballast lighting
- Industrial

**TO-220AB**



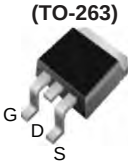

Top View

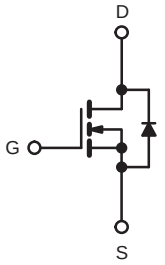
**TO-220 FULLPAK**




Top View

**D²PAK (TO-263)**




N-Channel MOSFET

| ABSOLUTE MAXIMUM RATINGS ($T_C$ = 25 °C, unless otherwise noted) | | | | | |
|---|---|---|---|---|---|
| **PARAMETER** | | | **SYMBOL** | **LIMIT** | **UNIT** |
| Drain-Source Voltage | | | $V_{DS}$ | 650 | V |
| Gate-Source Voltage | | | $V_{GS}$ | ± 30 | |
| Continuous Drain Current ($T_J$ = 150 °C) | $V_{GS}$ at 10 V | $T_C$ = 25 °C | $I_D$ | 10 | A |
| | | $T_C$ = 100 °C | | 8.0 | |
| Pulsed Drain Current [a] | | | $I_{DM}$ | 40 | |
| Linear Derating Factor | | | | 3.2 | W/°C |
| Single Pulse Avalanche Energy [b] | | | $E_{AS}$ | 280 | mJ |
| Maximum Power Dissipation | | | $P_D$ | 106 /34 | W |
| Operating Junction and Storage Temperature Range | | | $T_J$, $T_{stg}$ | -55 to +150 | °C |
| Drain-Source Voltage Slope | $T_J$ = 125 °C | | dV/dt | 15 | V/ns |
| Reverse Diode dV/dt [d] | | | | 4.1 | |
| Soldering Recommendations (Peak Temperature) [c] | for 10 s | | | 300 | °C |

**Notes**

a. Repetitive rating; pulse width limited by maximum junction temperature.
b. $V_{DD}$ = 50 V, starting $T_J$ = 25 °C, L = 28.2 mH, $R_g$ = 25 Ω, $I_{AS}$ = 4.5 A.
c. 1.6 mm from case.
d. $I_{SD} \leq I_D$, dI/dt = 100 A/µs, starting $T_J$ = 25 °C.



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## THERMAL RESISTANCE RATINGS

| PARAMETER | SYMBOL | TYP. | MAX. | UNIT |
|---|---|---|---|---|
| Maximum Junction-to-Ambient | $R_{thJA}$ | - | 60 | °C/W |
| Maximum Junction-to-Case (Drain) | $R_{thJC}$ | - | 0.8 | |

## SPECIFICATIONS ($T_J$ = 25 °C, unless otherwise noted)

| PARAMETER | SYMBOL | TEST CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| **Static** | | | | | | |
| Drain-Source Breakdown Voltage | $V_{DS}$ | $V_{GS}$ = 0 V, $I_D$ = 250 µA | 650 | - | - | V |
| $V_{DS}$ Temperature Coefficient | $\Delta V_{DS}/T_J$ | Reference to 25 °C, $I_D$ = 1 mA | - | 0.75 | - | V/°C |
| Gate-Source Threshold Voltage (N) | $V_{GS(th)}$ | $V_{DS}$ = $V_{GS}$, $I_D$ = 250 µA | 2 | - | 4 | V |
| Gate-Source Leakage | $I_{GSS}$ | $V_{GS}$ = ± 20 V | - | - | ± 100 | nA |
| | | $V_{GS}$ = ± 30 V | - | - | ± 1 | µA |
| Zero Gate Voltage Drain Current | $I_{DSS}$ | $V_{DS}$ = 650 V, $V_{GS}$ = 0 V | - | - | 1 | µA |
| | | $V_{DS}$ = 520 V, $V_{GS}$ = 0 V, $T_J$ = 125 °C | - | - | 10 | |
| Drain-Source On-State Resistance | $R_{DS(on)}$ | $V_{GS}$ = 10 V, $I_D$ = 8 A | - | 0.86 | - | Ω |
| Forward Transconductance | $g_{fs}$ | $V_{DS}$ = 30 V, $I_D$ = 8 A | - | 16 | - | S |
| **Dynamic** | | | | | | |
| Input Capacitance | $C_{iss}$ | $V_{GS}$ = 0 V, $V_{DS}$ = 100 V, f = 1 MHz | - | 730 | - | pF |
| Output Capacitance | $C_{oss}$ | | - | 70 | - | |
| Reverse Transfer Capacitance | $C_{rss}$ | | - | 8 | - | |
| Effective Output Capacitance, Energy Related [a] | $C_{o(er)}$ | $V_{DS}$ = 0 V to 520 V, $V_{GS}$ = 0 V | - | 63 | - | |
| Effective Output Capacitance, Time Related [b] | $C_{o(tr)}$ | | - | 213 | - | |
| Total Gate Charge | $Q_g$ | $V_{GS}$ = 10 V; $I_D$ = 8 A, $V_{DS}$ = 520 V | - | 43 | - | nC |
| Gate-Source Charge | $Q_{gs}$ | | - | 5 | - | |
| Gate-Drain Charge | $Q_{gd}$ | | - | 22 | - | |
| Turn-On Delay Time | $t_{d(on)}$ | $V_{DD}$ = 520 V, $I_D$ = 8 A, $V_{GS}$ = 10 V, $R_g$ = 9.1 Ω | - | 13 | 25 | ns |
| Rise Time | $t_r$ | | - | 11 | 35 | |
| Turn-Off Delay Time | $t_{d(off)}$ | | - | 81 | 90 | |
| Fall Time | $t_f$ | | - | 25 | 40 | |
| Gate Input Resistance | $R_g$ | f = 1 MHz, open drain | - | 3.5 | - | Ω |
| **Drain-Source Body Diode Characteristics** | | | | | | |
| Continuous Source-Drain Diode Current | $I_S$ | MOSFET symbol showing the integral reverse p - n junction diode  | - | - | 15 | A |
| Pulsed Diode Forward Current | $I_{SM}$ | | - | - | 40 | |
| Diode Forward Voltage | $V_{SD}$ | $T_J$ = 25 °C, $I_S$ = 8 A, $V_{GS}$ = 0 V | - | - | 1.5 | V |
| Reverse Recovery Time | $t_{rr}$ | $T_J$ = 25 °C, $I_F$ = $I_S$ = 8 A, dI/dt = 100 A/µs, $V_R$ = 400 V | - | 345 | - | ns |
| Reverse Recovery Charge | $Q_{rr}$ | | - | 4.5 | - | µC |
| Reverse Recovery Current | $I_{RRM}$ | | - | 35 | - | A |

**Notes**

a. $C_{oss(er)}$ is a fixed capacitance that gives the same energy as $C_{oss}$ while $V_{DS}$ is rising from 0 % to 80 % $V_{DSS}$.

b. $C_{oss(tr)}$ is a fixed capacitance that gives the same charging time as $C_{oss}$ while $V_{DS}$ is rising from 0 % to 80 % $V_{DSS}$.



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**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)

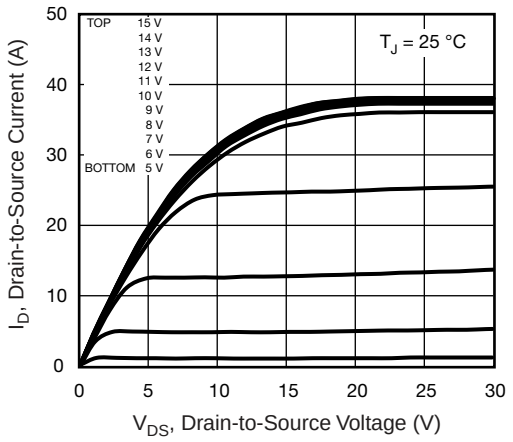



**Fig. 1 - Typical Output Characteristics**

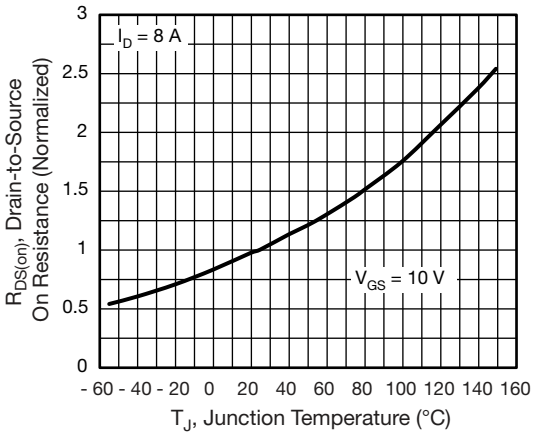



**Fig. 4 - Normalized On-Resistance vs. Temperature**

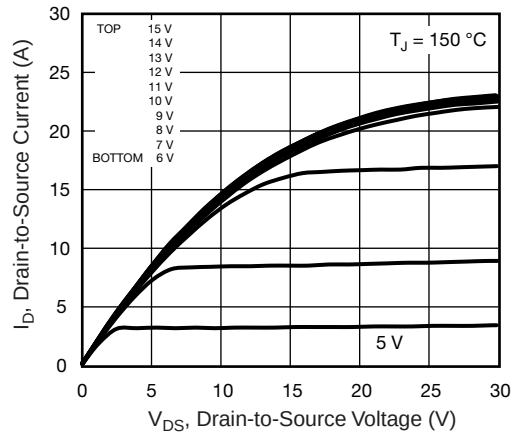



**Fig. 2 - Typical Output Characteristics**

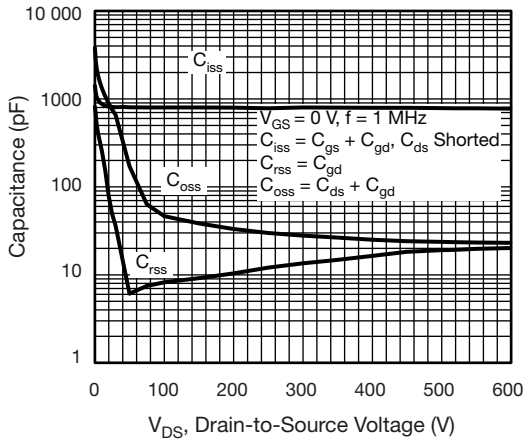



**Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage**

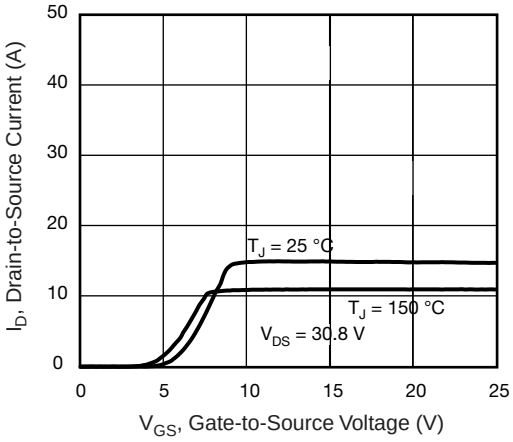



**Fig. 3 - Typical Transfer Characteristics**

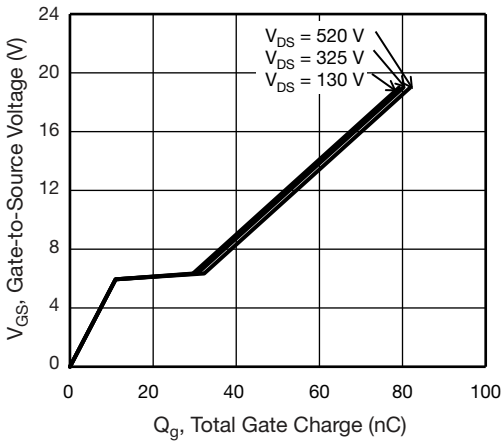



**Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage**



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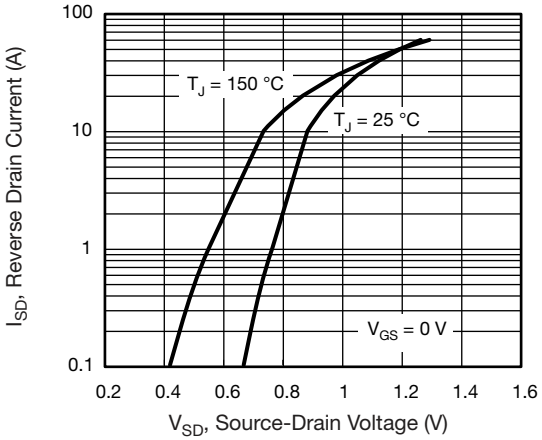



**Fig. 7 - Typical Source-Drain Diode Forward Voltage**

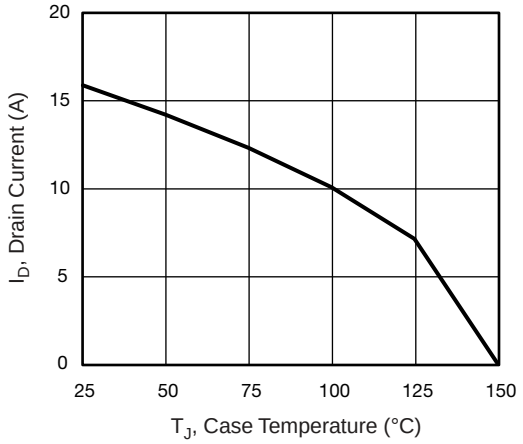



**Fig. 9 - Maximum Drain Current vs. Case Temperature**

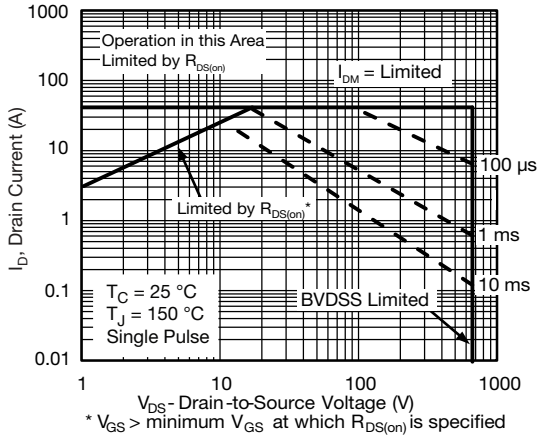



**Fig. 8 - Maximum Safe Operating Area**

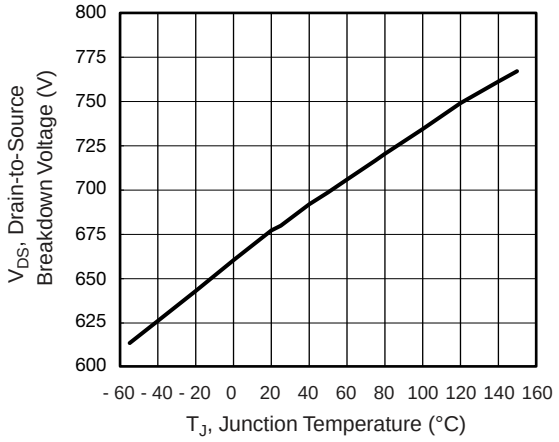



**Fig. 10 - Temperature vs. Drain-to-Source Voltage**

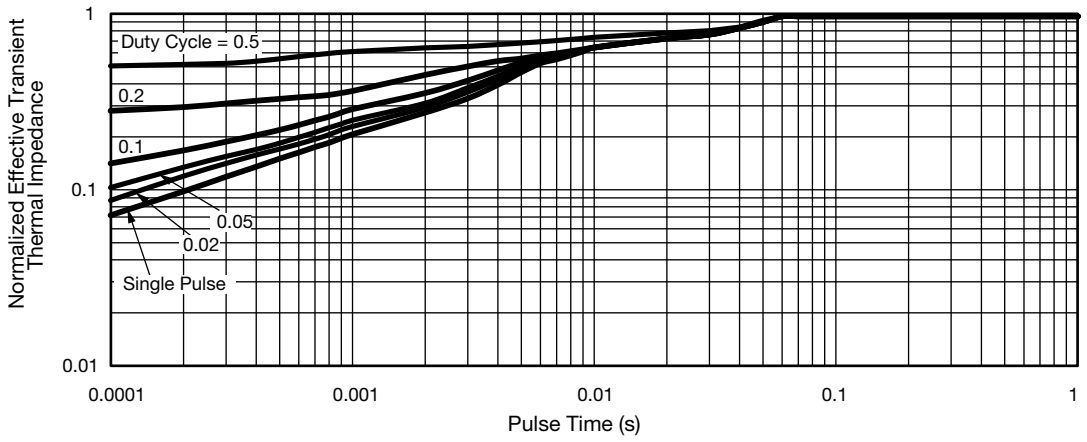



**Fig. 11 - Normalized Thermal Transient Impedance, Junction-to-Case**



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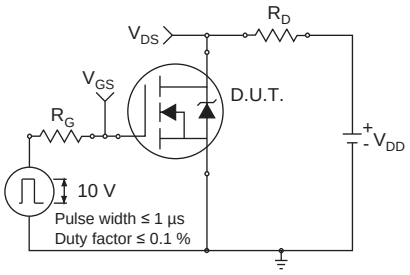



**Fig. 12 - Switching Time Test Circuit**

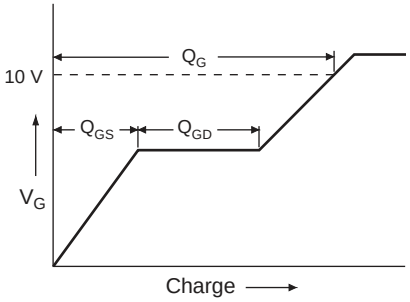



**Fig. 16 - Basic Gate Charge Waveform**

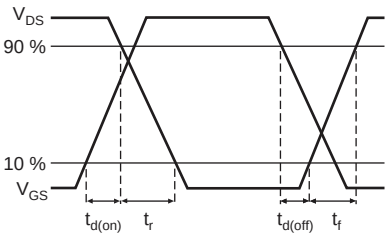



**Fig. 13 - Switching Time Waveforms**

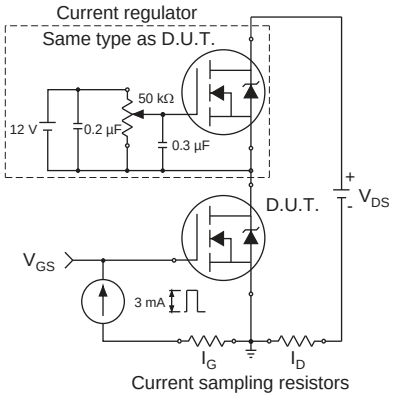



**Fig. 17 - Gate Charge Test Circuit**

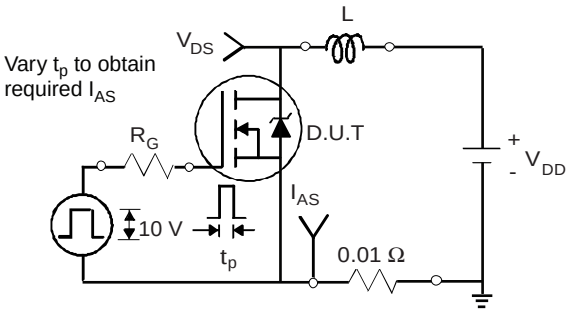



**Fig. 14 - Unclamped Inductive Test Circuit**

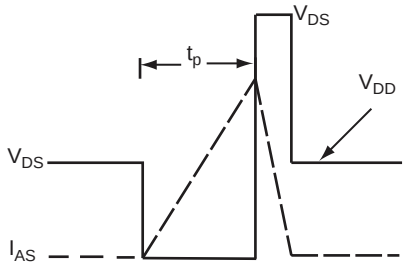
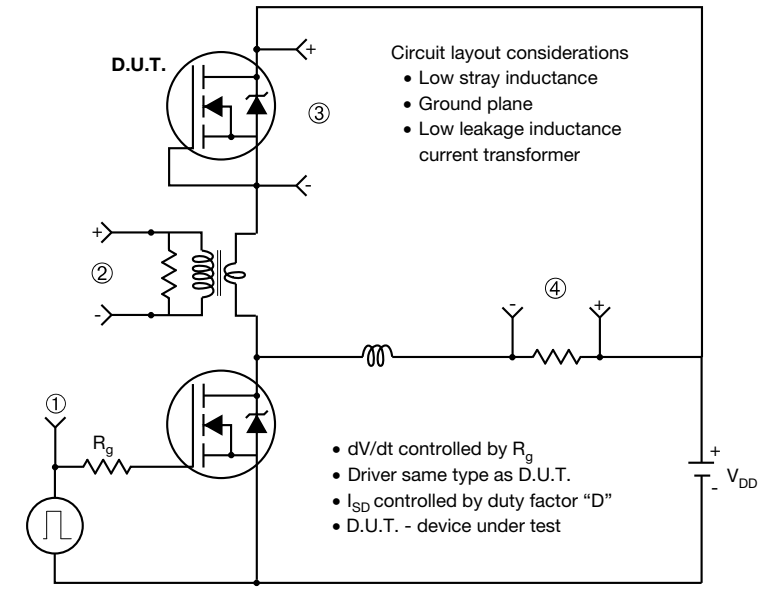


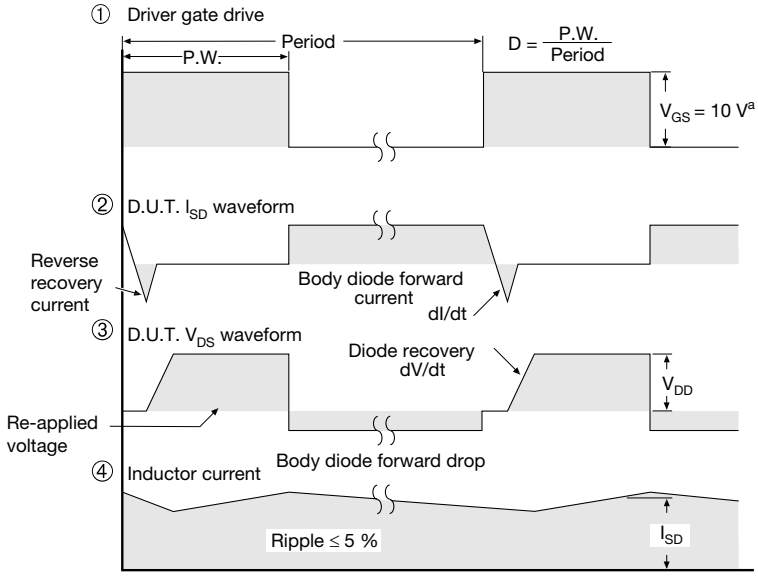

**Fig. 15 - Unclamped Inductive Waveforms**



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## Peak Diode Recovery dV/dt Test Circuit




**Note**

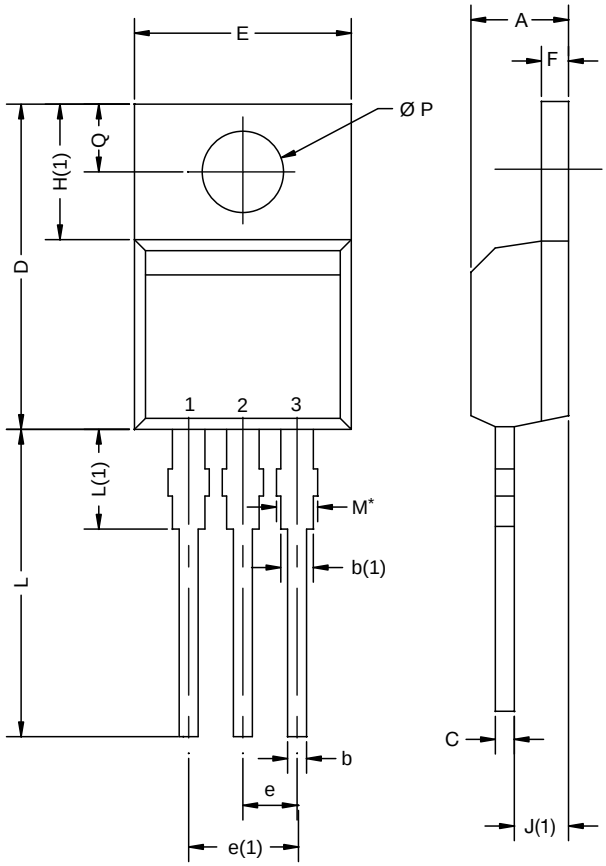
a. $V_{GS}$ = 5 V for logic level devices

**Fig. 18 - For N-Channel**



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# TO-220AB




| DIM. | MILLIMETERS | | INCHES | |
|---|---|---|---|---|
| | MIN. | MAX. | MIN. | MAX. |
| A | 4.25 | 4.65 | 0.167 | 0.183 |
| b | 0.69 | 1.01 | 0.027 | 0.040 |
| b(1) | 1.20 | 1.73 | 0.047 | 0.068 |
| c | 0.36 | 0.61 | 0.014 | 0.024 |
| D | 14.85 | 15.49 | 0.585 | 0.610 |
| E | 10.04 | 10.51 | 0.395 | 0.414 |
| e | 2.41 | 2.67 | 0.095 | 0.105 |
| e(1) | 4.88 | 5.28 | 0.192 | 0.208 |
| F | 1.14 | 1.40 | 0.045 | 0.055 |
| H(1) | 6.09 | 6.48 | 0.240 | 0.255 |
| J(1) | 2.41 | 2.92 | 0.095 | 0.115 |
| L | 13.35 | 14.02 | 0.526 | 0.552 |
| L(1) | 3.32 | 3.82 | 0.131 | 0.150 |
| Ø P | 3.54 | 3.94 | 0.139 | 0.155 |
| Q | 2.60 | 3.00 | 0.102 | 0.118 |
| ECN: X12-0208-Rev. N, 08-Oct-12<br>DWG: 5471 | | | | |

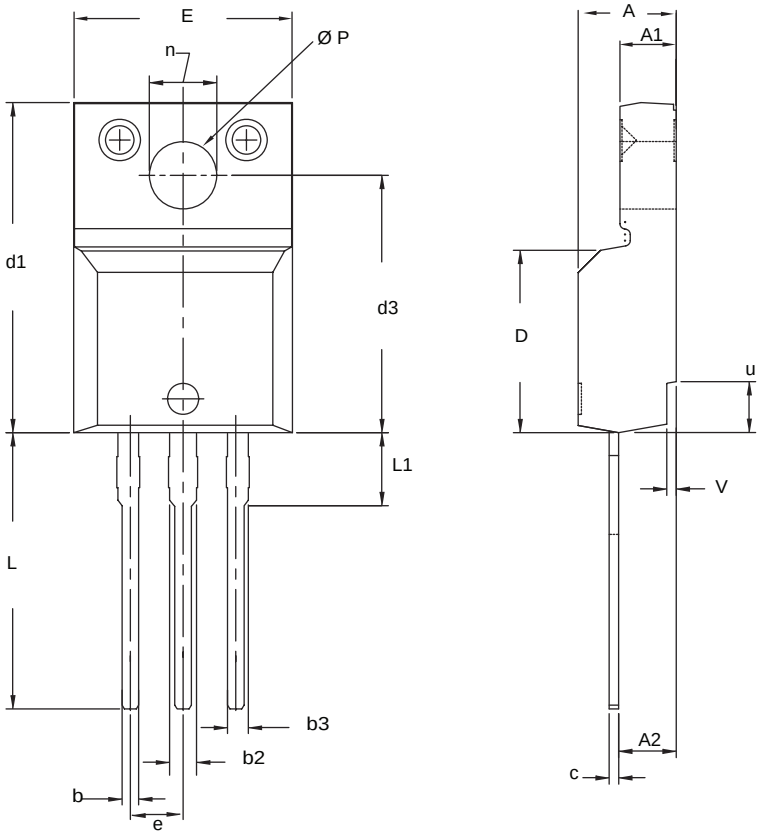
**Notes**

* M = 1.32 mm to 1.62 mm (dimension including protrusion) Heatsink hole for HVM



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## TO-220 FULLPAK (HIGH VOLTAGE)




| | MILLIMETERS | | INCHES | |
|---|---|---|---|---|
| **DIM.** | **MIN.** | **MAX.** | **MIN.** | **MAX.** |
| A | 4.570 | 4.830 | 0.180 | 0.190 |
| A1 | 2.570 | 2.830 | 0.101 | 0.111 |
| A2 | 2.510 | 2.850 | 0.099 | 0.112 |
| b | 0.622 | 0.890 | 0.024 | 0.035 |
| b2 | 1.229 | 1.400 | 0.048 | 0.055 |
| b3 | 1.229 | 1.400 | 0.048 | 0.055 |
| c | 0.440 | 0.629 | 0.017 | 0.025 |
| D | 8.650 | 9.800 | 0.341 | 0.386 |
| d1 | 15.88 | 16.120 | 0.622 | 0.635 |
| d3 | 12.300 | 12.920 | 0.484 | 0.509 |
| E | 10.360 | 10.630 | 0.408 | 0.419 |
| e | 2.54 BSC | | 0.100 BSC | |
| L | 13.200 | 13.730 | 0.520 | 0.541 |
| L1 | 3.100 | 3.500 | 0.122 | 0.138 |
| n | 6.050 | 6.150 | 0.238 | 0.242 |
| Ø P | 3.050 | 3.450 | 0.120 | 0.136 |
| u | 2.400 | 2.500 | 0.094 | 0.098 |
| v | 0.400 | 0.500 | 0.016 | 0.020 |
| ECN: X09-0126-Rev. B, 26-Oct-09<br>DWG: 5972 | | | | |

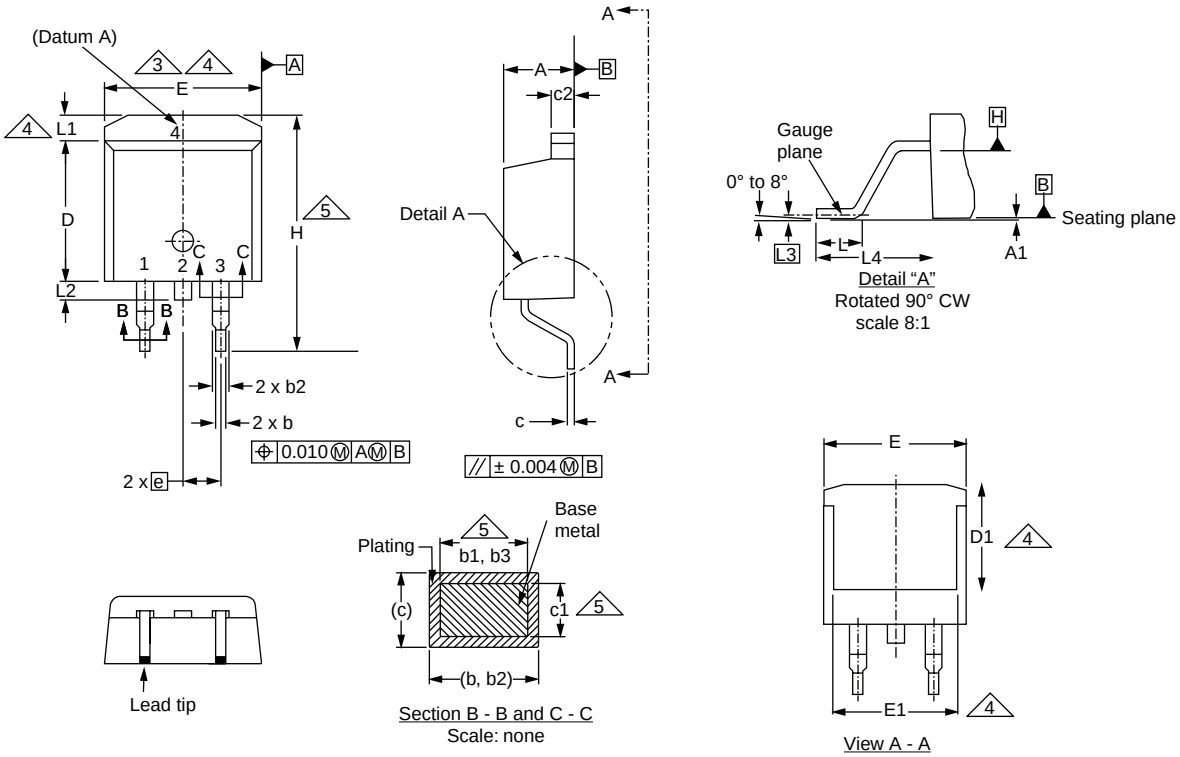
**Notes**

1. To be used only for process drawing.
2. These dimensions apply to all TO-220, FULLPAK leadframe versions 3 leads.
3. All critical dimensions should C meet $C_{pk} > 1.33$.
4. All dimensions include burrs and plating thickness.
5. No chipping or package damage.



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## TO-263AB (HIGH VOLTAGE)




| | MILLIMETERS | | INCHES | |
|---|---|---|---|---|
| DIM. | MIN. | MAX. | MIN. | MAX. |
| A | 4.06 | 4.83 | 0.160 | 0.190 |
| A1 | 0.00 | 0.25 | 0.000 | 0.010 |
| b | 0.51 | 0.99 | 0.020 | 0.039 |
| b1 | 0.51 | 0.89 | 0.020 | 0.035 |
| b2 | 1.14 | 1.78 | 0.045 | 0.070 |
| b3 | 1.14 | 1.73 | 0.045 | 0.068 |
| c | 0.38 | 0.74 | 0.015 | 0.029 |
| c1 | 0.38 | 0.58 | 0.015 | 0.023 |
| c2 | 1.14 | 1.65 | 0.045 | 0.065 |
| D | 8.38 | 9.65 | 0.330 | 0.380 |

| | MILLIMETERS | | INCHES | |
|---|---|---|---|---|
| DIM. | MIN. | MAX. | MIN. | MAX. |
| D1 | 6.86 | - | 0.270 | - |
| E | 9.65 | 10.67 | 0.380 | 0.420 |
| E1 | 6.22 | - | 0.245 | - |
| e | 2.54 BSC | | 0.100 BSC | |
| H | 14.61 | 15.88 | 0.575 | 0.625 |
| L | 1.78 | 2.79 | 0.070 | 0.110 |
| L1 | - | 1.65 | - | 0.066 |
| L2 | - | 1.78 | - | 0.070 |
| L3 | 0.25 BSC | | 0.010 BSC | |
| L4 | 4.78 | 5.28 | 0.188 | 0.208 |

ECN: S-82110-Rev. A, 15-Sep-08
DWG: 5970

**Notes**

1. Dimensioning and tolerancing per ASME Y14.5M-1994.
2. Dimensions are shown in millimeters (inches).
3. Dimension D and E do not include mold flash. Mold flash shall not exceed 0.127 mm (0.005") per side. These dimensions are measured at the outmost extremes of the plastic body at datum A.
4. Thermal PAD contour optional within dimension E, L1, D1 and E1.
5. Dimension b1 and c1 apply to base metal only.
6. Datum A and B to be determined at datum plane H.
7. Outline conforms to JEDEC outline to TO-263AB.



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# Material Category Policy

**Taiwan VBsemi Electronics Co., Ltd., hereby certify that all of the products are determined to be RoHS compliant and meets the definition of restrictions under Directive of the European Parliament 2011/65 / EU, 2011 Nian. 6. 8 Ri Yue restrict the use of certain hazardous substances in electrical and electronic equipment (EEE) - modification, unless otherwise specified as inconsistent.(www.VBsemi.tw)**

**Please note that some documents may still refer to Taiwan VBsemi RoHS Directive 2002/95 / EC. We confirm that all products identified as consistent with the Directive 2002/95 / EC European Directive 2011/65 /.**

**Taiwan VBsemi Electronics Co., Ltd. hereby certify that all of its products comply identified as halogen-free halogen-free standards required by the JEDEC JS709A. Please note that some Taiwanese VBsemi documents still refer to the definition of IEC 61249-2-21, and we are sure that all products conform to confirm compliance with IEC 61249-2-21 standard level JS709A.**



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