High Performance Current Mode Controller

The PJ3842B and PJ3843B series are high performance fixed frequency current mode controllers. This is specifically designed for Off-Line and DC-to-DC converter applications offering the designer a cost effective solution with minimal external components.This integrated circuits feature a trimmed oscillator for precise duty cycle control, a temperature compensated reference, high gain error amplifier, current sensing comparator,and a high current totem pole output ideally suited for driving a power MOSFET.

Also included are protective features consisting of input and reference undervoltage lockouts each with hysteresis, cycle-by-cycle current limiting, programmable output deadtime, and a latch for single pulse metering.

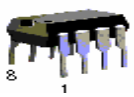
This device is available in 8-pin dual-in-line plastic packages as well as the 8-pin plastic surface mount (SOP-8). The SOP-8 package has separate power and ground pins for the totem pole output stage.

The PJ3842B has UVLO thresholds of 16V (on) and 10V (off), ideally suited for off-line converters. The PJ3843B is tailored for lowervoltage applications having UVLO thresholds of 8.5V (on) and 7.6V (off).

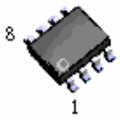
FEATURES

- Trimmed Oscillator Discharge Current for Precise Duty Cycle Control
- Current Mode Operation to 500KHz
- Automatic Feed Forward Compensation
- Latching PWM for Cycle-By-Cycle Current Limiting
- Internally Trimmed Reference with Undervoltage Lockout
- High Current Totem Pole Output
- Undervoltage Lockout with Hystersis
- Low Start-Up and Operating Current

DIP-8



SOP-8

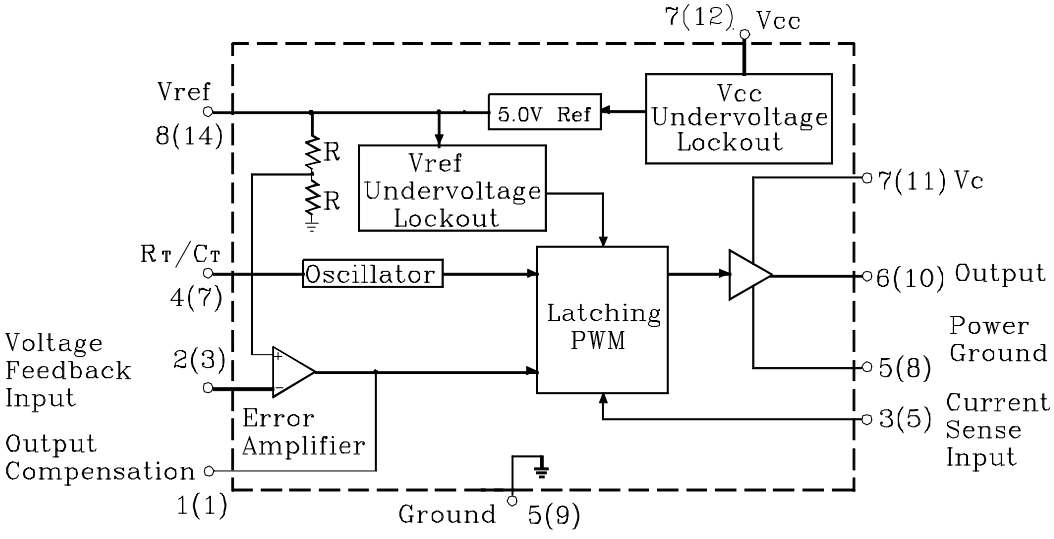


Pin：1. Compensation
2. Voltage Feedback
3. Current Sense
4. R_T/C_T
5. Gnd
6. Output
7. Vcc
8. Vref

ORDERING INFORMATION

Device	Operating Temperature (Ambient)	Package
PJ3842/3843BCD	-20℃ TO +85℃	DIP-8
PJ3842/3843BCS		SOP-8

SIMPLIFIED BLOCK DIAGRAM



The document contains information on a new product.Specifications and information herein are subject to change without notice.

MAXIMUM RATING

Parameter	Symbol	Value	Unit
Supply Voltage (low impedance source)	Vi	30	V
Supply Voltage (Ii<30mA)	Vi	Self Limiting	
Output Current	IO	±1	A
Output Energy (capacitive load)	EO	5	V
Analog Inputs (pins 2,3)		-0.3 to 6.3	mJ
Error Amplifier Output Sink Current		10	mA
Storage Temperature Range	Tstg	-65 to +150	℃

* All voltages are with respect to pin 5,all currents are positive into the specified terminal.

ELECTRICAL CHARACTERISTICS

(Unless otherwise stated , these specifications apply for 0<Tamb<70℃ ; V_i = 15V (Note 5), R_T=10K, C_T=3.3nF)

Parameter	Symbol	Test Conditions	PJ3842B / PJ3843B			Unit
			Min	Typ	Max	
REFERENCE SECTION						
Output Voltage	V_{REF}	Io=1mA,T_J = 25℃	4.90	5.00	5.10	V
Line Regulation	$\triangle V_{REF}$	12V<Vi<25V	-	6	20	mV
Load Regulation	$\triangle V_{REF}$	1<Io<20mA	-	6	25	mV
Temperature Stability (Note2)	$\triangle V_{REF}/\triangle T$		-	0.2	0.4	mV/℃
Total Output Variantion		Line,Load, Temperature(2)	4.82	-	5.18	V
Output Noise Voltage	Vn	10Hz<f<10kHz T_J=25℃ (2)	-	50	-	mV
Long Term Stability		Tamb=125℃, 1000Hrs(2)	-	5	25	mV
Output Short Circuit	Isc		-30	-100	-180	mA
OSCILLATOR SECTION						
Initial Accuracy	fs	T_J=25℃	47	52	57	KHz
Voltage Stability		12<Vi<25V	-	0.5	3	%
Temperature Stability		T_{MIN} <Tamb<T_{MAX} (2)	-	5	-	%
Amplitude VPIN4 Peak to Peak	V_4		-	1.7	-	V
ERROR AMPLIFIER SECTION						
Input Voltage (Vo=2.5V)	V_2	VPIN1=2.5V	2.42	2.50	2.58	V
Input Bias Current	I_B		-	-0.3	-2.0	mA
	A_{VOL}	2<Vo<4V	65	90	-	dB
Unity Gain Bandwidth (2)	B		0.7	1.0	-	MHz
Supply Voltage Rejection	SVR		60	70	-	dB
Output Current						
Sink	I_{sink}	V_{PIN2}=2.7V, V_{PIN1}=1.1V	2.0	6	-	V
Source	I_{Source}	V_{PIN2}=2.3V, V_{PIN1}=5V	-0.5	-0.8	-	
Output Voltage Swing High State	V_{OH}	V_{PIN2}=2.3V, R_L=15KΩ to Ground	4.55	4.85	-	V
Output Voltage Swing Low State	V_{OL}	V_{PIN2}=2.7V, R_L=15KΩ to Pin8	-	0.7	1.1	V

Parameter	Symbol	Test Conditions	PJ3842B / PJ3843B			Unit
			Min	Typ	Max	
CURRENT SENSE SECTION						
Current Sense Input Voltage Gain (Note 3 &4)	Gv		2.8	3.0	3.2	V/V
Maximum Input Signal	V_3	V_{PIN1}=5V(Note 3)	0.9	1.0	1.1	V
Supply VoltageRejection	SVR	12<Vi<25V(Note 3)	-	70	-	dB
Input Bias Current	I_B		-	-2.0	-10	mA
Delay to Output	T_d		-	150	300	ns
OUTPUT SECTION						
Output Voltage						
Low State	V_{OL}	Isink=20mA	-	0.1	0.4	
		Isink=200mA	-	1.5	2.2	V
High State	V_{OH}	Isource=20mA	13	13.5	-	
		Isource=200mA	12	13.5	-	
Output Voltage Rise Time	tr	T_J=25℃, C_L=1.0nF (Note2)	-	50	150	ns
Output Voltage Fall Time	tf	T_J=25℃, C_L=1.0nF (Note2)	-	50	150	ns
UNDER-VOLTAGE LOCKOUT SECTION						
Start-Up Threshold						
PJ3842B	Vth		14.5	16	17.5	V
PJ3843B			7.8	8.4	9.0	
Minimum Operating Voltage After Turn-On						
PJ3842B	$V_{CC(min)}$		8.5	10	11.5	V
PJ3843B			7.0	7.6	8.2	
PWM SECTION						
Max. Duty Cycle	DCmax		93	97	100	%
TOTAL STANDBY CURRENT						
Start-Up Current	I_{st}		-	0.1	0.5	mA
Operating Supply Current	Ii	V_{PIN2}=V_{PIN3}=0V	-	11	20	mA
Zener Voltage	Viz	Ii=25mA	30	34	-	V

Note:

1. Toggle flip flop used only in PJ3844 and PJ3845.
2. These parameters, although guaranteed, are not 100% tested in production.
3. Parameter measured at trip point of latch with VPIN2=0
4. Gain defined as : $A = \frac{\Delta V_{PIN1}}{\Delta V_{PIN3}}$; $0 \leqq V_{PIN3} \leqq 0.8V$.
5. Adjust Vi above the start threshold before setting at 15V.

FIGURE 1- OUTPUT DEAD TIME versus OSCILLATOR FREQUENCY

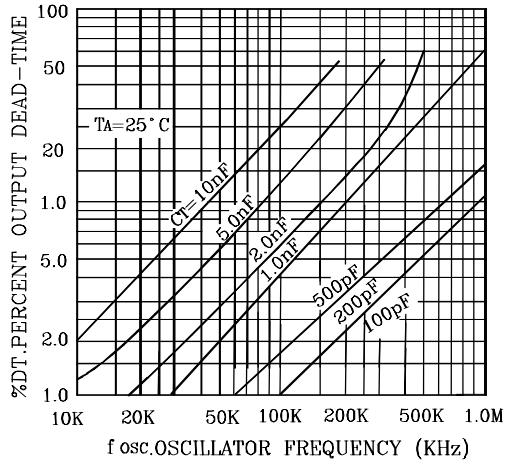


FIGURE 2- TIMING RESISTOR versus OSCILLATOR FREQUENCY

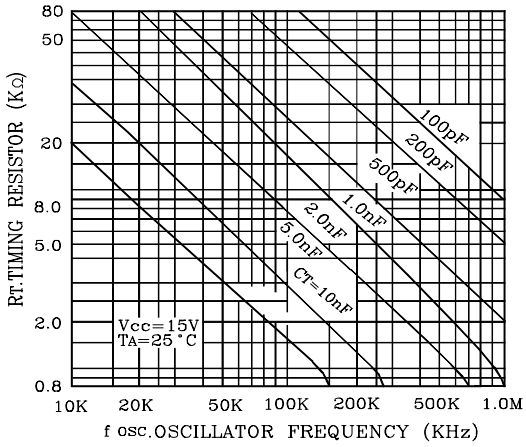


FIGURE 3-OSCILLATOR DISCHARGE CURRENT versus TEMPERATURE

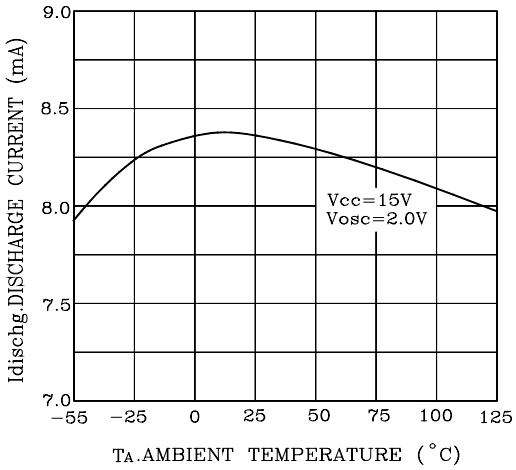


FIGURE 4-MAXIMUM OUTPUT DUTY CYCLE versus TIMING RESISTOR

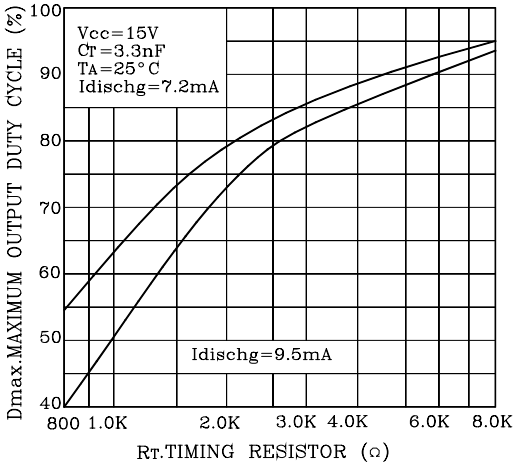


FIGURE 5-ERROR AMP SMALL SIGNAL TRANSIENT RESPONSE

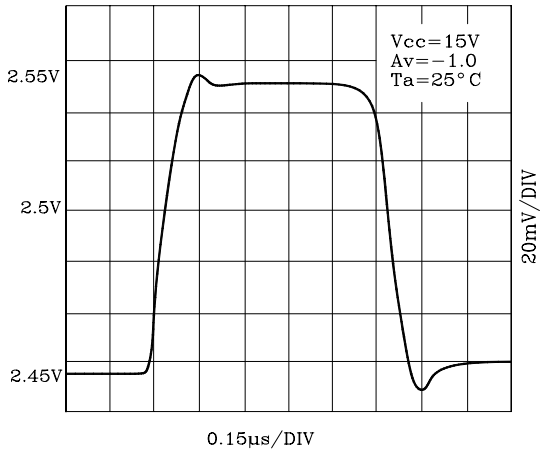


FIGURE 6-ERROR AMP LARGE SIGNAL TRANSIENT RESPONSE

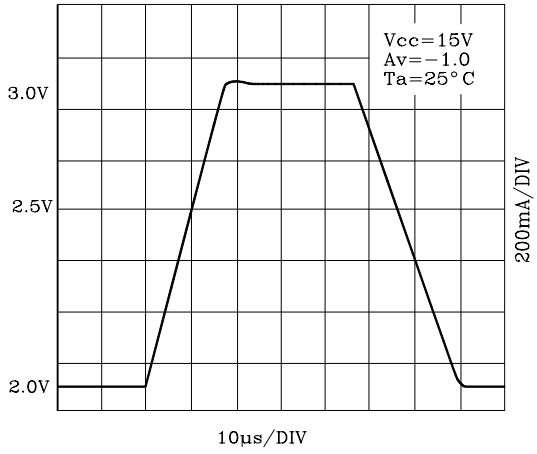


FIGURE 7-ERROR AMP OPEN-LOOP GAIN AND PHASE versus FREQUENCY

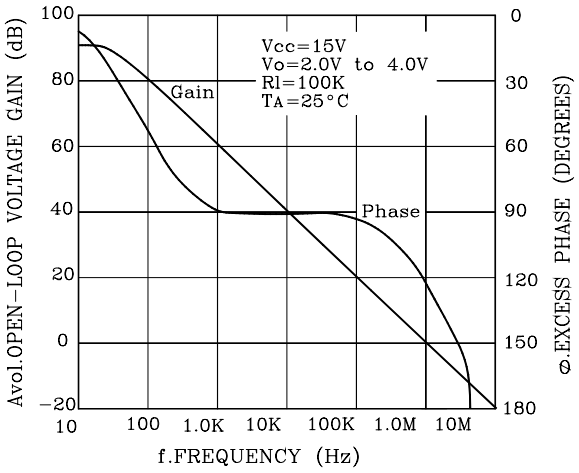


FIGURE 8-CURRENT SENSE INPUT THRESHOLD versus ERROR AMP OUTPUT VOLTAGE

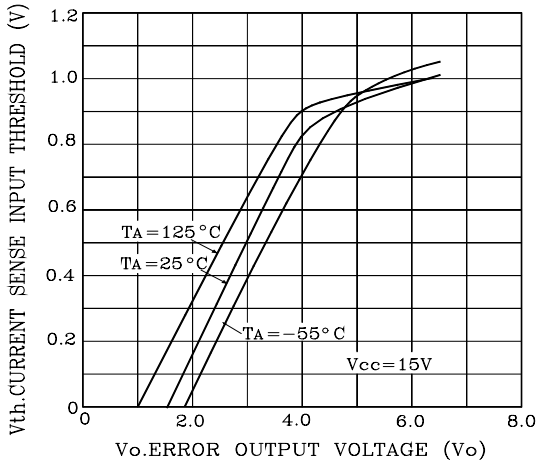


FIGURE 9-REFERENCE VOLTAGE CHANGE versus SOURCE CURRENT

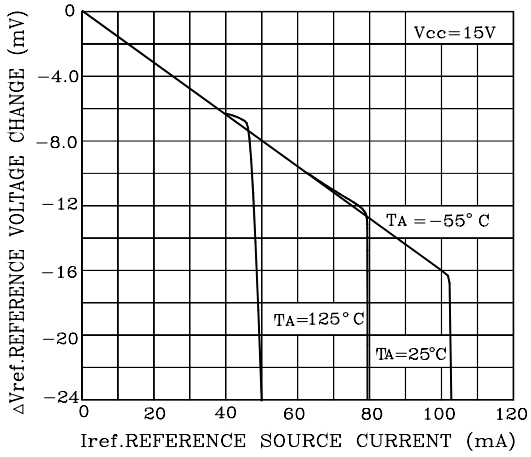


FIGURE 10-REFERENCE SHORT CIRCUIT CURRENT versus TEMPERATURE

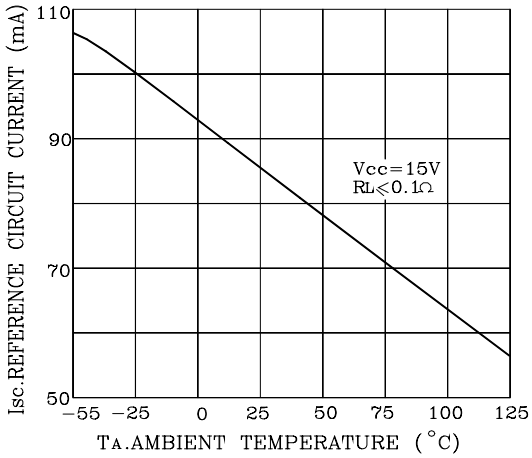


FIGURE 11- REFERENCE LOAD REGULATION

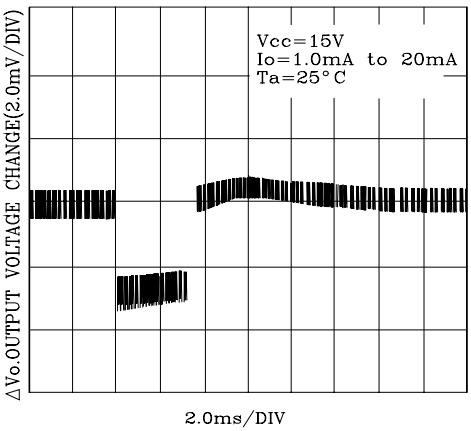


FIGURE 12-REFERENCE LINE REGULATION

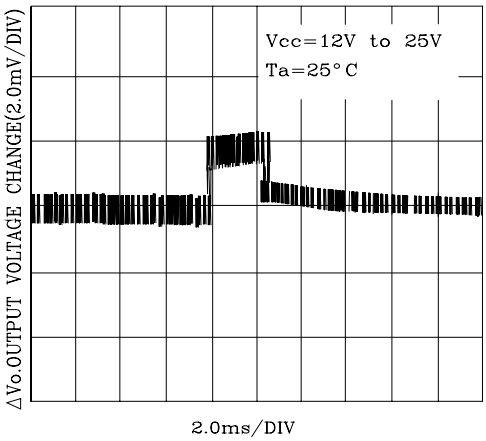


FIGURE 13-OUTPUT SATURATION VOLTAGE versus LOAD CURRENT

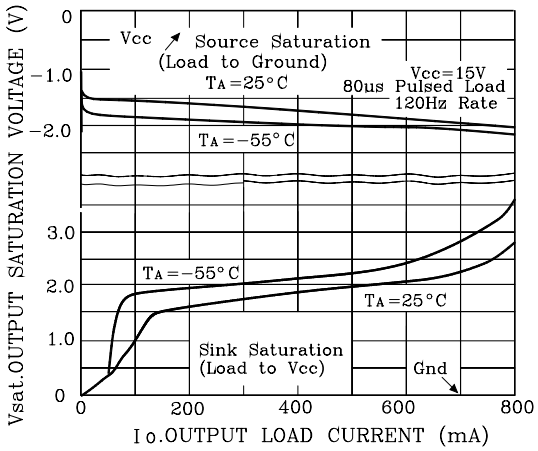


FIGURE 14-OUTPUT WAVEFORM

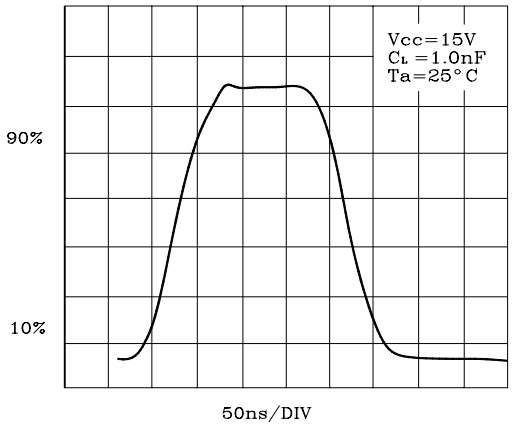


FIGURE 15-OUTPUT CROSS CONDUCTION

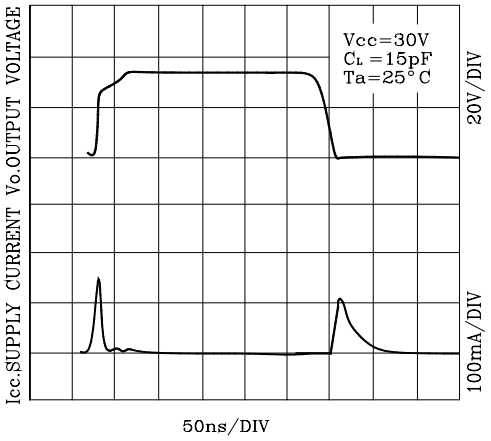


FIGURE 16-SUPPLY CURRENT versus SUPPLY VOLTAGE

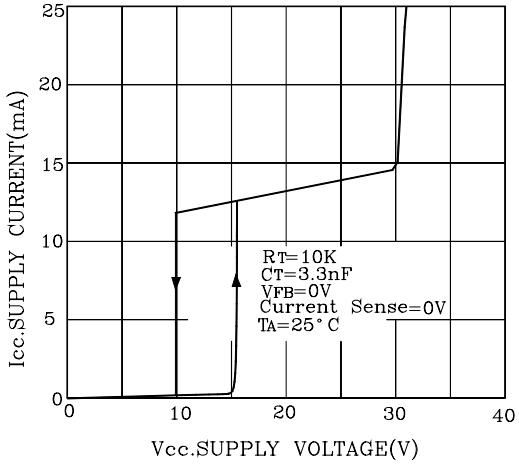
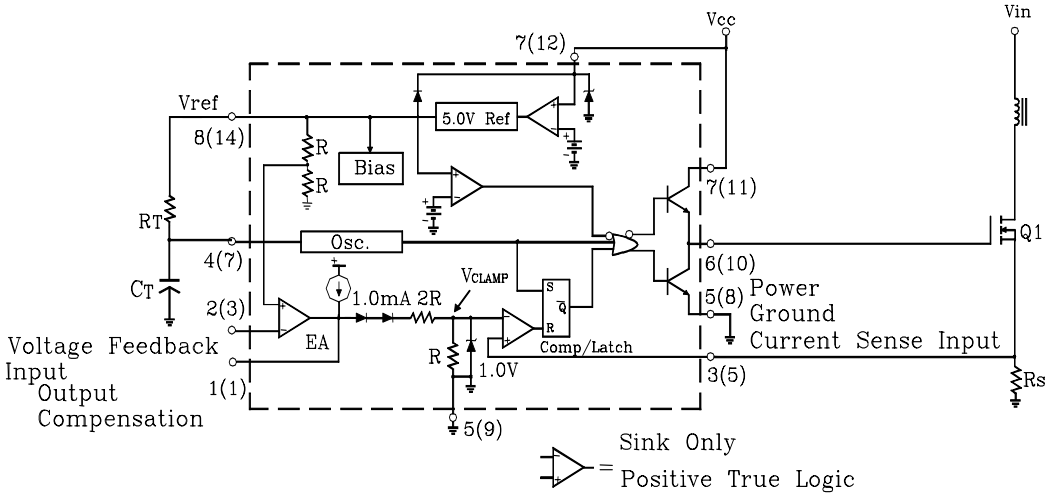
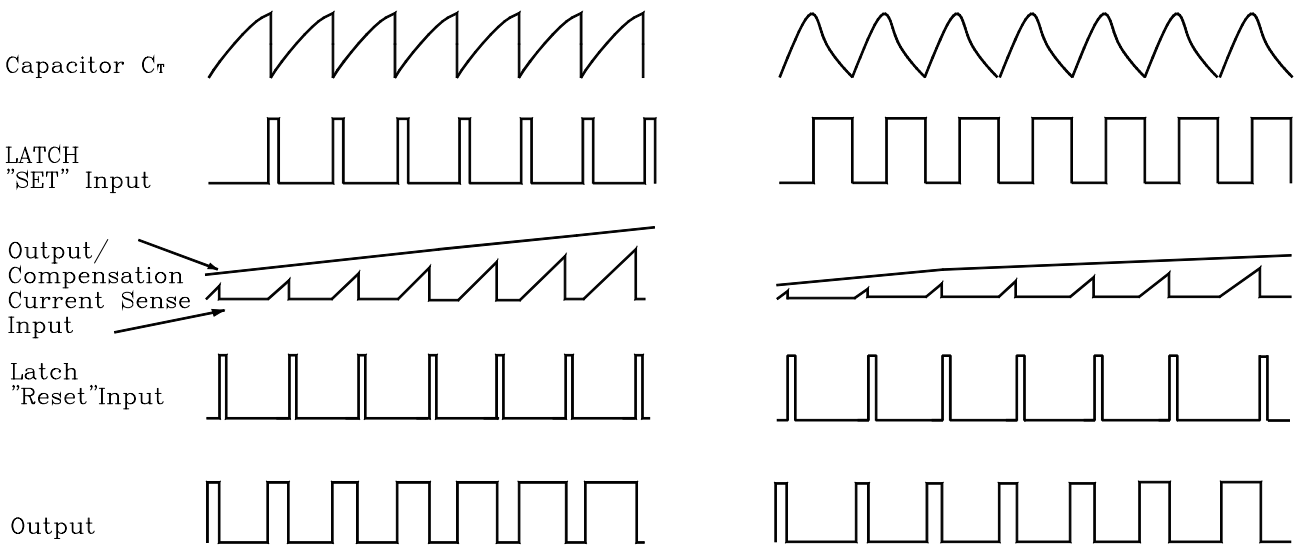


FIGURE 17-REPRESENTATIVE BLOCK DIAGRAM



Pin numbers adjacent to terminals are for the 8 pin dual-in-line package.
Pin numbers in parenthesis are for the SOP-14 package.

FIGURE 18-TIMING DIAGRAM



UNDERVOLTAGE LOCKOUT

Two undervoltage lockout comparators have been incorporated to guarantee that the IC is fully functional before the output stage is enabled. The positive power supply terminal (V_{CC}) and the reference output (Vref) are each monitored by separate comparators.Each has built-in hysteresis to prevent erratic output behavior as their respective thresholds are crossed. The large hysteresis and low start-up current of the PJ3842B makes it ideally suited in off-line converter applications where efficient bootstrap start-up technique (Figure 33). 36 V zener is connected as a shunt regulator from V_{CC} to ground.Its purpose is to protect the IC from excessive voltage that can occur during system start-up. The minimum operating voltage for the PJ3842B is 11V.

Output

These devices contain a single totem pole output stage that was specifically designed for direct drive of power MOSFET's. It is capable of up to ±1.0A peak drive current and has a typical rise and fall time of 50 ns with a 1.0nF load. Additional internal circuitry has been added to keep the Output in a sinking mode whenever an undervoltage lockout is active.This characteristic eliminates the need for an external pull-down resistor.

The SOP-8 surface mount package provides separate pins for Vc(output supply) and Power Ground.Proper implementation will significantly reduce the level of switching transient noise imposed on the control circuitry. This becomes particularly useful when reducing the Ipk(max) clamp level.The separate Vc supply input allows the designer added fiexlbility in tailoring the drive voltage independent of Vcc.A zener clamp is typically connected to this input when driving power MOSFETs in systems where Vcc is greater than 20V. Figure 25 shows proper power and control ground connections in a current sensing power MOSFET application.

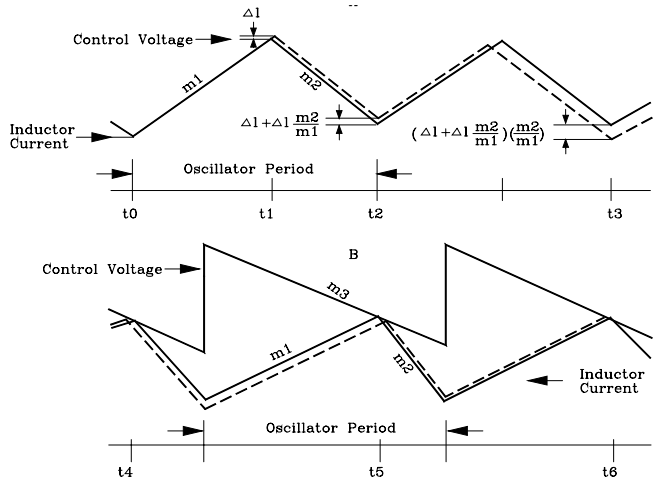
Reference

The 5.0V bandgap reference is trimmed to±2.0% on the PJ3842B.Its promary purpose to supply charging current to the oscillator timing capacitor.The reference has short circuit protection and is capable of providing in excess of 20mA for powering additional control system circuitry.

Design Considerations

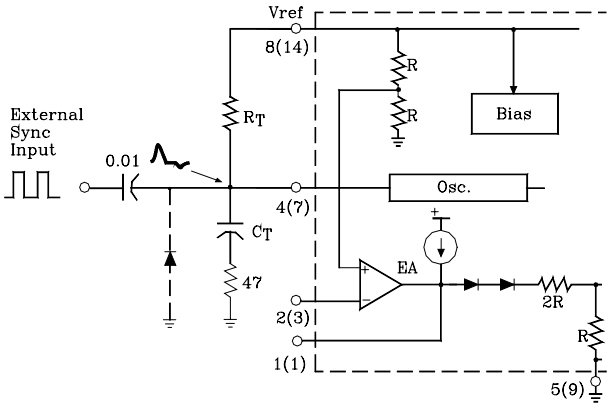
Do not attempt to construct the converter on wirewrap or plug-in prototype boards. High frequency circuit layout techniques are imperative to prevent pulsewidth jitter.This is usually caused by excessive noise pick-up imposed on the Current Sense or Voltage Feedback inputs.Noise immunity can be improved by lowering circuit impedances at these points.The printed circuit layout should contain a ground plane with lowcurrent signal and high-current switch and output grounds returning separate paths back to the input filter capacitor.Ceramic bypass capacitors(0.1 μ F) connected directly to Vcc,Vc, and Vref may be required depending upon circuit layout . This provides a low impedance path for filtering the high frequency noised. All high current loops should be kept as short as possible using heavy copper runs to minimize radiated EMI. The Error Amp compensation circuitry and the converter output voltage divider should be located close to the IC and as far as possible from the power switch and other noise generating components.

FIGURE 19-CONTINUOUS CURRENT WAVEFROMS



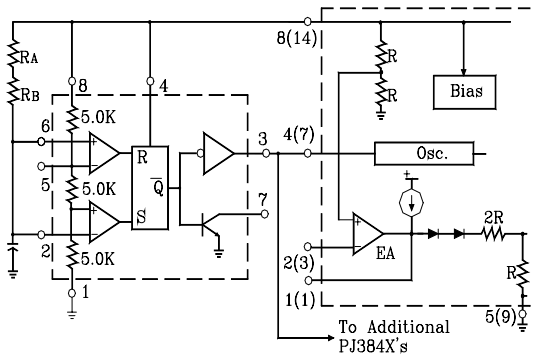
Current mode converters can exhibit subharmonic oscillations when operating at a duty cycle greater than 50% with continuous inductor current,This instability is independent of the regulators closed loop characteristics and is caused by the simultaneous operating conditions of fixed frequency and peak current detecting. Figure 19A shows the phenomenon graphically, At t_0 , switch conduction begins , causing the inductor current to rise at a slope of m_1. This slope is a function of the input voltage divided by the inductance. At t1, the Current Sense Input reaches the threshold established by the control voltage. This causes the switch to turn off and the current to decay at a slope of m_2, until the next oscillator cycle. This unstable condition can be shown if a perturbation is added to the control voltage , resulting in a small Δ1 (dashed line). With a fixed oscillator period, the current decay time is reduced, and the minimum current at switch turn-on(t_2) is increased by $\Delta 1+\Delta 1\ m_2/m_1$. The minimum current at the next cycle (t_3) decreases to ($\Delta 1+\Delta 1\ m_2/m_1)(m_2/m_1)$. This perturbation is multiplied by m_2/m_1 on each succeeding cycle , alternately increasing and decreasing the inductor current at switch turn-on, Several oscillator cycles may be required before the inductor current reaches zero causing the process to commence again. If m_2/m_1 is greater than 1, the converter will be unstable . Figure 19B shows that by adding an artificial ramp that is synchronized with the PWM clock to the control voltage . the Δ 1 perturbation will decrease to zero on succeeding cycles. This compensating ramp (m_3) must have a slope equal to or slightly greater than $m_2/2$ for stability . With $m_2/2$ slope compensation , the average inductor current follows the control voltage yielding true current mode operation. The compensating ramp can be derived from the oscillator and added to either the Voltage Feedback or Current Sense inputs (Figure 32).

FIGURE 20-EXTERNAL CLOCK SYNCHRONIZATION



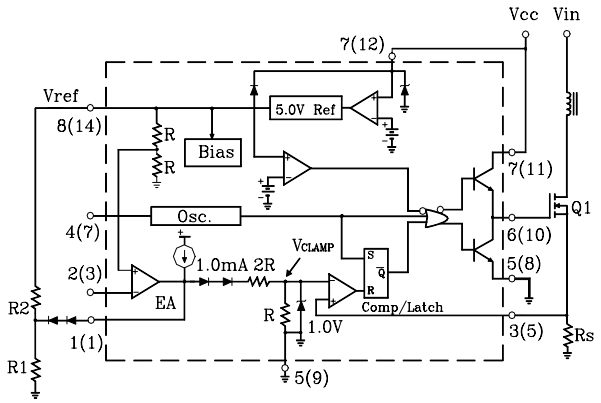
The diode clamp is required if the Sync amplitude is large enough to the cause the bottom side of C_T to go more than 300mV below ground.

FIGURE 21-EXTERNAL DUTY CYCLE CLAMP AND MULTI UNIT SYNCHRONIZATION



$$f = \frac{1.44}{(R_A + R_B)} \qquad D_{MAX} = \frac{R_B}{R_A + 2R_B}$$

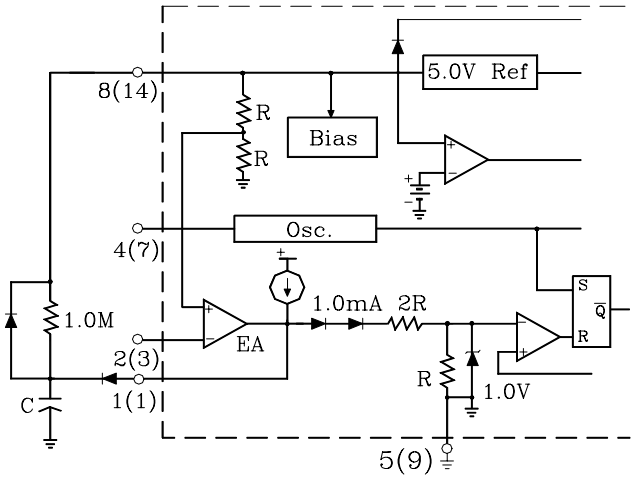
FIGURE 22-ADJUSTABLE REDUCTION OF CLAMP LEVEL



$$I_{pk}(max) = \frac{Vclmap}{Rs} \qquad \text{Where : } \le Vclmap \le 1.0V$$

$$Vclamp = \frac{1.67}{\left(\frac{R2}{R1} + 1\right)} + 0.33 \times 10^{-3}\left(\frac{R1\ R2}{R1 + R2}\right)$$

FIGURE 23-SOFT-START CIRCUIT



$I_{soft\text{-}Start}$=3600c in μF

FIGURE 24-ADJUSTABLE BUFFERED REDUCTION OF CLAMP LEVEL WITH SOFT-STAR

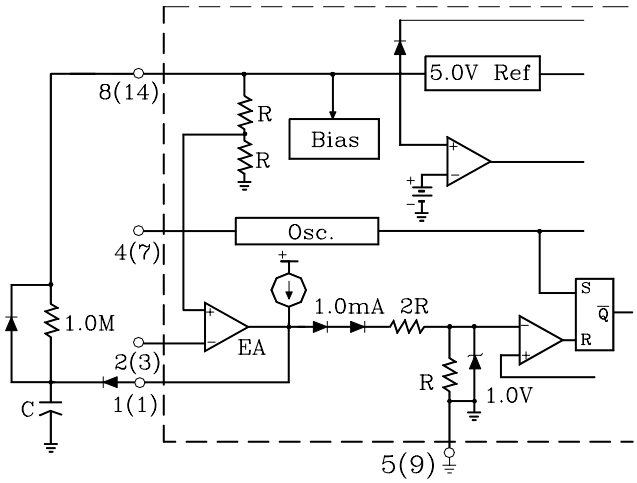
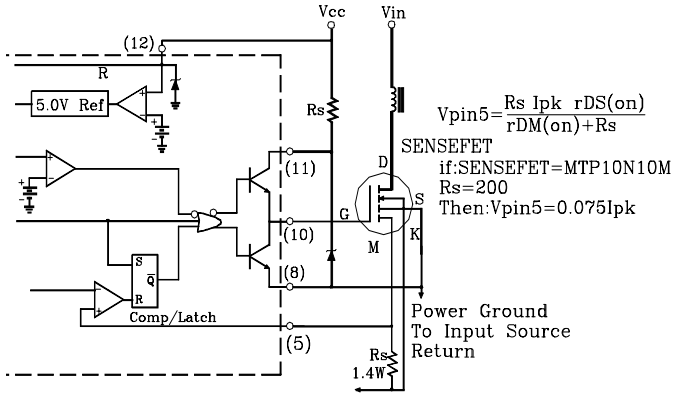
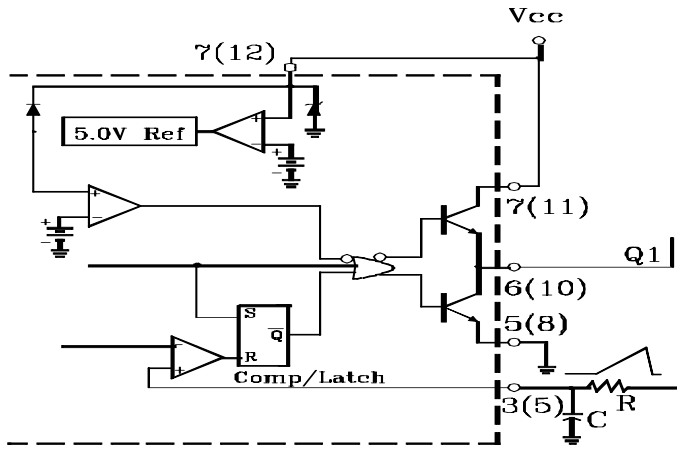


FIGURE 25-CURRENT SENSING POWER MOSFET



Virtually lossless current sensing can be achieved with the implementation of a SENSEFET power switch.For proper operation during over current conditions.a reduction of the Ipk(max) clamp level must be implemented.Refer to Figure 22 and 24

FIGURE 26-CURRENT WAVEFORM SPIKE SUPPRESSION



The addition of RC filter will eliminate instability caused by the leading edge splik on the current waveform.

FIGURE 27-MOSFET PARASITIC OSCILLATIONS

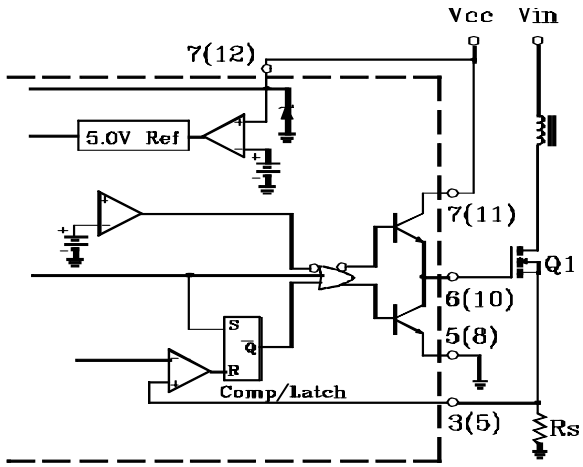
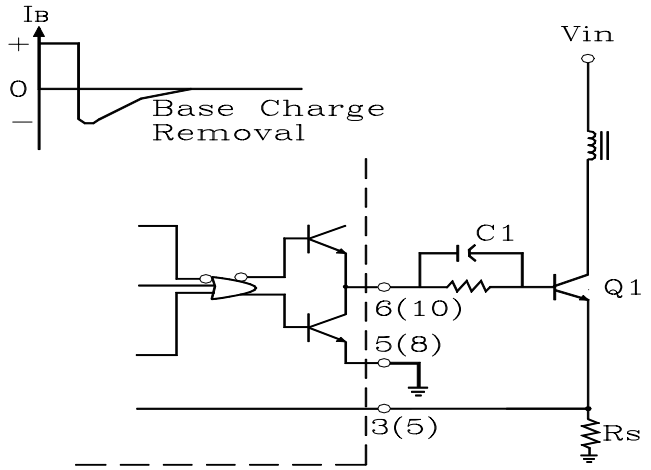


FIGURE 28-BIPOLAR TRANSISTOR DRIVE



The totem-pole output can furnish negative base current for enhanced transistor turn-off,with the additions of capacitor C1.

FIGURE 29-ISOLATED MOSFET DRIVE

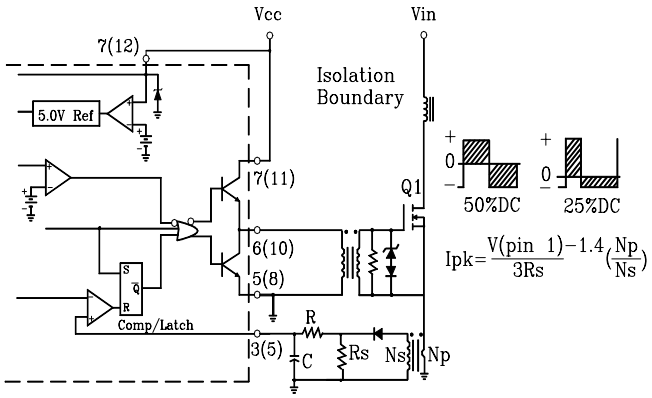
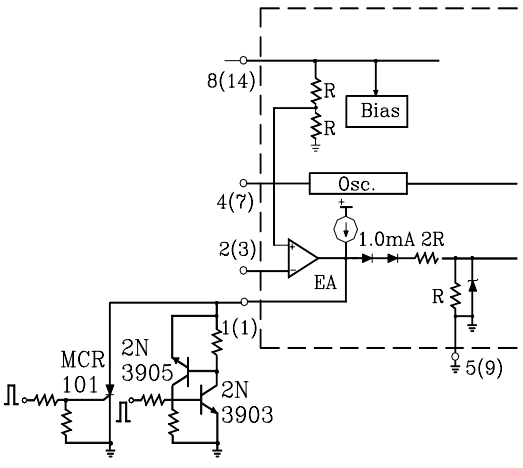
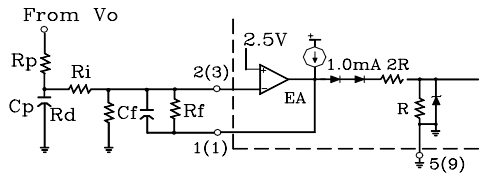


FIGURE 30-LATCHED SHUTDOWN

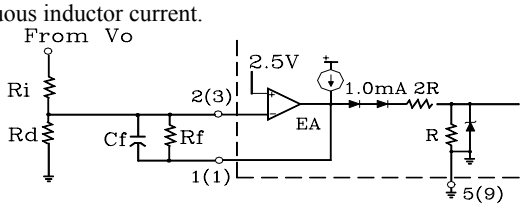


The MCR101 SCR must be selected for a holding of less than 0.5mA at T_A (min). The simple two transistor circuit can be used in place of the SCR as shown.All resistors are 10K

FIGURE 31-ERROR AMPLIFIER COMPENSATION

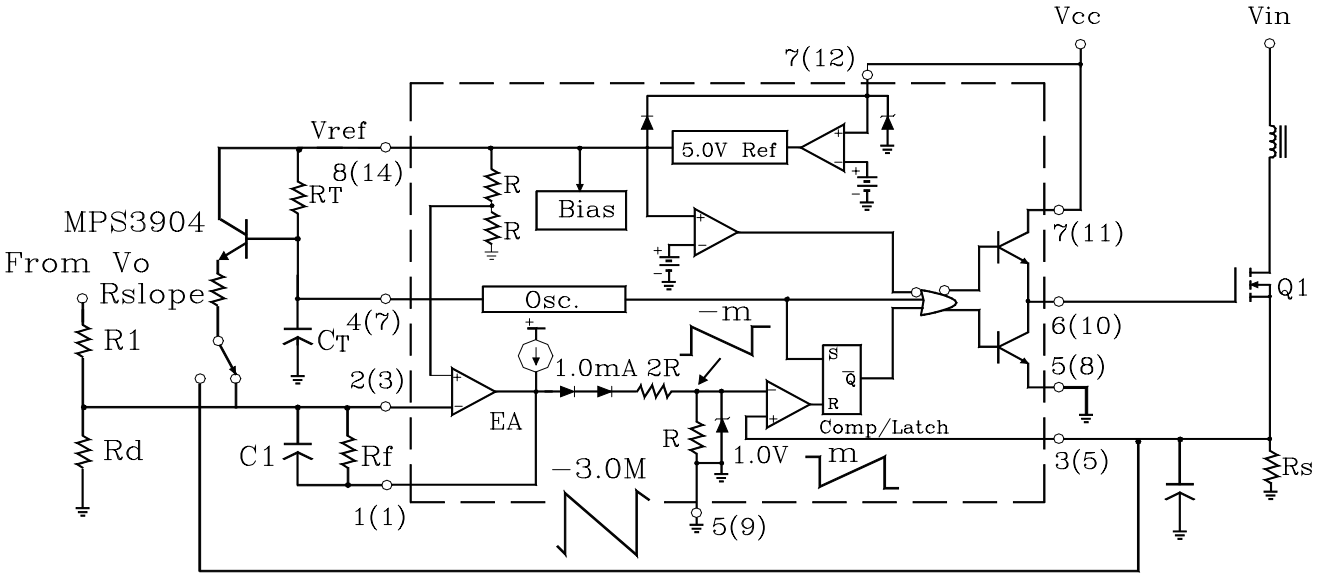


Error Amp compensation circuit for stabilizing any currentmode topology except for boost and flyback converters operating with continuous inductor current.



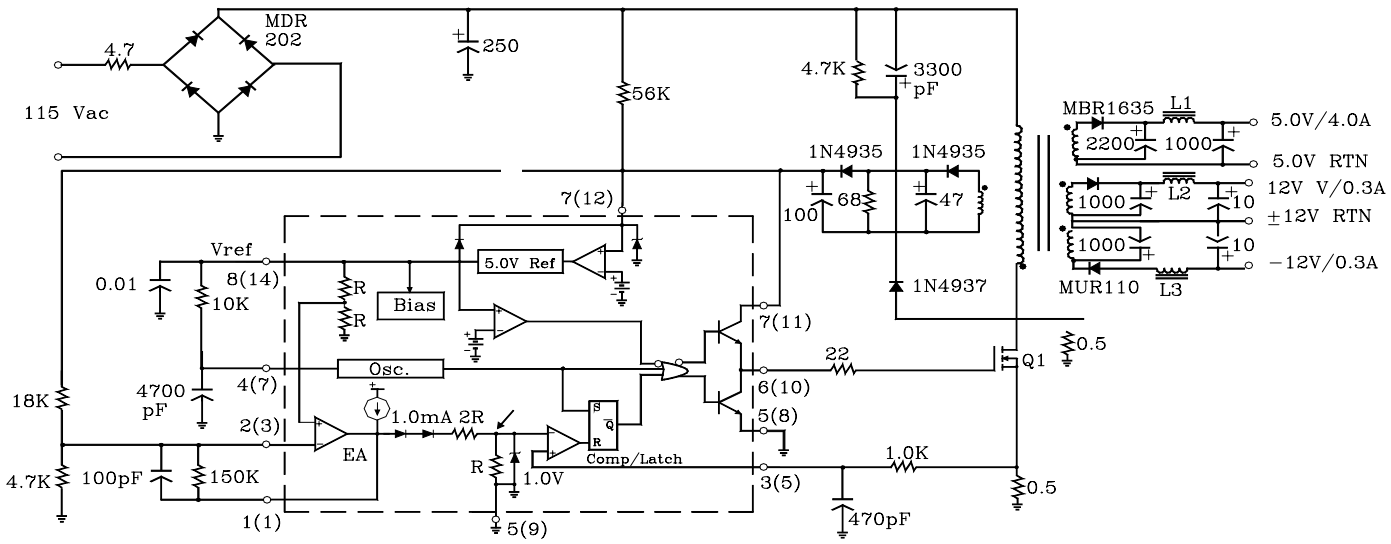
Error Amp compensation circuit for stabilizing any currentmode topology except for boost and flyback converters operating with continuous inductor current.

FIGURE 32-SLOPE COMPENSATION



The buffered oscillator ramp can resistively summed with either the voltage feedback or current sense inputs to provide slope compensation.

FIGURE 33-27 WATT OFF-LINE REGULATION



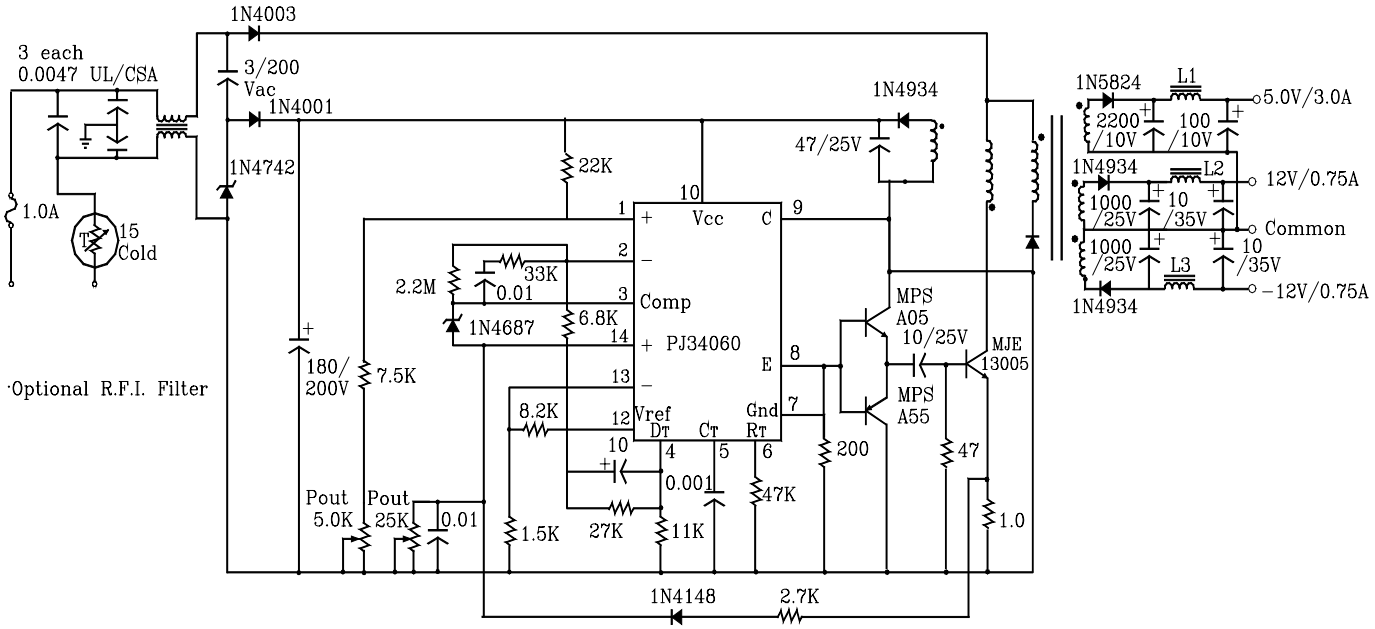
T1-Primary:45 Turns #26 AWG
Secondary ±12V :9 Turns #30 AWG (2 strands) Bifiliar Wound
Secondary 5.0V: 4 Turns (six strands) #26 Hexfiliar Wound
Secondary Feedback : 10 Turns #30 AWG (2 strands) Bifiliar Wound
Core: Ferroxcube EC35-3C8
Bobbin : Ferroxcube EC35PCB1
Gap：≅ 0.10 ” for a primary inductance of 1.0mH

L1-15 μH at 5.0A, Coilcraft 27156.
L2.L3-25 μH at 1.0A, Coilcraft 27157.

Line Regulation：5.0V ±12V	Vin=95 to 130 Vac	=50mV or ±0.5% =24mV or ±0.1%
Load Regulation：5.0V ±12V	Vin=115Vac, Iout =1.0A to 4.0A Vin=115Vac,Iout=100mA to 300mA	=300mV or ±3.0% =60mV or ±0.25%
Output Ripple：5.0V ±12V	Vin=115Vac	40mVp-p 80 Vp-p
Efficiency	Vin=115Vac	70%

All outputs are at nominal load currents unless otherwise noted.

FIGURE 21-33 WATT OFF-LINE FLYBACK CONVERTER WITH SOFT-START AND PRIMARY POWER LIMITING



TEST	CONDITIONS	RESULTS	
Line Regulation 5.0V	Vin=95 to 135 Vac, Io=3.0A	20mV	0.40%
Line Regulation± 12V	Vin=95 to 135 Vac, Io=±0.75A	52mV	0.26%
Line Regulation 5.0V	Vin=115 Vac, Io=1.0 to 4.0A	476mV	9.5%
Line Regulation± 12V	Vin=115 Vac, Io=±0.4 to ±0.9A	300mV	2.5%
Line Regulation 5.0V	Vin=115 Vac, Io=3.0A	45 mVp-p P.A.R.D.	
Line Regulation± 12V	Vin=115 Vac, Io=±0.75A	75 mV p-p P.A.R.D.	
Efficiency	Vin=115 Vac, Io 5.0V=3.0A Io ±12=±0.75A	74%	

T1
Coilcraft 11-464-16, 0.025" gap in each leg

Baobbin：
Coilcraft 37-573

Windings：
Primary, 2 each:
75 turns #26 Awg Bifilar wound

Feedback：
15 turns #26 Awg

Secondary , 5.0V：
6 turns #22 Awg Bifiar wound

Secondary , 5.0V：
14 turns #24 Awg Bifiar wound

L1
Coilcraft Z7156. 15 μF @ 5.0A

L2,L3
Coilcraft Z7157. 25 μF @ 1.0A

PIN FUNCTION DESCRIPTION

Pin No.	Function	Description
1	Compensation	This pin is the Error Amplifier output and is made available for loop compensation
2	Voltage Feedback	This is the inverting input of the Error Amplifier. It is normally connected to the switching power supply output through a resistor divider.
3	Current Sense	A voltage proportional to inductor current is connected to this input. The PWM uses this information to terminate the output switch conduction.
4	R_T/C_T	The Oscillator Frequency and maximum Output duty are programmed by connecting resistor R_T to Vref and capacitor C_T to ground operation to 500kHz is possible.
5	Gnd	This pin is the combined control circuitry and power ground (8-pin package only).
6	Output	This output directly drives the gate of a power MOSFET.Peak current up to 1.0A are soured and sunk by this pin.
7	Vcc	This pin is the positive supply of the control IC.
8	Vref	This pin is the reference output . It provides charging current for capacitor C_T through resistor R_T.

OPERATING DESCRIPTION

The PJ3842B series are high performance, fixed frequency, current mode controllers, They are specifically designed for Off-Line and DC-to-DC converter applications offering the designer a cost effective solution with minimal external components . A representative block diagram is shown in Figure 17.

OSCILLATOR

The oscillator frequency is programmed by the values selected for the timing components R_T and C_T. Capacitor C_T is charged from the 5.0V reference through resistor R_T to approximately 2.8V and discharge to 1.2V by an internal current sink.During the discharge of C_T, the oscillator generates an internal blanking pulse that holds the center input of the NOR gate high. This causes the Output to be in a low state, thus producing a controlled amount of output deadtime. Figure 1 shows R_T versus Oscillator Frequency and Figure 2, Output Deadtime versus Frequency, both for given values of C_T. Note that many values of R_T and C_T will give the same oscillator frequency but only onne combination will yield a specific output deadtime at a given frequency. The oscillator thresholds are temperature compensated, and the discharge current is trimmed and guaranteed to within ±10% at T_J =25℃. These internal circuit refinements minimum variations of oscillator frequency and maximum output duty cycle. The results are shown in Figure 3 and 4.

In many noise sensitive applications it may be desirable to frequency-lock the converter to an external system clock. This can be accomplished by applying a clock signal to the circuit shown in Figure 20. For reliable locking. The free-running oscillator frequency should be set about 10% less than the clock frequency . A method for multi unit synchronization is shown in Figure 21. By tailoring the clock waveform, accurate Output duty cycle clamping can be achieved.

ERROR AMPLIFIER

A fully compensated Error Amplifier with access to the inverting input and output is provided. It features a typical DC voltage gain of 90dB, and a unity gain bandwidth of 1.0MHz with 57 degrees of phase margin (Figure 7). The non-inverting input is internally biased at 2.5V and is not pinned out. The converter output voltage is typically divided down and monitored by the inverting input. The maximum input bias current is -2.0 μA which can cause an output voltage error that is equal to the product of the input bias current and the equivalent input divider source resistance.

The Error Amp Output (Pin 1) is provided for external loop compensation (Figure 31). The output voltage is offset by two diode drops (≈1.4V) and divided by three before it connects to the inverting input of the Current Sense Comparator. This guarantees that no drive pulses appear at the Output(Pin 6) when Pin 1 is at its lowest state (V_{OL}). This occurs when the power supply is operating and the load is removed, or at the beginning of a soft-start interval (Figure 23,24). The Error Amp minimum feedback resistance is limited by the amplifier's source current (0.5mA) and the required output voltage (V_{OH}) to reach the comparator's 1.0V clamp level:

$$R_{f(MIN)} = [3.0\ (1.0V)+1.4V] / \ 0.5mA \ = 8800\Omega$$

CURRENT SENSE COMPARATOR AND PWM LATCH

The PJ3842B operate as a current mode controller, whereby output switch conduction is initiated by the oscillator and terminated when the peak inductor current reaches the threshold level established by the Error Amplifier Output/Compensation (Pin 1). Thus the error signal controls the peak inductor current on a cycle-by-cycle basis. The Current Sense Comparator PWM Latch configuration used ensures that only a single appears at the Output during any given oscillator cycle. The inductor current is converted to a voltageby inserting the ground referenced sense resistor R_S in series with the source of output switch Q1. This voltage is monitored by the Current Sense Input (Pin 3) and compared to a level derived from the Error Amp Output. The peak inductor current under normal operating conditions is controlled by the voltage at pin 1 where:

$$I_{PK} = \ [V(Pin\ 1) - 1.4V] / 3R_S$$

Abnormal operating conditions occur when the power supply output is overloaded or if output voltage sensing is lost, Under these conditions, the Current Sense Comparator threshold will be internally clamped to 1.0V. Therefore the maximum peak switch current is:

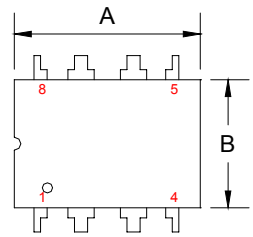
$$I_{PK\ (MAX)} = \ 1.0V / R_S$$

When designing a high power switching regulator it becomes desirable to reduce the internal clamp voltage in order to keep the power dissipation of R_S to a reasonable level. A simple method to adjust this voltage is shown in Figure 22. The two external diodes are used to compensate the internal diodes yielding a constant clamp voltage over temperature. Erratic operation due to noise pickup can result if there is an excessive reduction of the I_{PK} (max) clamp voltage.

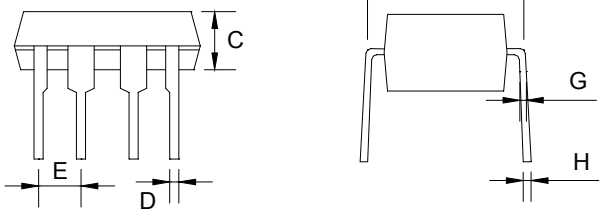
A narrow spike on the leading edge of the current waveform can usually be observed and may cause the power supply to exhibit an instability when the output is lightly loaded. This spike is due to the power transformer interwinding capacitance and output rectifier recovery time. The addition of an RC filter on the Current Sense Input with a time constant that approximates the spike duration will usually eliminate the instability: refer to Figure 26.

DIP-8 Mechanical drawing

1.Top View



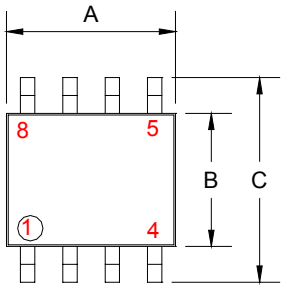
2.Side View



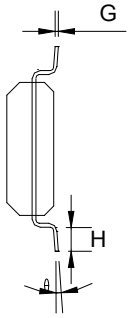
DIP-8 DIMENSION				
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	8.85	9.05	0.348	0.356
B	6.30	6.40	0.248	0.252
C	3.65	3.95	0.143	0.156
D	0.45	0.55	0.017	0.022
E	2.54BSC		0.10BSC	
F	7.75	8.00	0.305	0.315
G	0.20	0.30	0.007	0.012
H	-	10°	-	10°

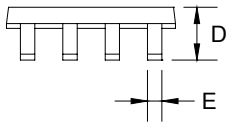
SOP-8 Mechanical drawing

1.Top View



2.Side View





SOP-8 DIMENSION				
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	5.80	6.20	0.228	0.244
D	1.40	1.50	0.055	0.059
E	0.33	0.51	0.013	0.020
F	1.27BSC		0.05BSC	
G	0.19	0.25	0.007	0.010
H	0.40	1.27	0.016	0.050
θ	0°	8°	0°	8°