MIC2772

Dual Voltage Supervisor

General Description

The MIC2772 is a dual power supply supervisor that provides under-voltage monitoring and power-on reset generation. It may replace two discrete voltage supervisors such as MIC1810, MIC1815, MIC809, MIC811, MIC6315, etc. The two voltage supervisors are completely independent. Each functional block features an under-voltage detector, a delay-generator, and a de-bounced manual reset input.

A wide choice of voltage thresholds is available. The reset output is asserted at power-on and any time the input voltage drops below the reference voltage. It remains asserted for the chosen timeout period after the input rises back above the threshold. Reset timeouts of 20, 140, and 1100ms (minimum) are available.

A reset can be generated at any time by asserting the manual reset input, /MR. This input is internally de-bounced, and the reset output will remain active for the timeout period after the release of /MR. The /MR input can also be used to daisy-chain one or more of the MIC2772's supervisors onto existing power monitoring circuitry or other supervisors.

The tiny 2x2mm MLF package has a footprint smaller than that of a single SOT23 voltage supervisor.

Data sheets and support documentation can be found on Micrel's web site at www.micrel.com.

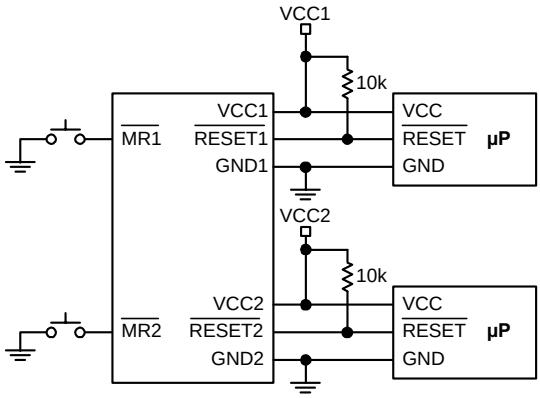
Features

- Two independent voltage supervisors
- Directly replaces discrete supervisors
- Generates power-on reset pulses
- De-bounced manual reset Inputs
- Choice of voltage thresholds
- 20, 140, or 1100ms reset timeouts
- Reset output may be pulled above VCC
- Rejects brief input transients
- Ultra-small 2x2mm MLF package

Applications

- Servers
- Embedded Controllers
- Telecommunications Systems
- Power Supply Sequencing
- Hot-swapping
- Power supplies

Typical Application



MIC2772 Typical Application Circuit

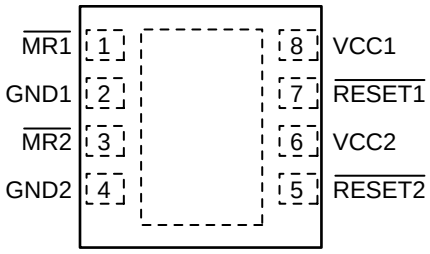
Ordering Information

Part Number		Top Mark		Supervisor 1		Supervisor 2	
Standard	**Pb-Free**	**Standard**	**Pb-Free**	**V_{TH} (V)**	**t_{RESET} (ms)**	**V_{TH} (V)**	**t_{RESET} (ms)**
	MIC2772-L2L3YML[2]		$\overline{UP0}$	4.63	20	4.63	140
	MIC2772-M2M3YML[2]		$\overline{UP1}$	4.38	20	4.38	140
MIC2772-L3L3BML[1]	MIC2772-L3L3YML[1]	UP2	$\overline{UP2}$	4.63	140	4.63	140
MIC2772-M3M3BML[1]	MIC2772-M3M3YML[1]	UP3	$\overline{UP3}$	4.38	140	4.38	140
MIC2772-T3T3BML[1]	MIC2772-T3T3YML[1]	UP4	$\overline{UP4}$	3.08	140	3.08	140
MIC2772-S3S3BML[1]	MIC2772-S3S3YML[1]	UP5	$\overline{UP5}$	2.93	140	2.93	140
	MIC2772-T2T3YML[2]		$\overline{UP6}$	3.08	20	3.08	140
	MIC2772-S2S3YML[2]		$\overline{UP7}$	2.93	20	2.93	140
	MIC2772-L3T3YML[2]		$\overline{UP8}$	4.63	140	3.08	140
	MIC2772-M3S3YML[2]		$\overline{UP9}$	4.38	140	2.93	140

Note:

1. Available now.
2. Contact factory.

Pin Configuration



8-lead 2mm X 2mm MLF(ML)

Pin Description

Pin Number	Pin Name	Pin Function
1	/MR1	Digital Input; supervisor 1. Driving this pin low initiates an immediate and unconditional reset. If VCC1 is above the threshold when /MR1 is released (returns high), RESET1 will be de-asserted no less than t_{RESET1} later. /MR1 may be driven by a CMOS or TTL logic signal or a mechanical switch. De-bouncing is performed internally. /MR1 has an internal pull-up to VCC1; leave open if unused.
2	GND1	Ground return for supervisor 1.
3	/MR2	Digital Input; supervisor 2. Driving this pin low initiates an immediate and unconditional reset. If VCC2 is above the threshold when /MR2 is released (returns high), the /RESET2 will be de-asserted no less than t_{RESET2} later. /MR2 may be driven by a CMOS or TTL logic signal or a mechanical switch. De-bouncing is performed internally. /MR2 has an internal pull-up to VCC2; leave open if unused.
4	GND2	Ground return for supervisor 2.
5	/RESET2	Digital Output; open-drain; supervisor 2. Asserted low whenever VCC2 falls below the threshold voltage. It remains asserted for no less than t_{RESET2} and is de-asserted after VCC2 returns above the threshold.
6	VCC2	Analog Input. Power supply input for supervisor 2.
7	/RESET1	Digital Output; open-drain; supervisor 1. Asserted low whenever VCC1 falls below the threshold voltage. It remains asserted for no less than t_{RESET1} and is de-asserted after VCC1 returns above the threshold.
8	VCC1	Analog Input. Power supply input for supervisor 1.

Absolute Maximum Ratings[1]

Supply Voltage, V_{CC} ..... -0.3V to 6.0V
Input Voltage, /MR ..... -0.3V to V_{CC} + 0.3V
Input Voltage, /RESET ..... -0.3V to 6.0V
Input Current (VCC, /MR) 20mA
Output Current (/RESET) 20mA
Storage Temperature..... -65°C to +150°C
ESD Rating (Note 3) 3kV

Operating Ratings[2]

Supply Voltage ..... 1V to 5.5V
Input Voltage (/MR) ..... 0 to 5.5V
Input Voltage (/RESET) ..... 0 to +5.5V
Operating Temperature Range (T_A)..... -40°C to +85°C
Lead Temperature – Soldering, 10s ..... 300°C
Package Thermal Resistance (θ_{JA})..... 93°C/W

Electrical Characteristics

For typical values, T_A = 25°C, 2.5V ≤ VCC*n* ≤ 5.5V; values in bold are for 2.5V ≤ VCC*n* ≤ 5.5V, $T_{MIN} \le T_A \le T_{MAX}$, unless otherwise noted.

Symbol	Parameter	Condition	Min	Typ	Max	Units
Power Supply						
I_{DD}	Supply Current	/MR1 = /MR2 = /RESET1 = /RESET2 = open, VCC1 = VCC2 = 5.5V		10	**30**	µA
		/MR1 = /MR2 = /RESET1 = /RESET2 = open, VCC1 = VCC2 = 3.6V		10	**20**	µA
		/MR1 = /MR2 = /RESET1 = /RESET2 = open, VCCn = 0V, VCCm = 5.5V		5	**15**	µA
		/MR1 = /MR2 = /RESET1 = /RESET2 = open, VCCn = 0V, VCCm = 3.6V		5	**10**	µA
/RESETn OUTPUTS						
V_{THn}	Reset-voltage threshold	L voltage code	**4.5**	4.63	**4.75**	V
		M voltage code	**4.25**	4.38	**4.50**	V
		S voltage code	**2.85**	2.93	**3.00**	V
		T voltage code	**3.00**	3.08	**3.15**	V
t_{RESET}	Reset Pulse Width	timeout code = 2	**20**		**44**	ms
		timeout code = 3	**140**		**320**	
		timeout code = 4	**1100**		**2500**	
V_{OL}	/RESET Output Voltage Low	$V_{CCn} \ge 4.25V$, I_{SINK} = 3.2mA			**0.4**	V
		$V_{CCn} \ge 2.5V$, I_{SINK} = 1.2mA			**0.3**	V
		$V_{CCn} \ge 1V$, I_{SINK} = 50µA			**0.3**	V
I_{LEAK}	Output leakage	/RESET not asserted			**±1**	µA
/MRn INPUTS						
V_{IH}	Input Voltage, High	V_{THn} > 4.0V	**2.3**			V
		V_{THn} < 4.0V	**0.7*VCC**			V
V_{IL}	Input Voltage, Low	V_{THn} > 4.0V			**0.8**	V
		V_{THn} < 4.0V			**0.25*VCC**	V

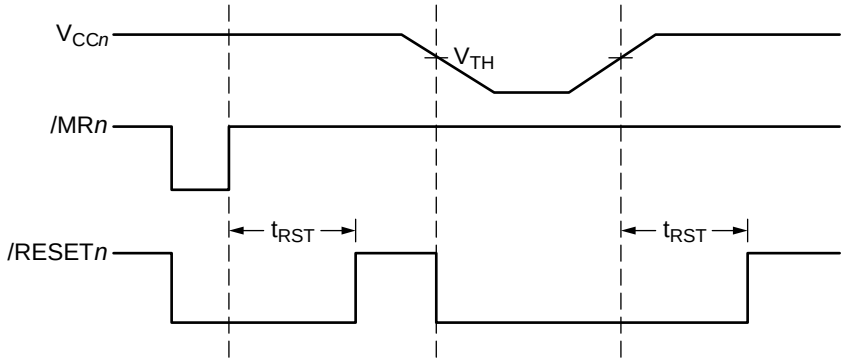
Electrical Characteristics cont.

Symbol	Parameter	Condition	Min	Typ	Max	Units
t_{PROP}	/MR to /RESET Propagation Delay	/MRn < V_{IL} → /RESETn < V_{IL}		0.5		µs
t_{MIN}	Minimum Input Pulse Width	Reset Occurs	**10**			µs
t_{REJECT}	Widest Pulse Ignored	No Reset Occurs		100		ns
R_{PU}	Pull-up Resistance		**10**	20	**30**	kΩ

Notes:

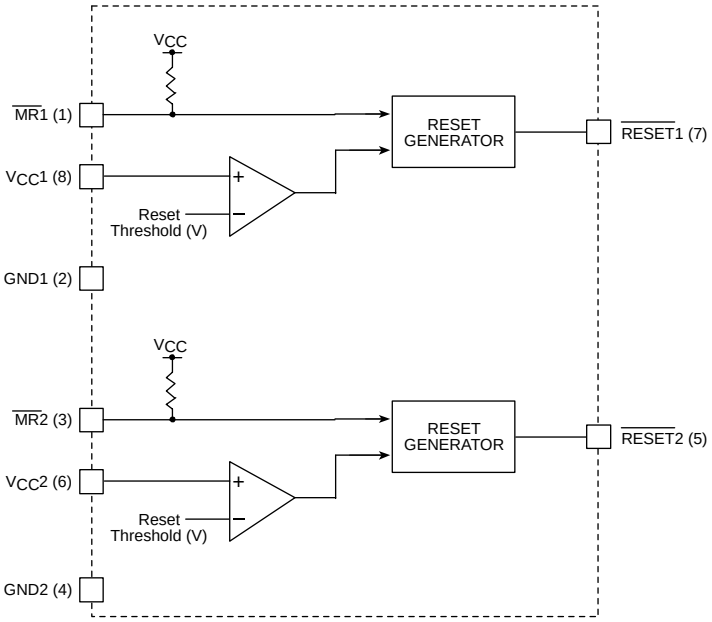
1. Exceeding the absolute maximum rating may damage the device.
2. The device is not guaranteed to function outside its operating rating.
3. Devices are ESD sensitive. Handling precautions recommended. Human body model, 1.5k in series with 100pF.

Timing Diagram



MIC2772 Timing Diagram

Functional Block Diagram



MIC2772 Block Diagram

Application Information

Reset Output, /RESET

The /RESET pin is active low (open drain) pin. The /RESET pin is asserted whenever VCC falls below the reset threshold voltage or if /MR (manual reset) is forced low. The /RESET pin remains asserted for the duration of the threshold timeout period after VCC has risen above the reset threshold and/or /MR has returned high. The reset function ensures the microprocessor is properly reset and power up in a known condition after a power failure. /RESET will remain valid with VCC as low as 1.0V.

The /RESET output is a simple open-drain N-channel MOSFET structure. A pull-up resistor must be used to pull this output to some voltage. For most applications, this voltage will be the same power supply that supplies VCC to MIC2772. It is possible however to tie this resistor to some other voltage. This will allow the MIC2772 to monitor one voltage while level-shifting the /RESET output to some other voltage. The pull-up voltage must be limited to 6.0V or less (absolute maximum) to avoid damage to the MIC2772. The resistor must be small enough to supply current to the inputs and leakage paths that are driven by the /RESET output.

Manual Reset Input, /MR

The ability to initiate a reset via external logic or a manual switch is provided in addition to the MIC2772's automatic supervisory functions. Driving the /MR input to a logic low causes an immediate and unconditional reset to occur. Assuming VCC is within tolerance when /MR is released (returns high), the /RESET output will be de-asserted no less than t_{RESET} later. /MR may be driven by a CMOS or TTL logic signal, or a mechanical switch. Typically, a momentary push-button switch is connected such that /MR is shorted to ground when the switch contacts close. Switch de-bouncing is performed internally; the switch may be connected directly between /MR and GND. /MR has an internal 20kΩ pull-up resistor (typical) to VCC and may be left open if unused.

Transients on VCC

The MIC2772 is inherently immune to very short "glitches" on VCC. In the case of very brief transients, VCC may drop below the reset-voltage threshold without triggering a reset. As shown in the graph, the MIC2772 is relatively immune to transients with typical duration of 25us. The lines on the graph represent the typical allowable transient duration for a given amount of threshold overdrive that will not generate a reset. The data was taken by adding negative-going square-wave pulse to a DC input voltage set at 0.5V above actual measured threshold for the part being characterized. Figure 1 shows the graph for the MIC2772[UP3] and Figure 2 shows the graph for the MIC2772[UP5]

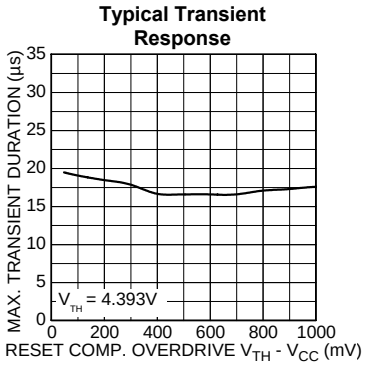


Figure 1

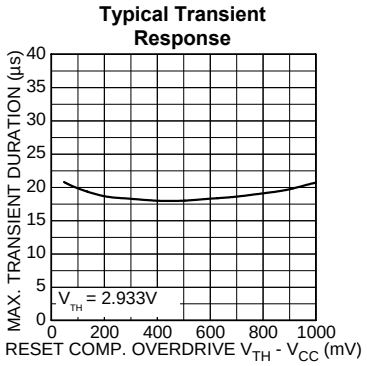


Figure 2

Interfacing to Processors with Bi-directional Reset Pins

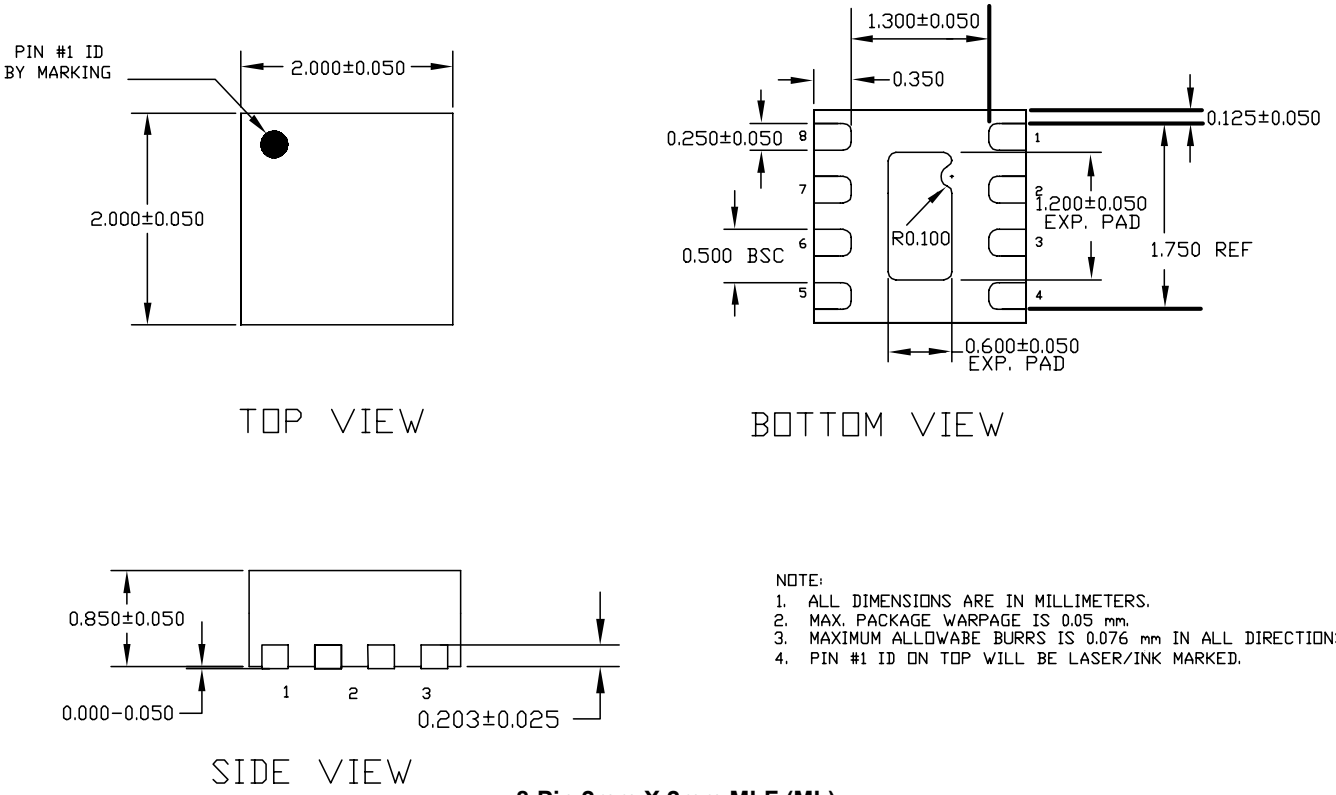
Some microprocessors have reset signal pins that are bi-directional, rather than input only. The Motorola 68HC11 family is one example. Because the MIC2772's output is active-low, open-drain, it can be connected directly to the processor's reset pin with only the pull-up resistor normally required.

MIC2772 Replaces Single Supervisor

The table below lists common single voltage supervisors that can be considered for replacement by MIC2772.

P/N Suffix	Supervisor #1	Supervisor #2
L2L3	MIC6315-46D2	MIC1810-5, MIC6315-46D3, MIC809L, MIC811L
M2M3	MIC6315-44D2	MIC1810-10, MIC6315-44D3, MIC809M, MIC811M
L3L3	MIC1810-5, MIC6315-46D3, MIC809L, MIC811L	MIC1810-5, MIC6315-46D3, MIC809L, MIC811L
M3M3	MIC1810-10, MIC6315-44D3, MIC809M, MIC811M	MIC1810-10, MIC6315-44D3, MIC809M, MIC811M
T3T3	MIC6315-31D3, MIC809T, MIC811T	MIC6315-31D3, MIC809T, MIC811T
S3S3	MIC1815-10, MIC6315-29D3, MIC809S, MIC811S	MIC1815-10, MIC6315-29D3, MIC809S, MIC811S
T2T3	MIC6315-31D2	MIC6315-31D3, MIC809T, MIC811T
S2S3	MIC6315-29D2	MIC1815-10, MIC6315-29D3, MIC809S, MIC811S
L3T3	MIC1810-5, MIC6315-46D3, MIC809L, MIC811L	MIC6315-31D3, MIC809T, MIC811T
M3S3	MIC1810-10, MIC6315-44D3, MIC809M, MIC811M	MIC1815-10, MIC6315-29D3, MIC809S, MIC811S

Package Information



8-Pin 2mm X 2mm MLF (ML)

MICREL, INC. 2180 FORTUNE DRIVE SAN JOSE, CA 95131 USA
TEL +1 (408) 944-0800 FAX +1 (408) 474-1000 WEB http:/www.micrel.com

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