Power Management ICs for TV / Monitor

General Description

The LP6283 generates all the supply rails for thin-film transistor (TFT) liquid-crystal display (LCD) panels in TVs and monitors. It includes boost and buck regulators, VGH and VGL charge pump regulators, gate pulse modulator (GPM) , HV LDO, voltage detector (XAO) and VCOM OP. The LP6283 supports input voltage from 8V to 14V and is optimized for LCD TV panel and LCD monitor applications running directly from 12V supply.

The boost and buck regulators feature internal power MOSFETs and high-frequency operation, allowing the use of small inductors and capacitors, for in a compact solution. Both switching regulators use fixed-frequency, current-mode control architectures, providing fast load-transient response and easy compensation.

The VGH and VGL charge-pump regulators provide supply voltages for the TFT gate driver. Both output voltages can be adjusted with external resistive voltage dividers.

Order Information

LP6283 □ □ □

- F: Pb-Free
- Package Type
  - QVF : TQFN-48

Applications

✧ LCD TV/Monitor

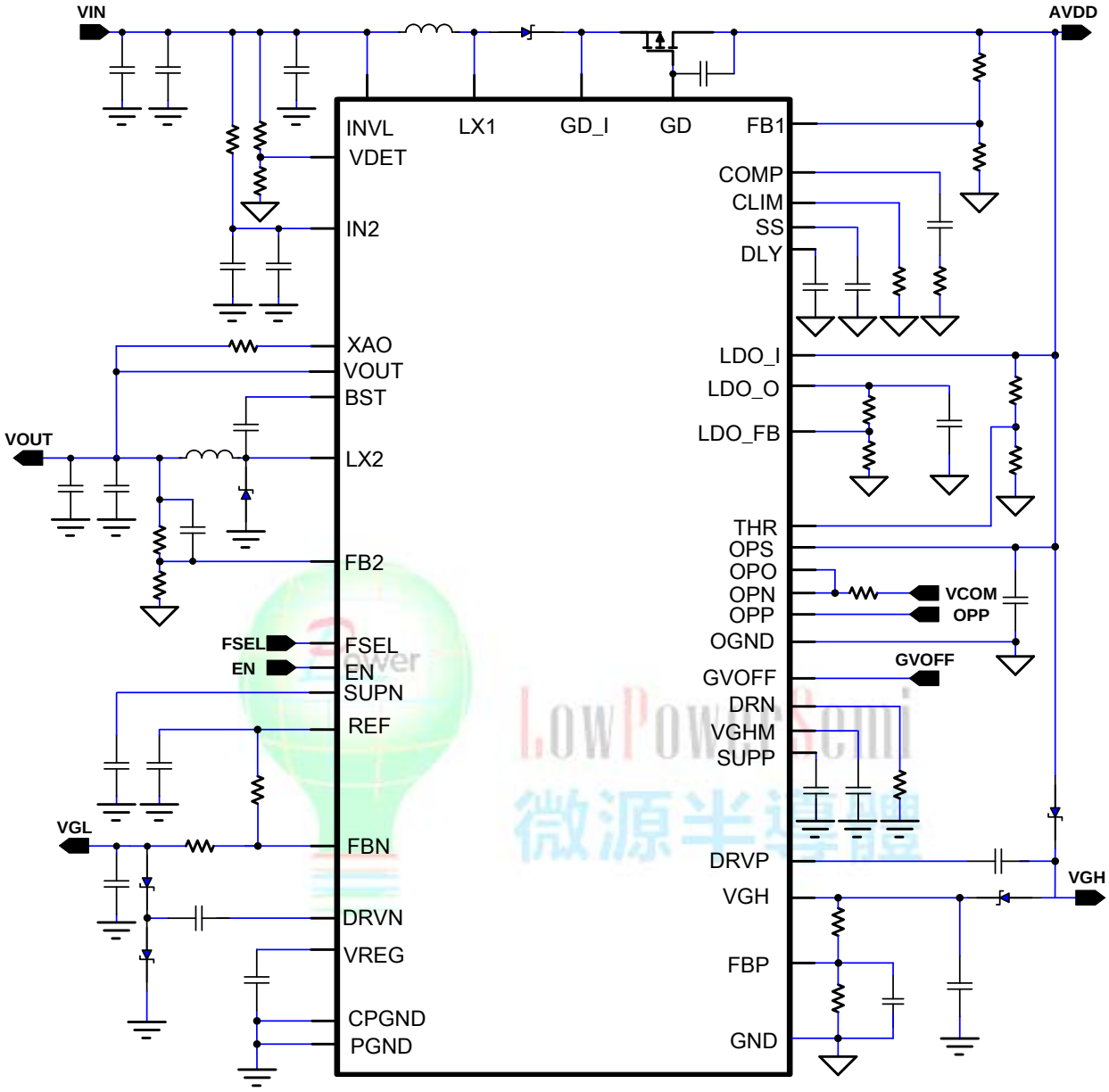
Features

- 8V to 14V Supply Input Voltage Range
- Current-Mode Boost Regulator
  - 20V 3.5A 0.1Ω Internal N-MOSFET
  - Programmable Over Current Protection
  - Programmable Soft-Start
- Current-Mode Buck Regulator
  - 16.5V 2A 0.15Ω Internal N-MOSFET
  - Over Current Protection
  - Adjustable Output Voltage from 1.8V to 3.3V
- Adjustable VGH Charge Pump
  - Continuous Output Current 50mA
- Adjustable VGL Charge Pump
  - Continuous Output Current 50mA
- Gate Pulse Modulator
  - 18V to 35V Positive Supply Input
  - Power-On/Off Sequence Control
  - On-Chip GPM Controller with Adjustable Falling Time and Falling Stop Voltage
- Voltage Detector (XAO)
  - Adjustable Detecting Voltage (±1%)
  - N-Channel Open-Drain Output
- VCOM OP
  - 5V to 20V Input Supply Voltage
  - ±300mA Output Short-Circuit Current for 1ms
  - 45V/μs Slew Rate
  - 20MHz, –3dB Bandwidth
- HV LDO
  - 5V to 20V Input Supply Voltage
  - Adjustable Output Voltage (±0.5%)
  - Over Current Protection (60mA)
  - Low Dropout Voltage 0.5V (60mA)
- Selectable Frequency (500kHz/750KHz)
- External PMOS Isolation Switch Controlled by Gate Drive Signal
- Over Temperature Protection
- Power On Sequence Control
- TQFN 48 Package
- RoHS Compliant and Halogen Free
- Pb-Free Package

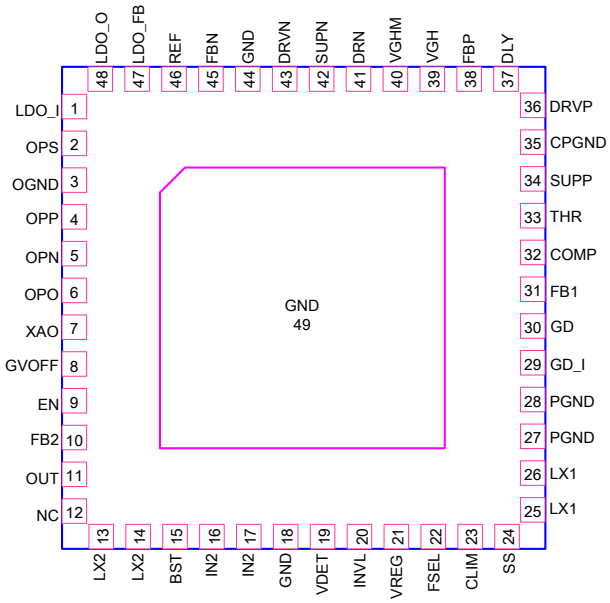
Marking Information

Device	Marking	Package	Shipping
LP6283	LPS LP6283 YWX	TQFN-48	
Y: Y is year code. W: W is week code. X: X is series number.			

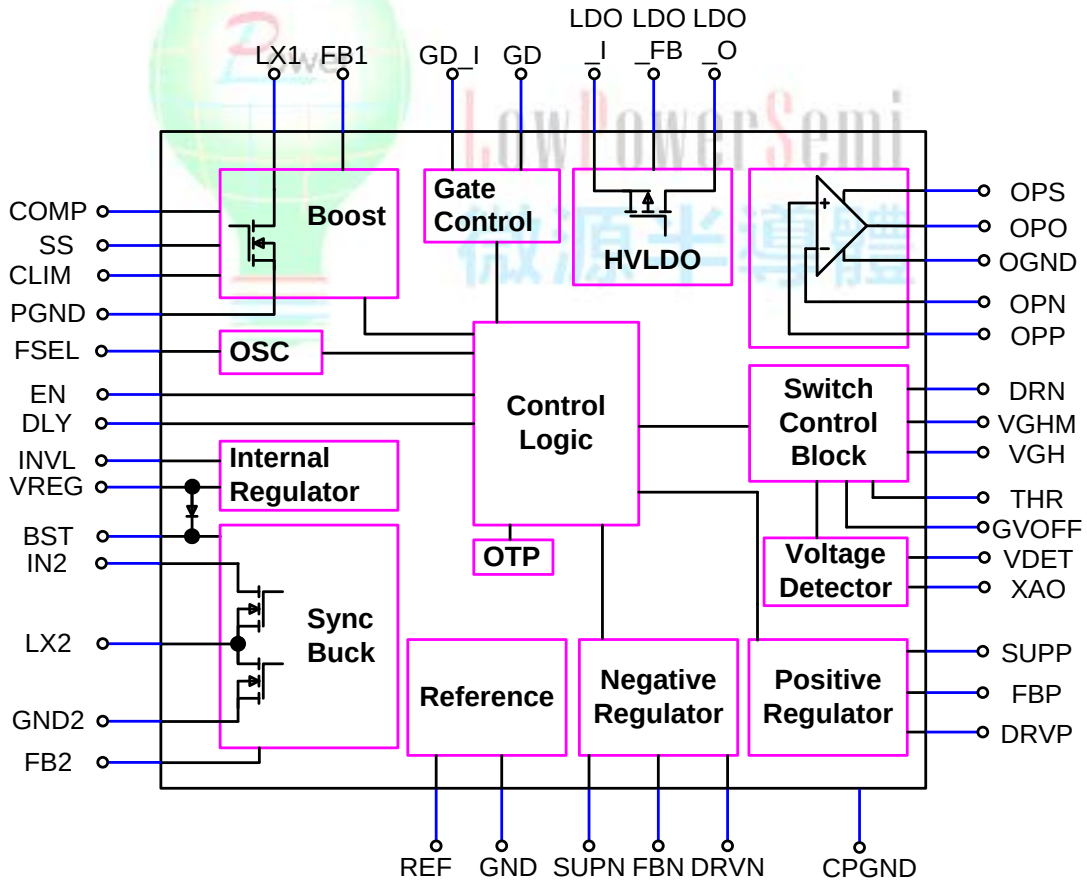
Typical Application Circuit



Pin Configuration



Function Block Diagram



Functional Pin Description

Pin Num	Pin Name	Description
1	LDO_I	Linear Regulator Power Source. Bypass LDO_I to GND a capacitor.
2	OPS	OPA Power Source. Bypass OPS to OGND a capacitor.
3	OGND	Ground for OPA. Connect this pin to ground.
4	OPP	OPA Non-Inverting Input.
5	OPN	OPA Inverting Input.
6	OPO	OPA Output.
7	XAO	Reset Function Output. Open drain.
8	GVOFF	High-Voltage Switch Control Input. When GVOFF is high the high voltage switch between VGH and VGHM is on and the high-voltage switch between VGHM and DRN is off. When GVOFF is low, the switch between VGH and VGHM is off and the switch between VGHM and DRN is on.
9	EN	Enable Input. Pulling EN high, turn on boost regulator and VGH charge pump.
10	FB2	Buck Regulator Feedback Input. Connect to an external resistive voltage divider from the output to FB2 to set the output voltage.
11	OUT	Buck Regulator Output Sense. Connect OUT pin to the Buck regulator output.
12	NC	No Connection.
13, 14	LX2	Buck Regulator Switching Node. LX2 is the source of the internal NMOS. Connect the inductor and schottky diode to LX2.
15	BST	Buck Regulator Bootstrap Pin. BST is the supply for the high-side MOSFET gate driver. Connect a 0.1μF ceramic capacitor from BST to LX2.
16, 17	IN2	Buck Regulator Supply Input. Bypass IN2 to PGND a capacitor.
18	GND	Analog GND.
19	VDET	Voltage Detector Input. Connect to an external resistive voltage divider from the VIN to AGND.
20	INVL	Internal Regulator and Startup Circuitry Supply Input. The input voltage range of INVL is between +8V to +14V. Connect a ceramic capacitor between INVL and GND.
21	VREG	Internal Regulator Output. Bypass VREG to GND a capacitor.
22	FSEL	Frequency Select Pin. Set FSEL to high for 750kHz operation. Set this pin to low for 500kHz operation.
23	CLIM	Boost Regulator OCP level setting by an external resistor to GND.
24	SS	Soft-Start Control Pin. Connect a soft-start capacitor to this pin. If external capacitor is less than 220pF, soft-start is controlled internally and soft-start time is 10ms.
25, 26	LX1	Boost Regulator Switching Node. Connect the inductor and the schottky diode to LX1.
27, 28	PGND	Power Ground.
29	GD_I	Boost Regulator Output Sense Pin. Connected this pin to the boost regulator output.
30	GD	External PMOS Gate Drive Pin. GD pin will be pulled low when EN is high.
31	FB1	Boost Regulator Feedback Input. Connect to an external resistive voltage divider from the output to FB1 to set the output voltage.
32	COMP	Boost Regulator Error Amplifier Compensation Pin.
33	THR	VGHM Falling Regulation Adjustment Input. Connect to an external resistive voltage divider from the supply to GND to adjust the VGHM falling regulation set point.
34	SUPP	VGH Charge-Pump Regulator Power Source. Bypass SUPP to CPGND a ceramic capacitor.
35	CPGND	Power Ground for Charge Pump.
36	DRVP	VGH Charge-Pump Regulator Driver Output.
37	DLY	GPM Delay Input. Connect a capacitor between DLY and GND.
38	FBP	VGH Charge-Pump Regulator Feedback Input. Connect to an external resistive voltage divider from the VGH to GND to set the output voltage.
39	VGH	GPM Input.
40	VGHM	GPM Output.

41	DRN	GPM Discharge Pin.
42	SUPN	VGL Charge-Pump Regulator Power Source. Bypass SUPN to GND with a ceramic capacitor.
43	DRVN	VGL Charge-Pump Regulator Driver Output.
44	GND	Analog Ground.
45	FBN	VGL Charge-Pump Regulator Feedback Input. Connect to an external resistive voltage divider from the VGL to REF to set the output voltage.
46	REF	Reference Output. Connect a ceramic capacitor between REF and GND.
47	LDO_FB	Linear Regulator Feedback Input. Connect to an external resistive voltage divider from the LDO_O to GND to set the output voltage.
48	LDO_O	Linear Regulator Output. Bypass LDO_O to GND with a capacitor.
49(EP)	GND	Exposed Pad. Connect EP to GND.

LowPowerSemi 微源半導體

Absolute Maximum Ratings Note 1

- IN2, INVL SUPN, FSEL to GND ---------- -0.3V to +16.5V
- SUPP, GD_I, OPS, LDO_I to GND ---------- -0.3V to +20V
- DRVP to CPGND ---------- −0.3V to (V_{SUPP} + 0.3V)
- DRVN to GND ---------- −0.3V to (V_{SUPN} + 0.3V)
- OPO, OPP, OPN to OGND ---------- −0.3V to (V_{OPS} + 0.3V)
- LDO_O to GND ---------- −0.3V to (V_{LDO} + 0.3V)
- FB1, FB2, FBP, FBN, GVOFF, DLY, LDO_FB, THR, EN to GND ---------- −0.3V to 6.5V
- OUT, REF, COMP, SS,XAO, VDET, CLIM to GND ---------- −0.3V to 6.5V
- PGND, OGND, CPGND to GND ---------- ±0.3V
- BST to PGND ---------- −0.3V to 20V
- LX1 to PGND ---------- −0.3V to 20V
- LX2 to PGND ---------- −0.3V to (IN2+0.3V)
- VGHM, VGH, DRN to GND ---------- −0.3V to 40V
- VGH to VGHM ---------- −0.3V to 40V
- VGH, VGHM to DRN ---------- −0.3V to 40V
- Operating Junction Temperature Range (T_J) ---------- -40℃ to 150℃
- Operation Ambient Temperature Range---------- -40°C to +85°C
- Storage Temperature Range ---------- -65°C to +150°C
- Maximum Soldering Temperature (at leads, 10sec) ---------- +260°C
- Maximum Junction Temperature ---------- 150°C

Note 1. Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Thermal Information

- Thermal Resistance

TQFN-48 7x7, θJA ---------- 35°C/W

TQFN-48 7x7, θJC ---------- 6°C/W

ESD Susceptibility

- HBM(Human Body Mode) Note 2 ---------- 2KV
- MM(Machine Mode) Note 3 ---------- 200V

Note 2. The Human body model (HBM) is a 100pF capacitor discharged through a 1.5kΩ resistor into each pin. The testing is done according JEDEC.

Note 3. Machine Model (MM) is a 200pF capacitor discharged through a 500nH inductor with no series resistor into each pin. The testing is done according JEDEC.

Electrical Characteristics

(VIN = 12V, TA = 25°C unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
General						
IN2, INVL Input Voltage Range			8	12	14	V
Quiescent Current into INVL	I_{Q-IN}	LX not switching		0.02	2	mA
Under-Voltage Lockout Threshold	V_{UVLO}	V_{IN} Rising	5.4	6	6.6	V
		Falling Hystersis	0.1	-	0.5	V
Switching Frequency	F_{SW}	FSEL = GND		500		kHz
		FSEL = VIN		750		
Maximum Duty-Cycle	D_{MAX}			80		%
Thermal Shutdown Threshold	T_{SD}			160		°C
Boost Regulator						
Output Voltage Range	V_{AVDD}		VIN		18	V
FB1 Reference Voltage	V_{FB1}		1.2375	1.25	1.2625	V
FB Line Regulation		V_{IN}= 10.8V to 13.2V		0.15	0.2	%/V
Transconductance	Gm1	ΔI = ±2.5μA at V_{COMP} = 1V		120		μA/V
Voltage Gain	AV	FB to COMP		1250		V/V
Current Limit	I_{LIM1}		3	4		A
On-Resistance	$R_{DS(ON)}$			100	250	mΩ
Current-Sense Transresistance	R_{CS}			0.25		V/A
Soft-start Charge Current	I_{SS}			5		μA
Internal Soft-Start	T_{SS1}	C8 < 220pF		10		ms
Reference						
REF Output Voltage	V_{REF}	No external load,		1.25		V
REF Load Regulation		0 < I_{REF} < 50μA		10		mV
REF Sink Current		REF in Regulation		10		μA
Buck Regulator						
FB2 Reference Voltage	V_{FB2}		1.2375	1.25	1.2625	V
FB2 Reference Voltage	V_{FB2}			0.2		V
DC Line Regulation		10.8V < V_{IN} < 13.2V		0.1		%/V
LX2-IN2 Switch MOS	$R_{DS(ON)}$			150	300	mΩ
LX2-PGND Switch MOS	$R_{DS(ON)}$			20		Ω
Current Limit	I_{LIM2}		2.5	3.2		A
Error Amplifier Transconductance	Gm2			100		μA/V
Error Amplifier Voltage Gain	AV			700		V/V

Current-Sense Transresistance	R_{CS}			0.3		V/A
Soft-Start Ramp Time	T_{SS2}			3		ms
FB2 UVP Trip Level	V_{UVP2}	Falling edge		1		V
Duration to Trigger UVP Condition	T_{UVP2}			50		ms
FB2 SCP Trip Level	V_{SCP2}	Falling edge		0.5		V
Positive Charge-Pump Regulator						
FBP Reference Voltage	V_{FBP}		1.225	1.25	1.275	V
FBP Line Regulation Error		V_{IN} = 10.8V to 13.2V			6	mV/V
DRVP P-MOSFET On-Resistance	$R_{DS(ON)}$			2		Ω
DRVP N-MOSFET On-Resistance	$R_{DS(ON)}$			1		Ω
Soft-Start Ramp Time	T_{SSP}			3		ms
FBP UVP Trip Level	V_{UVPP}	Falling edge		1		V
Duration to Trigger Fault Condition	T_{UVPP}			50		ms
FBP Short-Circuit Level	V_{SCPP}	Falling edge		0.5		V
Negative Charge-Pump Regulator						
FBN Regulation Voltage	V_{FBN}		0.21	0.25	0.29	V
Final FBN Regulation Voltage		V_{REF} - V_{FBN}	0.98	1	1.02	V
FBN Line Regulation Error		VIN = 10.8V to 13.2V			6	mV/V
DRVN P-MOSFET On-Resistance	$R_{DS(ON)}$			6		Ω
DRVN N-MOSFET On-Resistance	$R_{DS(ON)}$			2		Ω
Soft-Start Ramp Time	T_{SSN}			3		ms
FBN UVP Trip Level	V_{UVPN}	V_{REF} - V_{FBN}		0.4		V
Duration to Trigger Fault Condition	T_{UVPN}			50		ms
FBN Short Circuit Protection Level	V_{SCPN}	V_{REF} - V_{FBN}		0.8		V
Sequence Control						
EN Input Low Voltage	V_{ENL}				0.6	V
EN Input High Voltage	V_{ENH}		1.5		5.5	V
DLY Capacitor Charge Current	I_{DLY}			8		μA
VDL Turn-On Threshold				1.25		V
GD Output Sink Current		EN = High, VGD_I = VIN		10		μA
GD On-Voltage		EN = High, VGD_I = VIN		VIN−5		V
Gate Pulse Modulator (GPM)						
GVOFF Input Low Voltage					0.6	V
GVOFF Input High Voltage			1.5		5.5	V
GVOFF Input Leakage Current			−1		1	μA
GVOFF-to-VGHM Rising Propagation Delay		1kΩ from DRN to GND, 1.5nF from VGHM to GND		100		ns
GVOFF-to-VGHM Falling Propagation Delay		1kΩ from DRN to GND, 1.5nF from VGHM to GND		250		ns
VGH Input Current		V_{DLY} = GVOFF = 3V		50		uA

		V_{DLY} = 3V, GVOFF = 0		40		
DRN Input Current		DRN = 8V, V_{DLY} = 3V, VGHM > DRN, GVOFF = 0		0	1	μA
VGH Switch On-Resistance		V_{DLY} = GVOFF = 3V		5	10	Ω
DRN Switch On-Resistance		V_{DLY} = 3V, GVOFF = 0, VGHM= 28V, V_{THR} = 1.4V		20	50	Ω
VGHM Stop Level				10 x V_{THR}		V
Voltage Detector (XAO)						
Detecting Voltage Adjustment	V_{DET}	Falling edge		1.25		V
Detecting Voltage Accuracy			-1		1	%
VCOMP OPAmp						
Supply Voltage Range	V_{IN-OP}		4.5		18	V
Supply Current	I_{Q-OP}			3		mA
Input Offset Voltage	V_{OS}	V_{COM} =AVDD/2			20	mV
Input Bias Current	I_{Bias}			1	100	nA
Output Voltage Swing High	V_{OH}	I_{Load} = 10mA		V_{SUP} -100		mV
Output Voltage Swing Low	V_{OL}	I_{Load} = -10mA		100		mV
Short-Circuit Current		To AVDD/2 Source or Sink for 1ms		300		mA
-3dB Bandwidth	F_{3dB}	R_L = 10kΩ, C_L= 10pF		20		MHz
Gain Bandwidth Product	GBW	R_L = 10kΩ, C_L = 10pF		8		MHz
Slew Rate				45		V/μs
HVLDO						
Quiescent Current	I_Q			40		μA
LDO Feedback Reference Voltage	V_{REF_FB}			1.25		V
Feedback Voltage Tolerance			-0.5		0.5	%
Output Current Limit		V_{REF_I}= 15V, V_{REF_O}= 14V, R_{OUT}= 50Ω	60			mA
Dropout Voltage	V_{Drop}	I_{Load} = 60mA		0.5		V
Power Supply Rejection Rate	PSRR	V_{REF_I} = V_{REF_O} + 1V, I_{OUT}= 10mA		60		dB
Switching-Frequency Selection						
FSEL Input Levels		FSEL = High	1.5			V
		FSEL = Low			0.6	
FSEL Pull High Current				1		μA

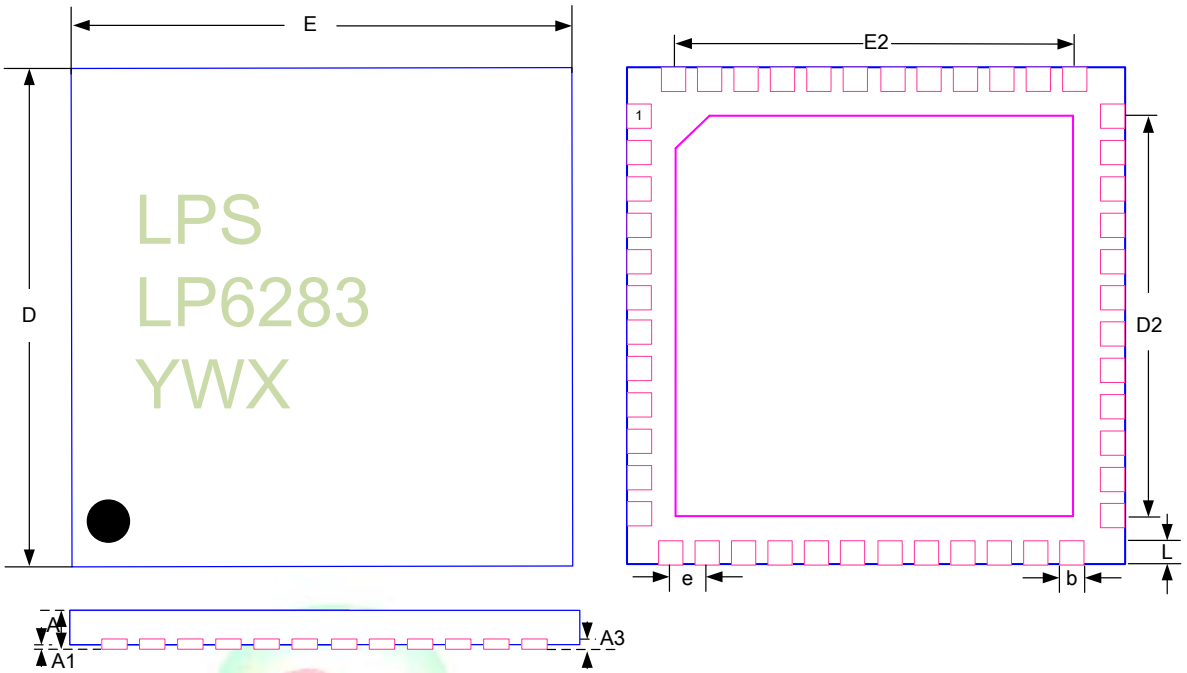
Note 1. Stresses listed as the above "Absolute Maximum Ratings" may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.

Note 2. The device is not guaranteed to function outside its operating conditions.

Note 3. θ_{JA} is measured in the natural convection at T_A = 25°C on a high effective thermal conductivity four layers test board. The case position of θ_{JC} is on the exposed pad of the package.

Outline Information

TQFN-48 (7mm X 7mm) pitch 0.5mm (Unit: mm)



SYMBOLS UNIT	DIMENSION IN MILLIMETER	
	MIN	MAX
A	0.700	0.800
A1	0.000	0.050
A3	0.175	0.250
b	0.200	0.300
D	6.950	7.050
D2	5.050	5.250
E	6.950	7.050
E2	5.050	5.250
L	0.350	0.450
e	0.5	