



128Kx64 3.3V SRAM MODULE

ADVANCED*

FEATURES

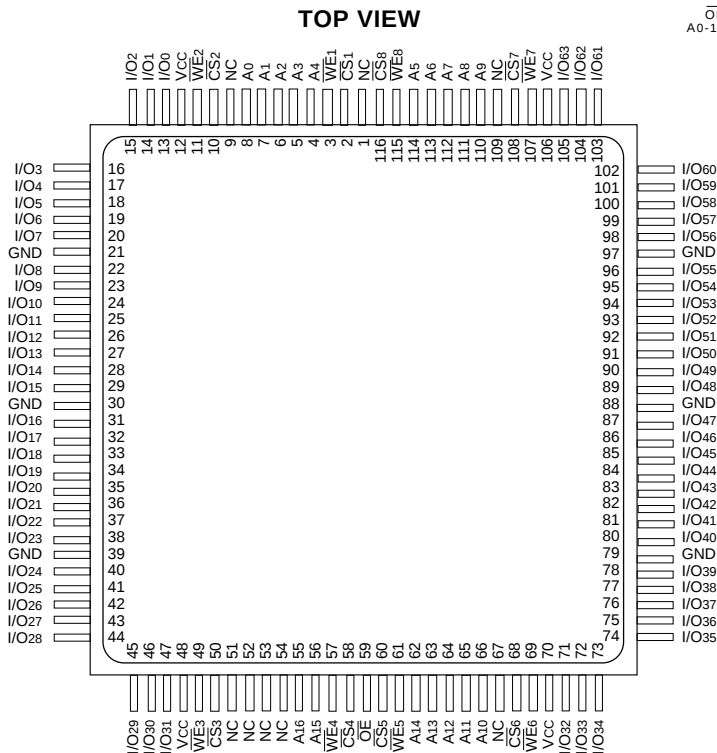
- Access Times of 15, 17, 20, 25ns
- Packaging
 - 116 lead, 40mm square, Hermetic CQFP (Package 504)
- Organized as 128Kx64, User Configurable as 256Kx32, 512Kx16 or 1Mx8.
- Commercial, Industrial and Military Temperature Ranges
- 3 Volt Power Supply
- Low Power CMOS

- 2V Data Retention Devices Available (Low Power Version)
- TTL Compatible Inputs and Outputs
- Built in Decoupling Caps and Multiple Ground Pins for Low Noise Operation
- Weight
WF128K64V-XG4WX - 20 grams typical

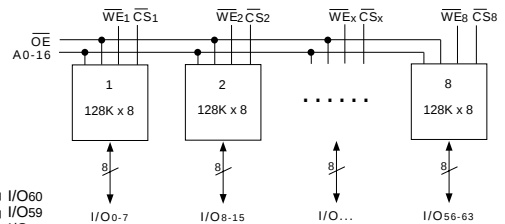
* This data sheet describes a product that may or may not be under development and is subject to change or cancellation without notice.

Note: Programming information available upon request.

FIG. 1 PIN CONFIGURATION FOR WF128K64V-XG4WX



BLOCK DIAGRAM



PIN DESCRIPTION

I/O0-63	Data Inputs/Outputs
A0-16	Address Inputs
WE1-8	Write Enables
CS1-8	Chip Selects
OE	Output Enable
Vcc	Power Supply
GND	Ground
NC	Not Connected



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Unit
Operating Temperature	T _A	-55	+125	°C
Storage Temperature	T _{STG}	-65	+150	°C
Signal Voltage Relative to GND	V _G	-0.5	4.6	V
Junction Temperature	T _J		150	°C
Supply Voltage	V _{CC}	-0.5	4.6	V

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Max	Unit
Supply Voltage	V _{CC}	3.0	3.6	V
Input High Voltage	V _{IH}	2.2	V _{CC} + 0.3	V
Input Low Voltage	V _{IL}	-0.3	+0.8	V
Operating Temp. (Mil.)	T _A	-55	+125	°C

TRUTH TABLE

CS	OE	WE	Mode	Data I/O	Power
H	X	X	Standby	High Z	Standby
L	L	H	Read	Data Out	Active
L	X	L	Write	Data In	Active
L	H	H	Out Disable	High Z	Active

CAPACITANCE

(T_A = +25°C)

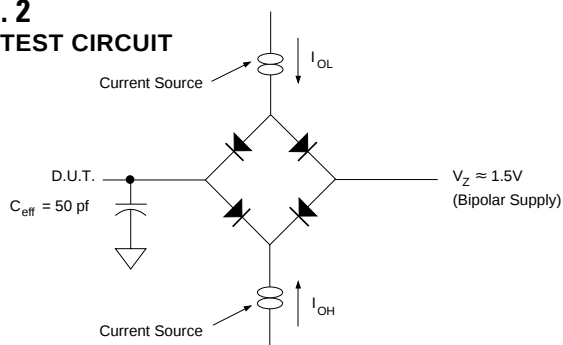
Parameter	Symbol	Conditions	Max	Unit
OE capacitance	C _{OE}	V _{IN} = 0 V, f = 1.0 MHz	100	pF
WE capacitance	C _{WE}	V _{IN} = 0 V, f = 1.0 MHz	20	pF
CS capacitance	C _{CS}	V _{IN} = 0 V, f = 1.0 MHz	20	pF
Data I/O capacitance	C _{I/O}	V _{I/O} = 0 V, f = 1.0 MHz	20	pF
Address input capacitance	C _{AD}	V _{IN} = 0 V, f = 1.0 MHz	100	pF

This parameter is guaranteed by design but not tested.

DC CHARACTERISTICS

(V_{CC} = 3.3V ± 0.3V, T_A = -55°C to +125°C)

Parameter	Sym	Conditions			Units
			Min	Max	
Input Leakage Current	I _{LI}	V _{IN} = GND to V _{CC}		10	μA
Output Leakage Current	I _{LO}	$\overline{CS}$ = V _{IH} , $\overline{OE}$ = V _{IH} , V _{OUT} = GND to V _{CC}		10	μA
Operating Supply Current	I _{CC}	$\overline{CS}$ = V _{IL} , $\overline{OE}$ = V _{IH} , f = 5MHz, V _{CC} = 3.6		1	A
Standby Current	I _{SB}	$\overline{CS}$ = V _{IH} , $\overline{OE}$ = V _{IH} , f = 5MHz, V _{CC} = 3.6		64	mA
Output Low Voltage	V _{OL}	I _{OL} = 8mA		0.4	V
Output High Voltage	V _{OH}	I _{OH} = -4.0mA	2.4		V

NOTE: DC test conditions: V_{IH} = V_{CC} - 0.3V, V_{IL} = 0.3V**FIG. 2**
AC TEST CIRCUIT

AC TEST CONDITIONS

Parameter	Typ	Unit
Input Pulse Levels	V _{IL} = 0, V _{IH} = 2.5	V
Input Rise and Fall	5	ns
Input and Output Reference Level	1.5	V
Output Timing Reference Level	1.5	V

NOTES:

V_Z is programmable from -2V to +7V.
I_{OL} & I_{OH} programmable from 0 to 16mA.
Tester Impedance Z₀ = 75 Ω.
V_Z is typically the midpoint of V_{OH} and V_{OL}.
I_{OL} & I_{OH} are adjusted to simulate a typical resistive load circuit.
ATE tester includes jig capacitance.

**AC CHARACTERISTICS**(V_{CC} = 3.3V ± 0.3V, T_A = -55°C To +125°C)

Parameter Read Cycle	Symbol	-15		-17		-20		-25		Units
		Min	Max	Min	Max	Min	Max			
Read Cycle Time	t _{RC}	15		17		20		25		ns
Address Access Time	t _{AA}		15		17		20		25	ns
Output Hold from Address Change	t _{OH}	0		0		0		0		ns
Chip Select Access Time	t _{ACS}		15		17		20		25	ns
Output Enable to Output Valid	t _{OE}		10		10		12		15	ns
Chip Select to Output in Low Z	t _{CLZ} ¹	3		3		3		3		ns
Output Enable to Output in Low Z	t _{OLZ} ¹	0		0		0		0		ns
Chip Disable to Output in High Z	t _{CHZ} ¹		10		10		12		12	ns
Output Disable to Output in High Z	t _{OHZ} ¹		10		10		12		12	ns

1. This parameter is guaranteed by design but not tested.

AC CHARACTERISTICS(V_{CC} = 3.3V ± 0.3V, T_A = -55°C To +125°C)

Parameter Write Cycle	Symbol	-15		-17		-20		-25		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
Write Cycle Time	t _{WC}	15		17		20		25		ns
Chip Select to End of Write	t _{CW}	14		14		15		20		ns
Address Valid to End of Write	t _{AW}	14		14		15		20		ns
Data Valid to End of Write	t _{DW}	10		10		12		15		ns
Write Pulse Width	t _{WP}	14		14		15		20		ns
Address Setup Time	t _{AS}	0		0		0		0		ns
Address Hold Time	t _{AH}	0		0		0		0		ns
Output Active from End of Write	t _{OW} ¹	3		3		3		3		ns
Write Enable to Output in High Z	t _{WHZ} ¹		10		10		12		15	ns
Data Hold Time	t _{DH}	0		0		0		0		ns

1. This parameter is guaranteed by design but not tested.



FIG. 3
TIMING WAVEFORM - READ CYCLE

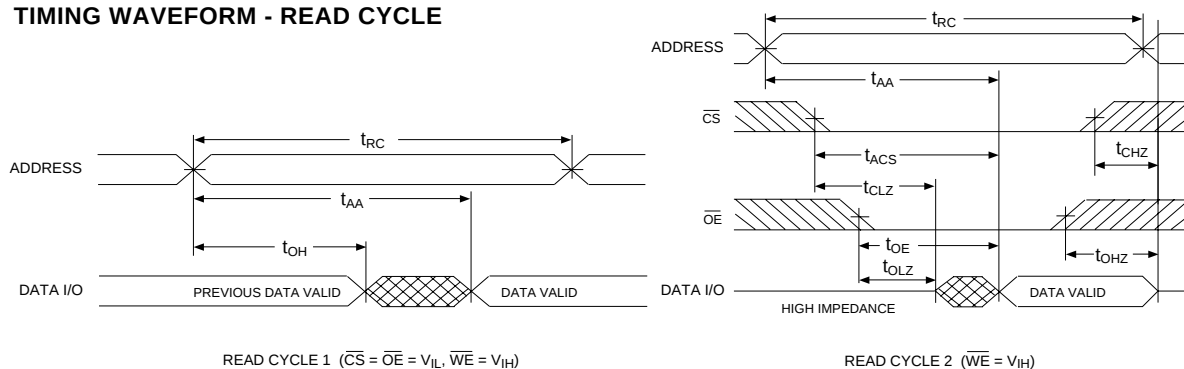


FIG. 4
WRITE CYCLE - $\overline{WE}$ CONTROLLED

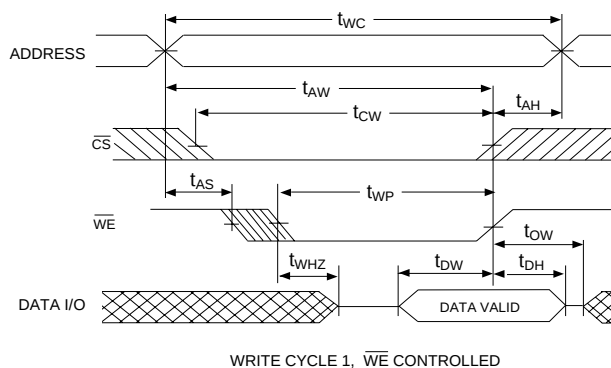
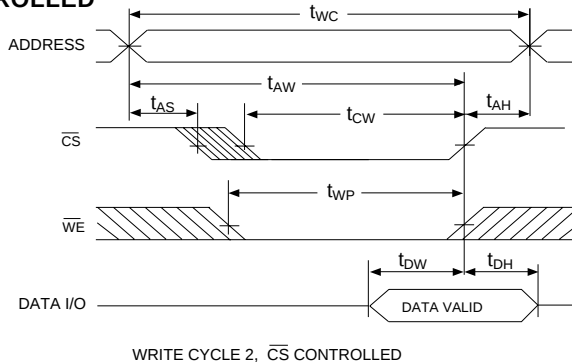
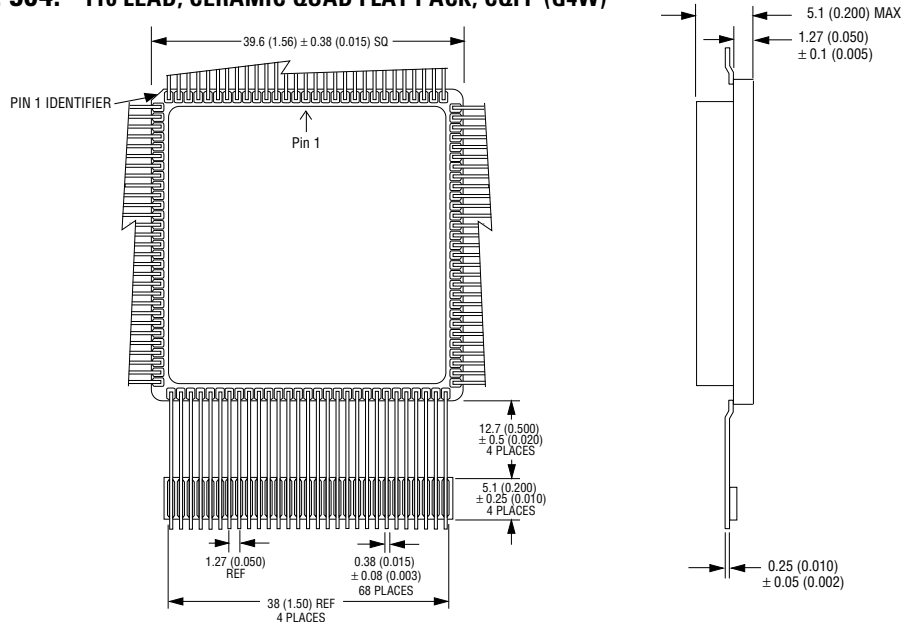


FIG. 5
WRITE CYCLE - $\overline{CS}$ CONTROLLED





PACKAGE 504: 116 LEAD, CERAMIC QUAD FLAT PACK, CQFP (G4W)



ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

ORDERING INFORMATION

W S 128K64 V - XXX G4W X

DEVICE GRADE:

M = Military Screened -55°C to +125°C
I = Industrial -40°C to +85°C
C = Commercial 0°C to +70°C

PACKAGE TYPE:

G4W = 116 Lead 40mm Ceramic Quad Flat Pack, CQFP (Package 504)

ACCESS TIME (ns)

Low Voltage Supply 3.3V $\pm$ 10%

ORGANIZATION, 128K x 64

User configurable as 256K x 32, 512K x 16 and 1M x 8

SRAM

WHITE MICROELECTRONICS