SONY

CXR702F080

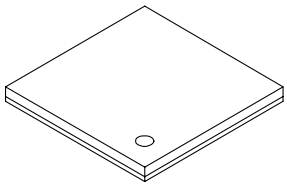
CMOS 32-bit Single Chip Microcomputer

Description

The CXR702F080 is a CMOS 32-bit microcomputer integrating on a single chip an A/D converter, serial interface, timer, bus interface unit, DMA controller, memory stick interface, and as well as basic configurations like a 32-bit RISC CPU, ROM, RAM, and I/O port.

This also provides the idle/sleep/stop functions that enable lower power consumption.

176 pin LFLGA (Plastic)



Features

- CPU — SR11 series 32-bit RISC CPU core
- Minimum instruction cycle — 54.3ns (f_{SRC}: 18.432MHz)
  30.5µs (f_{TEX}: 32.768kHz)
- Incorporated FLASH EEPROM — 256K bytes
- Incorporated RAM — 16K bytes
- Peripheral functions
  - — Bus interface unit
  - — DMA controller — 4 channels
  - — A/D converter — 8-bit 4-analog input, successive approximation system
  - — Serial interface — Clock synchronization, 2 channels
    Clock synchronization, 1 channel (Incorporated 64-byte buffer RAM)
    Asynchronization, 2 channels
  - — Timers — 8-bit timer, 8 channels
    16-bit capture timer, 3 channels
    8-bit time-base timer
    Clock prescaler
    16-bit watchdog timer
  - — Memory stick interface
  - — Beep output circuit
  - — External interruption — 11 channels (polarity selection and both edge detection possible)
- Standby mode — Idle/sleep/stop
- Package — 176-pin plastic LFLGA

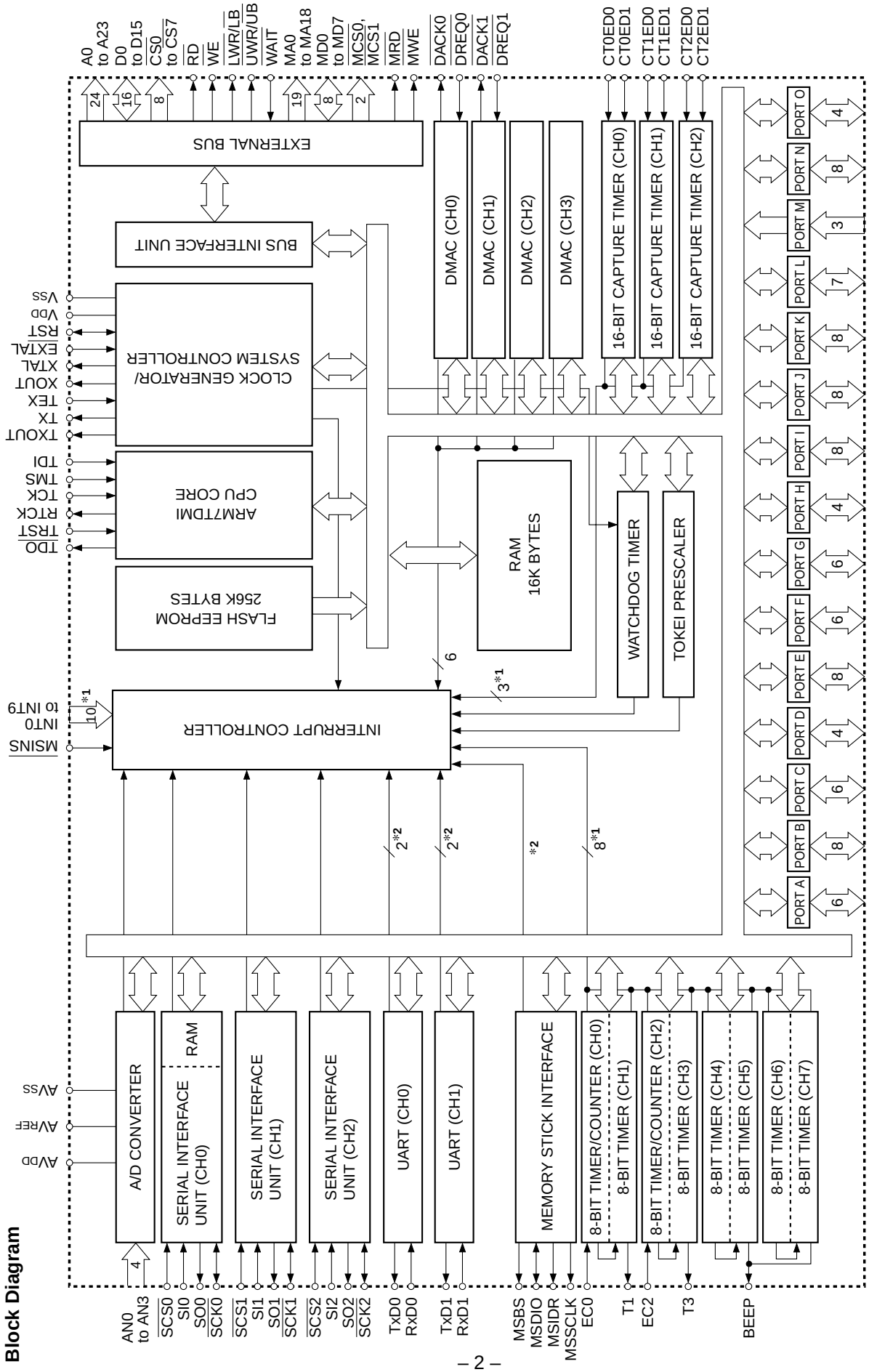
Structure

Silicon gate CMOS IC

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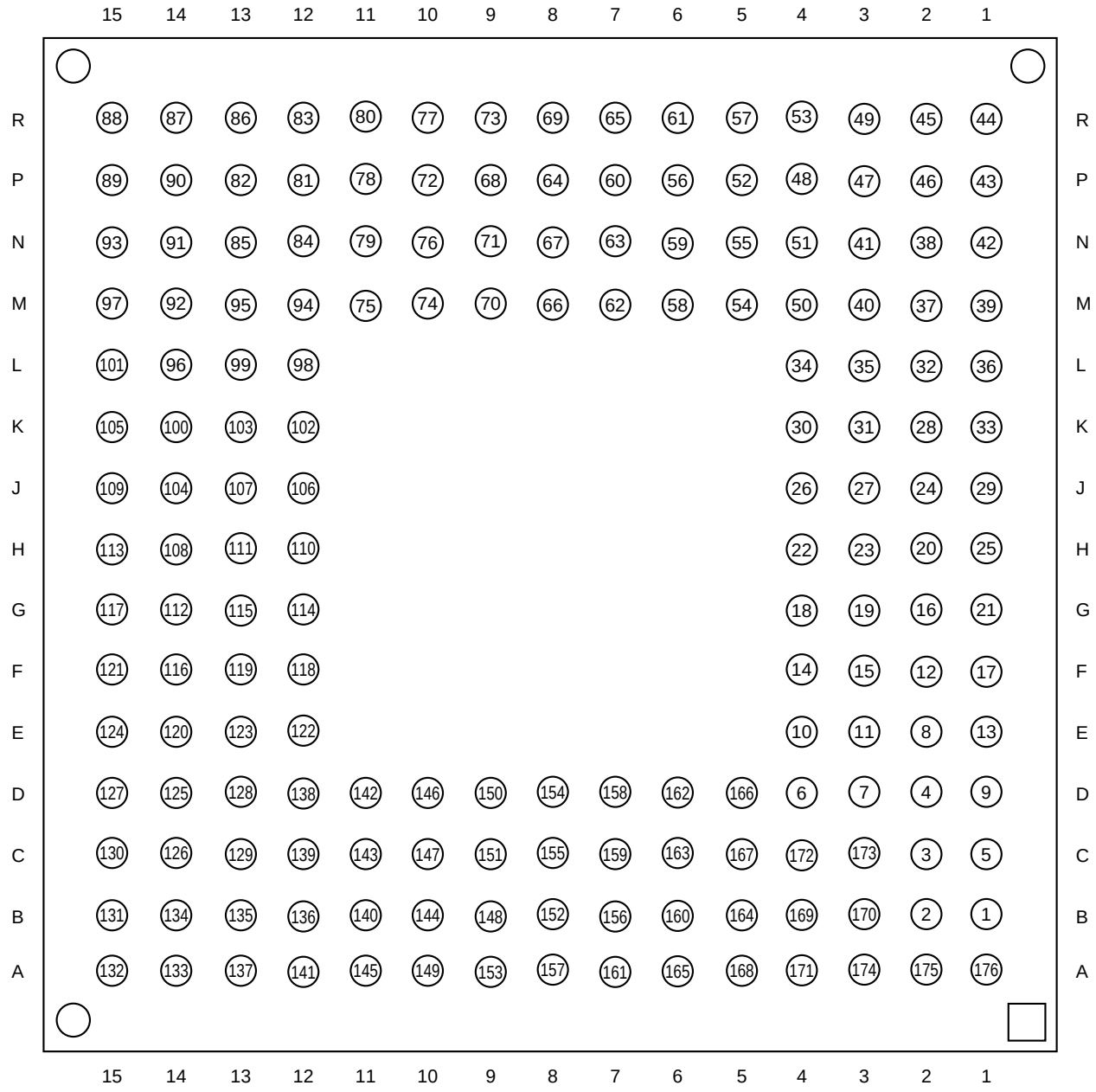
Block Diagram



*1 The number of causes of interrupts generated from the module is as shown. But the number of causes input to the interrupt controller differs from the shown becauses of OR.
*2 A part of the interrupt signals generated from UART, MEMORY STICK INTERFACE is input to the interrupt controller via DMA depending on applications.

Pin Assignment (Top View) 176-pin LFLGA package

• Pin Assignment



• Pin Assignment Table

Pin No.	Pin position	Symbol	Pin No.	Pin position	Symbol	Pin No.	Pin position	Symbol
1	B1	PB3	38	N2	PG2/CT1ED0	75	M11	PK7/D15
2	B2	PB4	39	M1	PG3/CT1ED1	76	N10	V_{DD}
3	C2	PB5	40	M3	PG4/CT2ED0	77	R10	TEX
4	D2	PB6	41	N3	PG5/CT2ED1	78	P11	TX
5	C1	PB7	42	N1	PH0/TxD0	79	N11	V_{SS}
6	D4	V_{DD}	43	P1	PH1/RxD0	80	R11	$\overline{CS0}$
7	D3	V_{SS}	44	R1	PH2/TxD1	81	P12	$\overline{CS1}$
8	E2	PC0	45	R2	PH3/RxD1	82	P13	$\overline{RD}$
9	D1	PC1	46	P2	V_{DD}	83	R12	$\overline{LWR}/\overline{LB}$
10	E4	PC2	47	P3	V_{SS}	84	N12	$\overline{UWR}/\overline{UB}$
11	E3	PC3	48	P4	PI0/MD0	85	N13	$\overline{MRD}$
12	F2	PC4	49	R3	PI1/MD1	86	R13	$\overline{MWE}/\overline{WE}$
13	E1	PC5	50	M4	PI2/MD2	87	R14	$\overline{MCS0}$
14	F4	PD0	51	N4	PI3/MD3	88	R15	V_{DD}
15	F3	PD1	52	P5	PI4/MD4	89	P15	V_{SS}
16	G2	PD2	53	R4	PI5/MD5	90	P14	MA0
17	F1	PD3	54	M5	PI6/MD6	91	N14	MA1/A9
18	G4	V_{DD}	55	N5	PI7/MD7	92	M14	MA2/A10
19	G3	V_{SS}	56	P6	V_{DD}	93	N15	MA3/A11
20	H2	PE0/INT0	57	R5	V_{SS}	94	M12	MA4/A12
21	G1	PE1/INT1	58	M6	PJ0/D0	95	M13	MA5/A13
22	H4	PE2/INT2	59	N6	PJ1/D1	96	L14	MA6/A14
23	H3	PE3/INT3	60	P7	PJ2/D2	97	M15	MA7/A15
24	J2	PE4/INT4	61	R6	PJ3/D3	98	L12	MA8/A16
25	H1	PE5/INT5	62	M7	PJ4/D4	99	L13	PL0/MA9/A17
26	J4	PE6/INT6	63	N7	PJ5/D5	100	K14	PL1/MA10/A18
27	J3	PE7/INT7	64	P8	PJ6/D6	101	L15	PL2/MA11/A19
28	K2	PF0/EC0	65	R7	PJ7/D7	102	K12	PL3/MA12/A20
29	J1	PF1/T1	66	M8	V_{DD}	103	K13	PL4/MA13/A21
30	K4	PF2/EC2	67	N8	V_{SS}	104	J14	PL5/MA14/A22
31	K3	PF3/T3	68	P9	PK0/D8	105	K15	PL6/MA15/A23
32	L2	PF4/BEEP	69	R8	PK1/D9	106	J12	V_{DD}
33	K1	PF5/TXOUT	70	M9	PK2/D10	107	J13	V_{SS}
34	L4	V_{DD}	71	N9	PK3/D11	108	H14	MA16
35	L3	V_{SS}	72	P10	PK4/D12	109	J15	MA17
36	L1	PG0/CT0ED0	73	R9	PK5/D13	110	H12	MA18/A0
37	M2	PG1/CT0ED1	74	M10	PK6/D14	111	H13	A1

Pin No.	Pin position	Symbol	Pin No.	Pin position	Symbol	Pin No.	Pin position	Symbol
112	G14	A2	134	B14	TEST1	156	B7	PN5/SO1
113	H15	A3	135	B13	AN0	157	A8	PN6/SI1
114	G12	A4	136	B12	PM0/AN1	158	D7	PN7/$\overline{\text{SCS1}}$/INT9
115	G13	A5	137	A13	PM1/AN2	159	C7	PO0/$\overline{\text{SCK2}}$
116	F14	A6	138	D12	PM2/AN3	160	B6	PO1/SO2
117	G15	A7	139	C12	AV_{SS}	161	A7	PO2/SI2
118	F12	A8	140	B11	AV_{REF}	162	D6	PO3/$\overline{\text{SCS2}}$
119	F13	V_{DD}	141	A12	AV_{DD}	163	C6	XOUT/CKO
120	E14	EXTAL	142	D11	TDI	164	B5	V_{DD}
121	F15	XTAL	143	C11	TMS	165	A6	V_{SS}
122	E12	V_{SS}	144	B10	$\overline{\text{TRST}}$	166	D5	PWE
123	E13	MSDIO	145	A11	TCK	167	C5	NC
124	E15	MSBS	146	D10	RTCK	168	A5	PA0/$\overline{\text{WAIT}}$
125	D14	MSSCLK	147	C10	TDO	169	B4	PA1/$\overline{\text{CS2}}$
126	C14	MSDIR	148	B9	$\overline{\text{RST}}$	170	B3	PA2/$\overline{\text{CS3}}$
127	D15	$\overline{\text{MSINS}}$	149	A10	V_{DD}	171	A4	PA3/$\overline{\text{CS4}}$
128	D13	$\overline{\text{DACK0}}$	150	D9	V_{SS}	172	C4	PA4/$\overline{\text{CS5}}$
129	C13	$\overline{\text{DACK1}}$	151	C9	PN0/$\overline{\text{SCK0}}$	173	C3	PA5/$\overline{\text{MCS1}}$
130	C15	$\overline{\text{DREQ0}}$	152	B8	PN1/SO0	174	A3	PB0
131	B15	$\overline{\text{DREQ1}}$	153	A9	PN2/SI0	175	A2	PB1
132	A15	TEST2	154	D8	PN3/$\overline{\text{SCS0}}$/INT8	176	A1	PB2
133	A14	TEST0	155	C8	PN4/$\overline{\text{SCK1}}$			

Pin Functions

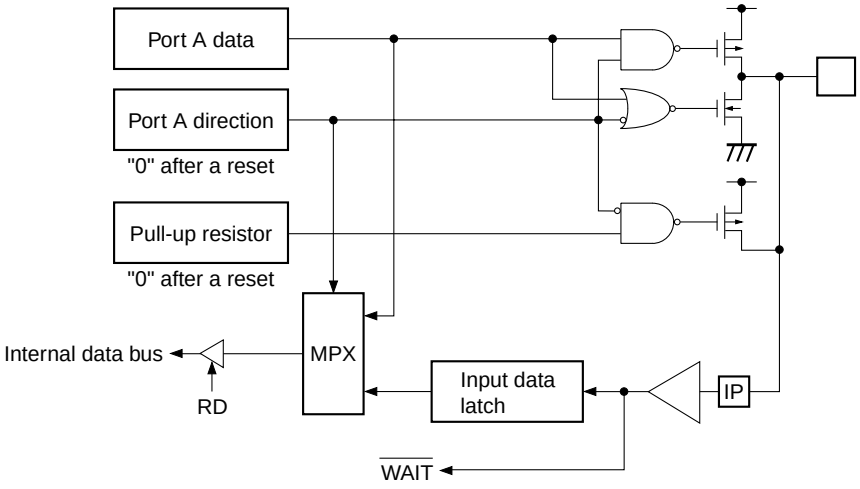
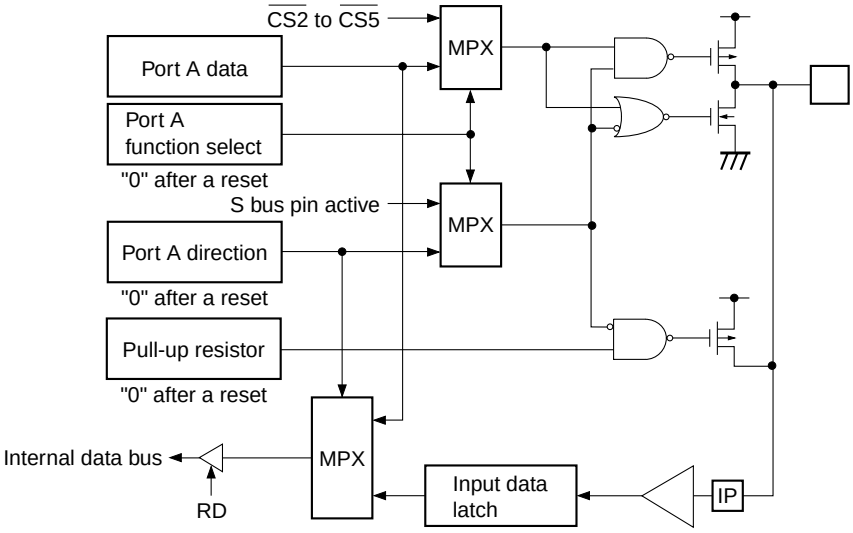
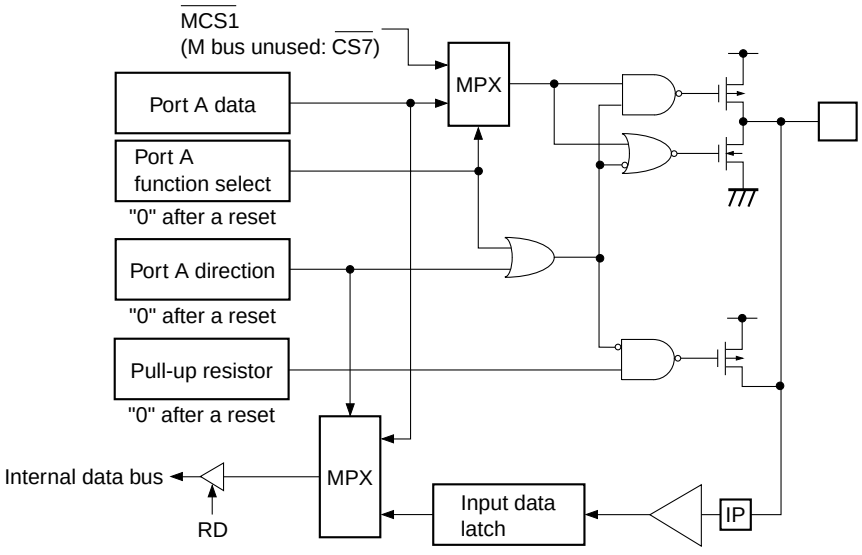
Symbol	I/O	Functions	
PA0/$\overline{WAIT}$	I/O / Input	(Port A) 6-bit I/O port. I/O can be specified in 1-bit units. Pull-up resistor can be incorporated through program in 1-bit units. (6 pins)	Wait input for external bus
PA1/$\overline{CS2}$ to PA4/$\overline{CS5}$	I/O / Output		Chip select output for external S bus (4 pins)
PA5/$\overline{MCS1}$	I/O / Output		Chip select output for external M bus.
PB0 to PB7	I/O	(Port B) 8-bit I/O port. I/O can be specified in 1-bit units. Pull-up resistor can be incorporated through program in 1-bit units. (8 pins)	
PC0 to PC5	I/O	(Port C) 6-bit I/O port. I/O can be specified in 1-bit units. Pull-up resistor can be incorporated through program in 1-bit units. (6 pins)	
PD0, PD1	Output	(Port D) 4-bit open drain port. Lower 2 bits are for output; upper 2 bits are for I/O. (4mA drive) Upper 2 bits can be specified in 1-bit units. (4 pins)	
PD2, PD3	I/O		
PE0/INT0 to PE7/INT7	I/O / Input	(Port E) 8-bit I/O port. I/O can be specified in 1-bit units. Pull-up resistor can be incorporated through program in 1-bit units. (8 pins)	External interruption request input. (8 pins)
PF0/EC0	I/O / Input	(Port F) 6-bit I/O port. I/O can be specified in 1-bit units. Pull-up resistor can be incorporated through program in 1-bit units. (6 pins)	External event input to 8-bit timer (CH0).
PF1/T1	I/O / Output		8-bit timer (CH1) output.
PF2/EC2	I/O / Input		External event input to 8-bit timer (CH2).
PF3/T3	I/O / Output		8-bit timer (CH3) output.
PF4/BEEP	I/O / Output		Beep output.
PF5/TXOUT	I/O / Output		Sub oscillation output.
PG0/CT0ED0 to PG5/ CT2ED1	I/O / Input	(Port G) 6-bit I/O port. I/O can be specified in 1-bit units. Pull-up resistor can be incorporated through program in 1-bit units. (6 pins)	Capture input of 16-bit capture timer. (6 pins)

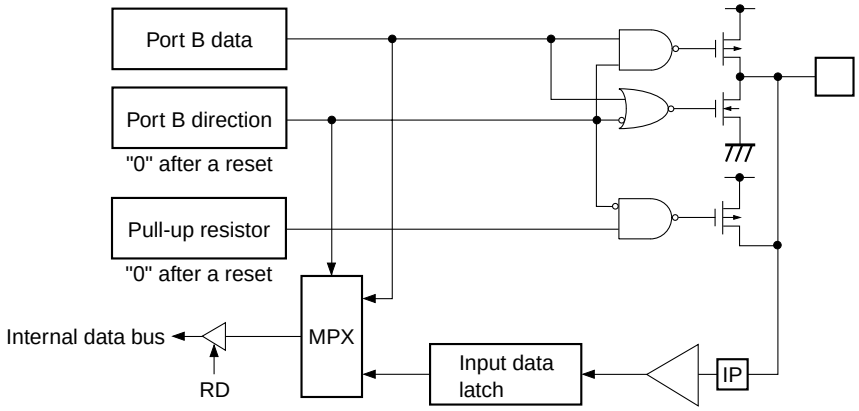
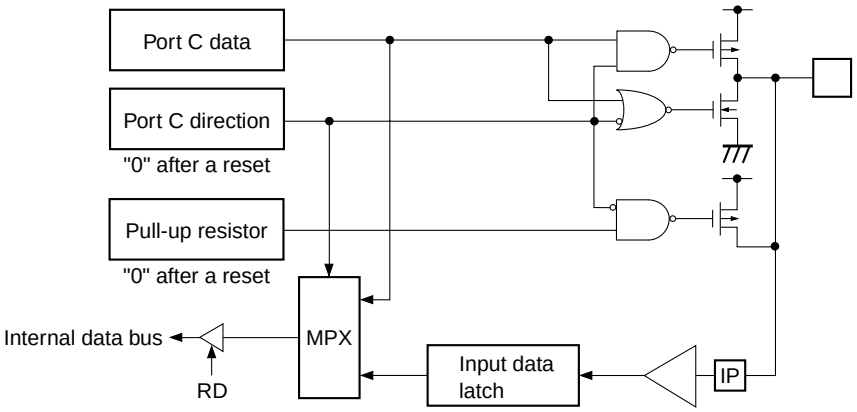
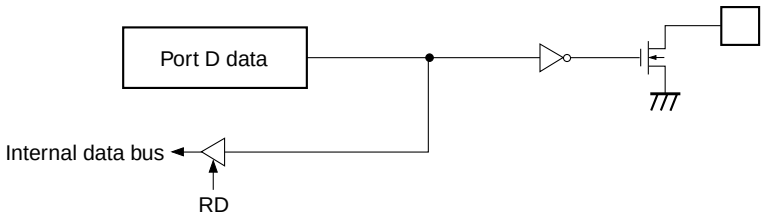
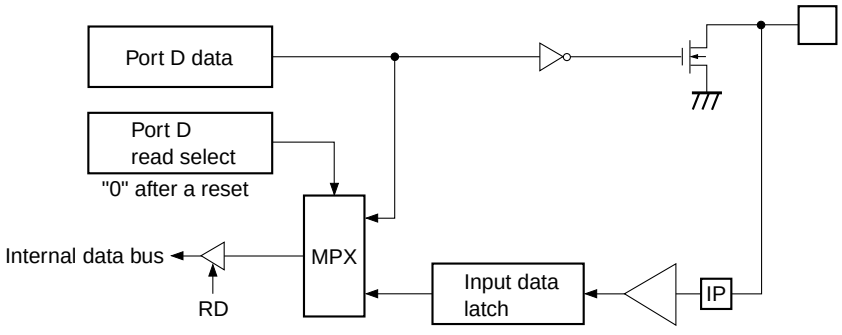
<table>
<tr><th>Symbol</th><th>I/O</th><th colspan="2">Functios</th></tr>
<tr><td>PH0/TxD0</td><td>I/O / Output</td><td rowspan="4">(Port H)
4-bit I/O port.
I/O can be specified in 1-bit units.
Pull-up resistor can be incorporated through program in 1-bit units.
(4 pins)</td><td>UART (CH0) transmit data output.</td></tr>
<tr><td>PH1/RxD0</td><td>I/O / Input</td><td>UART (CH0) receive data input.</td></tr>
<tr><td>PH2/TxD1</td><td>I/O / Output</td><td>UART (CH1) transmit data output.</td></tr>
<tr><td>PH3/RxD1</td><td>I/O / Input</td><td>UART (CH1) receive data input.</td></tr>
<tr><td>PI0/MD0
to PI7/MD7</td><td>I/O / I/O</td><td>(Port I)
8-bit I/O port.
I/O can be specified in 1-bit units.
Pull-up resistor can be incorporated through program in 1-bit units.
(8 pins)</td><td>Data bus for external M bus.
(8 pins)</td></tr>
<tr><td>PJ0/D0
to PJ7/D7</td><td>I/O / I/O</td><td>(Port J)
8-bit I/O port.
I/O can be specified in 1-bit units.
Pull-up resistor can be incorporated through program in 1-bit units.
(8 pins)</td><td rowspan="2">Data bus for external S bus.
(16 pins)</td></tr>
<tr><td>PK0/D8
to PK7/D15</td><td>I/O / I/O</td><td>(Port K)
8-bit I/O port.
I/O can be specified in 1-bit units.
Pull-up resistor can be incorporated through program in 1-bit units.
(8 pins)</td></tr>
<tr><td>A1 to A8</td><td>Output</td><td colspan="2" rowspan="4"></td><td rowspan="4">Address bus output for external S bus.
(24 pins)</td></tr>
<tr><td>MA18/A0</td><td>Output / Output</td></tr>
<tr><td>MA1/A9
to MA8/A16</td><td>Output / Output</td></tr>
<tr><td>PL0/MA9/A17
to PL6/MA15/A23</td><td>I/O / Output / Output</td><td>(Port L)
7-bit I/O port.
I/O can be specified in 1-bit units.
Pull-up resistor can be incorporated through program in 1-bit units.
(7 pins)</td><td>Address bus output for external M bus
(19 pins)</td></tr>
<tr><td>MA0</td><td>Output</td><td colspan="3" rowspan="2"></td></tr>
<tr><td>MA16, MA17</td><td>Output</td></tr>
<tr><td>AN0</td><td>Input</td><td colspan="3" rowspan="2"></td></tr>
<tr><td>PM0/AN1
to PM2/AN3</td><td>Input / Input</td><td>(Port M)
3-bit input port.
(3-pins)</td><td colspan="2">Analog input to A/D converter.
(4 pins)</td></tr>
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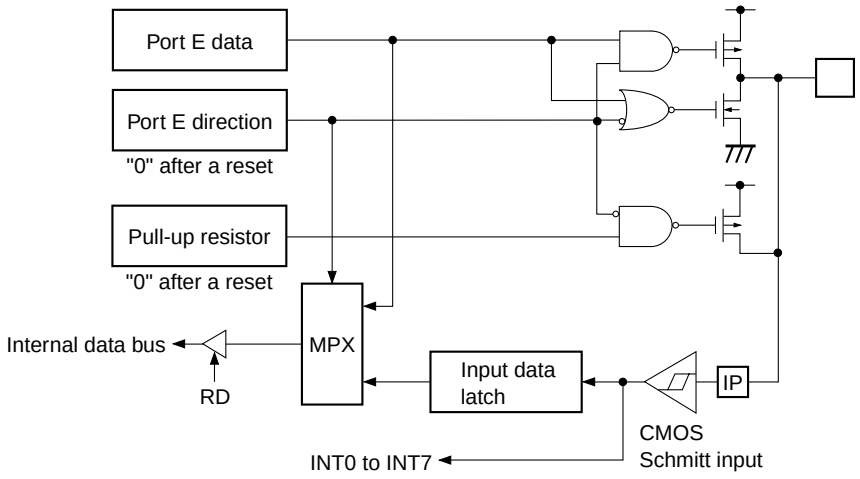
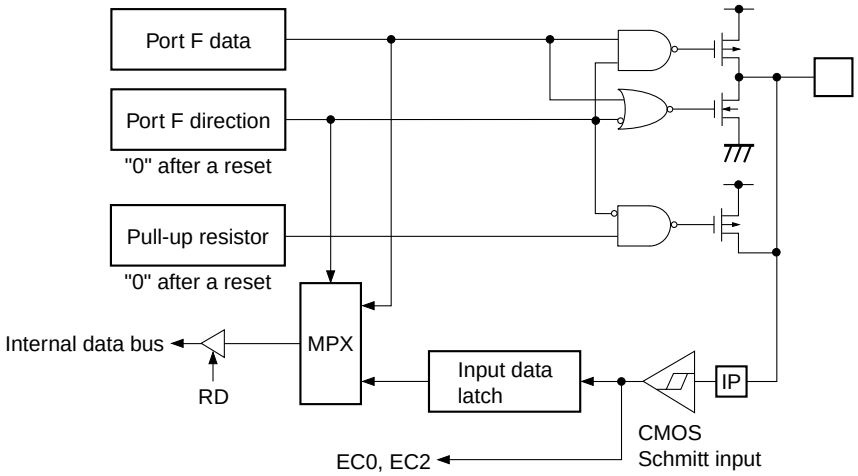
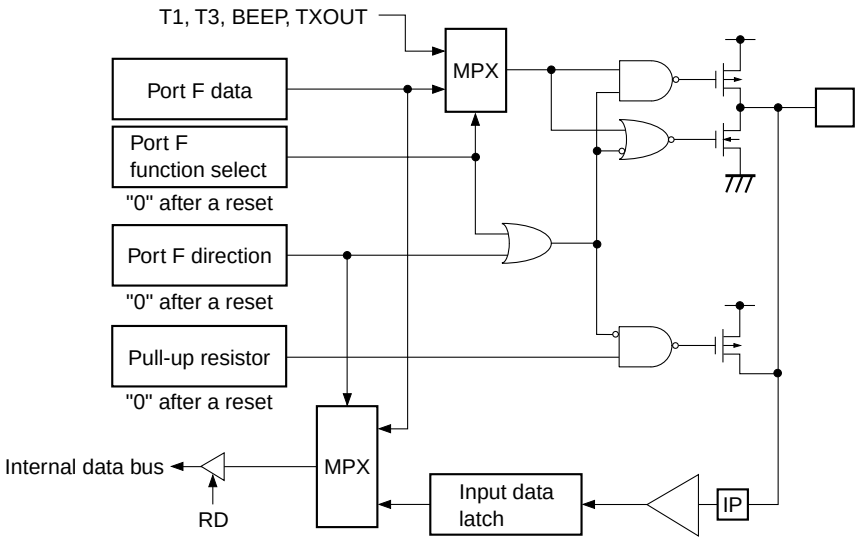
Symbol	I/O	Functios		
PN0/$\overline{SCK0}$	I/O / I/O	(Port N) 8-bit I/O port. I/O can be specified in 1-bit units. Pull-up resistor can be incorporated through program in 1-bit units. (8 pins)	Serial clock (CH0) I/O.	
PN1/SO0	I/O / Output		Serial data (CH0) output.	
PN2/SI0	I/O / Input		Serial data (CH0) input.	
PN3/$\overline{SCS0}$/ INT8	I/O / Input / Input		Serial chip select (CH0) input.	External interruption request input.
PN4/$\overline{SCK1}$	I/O / I/O		Serial clock (CH1) I/O.	
PN5/SO1	I/O / Output		Serial data (CH1) output.	
PN6/SI1	I/O / Input		Serial data (CH1) input.	
PN7/$\overline{SCS1}$/ INT9	I/O / Input / Input		Serial chip select (CH1) input.	External interruption request input.
PO0/$\overline{SCK2}$	I/O / I/O	(Port O) 4-bit I/O port. I/O can be specified in 1-bit units. Pull-up resistor can be incorporated through program in 1-bit units. (4 pins)	Serial clock (CH2) I/O.	
PO1/SO2	I/O / Output		Serial data (CH2) output.	
PO2/SI2	I/O / Input		Serial data (CH2) input.	
PO3/$\overline{SCS2}$	I/O / Input		Serial chip select (CH2) input.	
$\overline{CS0}$, $\overline{CS1}$	Output	Chip select output for external S bus. (2 pins)		
$\overline{RD}$	Output	Read signal output for external S bus.		
$\overline{LWR}$/$\overline{LB}$	Output / Output	Write strobe signal output for D0 to D7.	Strobe signal output indicates access to D0 to D7.	
$\overline{UWR}$/$\overline{UB}$	Output / Output	Write strobe signal output for D8 to D15.	Strobe signal output indicates access to D8 to D15.	
$\overline{MRD}$	Output	Read signal output for external M bus.		
$\overline{MWE}$/$\overline{WE}$	Output / Output	Write signal output for external M bus.	Write signal output for external S bus.	
$\overline{MCS0}$	Output	Chip select output for external M bus.		
$\overline{DACK0}$	Output	Transfer request acknowledge signal output from DMA controller (CH0).		
$\overline{DREQ0}$	Input	Transfer request input to DMA controller (CH0).		
$\overline{DACK1}$	Output	Transfer request acknowledge signal output from DMA controller (CH1).		
$\overline{DREQ1}$	Input	Transfer request input to DMA controller (CH1).		
MSDIR	Output	Memory stick interface data I/O direction monitor.		
MSBS	Output	Memory stick interface bus state output.		
MSSCLK	Output	Memory stick interface clock output.		
MSDIO	I/O	Memory stick interface data I/O direction monitor.		
$\overline{MSINS}$	Input	Memory stick interface card detection.		
TEST0	Input	Test. (Connect to Vss.)		
TEST1	Input			
TEST2	Input			
TDI	Input	Data input for JTAG boundary scanning test.		

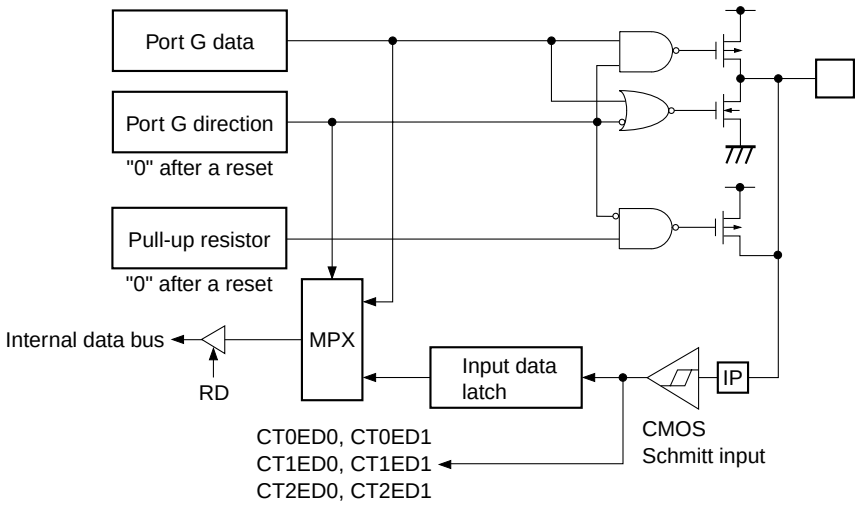
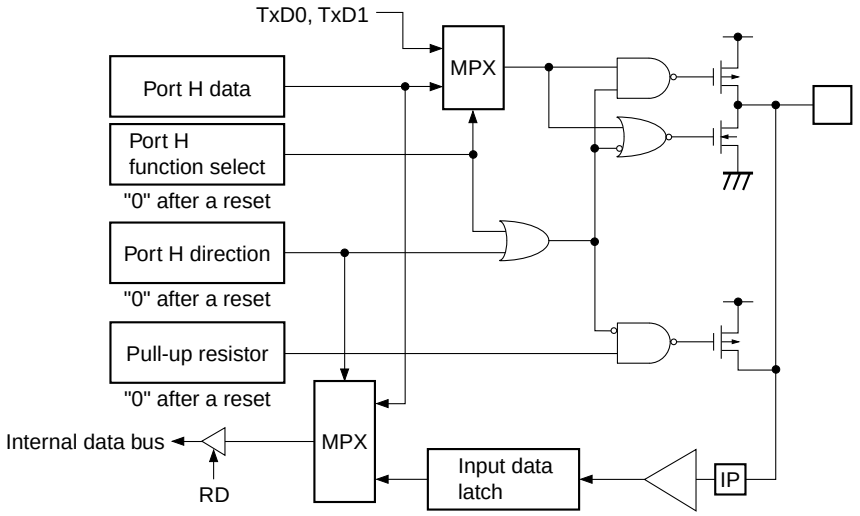
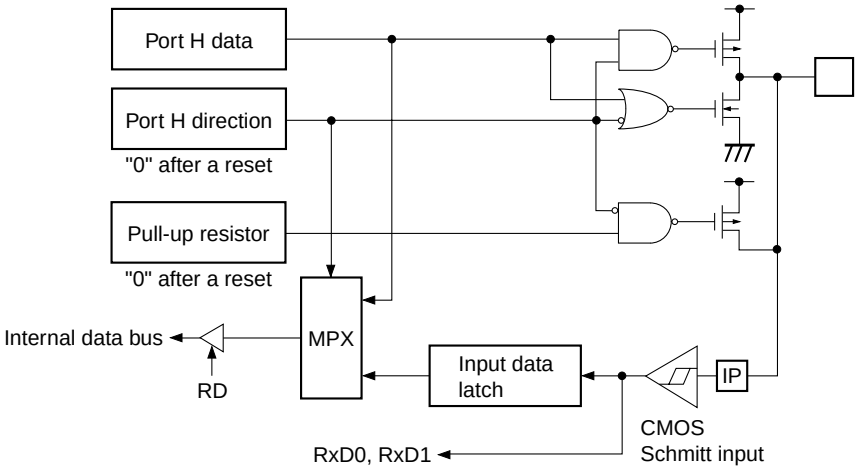
Symbol	I/O	Functions	
TMS	Input	Test mode control input for JTAG boundary scanning test.	
$\overline{\text{TRST}}$	Input	Reset input for JTAG boundary scanning test.	
TCK	Input	Clock input for JTAG boundary scanning test.	
RTCK	Output	Clock output for JTAG boundary scanning test.	
TDO	Output	Data output for JTAG boundary scanning test.	
EXTAL	Input	Oscillation connector of main oscillation. (When a clock is supplied externally, input it to EXTAL; opposite phase clock should be input to XTAL.)	
XTAL	Output		
XOUT/CKO	Output / Output	Main oscillation output.	System clock output.
TEX	Input	Oscillation connector of main oscillation. (When a clock is supplied externally, input it to TEX; opposite phase clock should be input to TX.)	
TX	Output		
$\overline{\text{RST}}$	I/O	System reset.	
PWE	Input	FLASH EEPROM miswriting protection signal input.	
NC		NC. (Leave this pin open or connect to Vss.)	
AV_{DD}		Positive power supply for A/D converter.	
AV_{REF}	Input	Reference voltage input for A/D converter.	
AV_{SS}		GND for A/D converter.	
V_{DD}		Positive power supply (Connect all twelve V_{DD} pins to positive power supply.)	
V_{SS}		GND (Connect all twelve Vss pins to GND)	

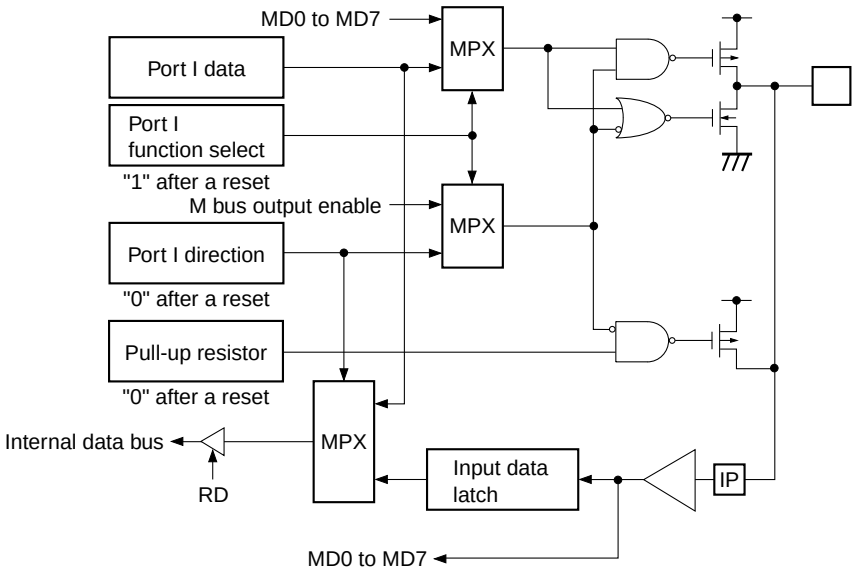
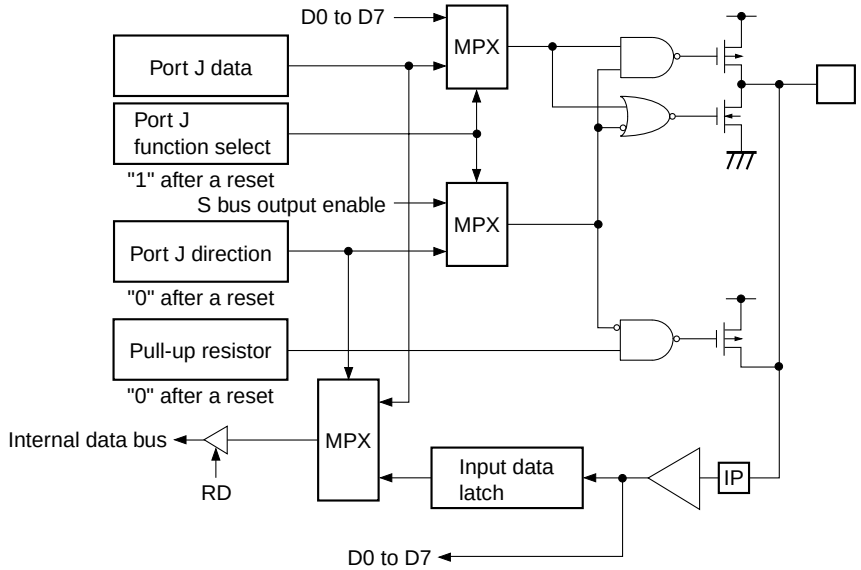
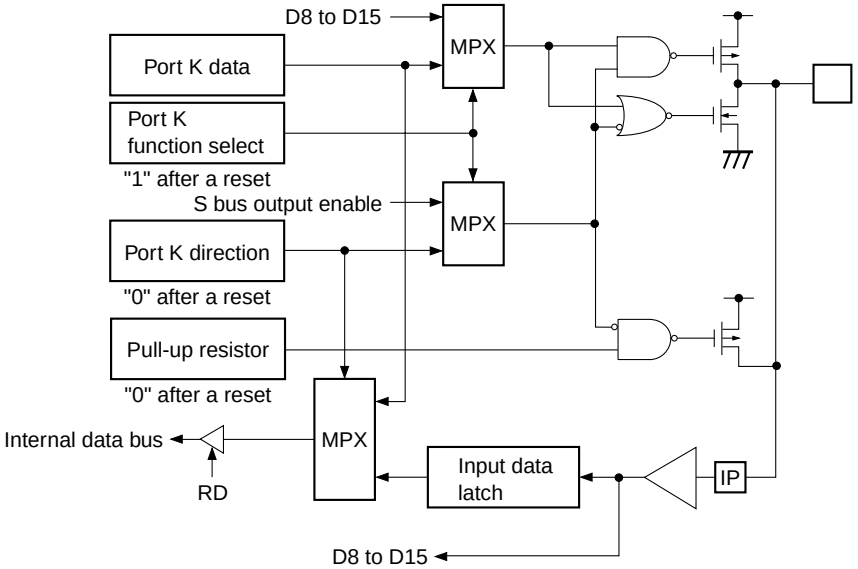
I/O Circuit Format for Pins

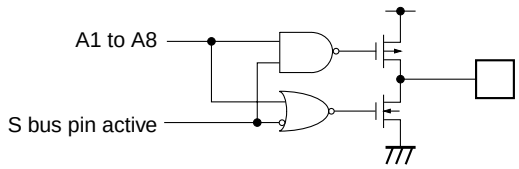
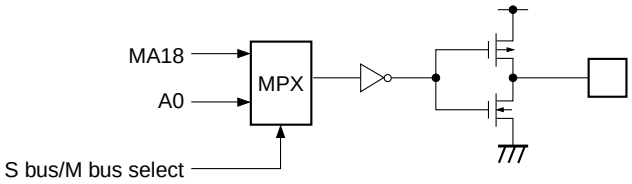
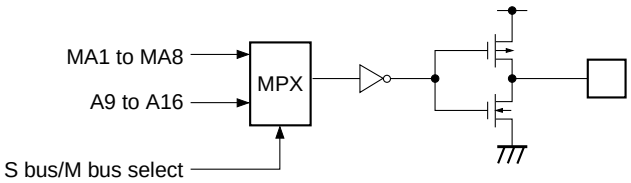
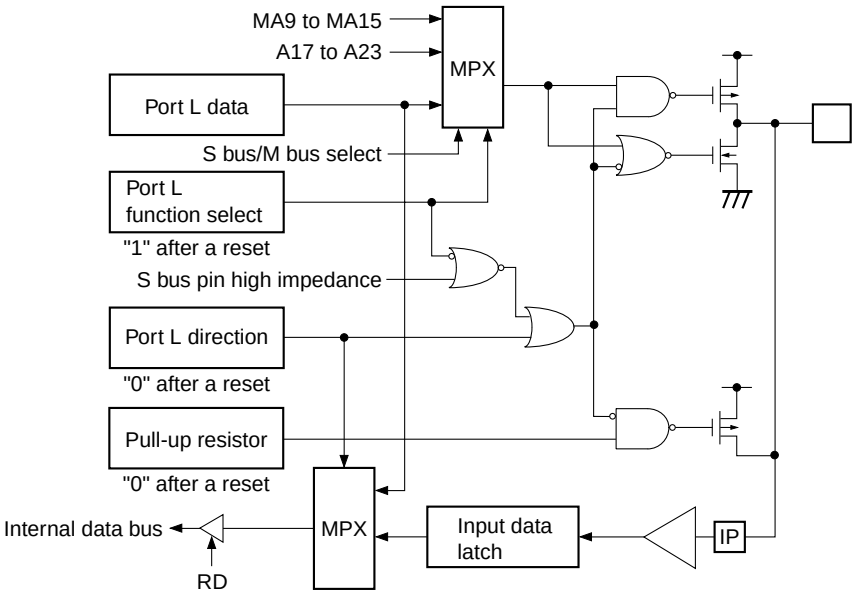
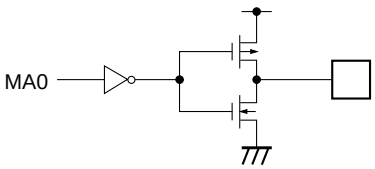
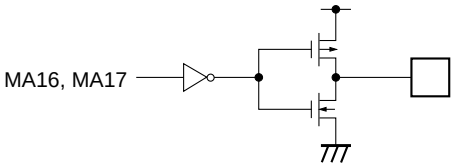
Pin	Circuit format	After a reset
PA0/$\overline{WAIT}$		Hi-Z
PA1/$\overline{CS2}$ to PA4/$\overline{CS5}$		Hi-Z
PA5/$\overline{MCS1}$		Hi-Z

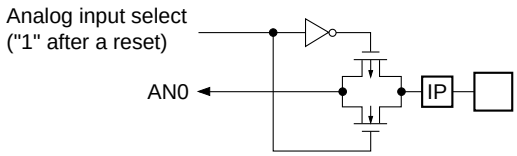
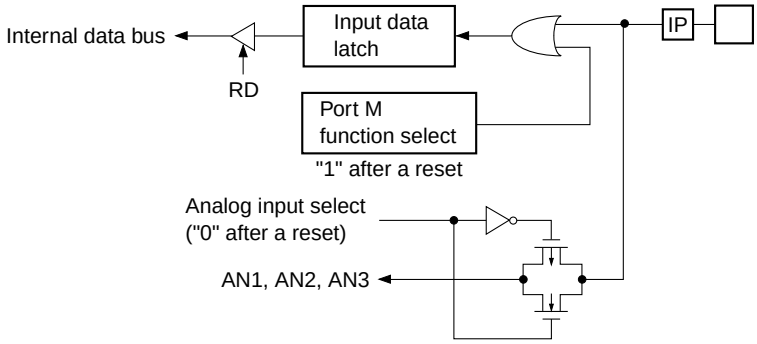
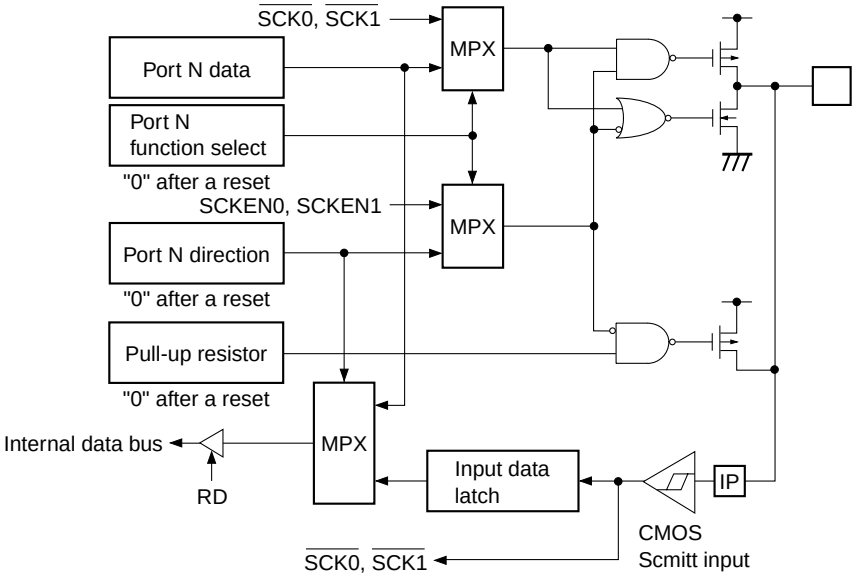
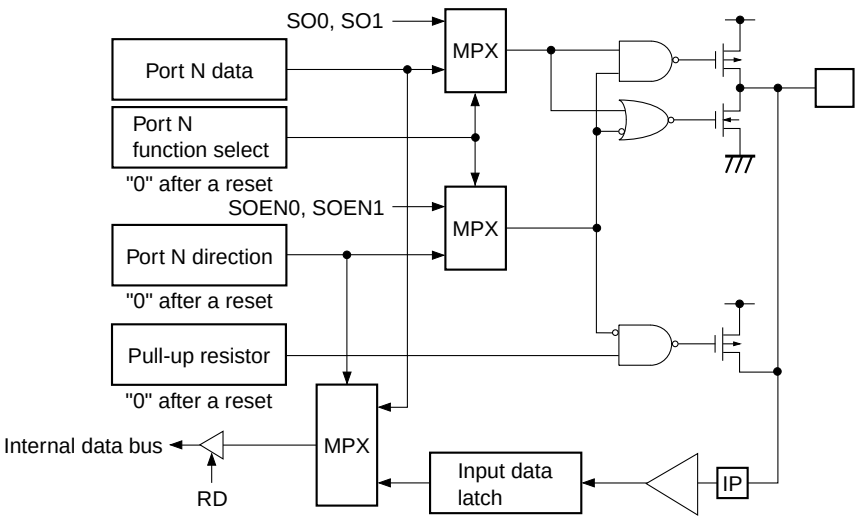
Pin	Circuit format	After a reset
PB0 to PB7		Hi-Z
PC0 to PC5		Hi-Z
PD0 PD1		Hi-Z
PD2 PD3		Hi-Z

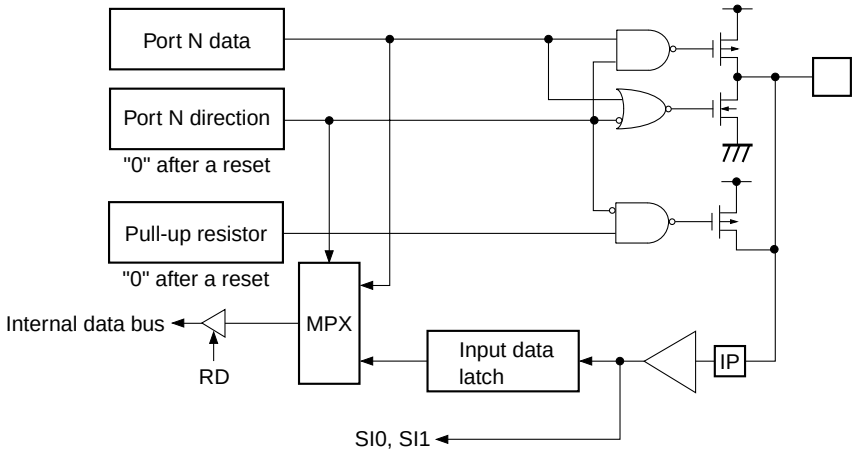
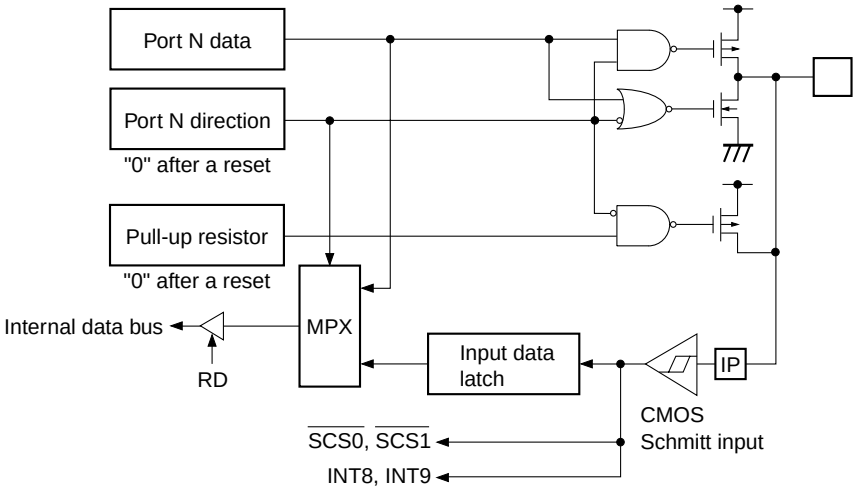
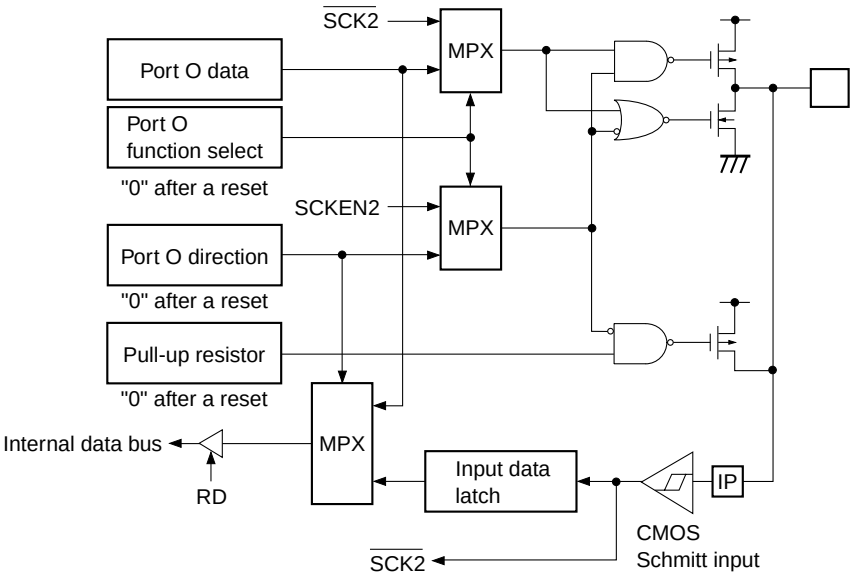
Pin	Circuit format	After a reset
PE0/INT0 to PE7/INT7		Hi-Z
PF0/EC0 PF2/EC2		Hi-Z
PF1/T1 PF3/T3 PF4/BEEP PF5/TXOUT		Hi-Z

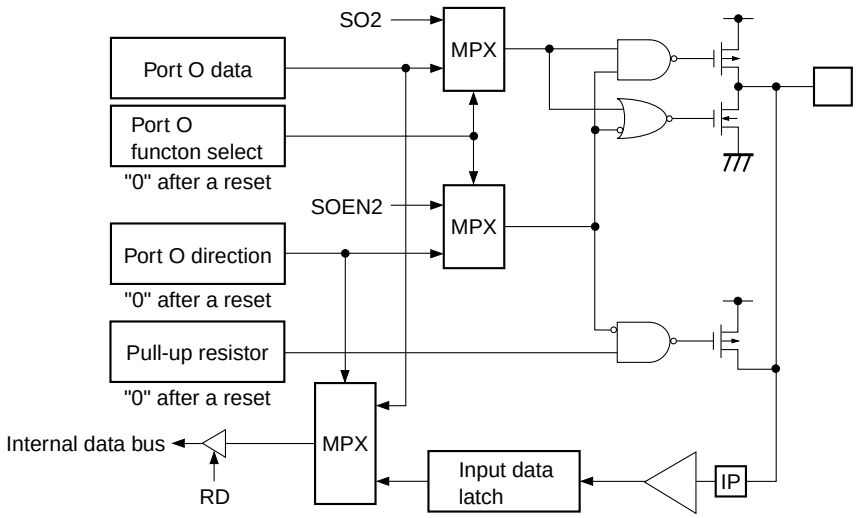
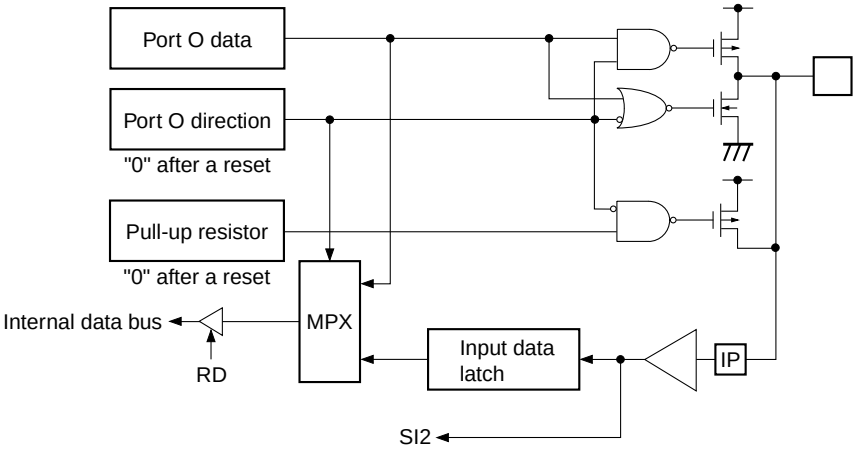
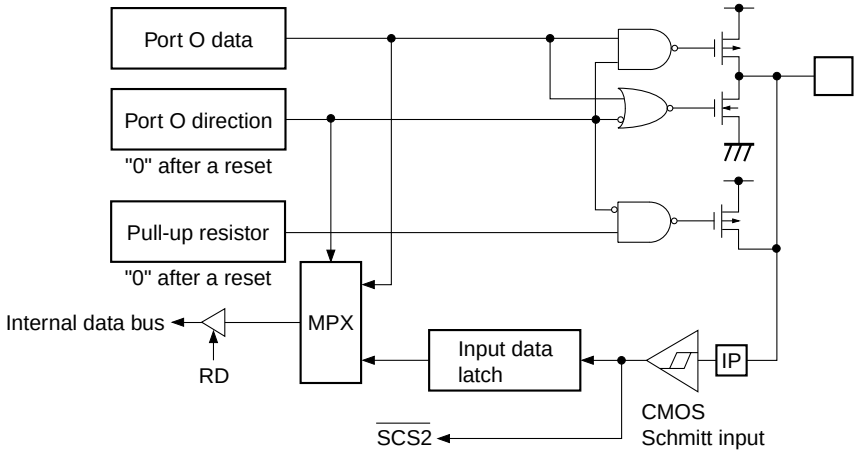
Pin	Circuit format	After a reset
PG0/CT0ED0 PG1/CT0ED1 PG2/CT1ED0 PG3/CT1ED1 PG4/CT2ED0 PG5/CT2ED1		Hi-Z
PH0/TxD0 PH2/TxD1		Hi-Z
PH1/RxD0 PH3/RxD1		Hi-Z

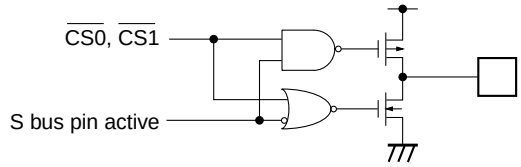
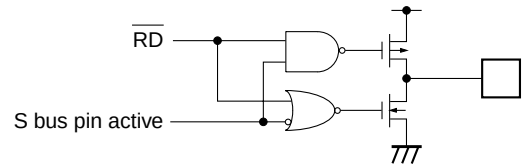
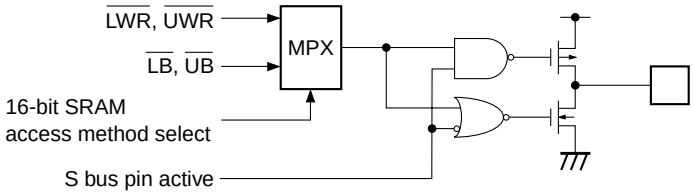
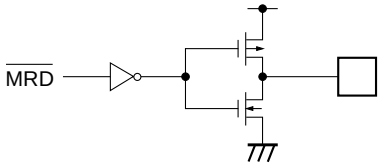
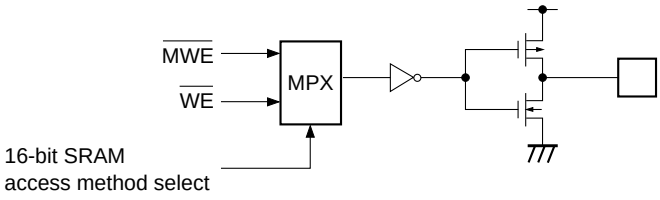
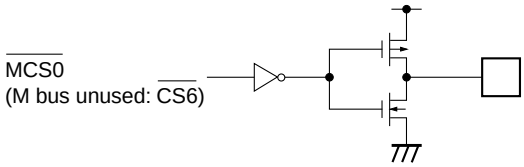
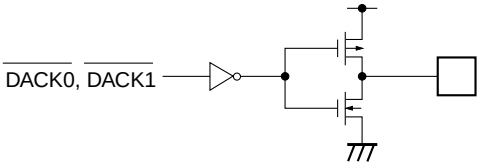
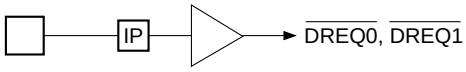
Pin	Circuit format	After a reset
PI0/MD0 to PI7/MD7		Hi-Z
PJ0/D0 to PJ7/D7		Hi-Z
PK0/D8 to PK7/D15		Hi-Z

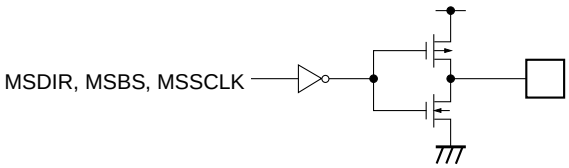
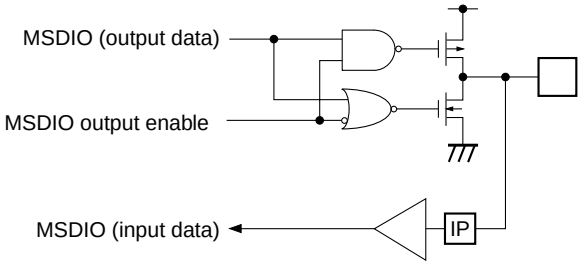
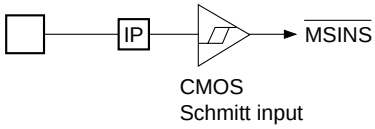
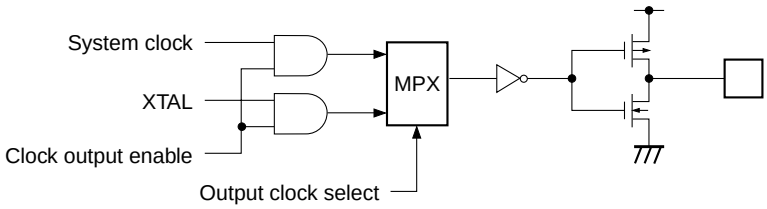
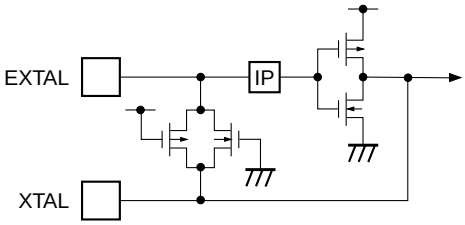
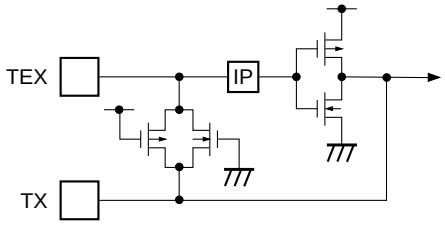
Pin	Circuit format	After a reset
A1 to A8		Low
MA18/A0		Low
MA1/A9 to MA8/A16		Low
PL0/MA9/A17 to PL6/MA15/A23		Low
MA0		Low
MA16 MA17		Low

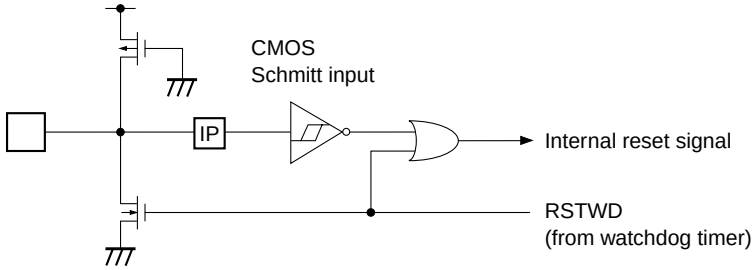
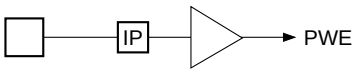
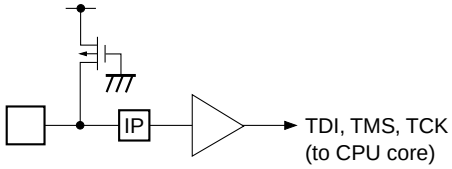
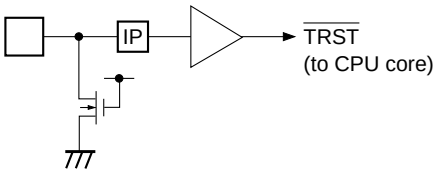
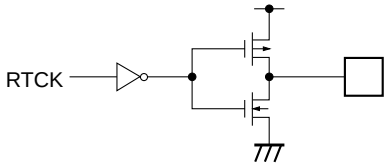
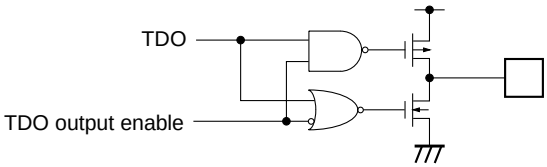
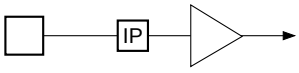
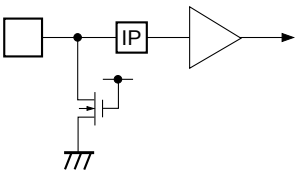
Pin	Circuit format	After a reset
AN0		Hi-Z
PM0/AN1 to PM2/AN3		Hi-Z
PN0/$\overline{\text{SCK0}}$ PN4/$\overline{\text{SCK1}}$		Hi-Z
PN1/SO0 PN5/SO1		Hi-Z

Pin	Circuit format	After a reset
PN2/SI0 PN6/SI1		Hi-Z
PN3/$\overline{\text{SCS0}}$/INT8 PN7/$\overline{\text{SCS1}}$/INT9		Hi-Z
PO0/$\overline{\text{SCK2}}$		Hi-Z

Pin	Circuit format	After a reset
PO1/SO2		Hi-Z
PO2/SI2		Hi-Z
PO3/$\overline{\text{SCS2}}$		Hi-Z

Pin	Circuit format	After a reset
$\overline{CS0}$ $\overline{CS1}$		High
$\overline{RD}$		High
$\overline{LWR}/\overline{LB}$ $\overline{UWR}/\overline{UB}$		High
$\overline{MRD}$		High
$\overline{MWE}/\overline{WE}$		High
$\overline{MCS0}$		High
$\overline{DACK0}$ $\overline{DACK1}$		High
$\overline{DREQ0}$ $\overline{DREQ1}$		Hi-Z

Pin	Circuit format	After a reset
MSDIR MSBS MSSCLK		Low
MSDIO		Hi-Z
$\overline{\text{MSINS}}$		Hi-Z
XOUT/CKO		Oscillation output
EXTAL XTAL	 • Diagram shows circuit configuration during oscillation. • Feedback resistor is removed during stop mode, and XTAL is driven at “H” level.	Oscillation
TEX TX	 • Diagram shows circuit configuration during oscillation. • Feedback resistor is removed during stop mode, and TEX is driven at “L” level; TX at “H” level.	Oscillation

Pin	Circuit format	After a reset
$\overline{\text{RST}}$		Pull-up
PWE		Hi-Z
TDI TMS TCK		Pull-up
$\overline{\text{TRST}}$		Pull-down
RTCK		High
TDO		Low
TEST0 TEST1		Hi-Z
TEST2		Pull-down

Absolute Maximum Ratings (Vss = 0V reference)

Item	Symbol	Rating	Unit	Remarks
Supply voltage	V_{DD}	–0.3 to +4.6	V	
	AV_{DD}	AV_{SS} to +4.6*1	V	
	AV_{SS}	–0.3 to +0.3	V	
	AV_{REF}	AV_{SS} to +4.6	V	
Input voltage	V_{IN}	–0.3 to +4.6*2	V	
Output voltage	V_{OUT}	–0.3 to +4.6*2	V	
High level output current	I_{OH}	–5	mA	Output (value per pin)
High level total output current	ΣI_{OH}	–40	mA	Total for all output pins
Low level output current	I_{OL}	10	mA	Output (value per pin)
Low level total output current	ΣI_{OL}	80	mA	Total for all output pins
Operating temperature	Topr	–20 to +75	°C	
Storage temperature	Tstg	–55 to +150	°C	
Allowable power dissipation	P_D	380	mW	

*1 AV_{DD} and V_{DD} must be the same voltage.

*2 V_{IN} and V_{OUT} must not exceed V_{DD} + 0.3V.

Note) Usage exceeding absolute maximum ratings may permanently impair the LSI. Normal operation should be conducted under the recommended operating conditions. Exceeding these conditions may adversely affect the reliability of the LSI.

Recommended Operating Conditions (Vss = 0V reference)

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Supply voltage	V_{DD}	2.7		3.6	V	
Analog voltage	AV_{DD}	2.7		3.6	V	*1
High level input voltage	V_{IH}	0.7V_{DD}		V_{DD}	V	CMOS input*2
	V_{IHS}	0.7V_{DD}		V_{DD}	V	CMOS Schmitt trigger input*3
	V_{IHEX}	0.9V_{DD}		V_{DD} + 0.3	V	EXTAL*4, TEX*4
Low level input voltage	V_{IL}	0		0.2V_{DD}	V	CMOS input*2
	V_{ILS}	0		0.2V_{DD}	V	CMOS Schmitt trigger input*3
	V_{ILEX}	–0.3		0.4	V	EXTAL*4, TEX*4
Hysteresis width	$V_{IHS} – V_{ILS}$		0.5		V	CMOS Schmitt trigger input*3
Operating temperature	Topr	–20		+75	°C	

*1 AV_{DD} and V_{DD} must be the same voltage.

*2 Normal input port (PA to PC, PD2, PD3, PE, PF1, PF3 to PF5, PH0, PH2, PI to PM, PN1, PN2, PN5, PN6, PO1, PO2, $\overline{DREQ0}$, $\overline{DREQ1}$, MSDIO, TDI, TMS, $\overline{TRST}$, TCK, PWE and TEST0 to TEST2).

*3 Each pin of EC0, EC2, CT0ED0, CT0ED1, CT1ED0, CT1ED1, CT2ED0, CT2ED1, RxD0, RxD1, $\overline{SCK0}$ to $\overline{SCK2}$, $\overline{SCS0}$ to $\overline{SCS2}$, INT8, INT9, $\overline{MSINS}$ and $\overline{RST}$.

*4 Specified only during external clock input.

Electrical Characteristics

DC Characteristics (V_{DD} = 2.7 to 3.6V) (Topr = –20 to +75°C, Vss = 0V reference)

Item	Symbol	Pins	Conditions	Min.	Typ.	Max.	Unit
High level output voltage	V_{OH}	PA to PC, PE to PL, PN, PO, T1, T3, TxD0, TxD1, MCS0, MCS1, MA0 to MA18, MD0 to MD7, MRD, MWE, CS0 to CS5, A0 to A23, D0 to D15, RD, LWR, LB, UWR, UB, WE, RST	I_{OH} = –0.5mA	V_{DD} – 0.4			V
		BEEP, TXOUT, SCK0 to SCK2, SO0 to SO2, DACK0, DACK1, MSDIR, MSBS, MSSCLK, MSDIO, RTCK, TDO, XOUT, CKO	I_{OH} = –4mA	V_{DD} – 0.4			V
Low level output voltage	V_{OL}	PA to PC, PE to PL, PN, PO, T1, T3, TxD0, TxD1, MCS0, MCS1, MA0 to MA18, MD0 to MD7, MRD, MWE, CS0 to CS5, A0 to A23, D0 to D15, RD, LWR, LB, UWR, UB, WE, RST	I_{OL} = 1mA			0.4	V
		PD, BEEP, TXOUT, SCK0 to SCK2, SO0 to SO2, DACK0, DACK1, MSDIR, MSBS, MSSCLK, MSDIO, RTCK, TDO, XOUT, CKO	I_{OL} = 4mA			0.4	V
Input current	I_{IHE}	EXTAL	V_{IH} = 3.6V	0.1		10	µA
	I_{ILE}		V_{IL} = 0.4V	–0.1		–10	µA
	I_{IHT}	TEX	V_{IH} = 3.6V	0.1		10	µA
	I_{ILT}		V_{IL} = 0.4V	–0.1		–10	µA
	I_{IH}	TRST	V_{IH} = 3.6V	20	100	240	µA
	I_{IL}	PA to PC, PE to PL, PN, PO, WAIT, INT0 to INT9, EC0, EC2, CT0ED0, CT0ED1, CT1ED0, CT1ED1, CT2ED0, CT2ED1, RxD0, RxD1, MD0 to MD7, D0 to D15, SCK0 to SCK2, SI0 to SI2, SCS0 to SCS2*1	V_{IL} = Vss	–20	–50	–120	µA
		TDI, TMS, TCK	V_{IL} = Vss	–20	–100	–240	µA

*1 PA to PC, PE to PL, PN, PO, WAIT, INT0 to INT9, EC0, EC2, CT0ED0, CT0ED1, CT1ED0, CT1ED1, CT2ED0, CT2ED1, RxD0, RxD1, MD0 to MD7, D0 to D15, SCK0 to SCK2, SI0 to SI2 and SCS0 to SCS2 pins specify the input current when the pull-up resistor is selected, and specify leakage current when non-resistor is selected.

Item	Symbol	Pins	Conditions	Min.	Typ.	Max.	Unit
I/O leakage current	I_{ZH}	PD2, PD3, PM, AN0 to AN3, DREQ0, DREQ1, MSDIO, MSINS, PA to PC, PE to PL, PN, PO, WAIT, INT0 to INT9, EC0, EC2, CT0ED0, CT0ED1, CT1ED0, CT1ED1, CT2ED0, CT2ED1, RxD0, RxD1, MD0 to MD7, D0 to D15, SCK0 to SCK2, SI0 to SI2, SCS0 to SCS2	V_I = 3.6V			10	µA
	I_{ZL}	PD2, PD3, PM, AN0 to AN3, DREQ0, DREQ1, MSDIO, MSINS, PA to PC, PE to PL, PN, PO, WAIT, INT0 to INT9, EC0, EC2, CT0ED0, CT0ED1, CT1ED0, CT1ED1, CT2ED0, CT2ED1, RxD0, RxD1, MD0 to MD7, D0 to D15, SCK0 to SCK2, SI0 to SI2, SCS0 to SCS2*1	V_I = 0V			–10	µA
Supply current*2	I_{DD1}	V_{DD}	Main execution mode 18.432MHz crystal oscillation (C_1 = C_2 = 10pF)			60	mA
	I_{DDI1}		Main idle mode 18.432MHz crystal oscillation (C_1 = C_2 = 10pF)			32	mA
	I_{DDS1}		Sub sleep mode 32.768kHz crystal oscillation (C_1 = C_2 = 10pF)			500	µA
			Ta = –20 to +25°C			80	µA
	I_{DDS2}		Stop mode 32.768kHz oscillation stop			500	µA
			Ta = –20 to +25°C			50	µA
Input capacity	C_{IN}	PA to PC, PD2, PD3, PE to PO, WAIT, INT0 to INT9, EC0, EC2, CT0ED0, CT0ED1, CT1ED0, CT1ED1, CT2ED0, CT2ED1, RxD0, RxD1, MD0 to MD7, D0 to D15, AN0 to AN3, SCK0 to SCK2, SI0 to SI2, SCS0 to SCS2, MSDIO, EXTAL, TEX, RST, TEST0	Clock 1MHz 0V other than the measured pins			11	pF
		DREQ0, DREQ1, MSINS, TDI, TMS, TRST, TCK, TEST1, TEST2, PWE				9	pF

*1 PA to PC, PE to PL, PN, PO, WAIT, INT0 to INT9, EC0, EC2, CT0ED0, CT0ED1, CT1ED0, CT1ED1, CT2ED0, CT2ED1, RxD0, RxD1, MD0 to MD7, D0 to D15, SCK0 to SCK2, SI0 to SI2 and SCS0 to SCS2 pins specify the input current when the pull-up resistor is selected, and specify leakage current when non-resistor is selected.

*2 When all output pins are left open and XOUT/CKO = “L” (POSL register SLCKO bit = “00” or “01”).

AC Characteristics

(1) Clock timing (Topr = –20 to +75°C, V_{DD} = 2.7 to 3.6V, Vss = 0V reference)

Item	Symbol	Pins	Conditions	Min.	Typ.	Max.	Unit
Main oscillation input clock frequency	f_{EX}	XTAL EXTAL	Fig. 1, Fig. 2	1		20	MHz
Main oscillation input clock pulse width	t_{XL}, t_{XH}	XTAL EXTAL	Fig. 1, Fig. 2 External clock drive	22.5			ns
Main oscillation input clock rise time, fall time	t_{CR}, t_{CF}	XTAL EXTAL	Fig. 1, Fig. 2 External clock drive			100/f_{EX}	ns
Sub oscillation input clock frequency	f_{TEX}	TEX TX	Fig. 2 32kHz clock applied condition		32.768		kHz
Event count input clock pulse width	t_{EH}, t_{EL}	EC0 EC2	Fig. 3	2/f_{PS4}			µs
Event count input clock rise time, fall time	t_{ER}, t_{EF}	EC0 EC2	Fig. 3			1	ms

Note) f_{PS4} is f_{SRC}/16 (MHz) for output f_{SRC} of main oscillation circuit.

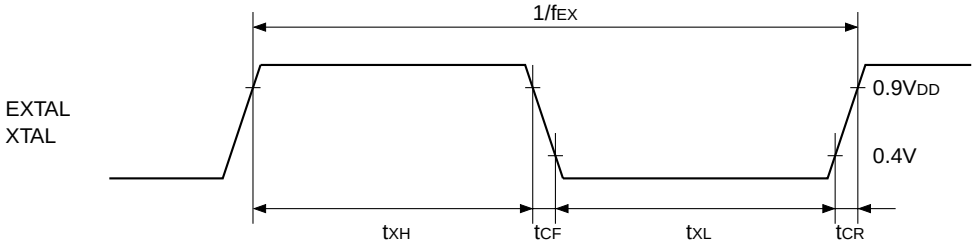


Fig. 1. Clock timing

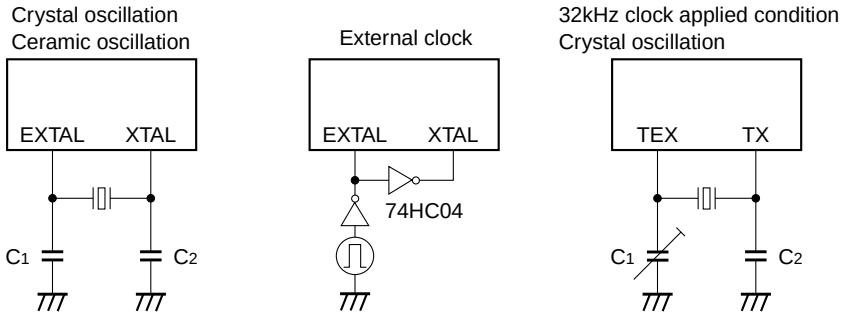


Fig. 2. System clock applied condition

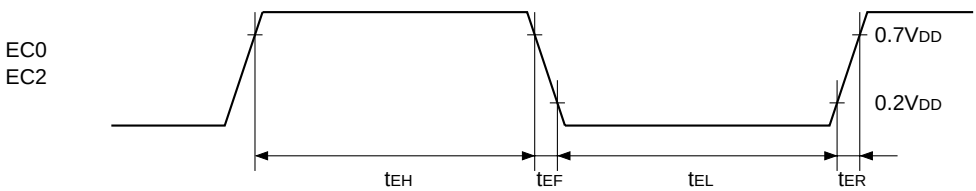


Fig. 3. Event count input timing

(2) Serial transfer (CH0, CH1, CH2) (Topr = –20 to +75°C, V_{DD} = 2.7 to 3.6V, Vss = 0V reference)

Item	Symbol	Pins	Conditions	Min.	Max.	Unit
$\overline{SCS} \downarrow \rightarrow \overline{SCK}$ delay time	t_{DCSK}	$\overline{SCK0}$ $\overline{SCK1}$ $\overline{SCK2}$	External start transfer mode			
			Input mode (SCKOE = "1")	100		ns
			Output mode		100	ns
$\overline{SCS} \uparrow \rightarrow \overline{SCK}$ float delay time	t_{DCSKF}	$\overline{SCK0}$ $\overline{SCK1}$ $\overline{SCK2}$	External start transfer mode ($\overline{SCK}$ = output mode, SCKOE = "1")		100	ns
$\overline{SCS} \downarrow \rightarrow$ SO delay time	t_{DCSO}	SO0 SO1 SO2	External start transfer mode (SOEN = "1")		100	ns
$\overline{SCS} \uparrow \rightarrow$ SO float delay time	t_{DCSOF}	SO0 SO1 SO2	External start transfer mode (SOEN = "1")		100	ns
$\overline{SCS}$ high level width	t_{WHCS}	$\overline{SCS0}$ $\overline{SCS1}$ $\overline{SCS2}$	External start transfer mode	200		ns
$\overline{SCK}$ interval time	t_{KINT}	$\overline{SCK0}$	$\overline{SCK}$ input mode			
			Internal start high-speed transfer mode	$\frac{6000}{f_{SYS}} + \frac{2000}{f_{SIO}} + \frac{t_{KCY}}{2}$		ns
			External start high-speed transfer mode	$\frac{6000}{f_{SYS}} + \frac{3000}{f_{SIO}} + \frac{t_{KCY}}{2}$		ns
$\overline{SCK}$ cycle time	t_{KCY}	$\overline{SCK0}$ $\overline{SCK1}$ $\overline{SCK2}$	Input mode	400		ns
			Output mode	$1000/f_{SCK}$		ns
$\overline{SCK}$ high, low pulse width	t_{KH} t_{KL}	$\overline{SCK0}$ $\overline{SCK1}$ $\overline{SCK2}$	Input mode	200		ns
			Output mode	$500/f_{SCK} - 50$		ns
Input setup time (for $\overline{SCK} \uparrow$)	t_{SIK}	SI0 SI1 SI2	$\overline{SCK}$ input mode	50		ns
			$\overline{SCK}$ output mode	75		ns
SI input hold time (for $\overline{SCK} \uparrow$)	t_{KSI}	SI0 SI1 SI2	$\overline{SCK}$ input mode	100		ns
			$\overline{SCK}$ output mode	50		ns
$\overline{SCK} \downarrow \rightarrow$ SO delay time	t_{KSO}	SO0 SO1 SO2	$\overline{SCK}$ input mode		75	ns
			$\overline{SCK}$ output mode		50	ns

Notes) 1. The load condition for the $\overline{SCK}$ output mode and SO output delay time is 50pF.

2. f_{SIO} is $f_{SRC}/2$ (MHz) for output f_{SRC} of main oscillation circuit. As for f_{SCK} and f_{SYS}, see the following.

Serial clock selection	f_{SCK} (MHz)
PS3*1	$f_{SRC}/8$
PS4*1	$f_{SRC}/16$
PS5	$f_{SRC}/32$
PS6	$f_{SRC}/64$
PS7*2	$f_{SRC}/128$
PS8*2	$f_{SRC}/256$

Serial clock frequency division ratio	f_{SCK} (MHz)
No frequency division	No
2 frequency division	$f_{SRC}/2$
4 frequency division	$f_{SRC}/4$
16 frequency division	$f_{SRC}/16$

*1 CH1, CH2 only *2 CH0 only

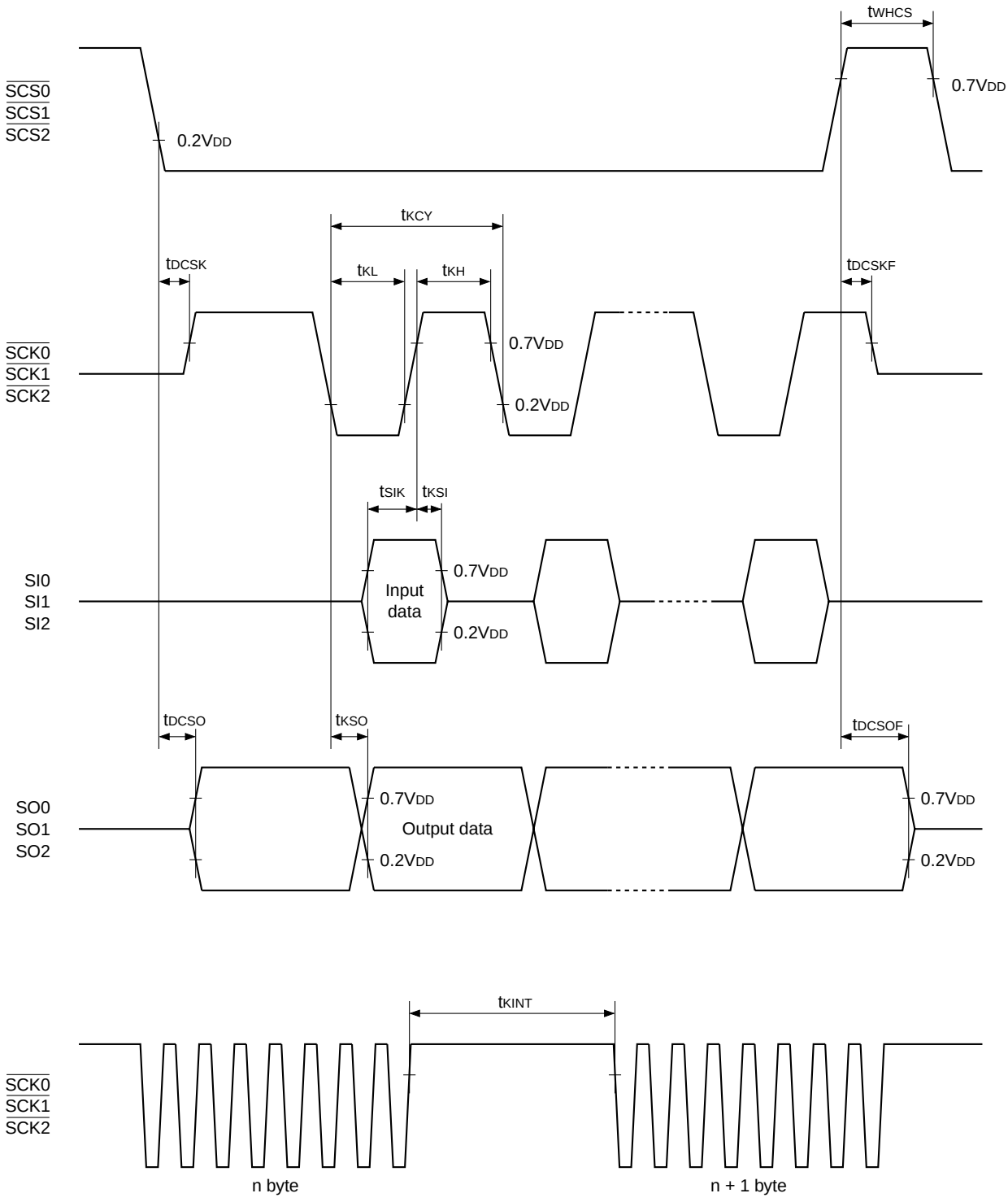


Fig. 4. Serial transfer CH0, CH1, CH2 timing

(3) Serial transfer (memory stick) (Topr = –20 to +75°C, V_{DD} = 2.7 to 3.6V, Vss = 0V reference)

Item	Symbol	Pins	Conditions	Min.	Max.	Unit
MSSCLK cycle time	t_{KCY}	MSSCLK		1000/f_{MSCK}		ns
MSSCLK high, low pulse width	t_{KH} t_{KL}	MSSCLK		500/f_{MSCK} – 5		ns
MSBS output delay time	t_{BSD}	MSBS	For MSSCLK ↓		10	ns
MSDIO output delay time	t_{DIOD}	MSDIO	For MSSCLK ↓		10	ns
MSDIO input setup time	t_{DIOS}	MSDIO	For MSSCLK ↑	18		ns
MSDIO input hold time	t_{DIOH}	MSDIO	For MSSCLK ↑	5		ns
MSDIR output delay time	t_{DIRD}	MSDIR	For MSSCLK ↓		10	ns

Notes) 1. The load condition is 26pF.

2. f_{MSCK} is as follows for output f_{SRC} of main oscillation circuit.

Shift clock frequency division ratio	f_{MSCK} (MHz)
No frequency division	f_{SRC}
2 frequency division	f_{SRC}/2
4 frequency division	f_{SRC}/4
8 frequency division	f_{SRC}/8

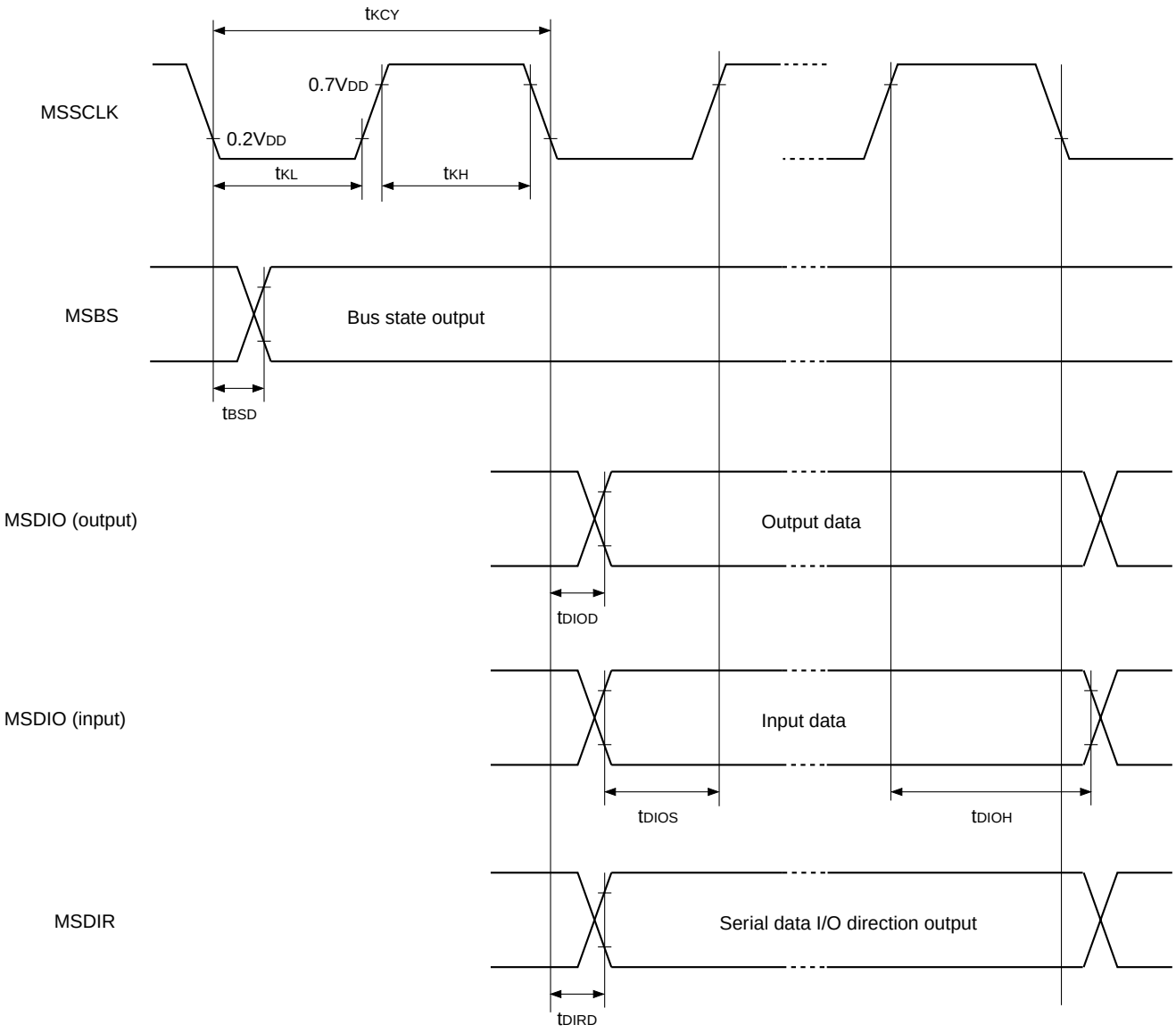


Fig. 5. Memory stick transfer timing

(4) A/D converter characteristics

(Topr = –20 to +75°C, V_{DD} = 2.7 to 3.6V, V_{DD} = AV_{DD}, Vss = AVss = 0V reference)

Item	Symbol	Pins	Conditions	Min.	Typ.	Max.	Unit
Resolution						8	Bits
Absolute error						±3	LSB
Conversion time	t_{CONV}			19/f_{PS4}		20/f_{PS4}	µs
Sampling time	t_{SAMP}				5/f_{PS4}		µs
Reference input voltage	V_{REF}	AV_{REF}	V_{DD} = AV_{DD} = 2.7V	AV_{DD} – 0.3		AV_{DD}	V
Analog input voltage	V_{IAN}	AN0 to AN3		0		AV_{REF}	V

Note) f_{PS4} is f_{SRC}/16 (MHz) for output f_{SRC} of main oscillation circuit.
Conversion time indicates the time required from conversion start to ADC interruption request occurrence when 1 channel is selected. This includes sampling time.

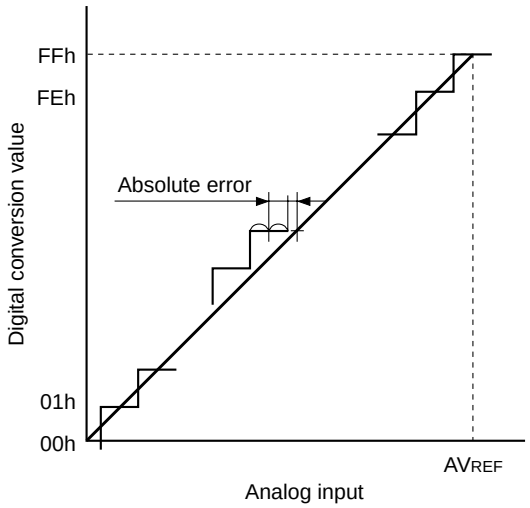


Fig. 6. Definition of A/D converter terms

(5) Interruption and reset input (Topr = –20 to +75°C, V_{DD} = 2.7 to 3.6V, Vss = 0V reference)

Item	Symbol	Pins	Conditions	Min.	Typ.	Max.	Unit
External interruption high, low level width	t_{IH} t_{IL}	INT0 to INT9		100	200		ns
Reset input high, low level width	t_{IH} t_{IL}	$\overline{RST}$			32/f_{SRC}		µs

Note) f_{SRC} is output of main oscillation circuit.

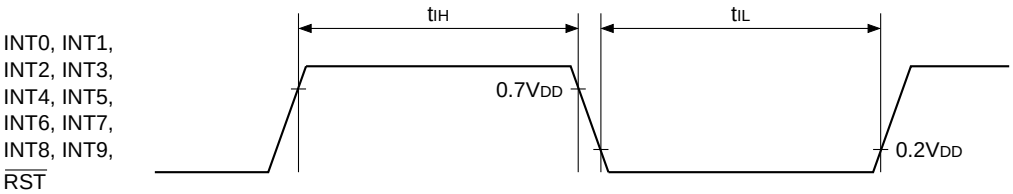


Fig. 7. Interruption input, $\overline{RST}$ input timing

Appendix

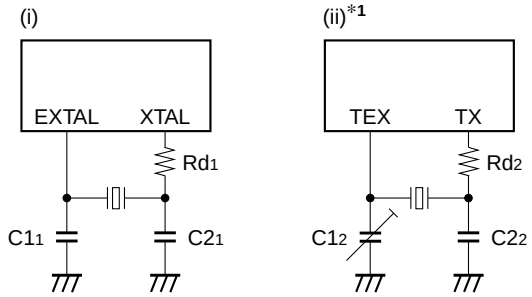


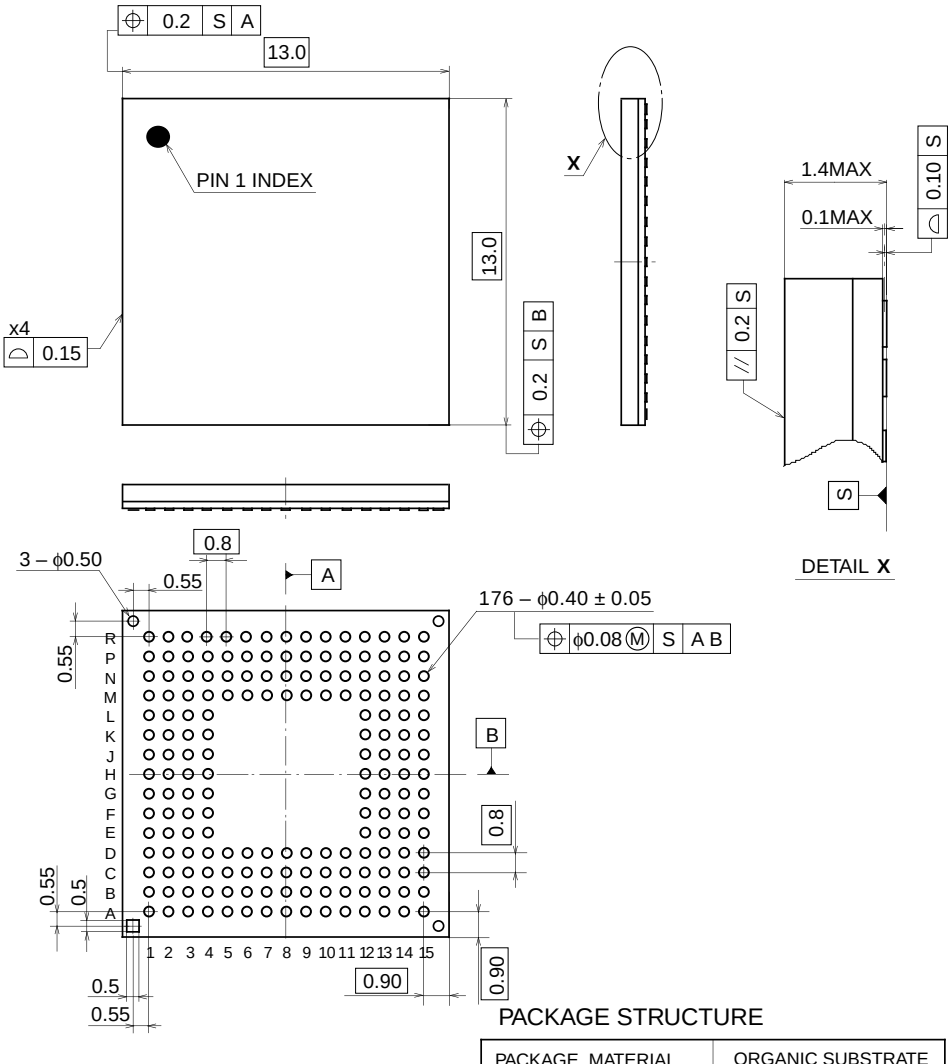
Fig. 8. Recommended oscillation circuit

Manufacturer	Model	fc (MHz)	$C1_1$ (pF)	$C2_1$ (pF)	Rd_1 (Ω)	Circuit example
RIVER EIETEC CO., LTD.	FCK-03	18.432	12	12	0	(i)

*1 As for (ii) sub oscillation circuit $C1_2$, $C2_2$ and Rd_2, decide them by seeing matching with oscillator.

Package Outline Unit: mm

176PIN LFLGA (PLASTIC)



PACKAGE STRUCTURE

SONY CODE	LFLGA-176P-01
EIAJ CODE	P-LFLGA176-13X13-0.8
JEDEC CODE	————

PACKAGE MATERIAL	ORGANIC SUBSTRATE
TERMINAL TREATMENT	NICKEL & GOLD PLATING
TERMINAL MATERIAL	COPPER
PACKAGE MASS	0.5g