SIEMENS

3.3V 4M x 4-Bit Dynamic RAM

HYB3116400BJ/BT(L) -50/-60/-70
HYB3117400BJ/BT(L) -50/-60/-70

Advanced Information

- 4 194 304 words by 4-bit organization
- 0 to 70 °C operating temperature
- Performance:

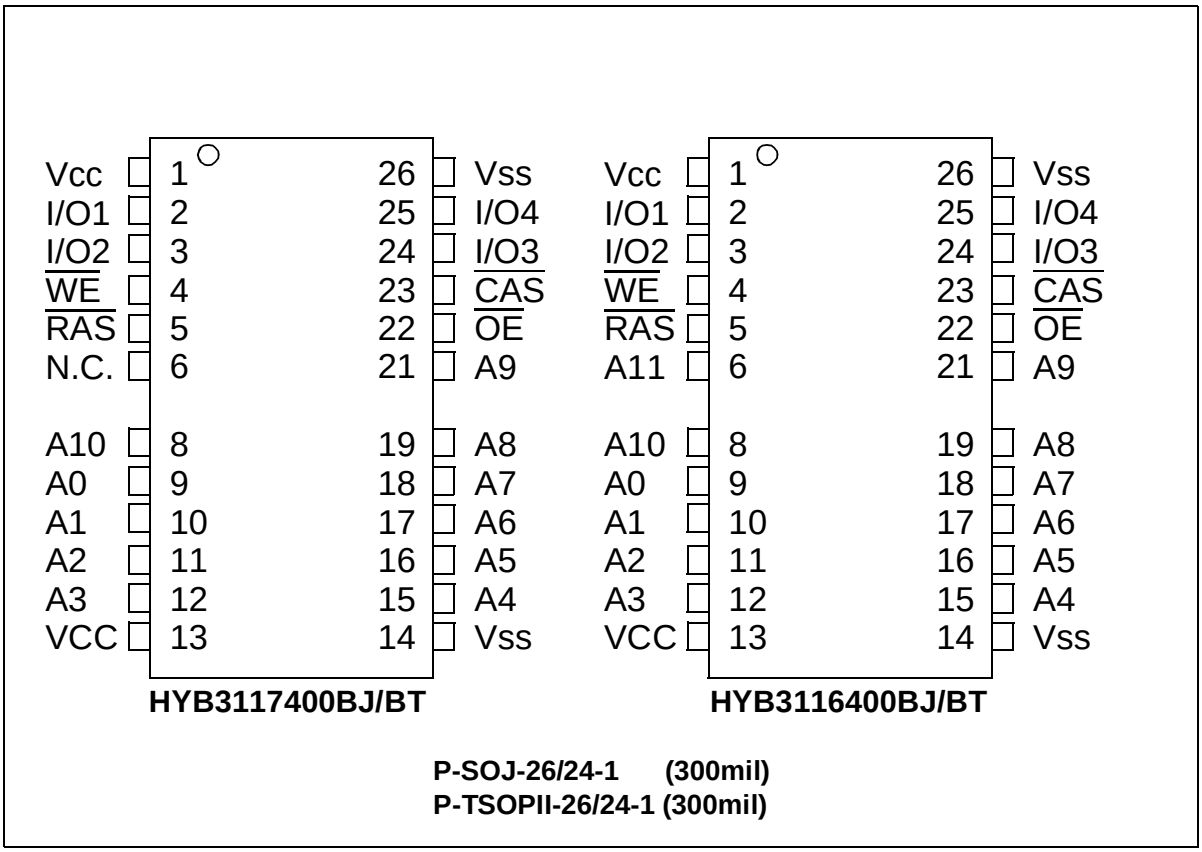
		-50	-60	-70	
t_{RAC}	$\overline{RAS}$ access time	50	60	70	ns
t_{CAC}	$\overline{CAS}$ access time	13	15	20	ns
t_{AA}	Access time from address	25	30	35	ns
t_{RC}	Read/Write cycle time	90	110	130	ns
t_{PC}	Fast page mode cycle time	35	40	45	ns

- Single + 3.3 V (± 0.3V) supply
- Low power dissipation
  max. 396 active mW (HYB3117400BJ/BT-50)
  max. 363 active mW (HYB3117400BJ/BT-60)
  max. 330 active mW (HYB3117400BJ/BT-70)
  max. 360 active mW (HYB3116400BJ/BT-50)
  max. 324 active mW (HYB3116400BJ/BT-60)
  max. 288 active mW (HYB3116400BJ/BT-70)
  7.2 mW standby (LV-TTL)
  3.6 mW standby (LV-CMOS)
  720 µW standby for L-version
- Output unlatched at cycle end allows two-dimensional chip selection
- Read, write, read-modify-write, $\overline{CAS}$-before-$\overline{RAS}$ refresh, $\overline{RAS}$-only refresh, hidden refresh, Self Refresh and test mode
- Fast page mode capability
- All inputs, outputs and clocks fully TTL-compatible
- 2048 refresh cycles / 32 ms for HYB3117400
  4096 refresh cycles / 64 ms for HYB3116400
- Plastic Package: P-SOJ-26/24-1 (300 mil)
  P-TSOPII-26/24-1 (300mil)

The HYB 3116(7)400BJ/BT is a 16MBit dynamic RAM organized as 4194304 words by 4-bits. The HYB 3116(7)400BJ/BT utilizes a submicron CMOS silicon gate process technology, as well as advanced circuit techniques to provide wide operating margins, both internally and for the system user. Multiplexed address inputs permit the HYB 3116(7)400BJ/BT to be packaged in a standard SOJ 26/24 300 mil or TSOPII-26/24 300 mil wide plastic package. These packages provide high system bit densities and are compatible with commonly used automatic testing and insertion equipment. System-oriented features include single + 3.3 V (± 0.3 V) power supply, direct interfacing with high-performance logic device families.The HYB3116400BTL parts have a very low power „sleep mode“ supported by Self Refresh.

Ordering Information

Type	Ordering Code	Package	Descriptions
HYB 3117400BJ-50		P-SOJ-26/24-1 300 mil	DRAM (access time 50 ns)
HYB 3117400BJ-60		P-SOJ-26/24-1 300 mil	DRAM (access time 60 ns)
HYB 3117400BJ-70		P-SOJ-26/24-1 300 mil	DRAM (access time 70 ns)
HYB 3117400BT-50		P-TSOPII-26/24-1 300 mil	DRAM (access time 50 ns)
HYB 3117400BT-60		P-TSOPII-26/24-1 300 mil	DRAM (access time 60 ns)
HYB 3117400BT-70		P-TSOPII-26/24-1 300 mil	DRAM (access time 70 ns)
HYB 3116400BJ-50		P-SOJ-26/24-1 300 mil	DRAM (access time 50 ns)
HYB 3116400BJ-60		P-SOJ-26/24-1 300 mil	DRAM (access time 60 ns)
HYB 3116400BJ-70		P-SOJ-26/24-1 300 mil	DRAM (access time 70 ns)
HYB 3116400BT-50		P-TSOPII-26/24-1 300 mil	DRAM (access time 50 ns)
HYB 3116400BT-60		P-TSOPII-26/24-1 300 mil	DRAM (access time 60 ns)
HYB 3116400BT-70		P-TSOPII-26/24-1 300 mil	DRAM (access time 70 ns)
HYB 3116400BTL-50		P-TSOPII-26/24-1 300 mil	LP-DRAM (access time 50 ns)
HYB 3116400BTL-60		P-TSOPII-26/24-1 300 mil	LP-DRAM (access time 60 ns)
HYB 3116400BTL-70		P-TSOPII-26/24-1 300 mil	LP-DRAM (access time 70 ns)

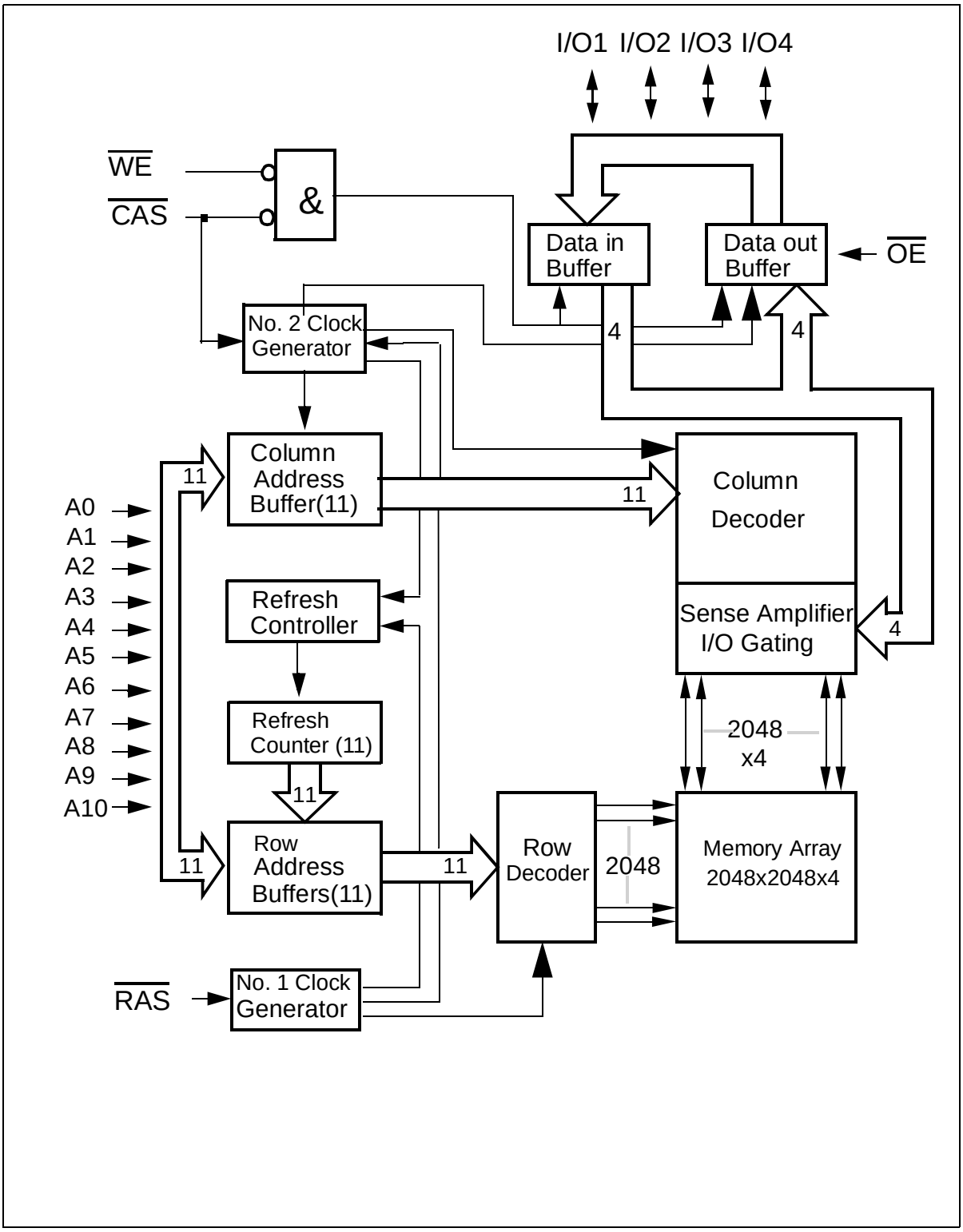


P-SOJ-26/24-1 (300mil)
P-TSOPII-26/24-1 (300mil)

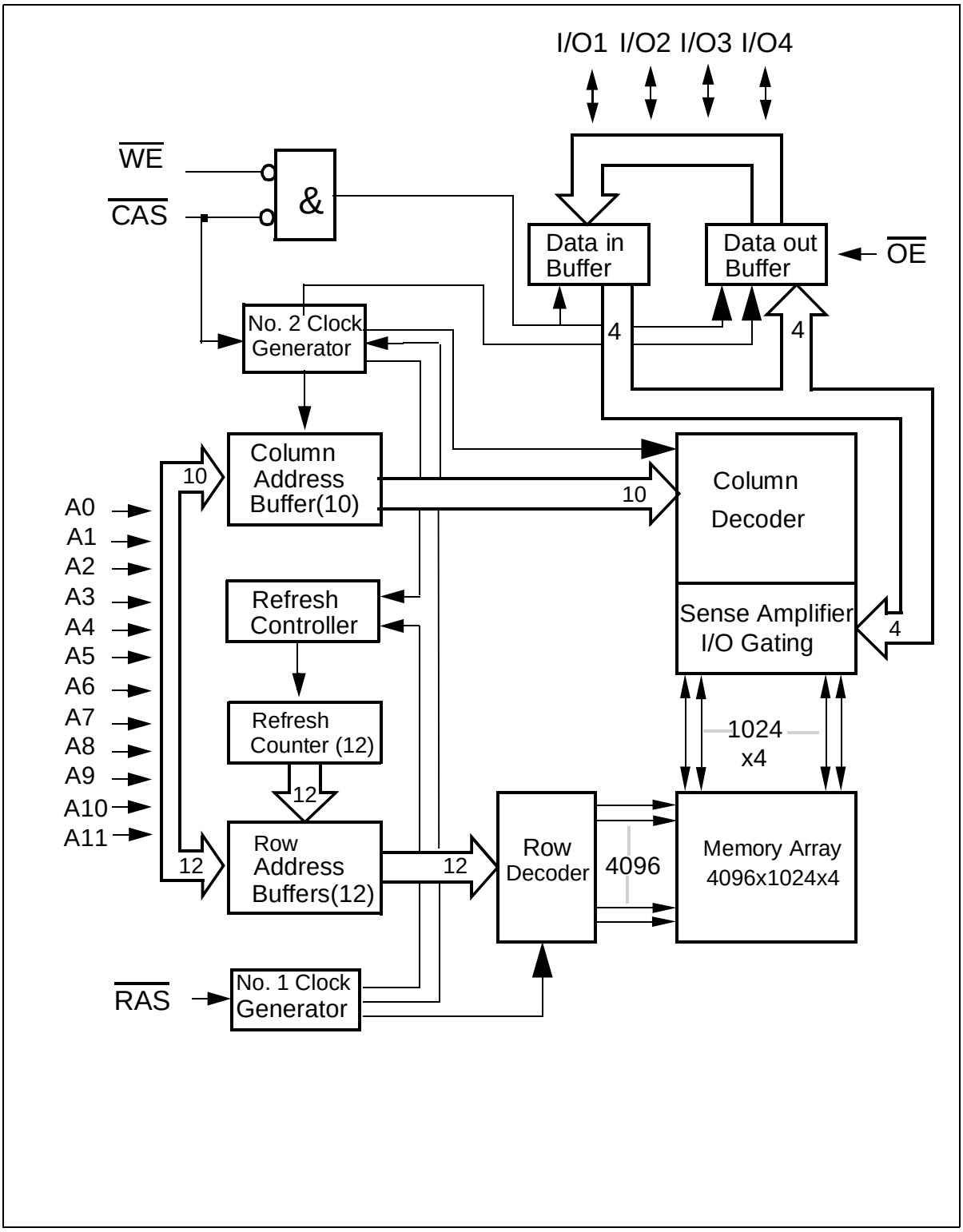
Pin Configuration

Pin Names

A0 to A10	Row & Column Address Inputs for HYB3117400
A0 to A11	Row Address Inputs for HYB3116400
A0 to A9	Column Address Inputs for HYB3116400
$\overline{RAS}$	Row Address Strobe
$\overline{OE}$	Output Enable
I/O1 -I/O4	Data Input/Output
$\overline{CAS}$	Column Address Strobe
$\overline{WE}$	Read/Write Input
V_{CC}	Power Supply (+ 3.3 V)
V_{SS}	Ground (0 V)
N.C.	not connected



Block Diagram for HYB3117400



Block Diagram for HYB3116400

Absolute Maximum Ratings

Operating temperature range .....0 to 70 °C
Storage temperature range.....– 55 to 150 °C
Input/output voltage .....-0.5 to min(Vcc+0.5, 4.6) V
Power supply voltage.....- 0.5 V to 4.6 V
Power dissipation..... 0.5 W
Data out current (short circuit) ..... 50 mA

Note:

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage of the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics (values in brackets for HYB3117400)
T_A = 0 to 70 °C, V_{SS} = 0 V, V_{CC} = 3.3 V ± 0.3 V, t_T = 5 ns

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Input high voltage	V_{IH}	2.0	Vcc+0.5	V	1)
Input low voltage	V_{IL}	– 0.5	0.8	V	1)
TTL Output high voltage (I_{OUT} = – 2 mA)	V_{OH}	2.4	–	V	1)
TTL Output low voltage (I_{OUT} = 2 mA)	V_{OL}	–	0.4	V	1)
CMOS Output high voltage (I_{OUT} = –100 uA)	V_{OH}	VCC-0.2	–	V	
CMOS Output low voltage (I_{OUT} = 100 uA)	V_{OL}	–	0.2	V	
Input leakage current (0 V ≤ V_{IH} ≤ Vcc + 0.3V, all other pins = 0 V)	$I_{I(L)}$	– 10	10	µA	1)
Output leakage current (DO is disabled, 0 V ≤ V_{OUT} ≤ Vcc + 0.3V)	$I_{O(L)}$	– 10	10	µA	1)
Average V_{CC} supply current: -50 ns version -60 ns version -70 ns version ($\overline{RAS}$, $\overline{CAS}$, address cycling, t_{RC} = t_{RC} min.)	I_{CC1}	 – – –	 100(120) 90 (110) 80 (100)	 mA mA mA	 2) 3) 4) 2) 3) 4) 2) 3) 4)
Standby V_{CC} supply current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC2}	–	2	mA	–

DC Characteristics (values in brackets for HYB3117400)
T_A = 0 to 70 °C, V_{SS} = 0 V, V_{CC} = 3.3 V ± 0.3 V, t_T = 5 ns

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Average V_{CC} supply current, during $\overline{RAS}$-only refresh cycles: -50 ns version	I_{CC3}	–	100(120)	mA	2) 4)
-60 ns version		–	90 (110)	mA	2) 4)
-70 ns version		–	80 (100)	mA	2) 4)
($\overline{RAS}$ cycling: $\overline{CAS}$ = V_{IH}, t_{RC} = t_{RC} min.)					
Average V_{CC} supply current, during fast page mode: -50 ns version	I_{CC4}	–	40 (40)	mA	2) 3) 4)
-60 ns version		–	35 (35)	mA	2) 3) 4)
-70 ns version		–	30 (30)	mA	2) 3) 4)
($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, address cycling, t_{PC} = t_{PC} min.)					
Standby V_{CC} supply current ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} – 0.2 V)	I_{CC5}	–	1 200	mA µA	1) L-version
Average V_{CC} supply current, during $\overline{CAS}$-before-RAS refresh mode: -50 ns version	I_{CC6}	–	100(120)	mA	2) 4)
-60 ns version		–	90 (110)	mA	2) 4)
-70 ns version		–	80 (100)	mA	2) 4)
($\overline{RAS}$, $\overline{CAS}$ cycling, t_{RC} = t_{RC} min.)					
Average Self Refresh Current (CBR cylce with tRAS>TRASSmin., $\overline{CAS}$ held low, $\overline{WE}$=Vcc-0.2V, Address and Din=Vcc-0.2V or 0.2V)	I_{CC7}	–	1 250	mA µA	 L-version

Capacitance
T_A = 0 to 70 °C, V_{CC} = 3.3 V ± 0.3V, f = 1 MHz

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Input capacitance (A0 to A10, A11)	C_{I1}	–	5	pF
Input capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$)	C_{I2}	–	7	pF
I/O capacitance (I/O1 - I/O4)	C_{IO}	–	7	pF

AC Characteristics 5)6) 16F

T_A = 0 to 70 °C, V_{CC} = 3.3 V ± 0.3 V, t_T = 5 ns

Parameter	Symbol	Limit Values						Unit	Note
		-50		-60		-70			
		min.	max.	min.	max.	min.	max.		
common parameters									
Random read or write cycle time	t_{RC}	90	–	110	–	130	–	ns	
$\overline{RAS}$ precharge time	t_{RP}	30	–	40	–	50	–	ns	
$\overline{RAS}$ pulse width	t_{RAS}	50	10k	60	10k	70	10k	ns	
$\overline{CAS}$ pulse width	t_{CAS}	13	10k	15	10k	20	10k	ns	
Row address setup time	t_{ASR}	0	–	0	–	0	–	ns	
Row address hold time	t_{RAH}	8	–	10	–	10	–	ns	
Column address setup time	t_{ASC}	0	–	0	–	0	–	ns	
Column address hold time	t_{CAH}	10	–	15	–	15	–	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	18	37	20	45	20	50		
$\overline{RAS}$ to column address delay time	t_{RAD}	13	25	15	30	15	35	ns	
$\overline{RAS}$ hold time	t_{RSH}	13		15	–	20	–	ns	
$\overline{CAS}$ hold time	t_{CSH}	50		60	–	70	–	ns	
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5	–	5	–	5	–	ns	
Transition time (rise and fall)	t_T	3	50	3	50	3	50	ns	7
Refresh period for HYB3117400	t_{REF}	–	32	–	32	–	32	ms	
Refresh period for HYB3116400	t_{REF}	–	64	–	64	–	64	ms	
Refresh period for L-version	t_{REF}	–	256	–	256	–	256	ms	
Read Cycle									
Access time from $\overline{RAS}$	t_{RAC}	–	50	–	60	–	70	ns	8, 9
Access time from $\overline{CAS}$	t_{CAC}	–	13	–	15	–	20	ns	8, 9
Access time from column address	t_{AA}	–	25	–	30	–	35	ns	8,10
$\overline{OE}$ access time	t_{OEA}	–	13	–	15	–	20	ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	25	–	30	–	35	–	ns	
Read command setup time	t_{RCS}	0	–	0	–	0	–	ns	
Read command hold time	t_{RCH}	0	–	0	–	0	–	ns	11
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	0	–	0	–	0	–	ns	11

AC Characteristics *(cont'd)* 5)6) 16F

T_A = 0 to 70 °C, V_{CC} = 3.3 V ± 0.3 V, t_T = 5 ns

Parameter	Symbol	Limit Values						Unit	Note
		-50		-60		-70			
		min.	max.	min.	max.	min.	max.		
$\overline{CAS}$ to output in low-Z	t_{CLZ}	0	–	0	–	0	–	ns	8
Output buffer turn-off delay	t_{OFF}	0	13	0	15	0	20	ns	12
Output buffer turn-off delay from $\overline{OE}$	t_{OEZ}	0	13	0	15	0	20	ns	12
Data to $\overline{OE}$ low delay	t_{DZO}	0	–	0	–	0	–	ns	13
$\overline{CAS}$ high to data delay	t_{CDD}	13	–	15	–	20	–	ns	14
$\overline{OE}$ high to data delay	t_{ODD}	13	–	15	–	20	–	ns	14
Write Cycle									
Write command hold time	t_{WCH}	8	–	10	–	10	–	ns	
Write command pulse width	t_{WP}	8	–	10	–	10	–	ns	
Write command setup time	t_{WCS}	0	–	0	–	0	–	ns	15
Write command to $\overline{RAS}$ lead time	t_{RWL}	13	–	15	–	20	–	ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	13	–	15	–	20	–	ns	
Data setup time	t_{DS}	0	–	0	–	0	–	ns	16
Data hold time	t_{DH}	10	–	10	–	15	–	ns	16
Data to $\overline{CAS}$ low delay	t_{DZC}	0	–	0	–	0	–	ns	13
Read-Modify-Write Cycle									
Read-write cycle time	t_{RWC}	126	–	150	–	180	–	ns	
$\overline{RAS}$ to WE delay time	t_{RWD}	68	–	80	–	95	–	ns	15
$\overline{CAS}$ to $\overline{WE}$ delay time	t_{CWD}	31	–	35	–	45	–	ns	15
Column address to $\overline{WE}$ delay time	t_{AWD}	43	–	50	–	60	–	ns	15
$\overline{OE}$ command hold time	t_{OEH}	13	–	15	–	20	–	ns	
Fast Page Mode Cycle									
Fast page mode cycle time	t_{PC}	35	–	40	–	45	–	ns	
$\overline{CAS}$ precharge time	t_{CP}	10	–	10	–	10	–	ns	
Access time from $\overline{CAS}$ precharge	t_{CPA}	–	30	–	35	–	40	ns	7
$\overline{RAS}$ pulse width	t_{RAS}	50	200k	60	200k	70	200k	ns	

AC Characteristics *(cont'd)* 5)6) 16F

T_A = 0 to 70 °C, V_{CC} = 3.3 V ± 0.3 V, t_T = 5 ns

Parameter	Symbol	Limit Values						Unit	Note
		-50		-60		-70			
		min.	max.	min.	max.	min.	max.		
$\overline{CAS}$ precharge to $\overline{RAS}$ Delay	t_{RHPC}	30	–	35	–	40	–	ns	
Fast Page Mode Read-Modify-Write Cycle									
Fast page mode read-write cycle time	t_{PRWC}	71	–	80	–	95	–	ns	
$\overline{CAS}$ precharge to $\overline{WE}$	t_{CPWD}	48	–	55	–	65	–	ns	
$\overline{CAS}$-before-$\overline{RAS}$ Refresh Cycle									
$\overline{CAS}$ setup time	t_{CSR}	10	–	10	–	10	–	ns	
$\overline{CAS}$ hold time	t_{CHR}	10	–	10	–	10	–	ns	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	t_{RPC}	5	–	5	–	5	–	ns	
Write to $\overline{RAS}$ precharge time	t_{WRP}	10	–	10	–	10	–	ns	
Write hold time referenced to $\overline{RAS}$	t_{WRH}	10	–	10	–	10	–	ns	
$\overline{CAS}$-before-$\overline{RAS}$ Counter Test Cycle									
$\overline{CAS}$ precharge time	t_{CPT}	35	–	40	–	40	–	ns	
Test Mode									
$\overline{CAS}$ hold time	t_{CHRT}	30	–	30	–	30	–	ns	
Write command setup time	t_{WTS}	10	–	10	–	10	–	ns	
Write command hold time	t_{WTH}	10	–	10	–	10	–	ns	
Self Refresh Cycle									
$\overline{RAS}$ pulse width	t_{RASS}	100k	_	100k	_	100k	_	ns	17
$\overline{RAS}$ precharge time	t_{RPS}	95	_	110	_	130	_	ns	17
$\overline{CAS}$ hold time	t_{CHS}	-50	_	-50	_	-50	_	ns	17

Notes:

1) All voltages are referenced to VSS.

2) ICC1, ICC3, ICC4 and ICC6 depend on cycle rate.

3) ICC1 and ICC4 depend on output loading. Specified values are measured with the output open.

4) Address can be changed once or less while $\overline{RAS}$ = VIL. In the case of ICC4 it can be changed once or less during a fast page mode cycle (tPC).

5) An initial pause of 200 µs is required after power-up followed by 8 RAS cycles of which at least one cycle has to be a refresh cycle, before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 CAS-before-RAS initialization cycles instead of 8 RAS cycles are required.

6) AC measurements assume tT = 5 ns.

7) VIH (min.) and VIL (max.) are reference levels for measuring timing of input signals. Transition times are also measured between VIH and VIL.

8) Measured with a load equivalent to 100 pF and at Voh=2.0 V (Ioh = -2mA) , Vol=0.8V (Iol=2mA).

9) Operation within the tRCD (max.) limit ensures that tRAC (max.) can be met. tRCD (max.) is specified as a reference point only: If tRCD is greater than the specified tRCD (max.) limit, then access time is controlled by tCAC.

10) Operation within the tRAD (max.) limit ensures that tRAC (max.) can be met. tRAD (max.) is specified as a reference point only: If tRAD is greater than the specified tRAD (max.) limit, then access time is controlled by tAA.

11) Either tRCH or tRRH must be satisfied for a read cycle.

12) tOFF (max.) and tOEZ (max.) define the time at which the outputs achieve the open-circuit condition and are not referenced to output voltage levels.

13) Either tDZC or tDZO must be satisfied.

14) Either tCDD or tODD must be satisfied.

15) tWCS, tRWD, tCWD, tAWD and tCPWD are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If tWCS > tWCS (min.), the cycle is an early write cycle and the I/O pin will remain open-circuit (high impedance) through the entire cycle; if tRWD > tRWD (min.), tCWD > tCWD (min.), tAWD > tAWD (min.) and tCPWD > tCPWD (min.) , the cycle is a read-write cycle and I/O pins will contain data read from the selected cells. If neither of the above sets of conditions is satisfied, the condition of the I/O pins (at access time) is indeterminate.

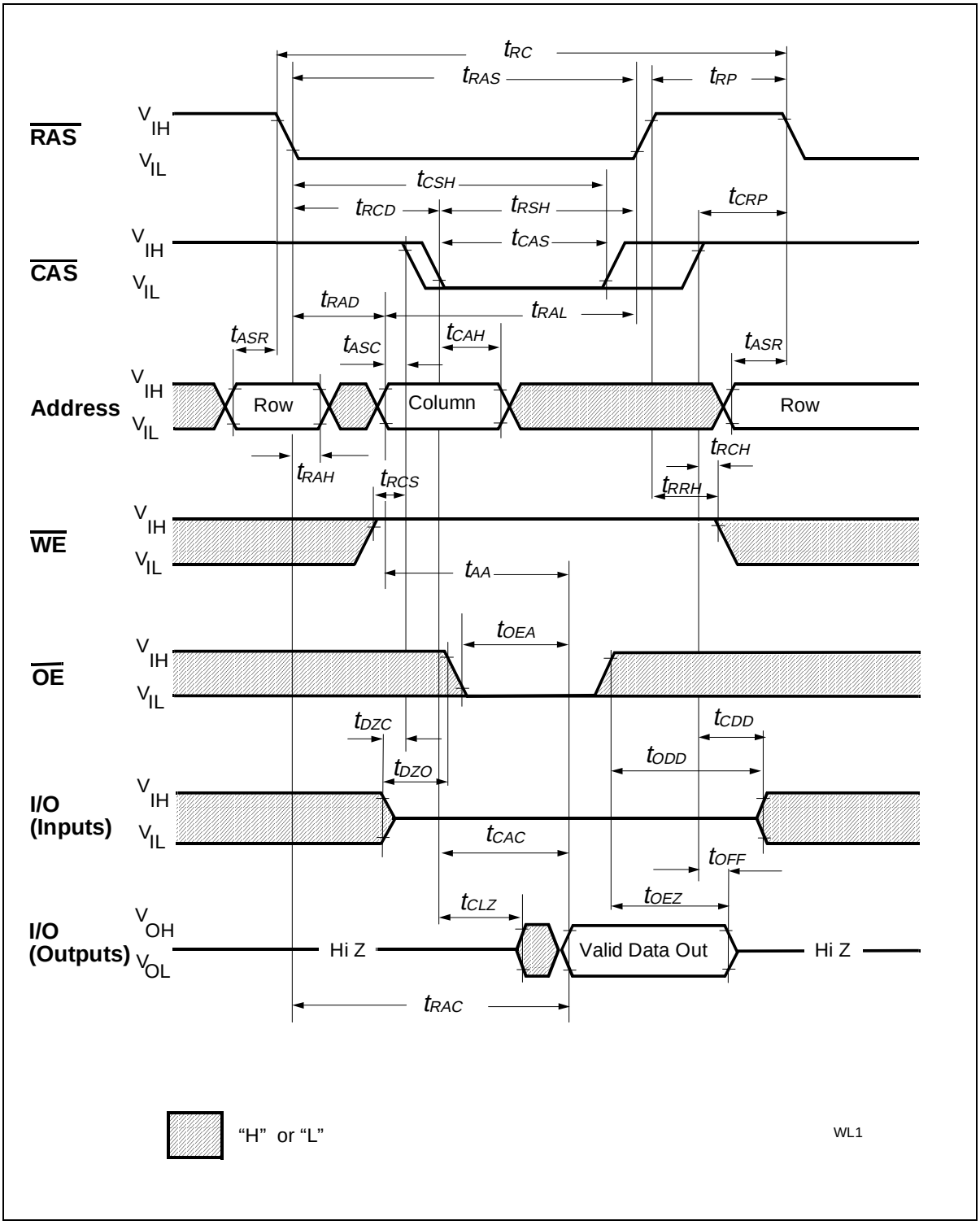
16) These parameters are referenced to the CAS leading edge in early write cycles and to the WE leading edge in read-write cycles.

17) When using Self Refresh mode, the following refresh operations must be performed to ensure proper DRAM operation:

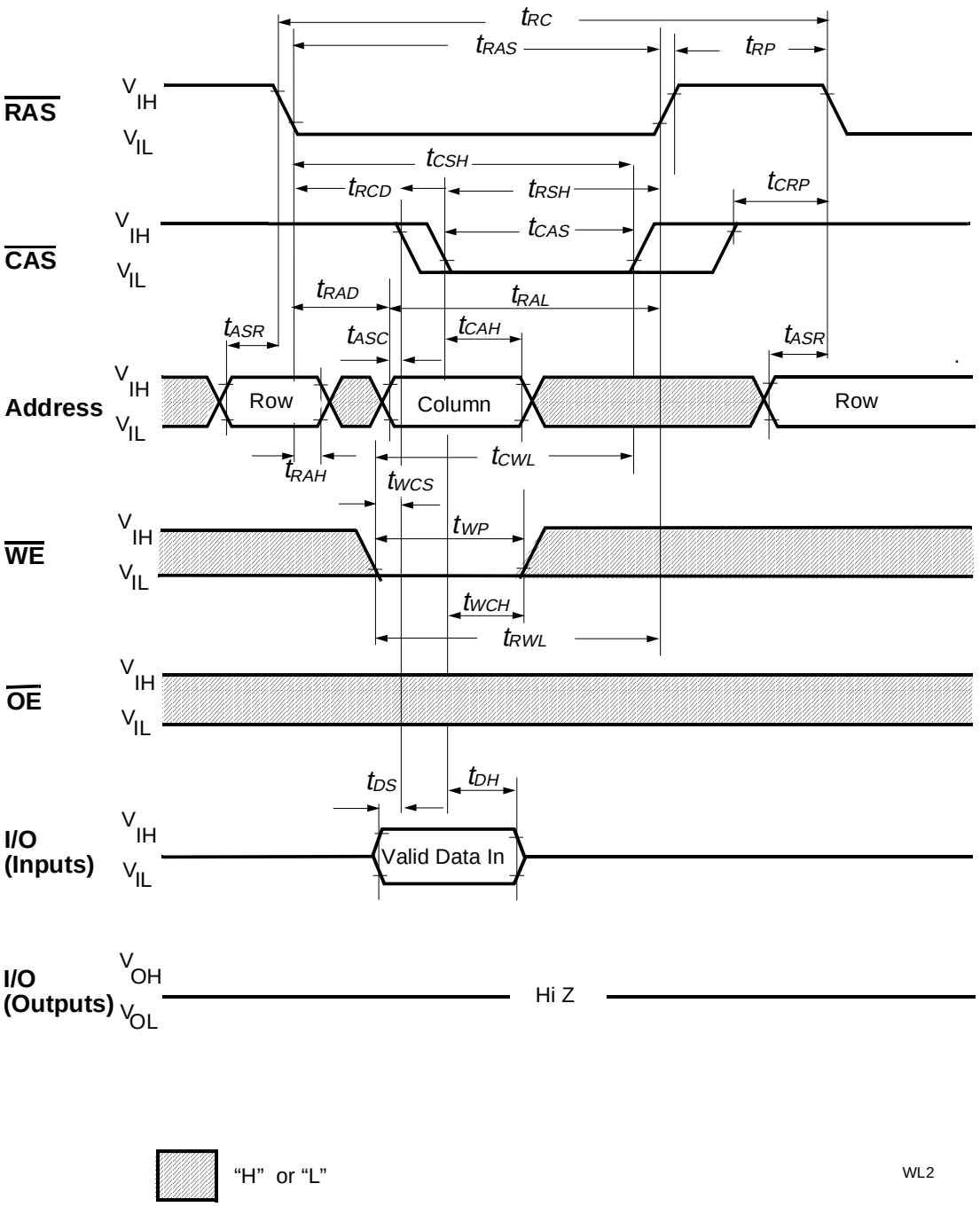
    If row addresses are being refreshed on an evenly distributed manner over the refresh interval using CBR refresh cycles, then only one CBR cycle must be performed immediately after exit from Self Refresh.

    If row addresses are being refreshed in any other manner (ROR - Distributed/Burst; or CBR-Burst) over the refresh interval, then a full set of row refreshes must be performed immediately before entry to and immediately after exit from Self Refresh.

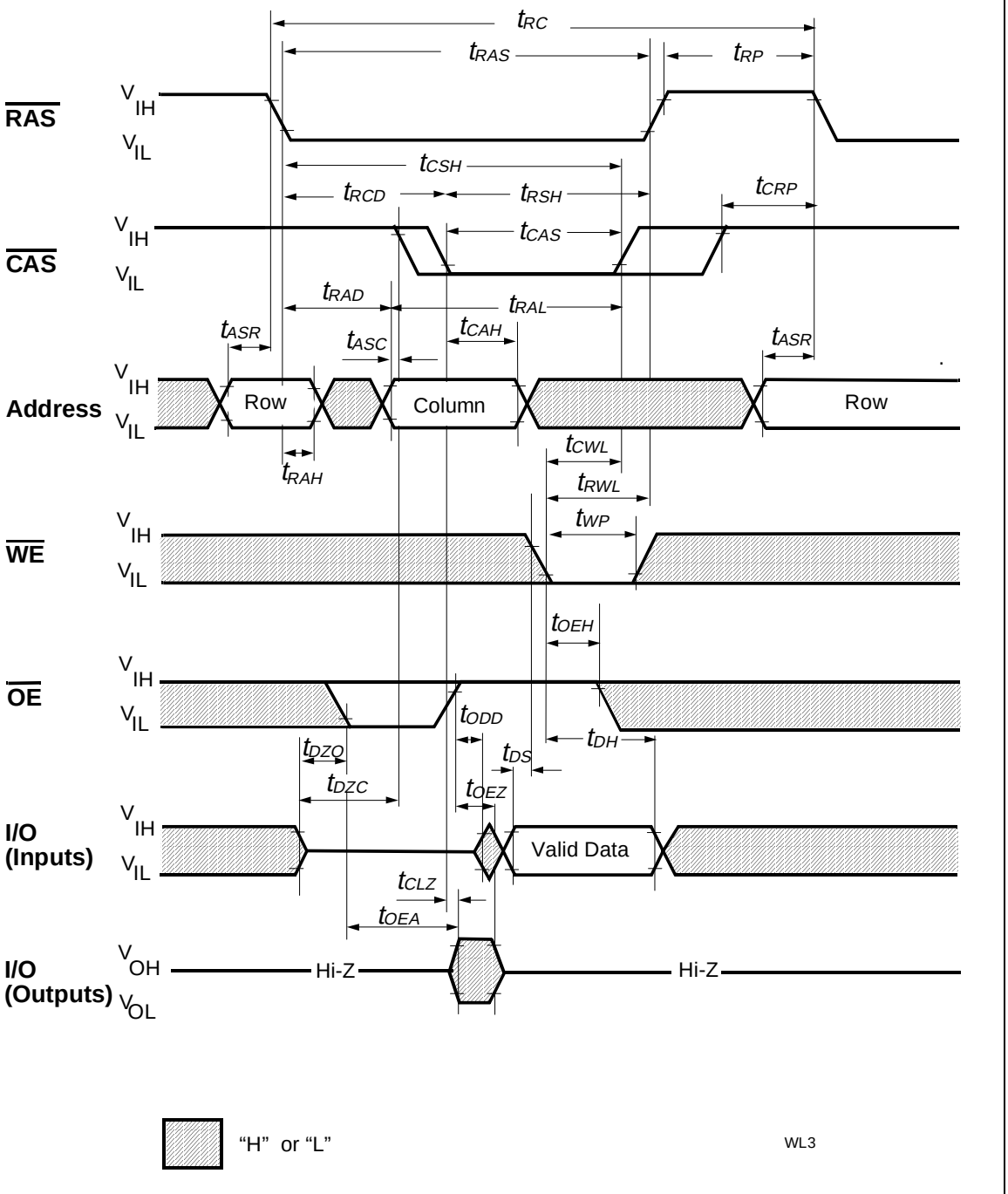
Waveforms



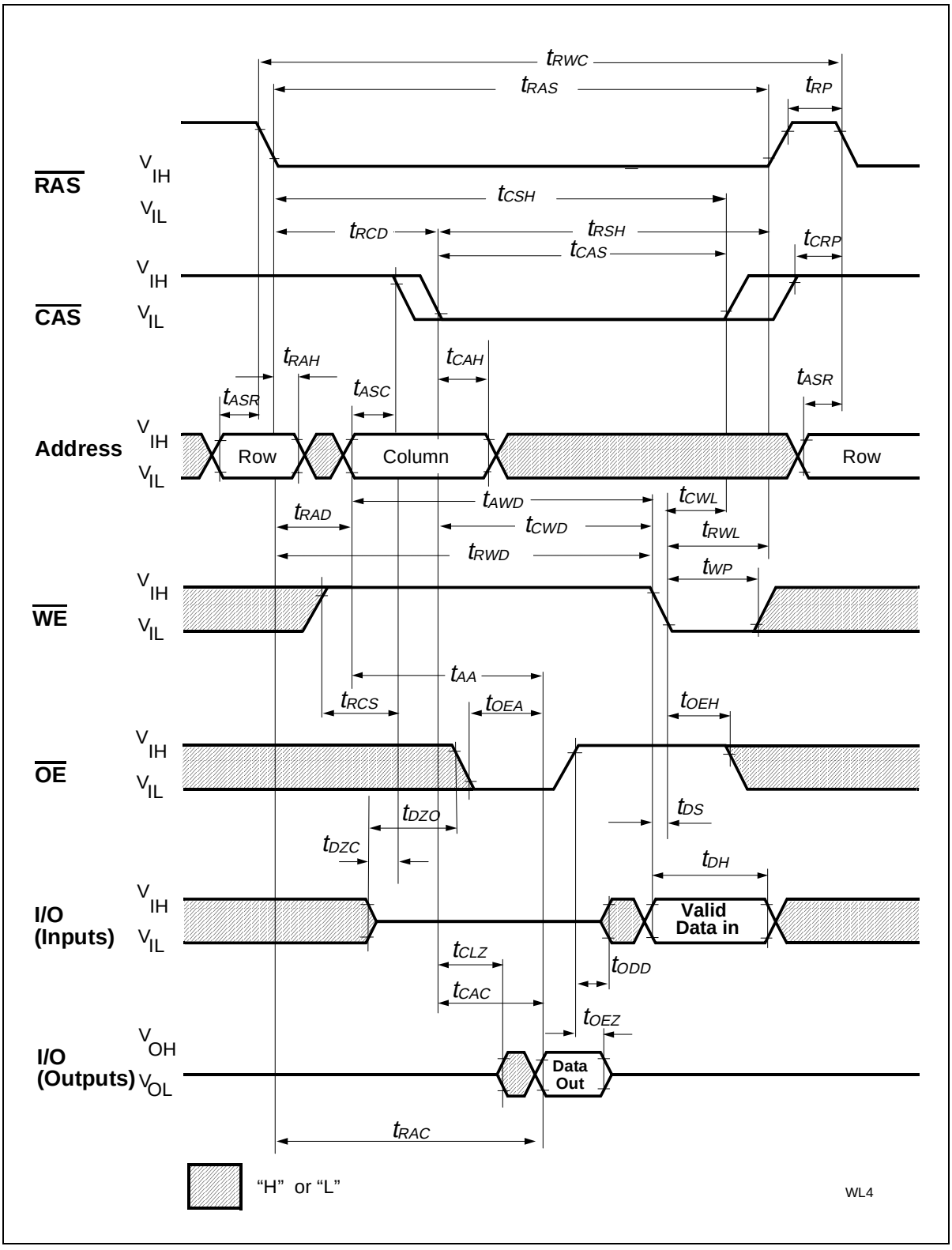
Read Cycle



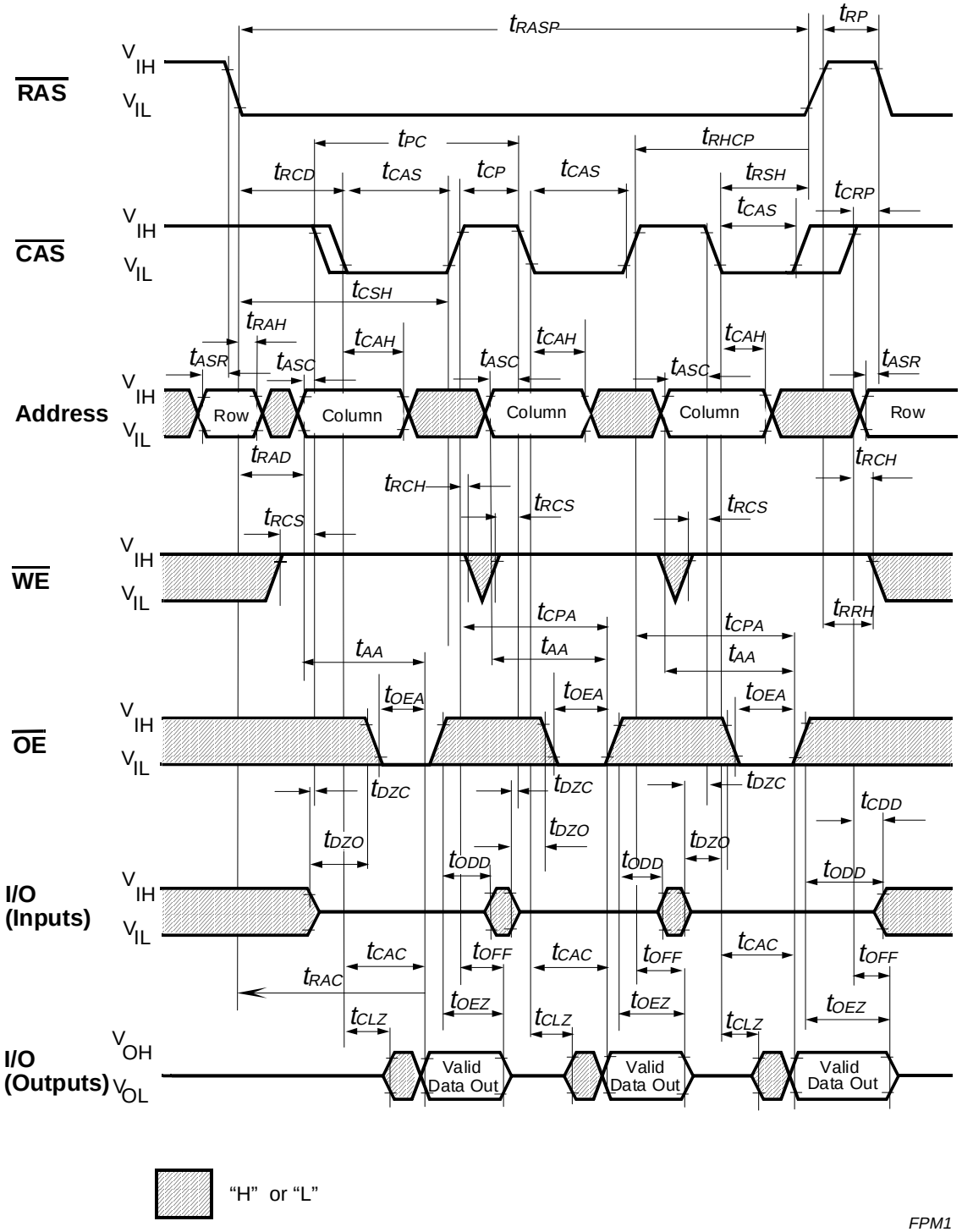
Write Cycle (Early Write)



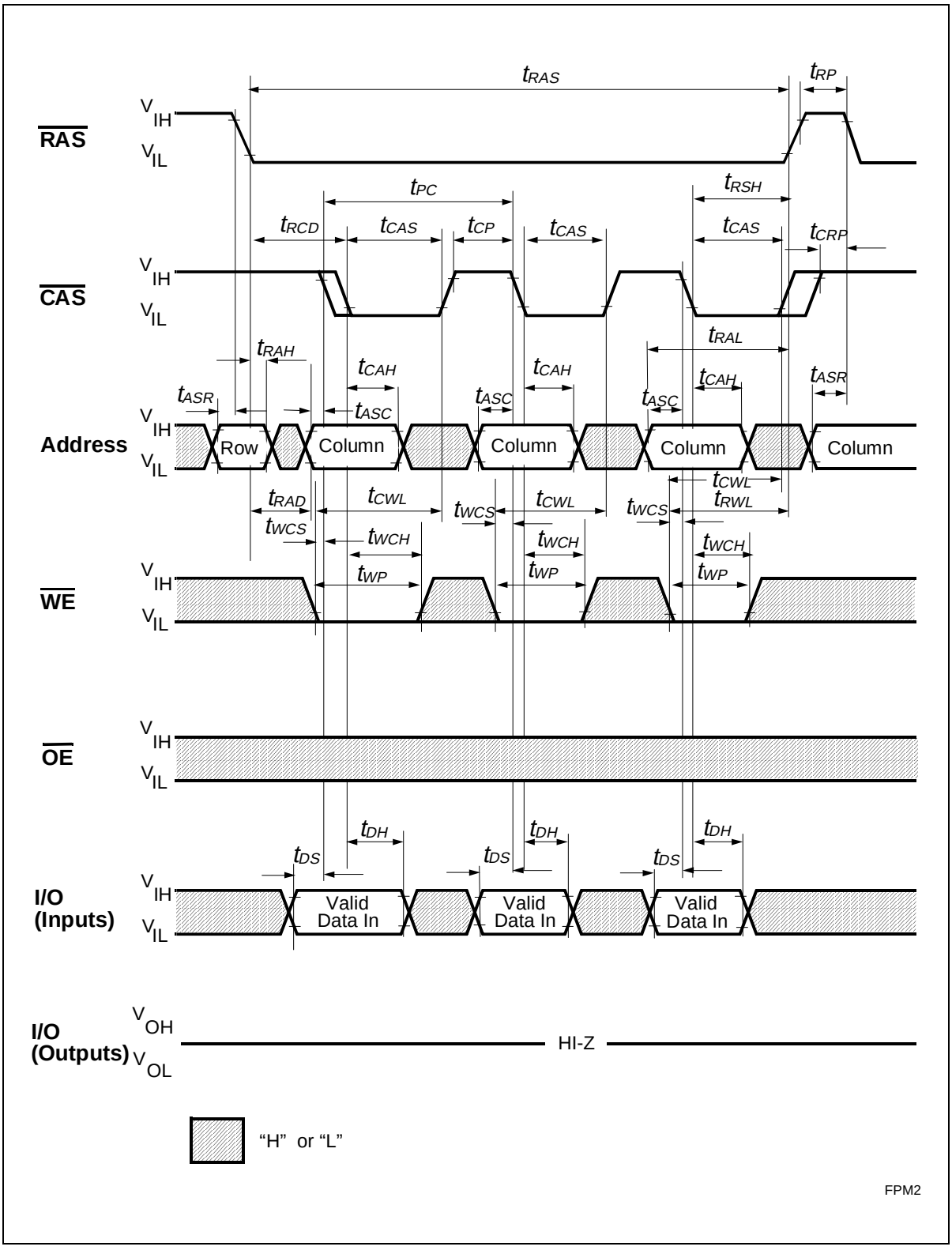
Write Cycle ($\overline{OE}$ Controlled Write)



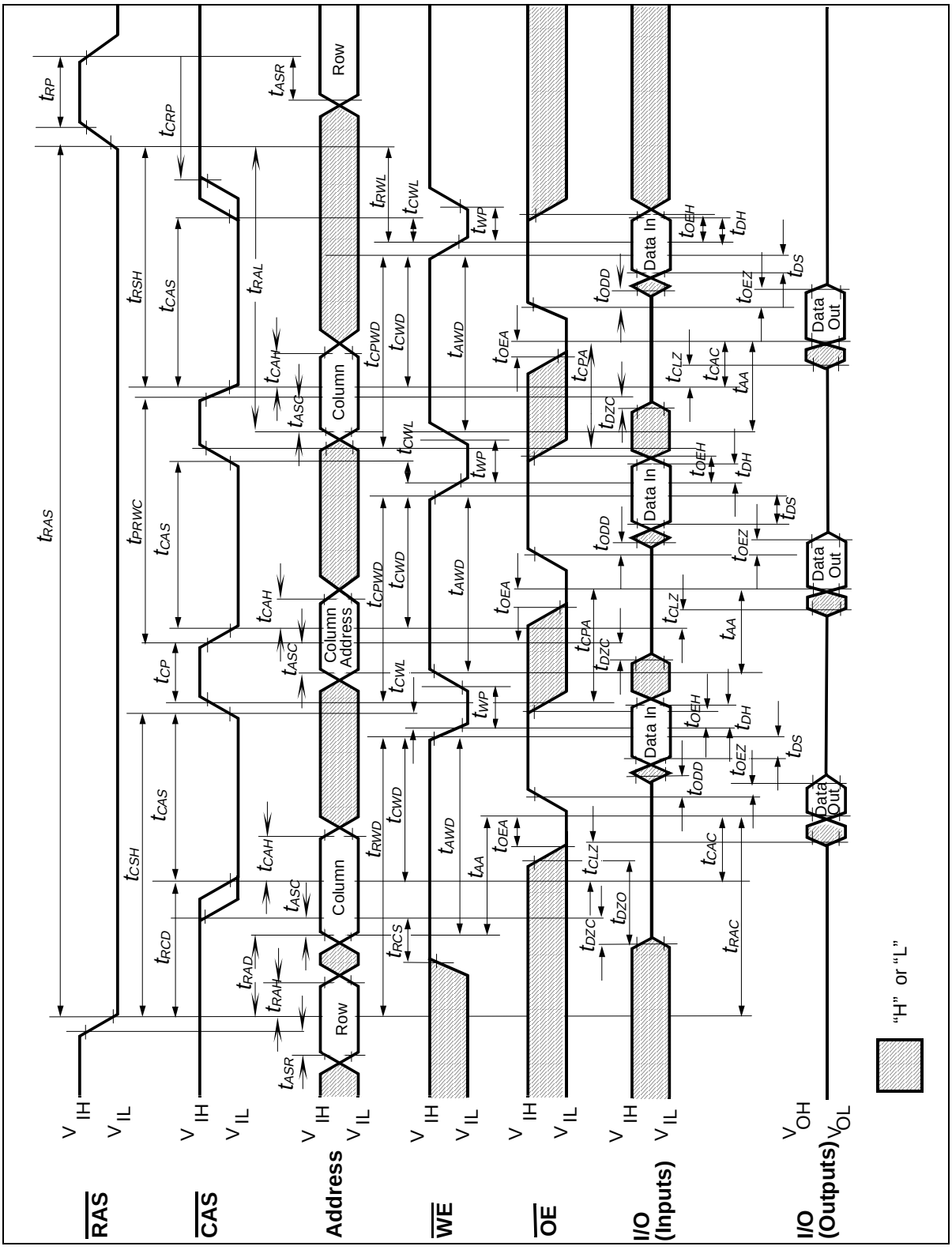
Read-Write (Read-Modify-Write) Cycle



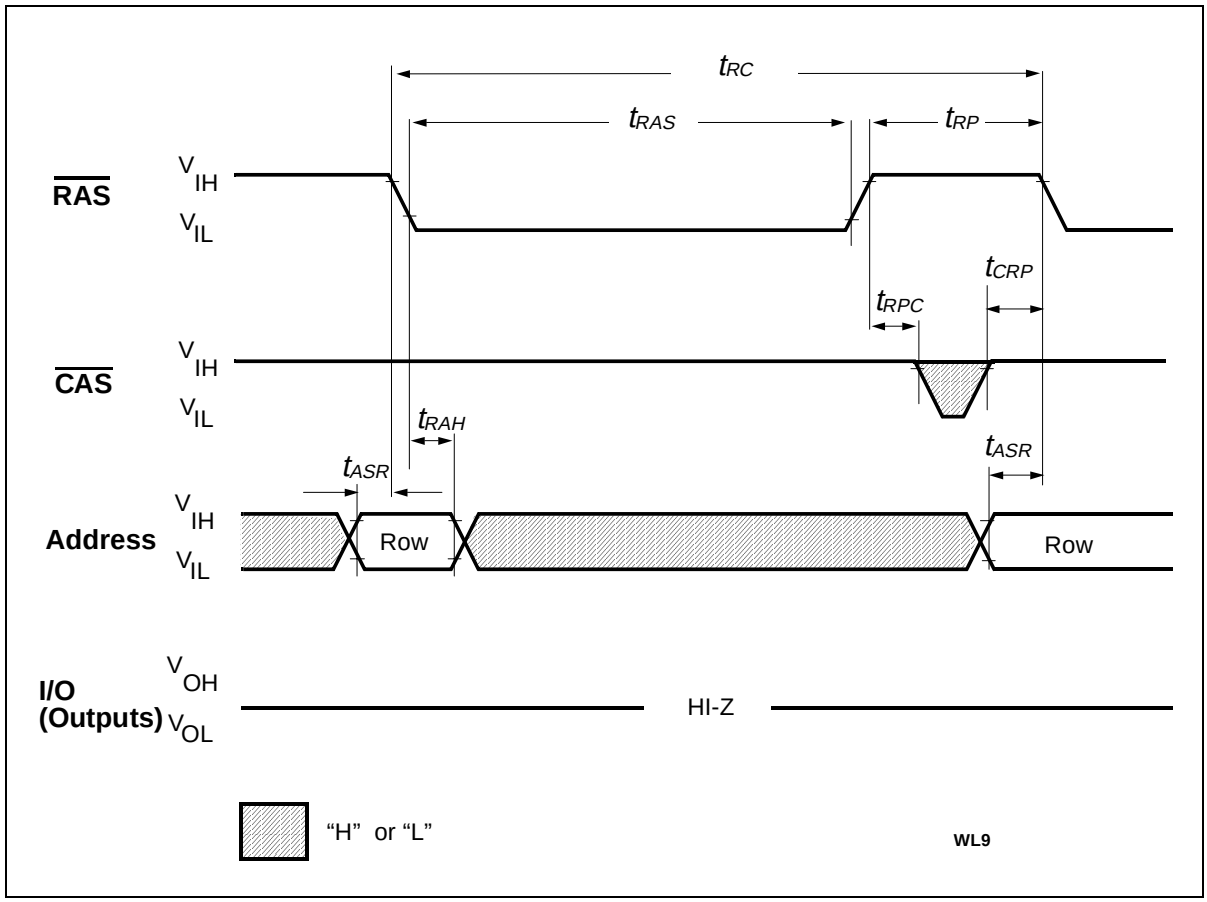
Fast Page Mode Read Cycle



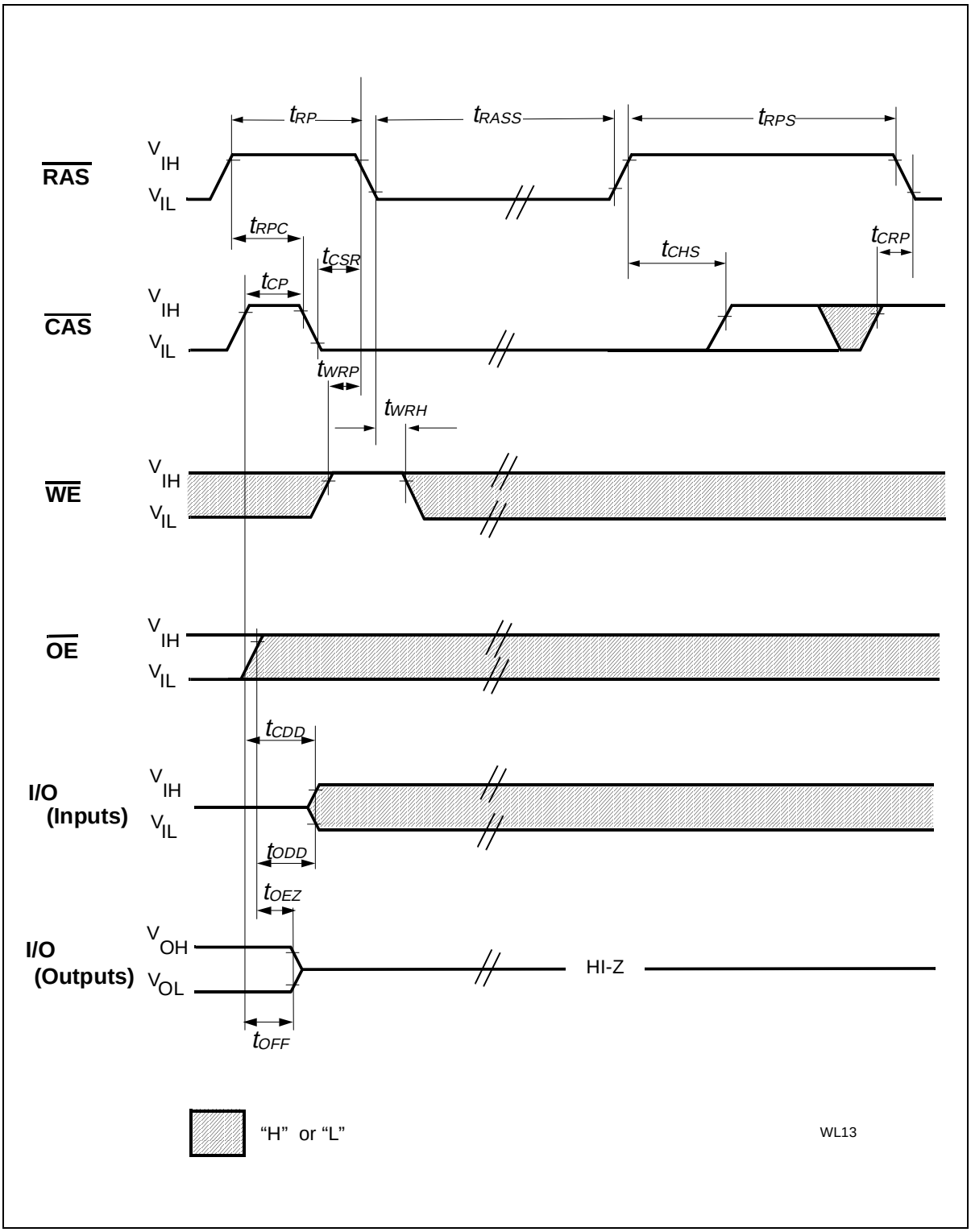
Fast Page Mode Early Write Cycle



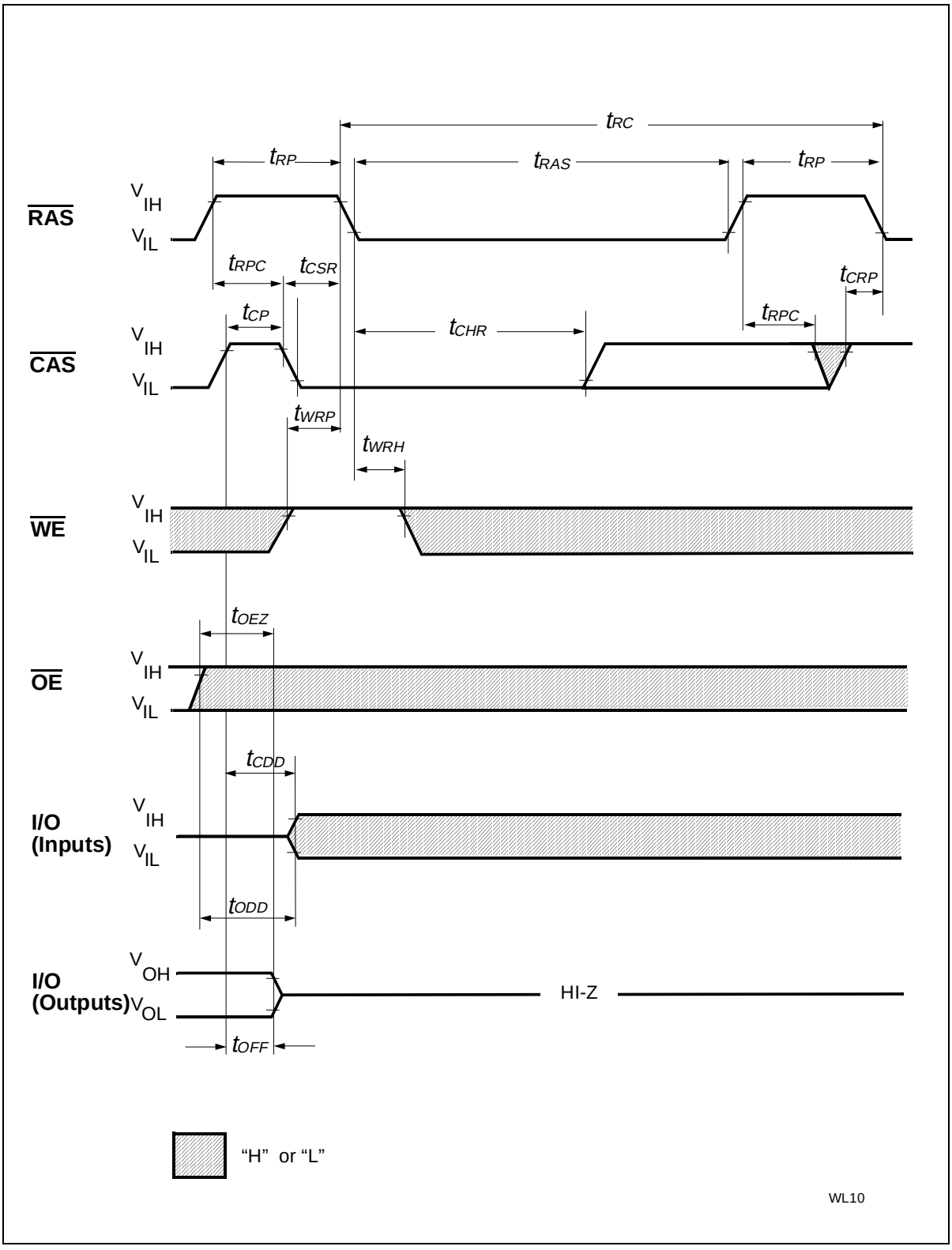
Fast Page Mode Read-Modify-Write Cycle



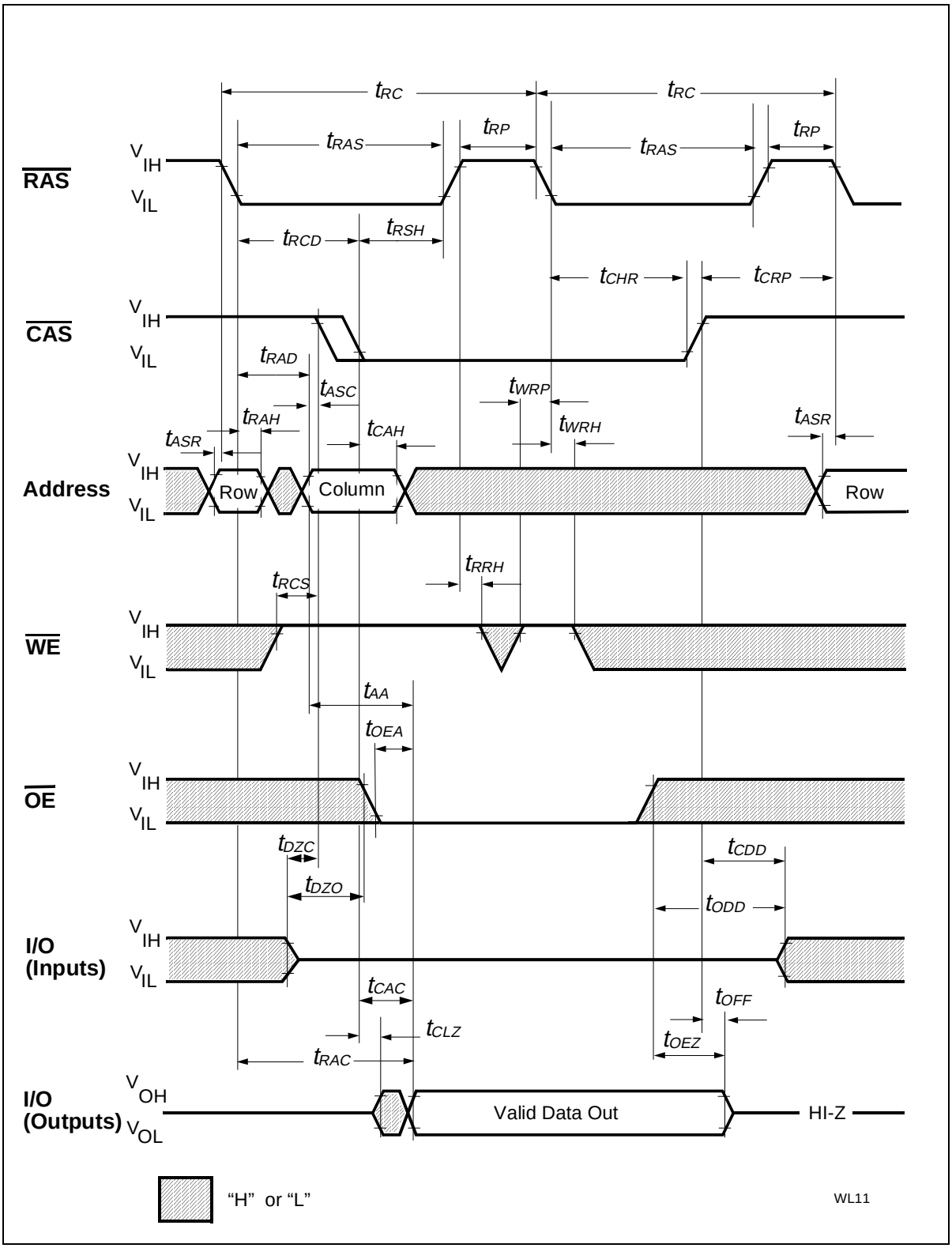
$\overline{\text{RAS}}$-Only Refresh Cycle



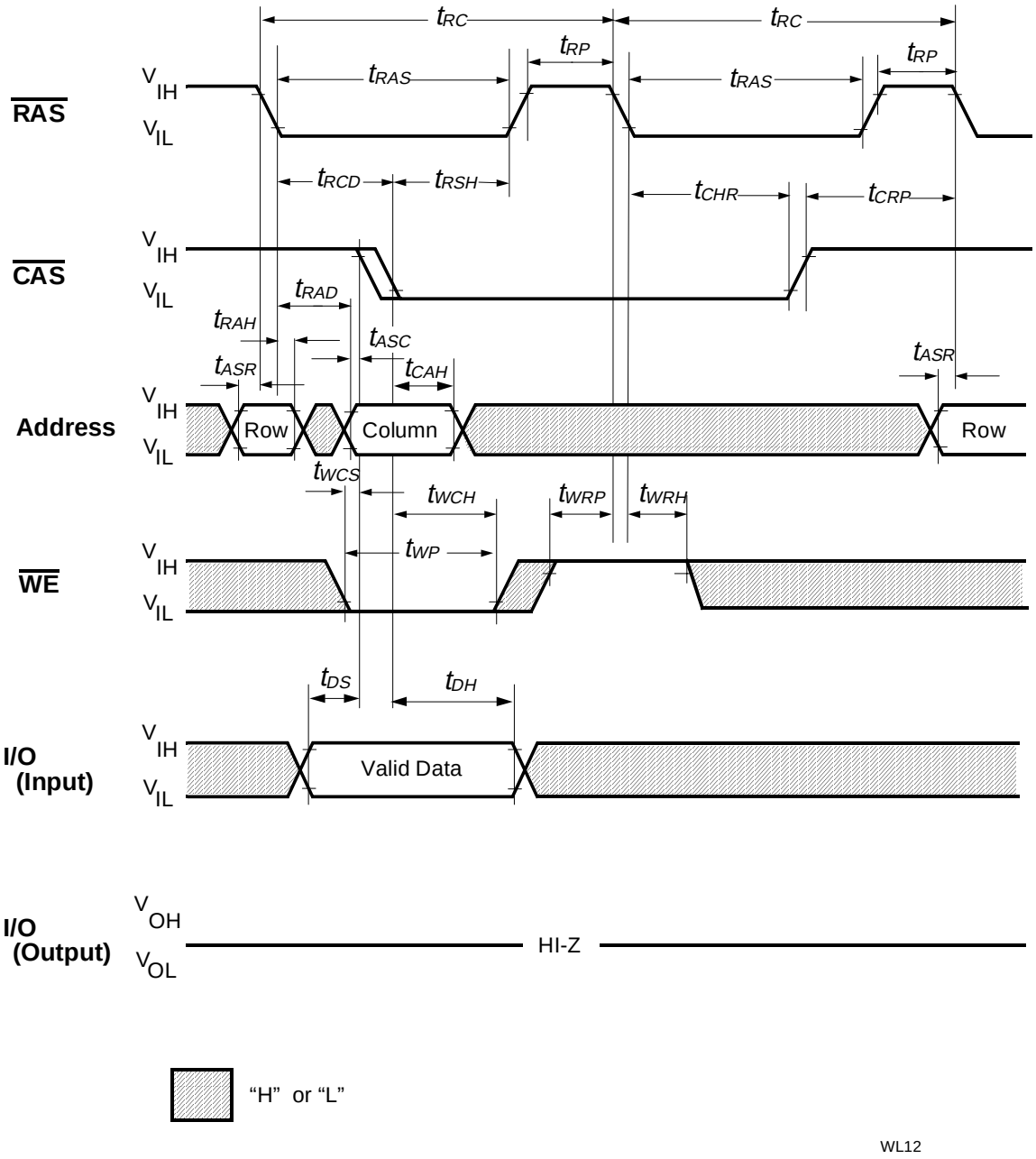
Self Refresh



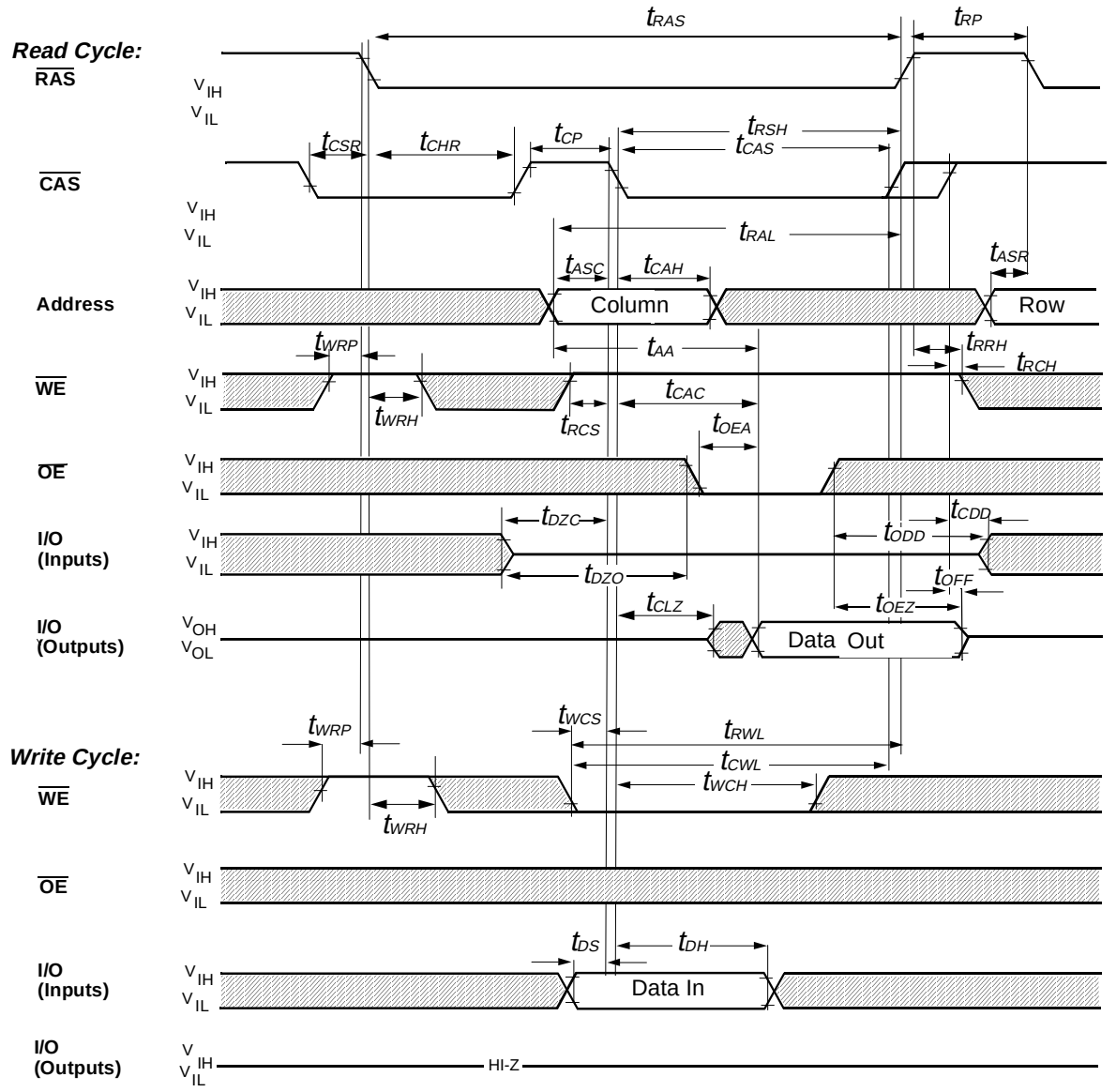
CAS-Before-RAS Refresh Cycle



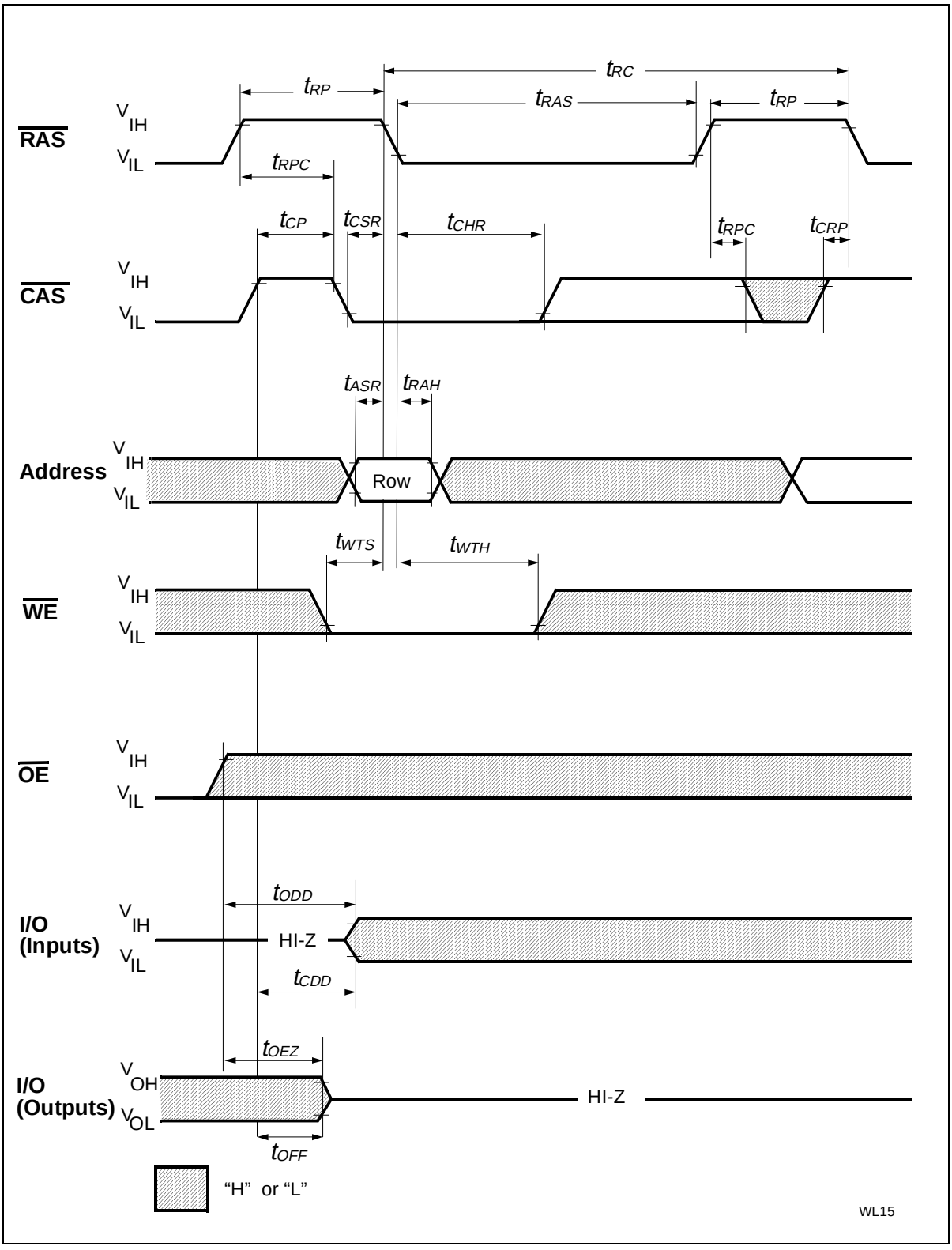
Hidden Refresh Cycle (Read)



Hidden Refresh Cycle (Early Write)



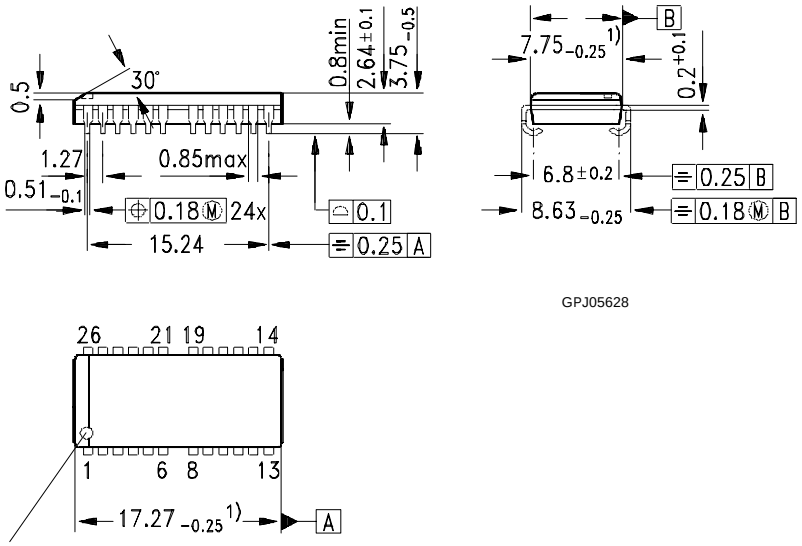
CAS-Before-RAS Refresh Counter Test Cycle



Test Mode Entry

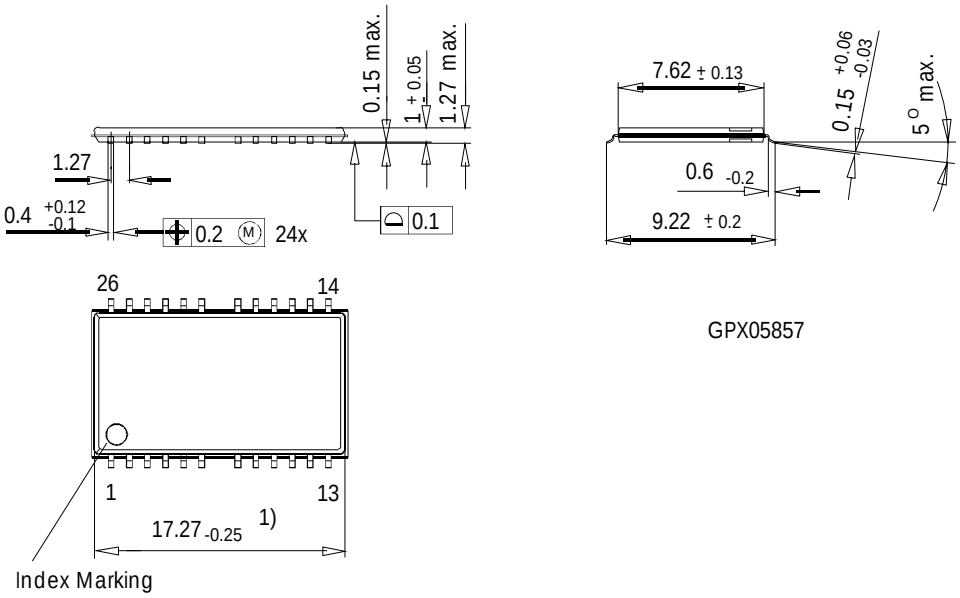
Package Outlines

Plastic Package P-SOJ-26/24-1 (300 mil)
(Small Outline J-leads, SMD)



1) Does not include plastic or metal protrusion of 0.15 max per side

Plastic Package P-TSOPII-26/24-1 (300mil)
(Thin Small Outline Package, SMD)



1) Does not include plastic or metal protrusion of 0.15 max. per side