HI5762

Dual 10-Bit, 60MSPS A/D Converter with Internal Voltage Reference

FN4318
Rev 3.00
January 22, 2010

The HI5762 is a monolithic, dual 10-bit, 60MSPS analog-to-digital converter fabricated in an advanced CMOS process. It is designed for high speed applications where integration, bandwidth and accuracy are essential. Built by combining two cores of the HI5767 single channel 10-bit 60MSPS analog-to-digital converter, the HI5762 reaches a new level of multi-channel integration. The fully pipeline architecture and an innovative input stage enable the HI5762 to accept a variety of input configurations, single-ended or fully differential. Only one external clock is necessary to drive both converters and an internal band-gap voltage reference is provided. This allows the system designer to realize an increased level of system integration resulting in decreased cost and power dissipation.

The HI5762 has excellent dynamic performance while consuming only 650mW of power at 60MSPS. The A/D only requires a single +5V power supply and encode clock. Data output latches are provided which present valid data to the output bus with a latency of 6 clock cycles.

For those customers needing dual channel 8-bit resolution, please refer to the HI5662. For single channel 10-bit applications, please refer to the HI5767.

Ordering Information

PART NUMBER	PART MARKING	TEMP. RANGE (°C)	PACKAGE	PKG. DWG. #
HI5762/6IN	HI5762/6IN	-40 to +85	44 Ld MQFP	Q44.10x10
HI5762/6INZ (Notes 1, 2)	HI5762 /6INZ	-40 to +85	44 Ld MQFP (Pb-free)	Q44.10x10
HI5762EVAL2		25	Evaluation Platform	

NOTES:

1. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
2. For Moisture Sensitivity Level (MSL), please see device information page for HI5762. For more information on MSL please see techbrief TB363.

Features

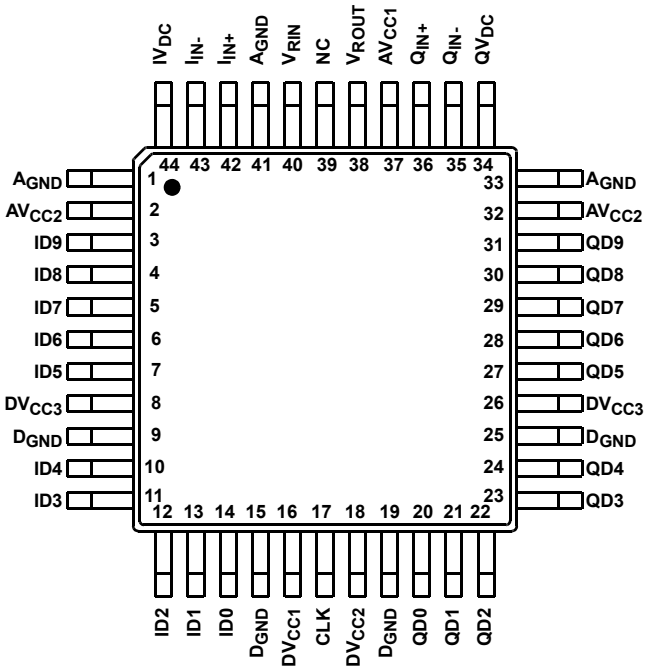
- Sampling Rate 60MSPS
- 8.8 Bits at f_{IN} = 10MHz
- Low Power at 60MSPS 650mW
- Wide Full Power Input Bandwidth 250MHz
- Excellent Channel-to-Channel Isolation . . . . . >75dB
- On-Chip Sample and Hold Amplifiers
- Internal Band-Gap Voltage Reference 2.5V
- Fully Differential or Single-Ended Analog Inputs
- Single Supply Voltage Operation . . . . . +5V
- TTL/CMOS Compatible Sampling Clock Input
- CMOS Compatible Digital Outputs 3.0V/5.0V
- Offset Binary Digital Data Output Format
- Dual 10-Bit A/D Converters on a Monolithic Chip

Applications

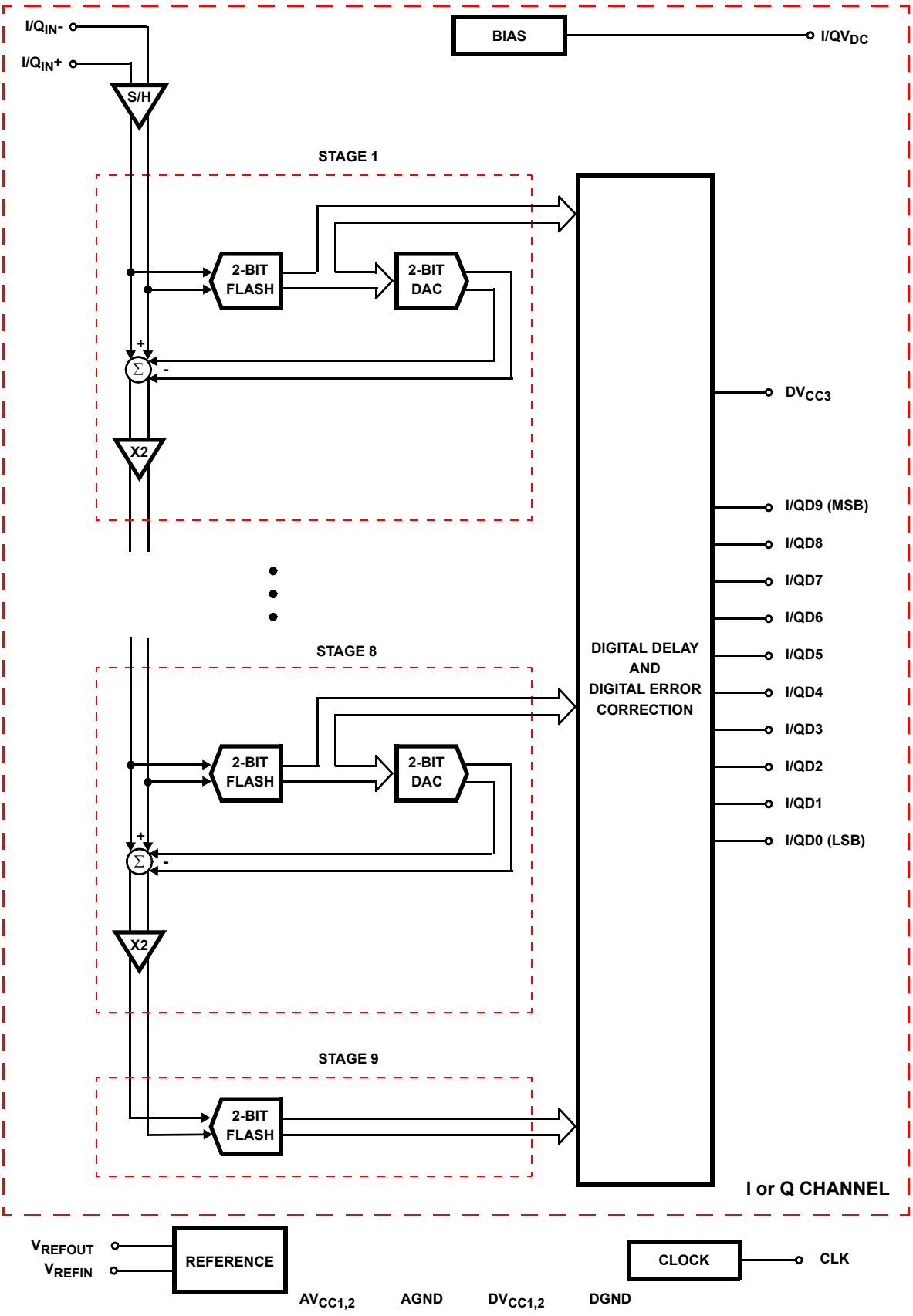
- Wireless Local Loop
- PSK and QAM I&Q Demodulators
- Medical Imaging
- High Speed Data Acquisition

Pinout

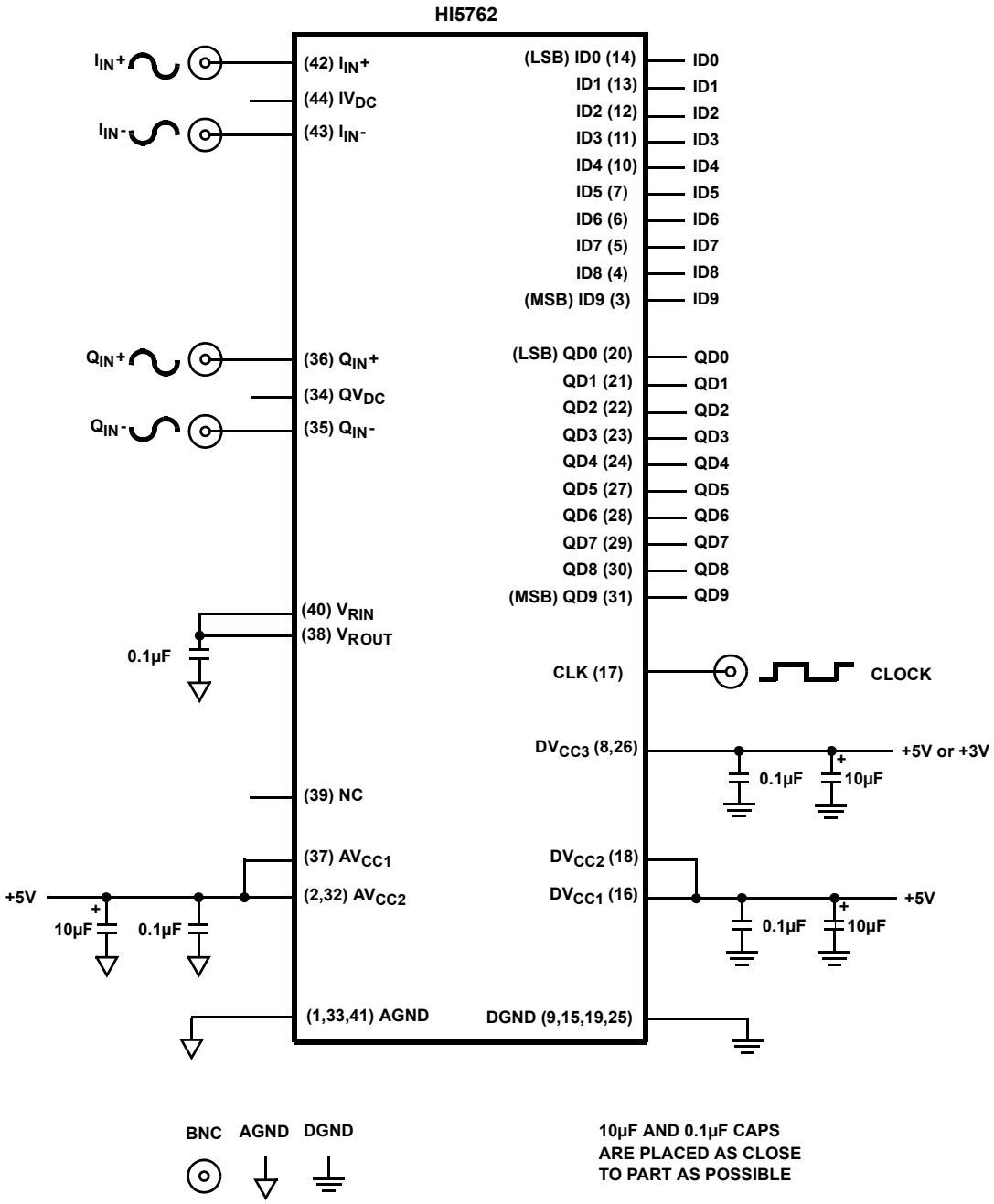
HI5762
(44 LD MQFP)
TOP VIEW



Functional Block Diagram



Typical Application Schematic



Pin Descriptions

PIN NO.	NAME	DESCRIPTION
1	A_{GND}	Analog Ground
2	AV_{CC2}	Analog Supply (+5.0V)
3	ID9	I-Channel, Data Bit 9 Output (MSB)
4	ID8	I-Channel, Data Bit 8 Output
5	ID7	I-Channel, Data Bit 7 Output
6	ID6	I-Channel Data Bit 6 Output
7	ID5	I-Channel, Data Bit 5 Output
8	DV_{CC3}	Digital Output Supply (+3.0V or +5.0V)
9	D_{GND}	Digital Ground
10	ID4	I-Channel, Data Bit 4 Output
11	ID3	I-Channel, Data Bit 3 Output
12	ID2	I-Channel, Data Bit 2 Output
13	ID1	I-Channel, Data Bit 1 Output
14	ID0	I-Channel, Data Bit 0 Output (LSB)
15	D_{GND}	Digital Ground
16	DV_{CC1}	Digital Supply (+5.0V)
17	CLK	Sample Clock Input
18	DV_{CC2}	Digital Supply (+5.0V)
19	D_{GND}	Digital Ground
20	QD0	Q-Channel, Data Bit 0 Output (LSB)
21	QD1	Q-Channel, Data Bit 1 Output
22	QD2	Q-Channel, Data Bit 2 Output
23	QD3	Q-Channel, Data Bit 3 Output

PIN NO.	NAME	DESCRIPTION
24	QD4	Q-Channel, Data Bit 4 Output
25	DGND	Digital Ground
26	DV_{CC3}	Digital Output Supply (+3.0V or +5.0V)
27	QD5	Q-Channel, Data Bit 5 Output
28	QD6	Q-Channel, Data Bit 6 Output
29	QD7	Q-Channel, Data Bit 7 Output
30	QD8	Q-Channel, Data Bit 8 Output
31	QD9	Q-Channel, Data Bit 9 Output (MSB)
32	AV_{CC2}	Analog Supply (+5.0V)
33	A_{GND}	Analog Ground
34	QV_{DC}	Q-Channel DC Bias Voltage Output
35	Q_{IN-}	Q-Channel Negative Analog Input
36	Q_{IN+}	Q-Channel Positive Analog Input
37	AV_{CC1}	Analog Supply (+5.0V)
38	V_{ROUT}	+2.5V Reference Voltage Output
39	NC	No Connect
40	V_{RIN}	+2.5V Reference Voltage Input
41	A_{GND}	Analog Ground
42	I_{IN+}	I-Channel Positive Analog Input
43	I_{IN-}	I-Channel Negative Analog Input
44	IV_{DC}	I-Channel DC Bias Voltage Output

Absolute Maximum Ratings T_A = +25°C

Supply Voltage, AV_{CC} or DV_{CC} to AGND or DGND 6V
DGND to AGND 0.3V
Digital I/O Pins . . . . . DGND to DV_{CC}
Analog I/O Pins . . . . . AGND to AV_{CC}

Operating Conditions

Temperature Range . . . . . .-40°C to +85°C

Thermal Information

Thermal Resistance (Typical, Note 3)	θ_{JA} (°C/W)
44 Ld MQFP Package	75

Maximum Junction Temperature . . . . . .+150°C
Maximum Storage Temperature Range . . . . . -65°C to +150°C
Pb-Free Reflow Profile. . . . . .see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTE:

3. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.

Electrical Specifications

$AV_{CC1,2}$ = $DV_{CC1,2}$ = +5.0V, DV_{CC3} = +3.0V; V_{RIN} = 2.50V; f_S = 60MSPS at 50% Duty Cycle; C_L = 10pF; T_A = +25°C; Differential Analog Input; Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
ACCURACY					
Resolution		10	-	-	Bits
Integral Linearity Error, INL	f_{IN} = 10MHz	-	±2	-	LSB
Differential Linearity Error, DNL (Guaranteed No Missing Codes)	f_{IN} = 10MHz	-	±0.4	±1.0	LSB
Offset Error, V_{OS}	f_{IN} = DC	-40	-	+40	LSB
Full Scale Error, FSE	f_{IN} = DC	-	4	-	LSB
DYNAMIC CHARACTERISTICS					
Minimum Conversion Rate	No Missing Codes	-	1	-	MSPS
Maximum Conversion Rate	No Missing Codes	60	-	-	MSPS
Effective Number of Bits, ENOB	f_{IN} = 10MHz	8.4	8.8	-	Bits
Signal to Noise and Distortion Ratio, SINAD = $\frac{\text{RMS Signal}}{\text{RMS Noise + Distortion}}$	f_{IN} = 10MHz	-	54.7	-	dB
Signal to Noise Ratio, SNR = $\frac{\text{RMS Signal}}{\text{RMS Noise}}$	f_{IN} = 10MHz	-	54.7	-	dB
Total Harmonic Distortion, THD	f_{IN} = 10MHz	-	-68	-	dBc
2nd Harmonic Distortion	f_{IN} = 10MHz	-	-70	-	dBc
3rd Harmonic Distortion	f_{IN} = 10MHz	-	-73	-	dBc
Spurious Free Dynamic Range, SFDR	f_{IN} = 10MHz	-	70	-	dBc
Intermodulation Distortion, IMD	f_1 = 1MHz, f_2 = 1.02MHz	-	64	-	dBc
I/Q Channel Crosstalk		-	-75	-	dBc
I/Q Channel Offset Match		-	10	-	LSB
I/Q Channel Full Scale Error Match		-	10	-	LSB
Transient Response	(Note 4)	-	1	-	Cycle
Overvoltage Recovery	0.2V Overdrive (Note 4)	-	1	-	Cycle
ANALOG INPUT					
Maximum Peak-to-Peak Differential Analog Input Range (V_{IN}+ - V_{IN}-)		-	±0.5	-	V
Maximum Peak-to-Peak Single-Ended Analog Input Range		-	1.0	-	V
Analog Input Resistance, R_{IN+} or R_{IN-}	V_{IN+}, V_{IN-} = V_{REF}, DC	-	1	-	MΩ

Electrical Specifications $AV_{CC1,2}$ = $DV_{CC1,2}$ = +5.0V, DV_{CC3} = +3.0V; V_{RIN} = 2.50V; f_S = 60MSPS at 50% Duty Cycle; C_L = 10pF; T_A = +25°C; Differential Analog Input; Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Analog Input Capacitance, C_{IN+} or C_{IN-}	V_{IN+}, V_{IN-} = 2.5V, DC	-	10	-	pF
Analog Input Bias Current, I_B+ or I_B-	V_{IN+}, V_{IN-} = V_{REF-}, V_{REF+},DC (Note 4, 5)	-10	-	10	µA
Differential Analog Input Bias Current I_{BDIFF} = (I_B+ - I_B-)	(Notes 4, 5)	-0.5	-	+0.5	µA
Full Power Input Bandwidth, FPBW	(Note 4)	-	250	-	MHz
Analog Input Common Mode Voltage Range (V_{IN}+ + V_{IN}-)/2	Differential Mode (Note 4)	0.25	-	4.75	V
INTERNAL VOLTAGE REFERENCE					
Reference Output Voltage, V_{ROUT} (Loaded)		2.35	2.5	2.65	V
Reference Output Current, I_{ROUT}		-	2	4	mA
Reference Temperature Coefficient		-	-400	-	ppm/^{o}C
REFERENCE VOLTAGE INPUT					
Reference Voltage Input, V_{RIN}		-	2.5	-	V
Total Reference Resistance, R_{RIN}	with V_{RIN} = 2.5V	-	1.25	-	kΩ
Reference Current, I_{RIN}	with V_{RIN} = 2.5V	-	2	-	mA
DC BIAS VOLTAGE					
DC Bias Voltage Output, V_{DC}		-	3.0	-	V
Maximum Output Current		-	-	0.4	mA
SAMPLING CLOCK INPUT					
Input Logic High Voltage, V_{IH}	CLK	2.0	-	-	V
Input Logic Low Voltage, V_{IL}	CLK	-	-	0.8	V
Input Logic High Current, I_{IH}	CLK, V_{IH} = 5V	-10.0	-	+10.0	µA
Input Logic Low Current, I_{IL}	CLK, V_{IL} = 0V	-10.0	-	+10.0	µA
Input Capacitance, C_{IN}	CLK	-	7	-	pF
DIGITAL OUTPUTS					
Output Logic High Voltage, V_{OH}	I_{OH} = 100µA; DV_{CC3} = 5V	4.0	-	-	V
Output Logic Low Voltage, V_{OL}	I_{OL} = 100µA; DV_{CC3} = 5V	-	-	0.8	V
Output Logic High Voltage, V_{OH}	I_{OH} = 100µA; DV_{CC3} = 3V	2.4	-	-	V
Output Logic Low Voltage, V_{OL}	I_{OL} = 100µA; DV_{CC3} = 3V	-	-	0.5	V
Output Capacitance, C_{OUT}		-	7	-	pF
TIMING CHARACTERISTICS					
Aperture Delay, t_{AP}		-	5	-	ns
Aperture Jitter, t_{AJ}		-	5	-	ps_{RMS}
Data Output Hold, t_H		-	10.7	-	ns
Data Output Delay, t_{OD}		-	11.7	-	ns
Data Latency, t_{LAT}	For a Valid Sample (Note 4)	6	6	6	Cycles
Power-Up Initialization	Data Invalid Time (Note 4)	-	-	20	Cycles
Sample Clock Pulse Width (Low)	(Note 4)	7.5	8.3	-	ns
Sample Clock Pulse Width (High)	(Note 4)	7.5	8.3	-	ns
Sample Clock Duty Cycle Variation		-	±5	-	%
POWER SUPPLY CHARACTERISTICS					
Analog Supply Voltage, AV_{CC}	(Note 4)	4.75	5.0	5.25	V

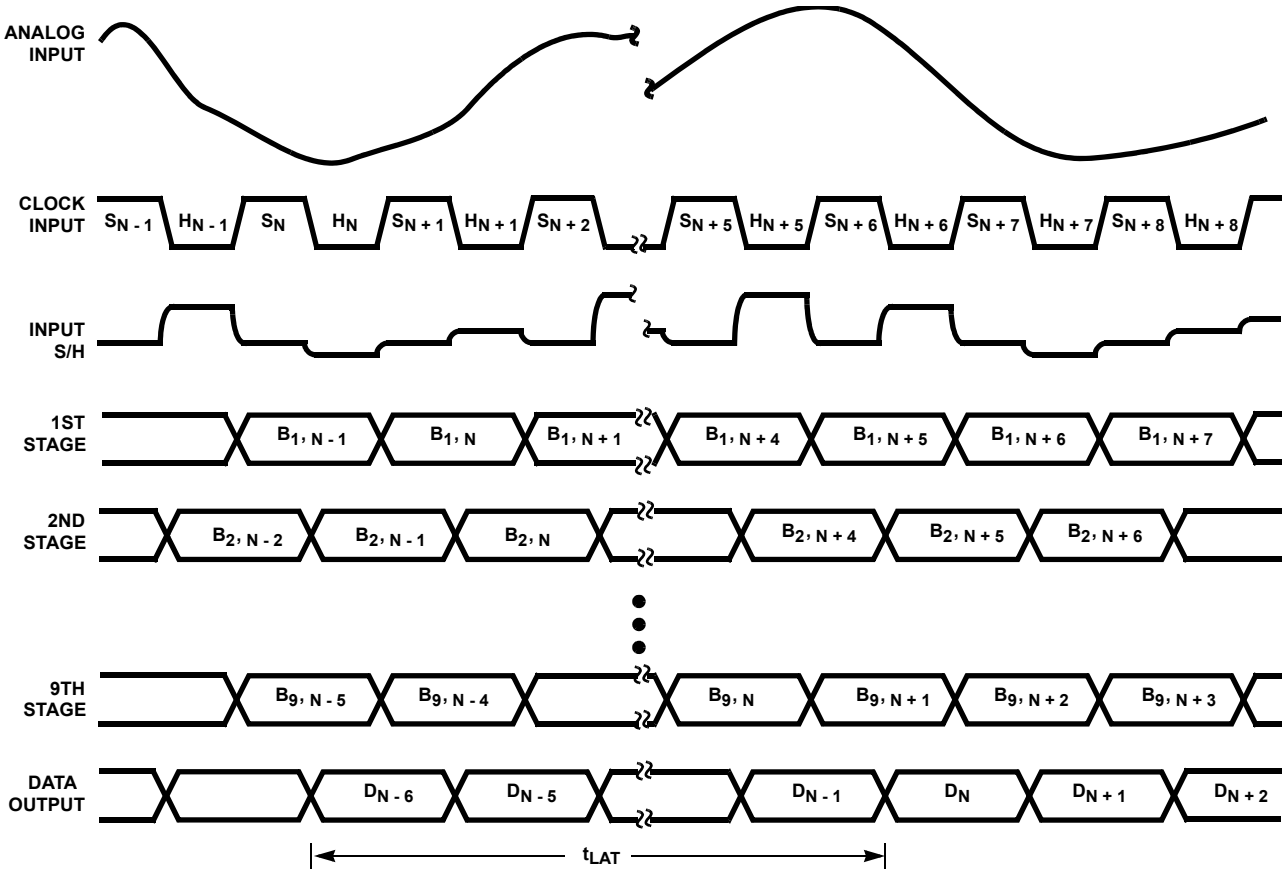
Electrical Specifications $AV_{CC1,2}$ = $DV_{CC1,2}$ = +5.0V, DV_{CC3} = +3.0V; V_{RIN} = 2.50V; f_S = 60MSPS at 50% Duty Cycle; C_L = 10pF; T_A = +25°C; Differential Analog Input; Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Digital Supply Voltage, DV_{CC1} and DV_{CC2}	(Note 4)	4.75	5.0	5.25	V
Digital Output Supply Voltage, DV_{CC3}	At 3.0V (Note 4)	2.7	3.0	3.3	V
	At 5.0V (Note 4)	4.75	5.0	5.25	V
Supply Current, I_{CC}	f_S = 60MSPS	-	130	-	mA
Power Dissipation		-	650	670	mW
Offset Error Sensitivity, ΔV_{OS}	AV_{CC} or DV_{CC} = 5V ±5%	-	±0.5	-	LSB
Gain Error Sensitivity, ΔFSE	AV_{CC} or DV_{CC} = 5V ±5%	-	±0.6	-	LSB

NOTES:

4. Limits established by characterization and are not production tested.
5. With the clock low and DC input.

Timing Waveforms



NOTES:

6. S_N: N-th sampling period.
7. H_N: N-th holding period.
8. $B_{M,N}$: M-th stage digital output corresponding to N-th sampled input.
9. D_N: Final data output corresponding to N-th sampled input.

FIGURE 1. HI5762 INTERNAL CIRCUIT TIMING

Timing Waveforms (Continued)

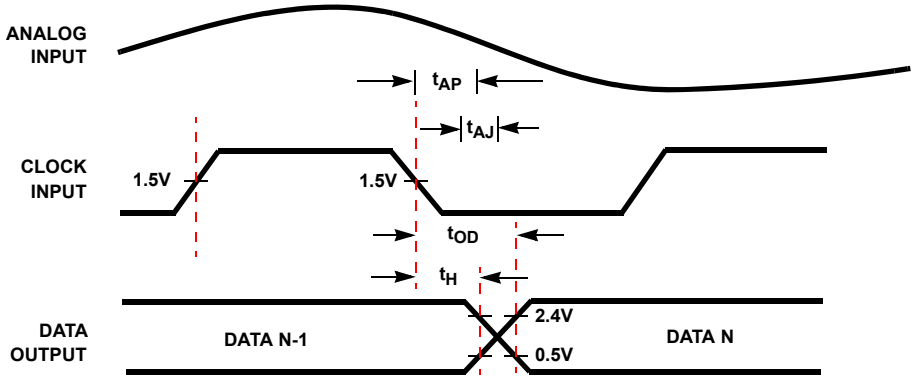


FIGURE 2. HI5762 INPUT-TO OUTPUT TIMING

Typical Performance Curves

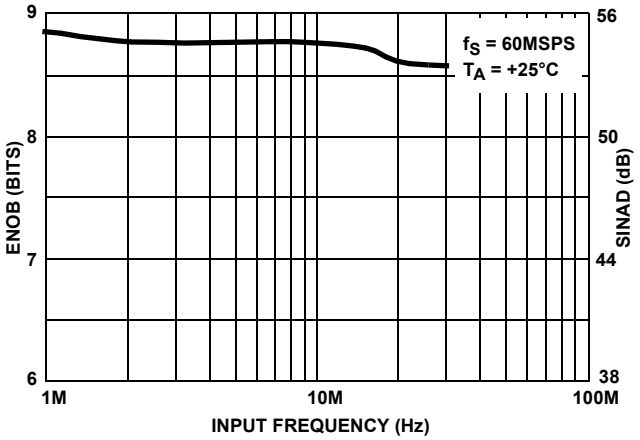


FIGURE 3. EFFECTIVE NUMBER OF BITS (ENOB) AND SINAD vs INPUT FREQUENCY

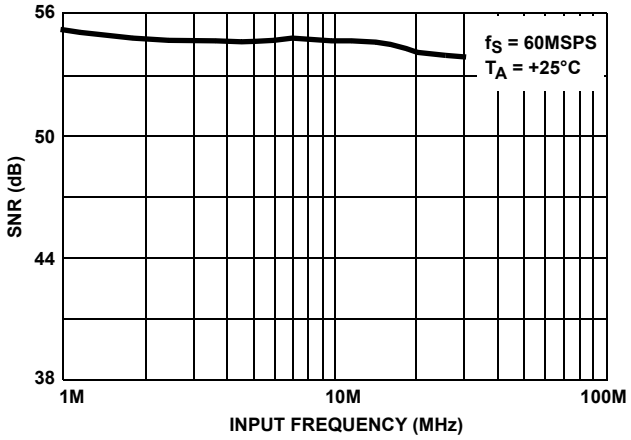


FIGURE 4. SNR vs INPUT FREQUENCY

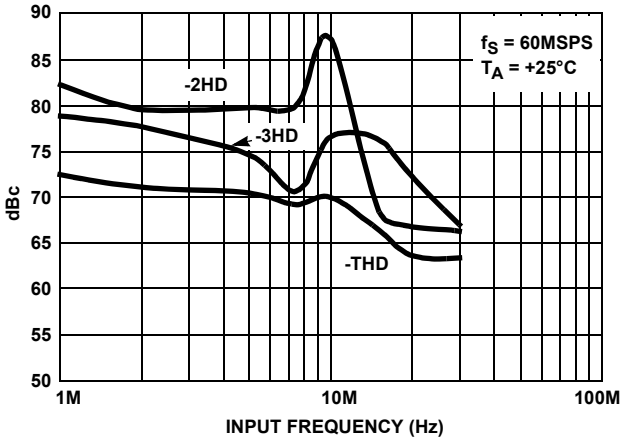


FIGURE 5. -THD, -2HD AND -3HD vs INPUT FREQUENCY

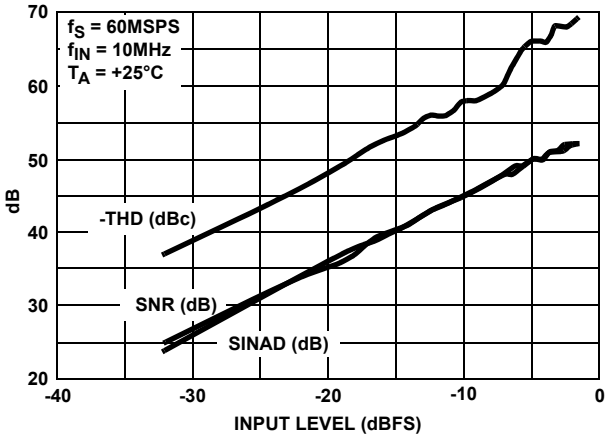


FIGURE 6. SINAD, SNR AND -THD vs INPUT AMPLITUDE

Typical Performance Curves (Continued)

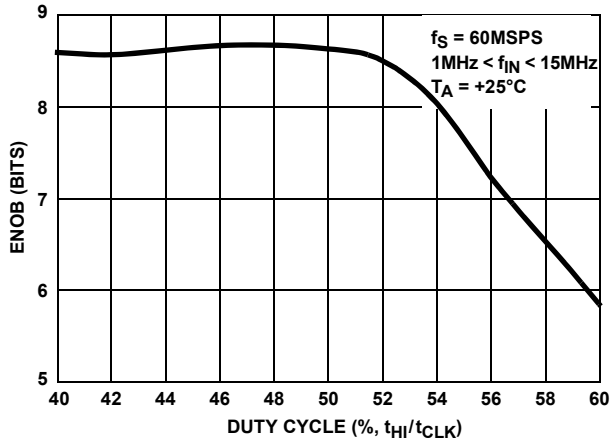


FIGURE 7. EFFECTIVE NUMBER OF BITS (ENOB) vs SAMPLE CLOCK DUTY CYCLE

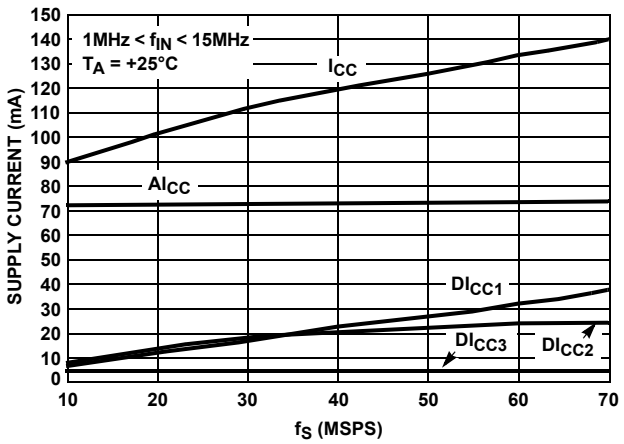


FIGURE 8. SUPPLY CURRENT vs SAMPLE CLOCK FREQUENCY

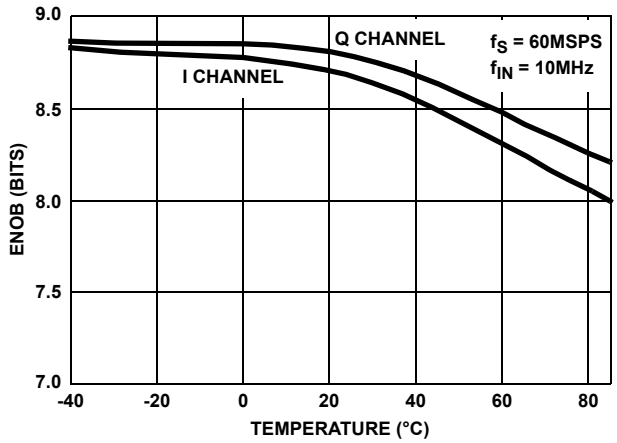


FIGURE 9. EFFECTIVE NUMBER OF BITS (ENOB) vs TEMPERATURE

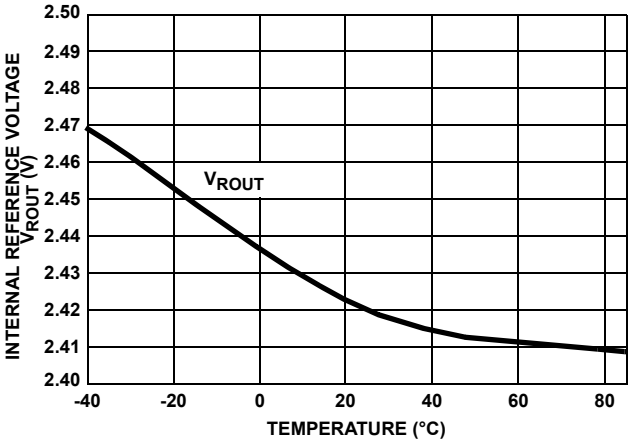


FIGURE 10. INTERNAL REFERENCE VOLTAGE (V_{ROUT}) vs TEMPERATURE

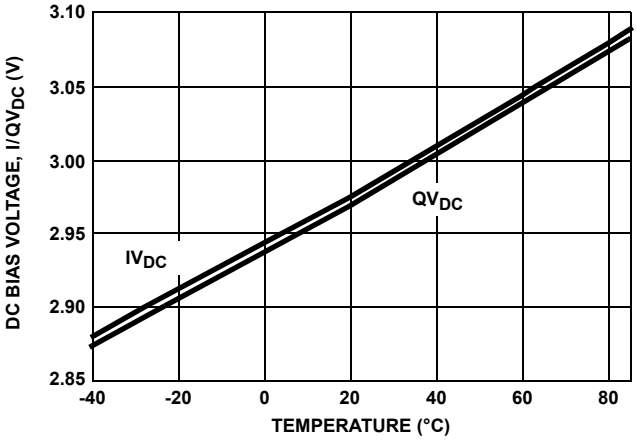


FIGURE 11. DC BIAS VOLTAGE (I/QV_{DC}) vs TEMPERATURE

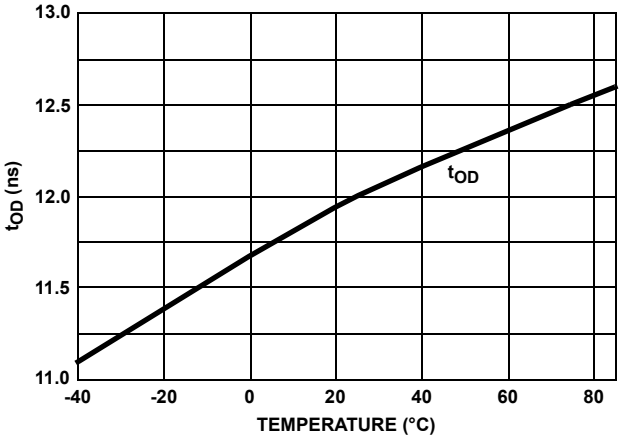


FIGURE 12. DATA OUTPUT DELAY (t_{OD}) vs TEMPERATURE

Typical Performance Curves (Continued)

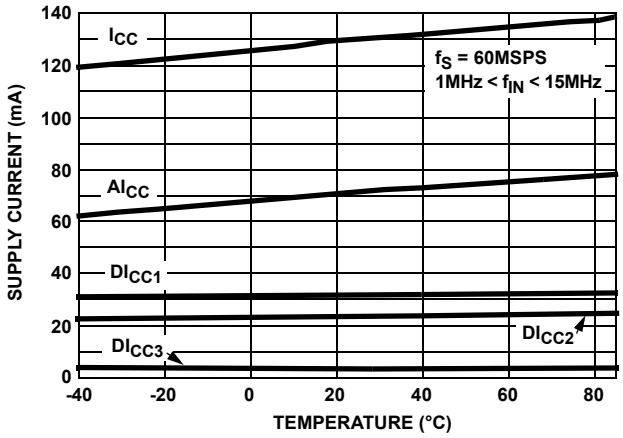


FIGURE 13. SUPPLY CURRENT vs TEMPERATURE

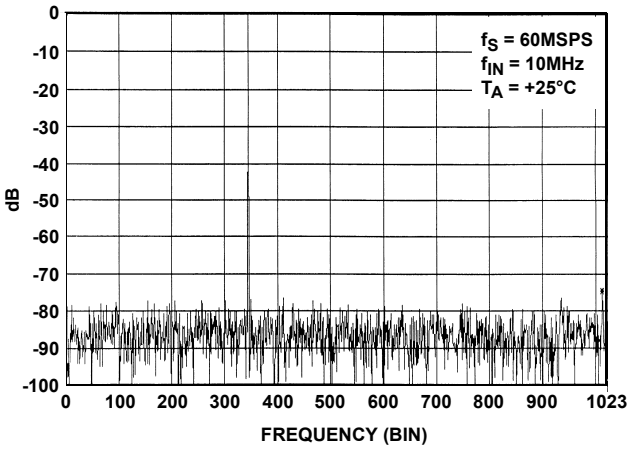


FIGURE 14. 2048 POINT FFT PLOT

TABLE 1. A/D CODE TABLE

CODE CENTER DESCRIPTION	DIFFERENTIAL INPUT VOLTAGE ($I/Q_{IN}+ - I/Q_{IN}-$)	OFFSET BINARY OUTPUT CODE									
		MSB									LSB
		I/QD9	I/QD8	I/QD7	I/QD6	I/QD5	I/QD4	I/QD3	I/QD2	I/QD1	I/QD0
+Full Scale (+FS) - $^1/_4$LSB	0.499756V	1	1	1	1	1	1	1	1	1	1
+FS - $1^1/_4$LSB	0.498779V	1	1	1	1	1	1	1	1	1	0
+ $^3/_4$LSB	732.422µV	1	0	0	0	0	0	0	0	0	0
- $^1/_4$LSB	-244.141µV	0	1	1	1	1	1	1	1	1	1
-FS + $1^3/_4$LSB	-0.498291V	0	0	0	0	0	0	0	0	0	1
-Full Scale (-FS) + $^3/_4$LSB	-0.499268V	0	0	0	0	0	0	0	0	0	0

NOTE:

10. The voltages listed above represent the ideal center of each output code shown with V_{REFIN} = +2.5V.

Detailed Description

Theory of Operation

The HI5762 is a dual 10-bit fully differential sampling pipeline A/D converter with digital error correction logic. Figure 15 depicts the circuit for the front-end differential-in-differential-out sample-and-hold (S/H) amplifiers. The switches are controlled by an internal sampling clock which is a non-overlapping two phase signal, Φ_1 and Φ_2, derived from the master sampling clock. During the sampling phase, Φ_1, the input signal is applied to the sampling capacitors, C_S. At the same time the holding capacitors, C_H, are discharged to analog ground. At the falling edge of Φ_1 the input signal is sampled on the bottom plates of the sampling capacitors. In the next clock phase, Φ_2, the two bottom plates of the sampling capacitors are connected together and the holding capacitors are switched to the op amp output nodes. The charge then redistributes between C_S and C_H completing one sample-and-hold cycle. The front end sample-and-hold output is a fully-differential, sampled-data representation of the analog input. The circuit not only performs the sample-and-hold function but will also convert a single-ended input to a fully-differential output for the converter core. During the sampling phase, the I/Q_{IN} pins see only the on-resistance of a switch and C_S. The relatively small values of these components result in a typical full power input bandwidth of 250MHz for the converter.

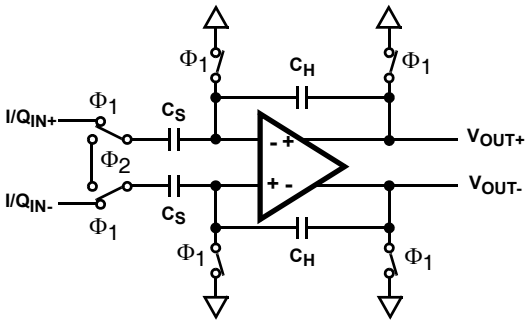


FIGURE 15. ANALOG INPUT SAMPLE-AND-HOLD

As illustrated in the “Functional Block Diagram” on page 3 and the timing diagram in Figure 1 on page 8, eight identical pipeline subconverter stages, each containing a two-bit flash converter and a two-bit multiplying digital-to-analog converter, follow the S/H circuit with the ninth stage being a two bit flash converter. Each converter stage in the pipeline will be sampling in one phase and amplifying in the other clock phase. Each individual subconverter clock signal is offset by 180° from the previous stage clock signal resulting in alternate stages in the pipeline performing the same operation.

The output of each of the eight identical two-bit subconverter stages is a two-bit digital word containing a supplementary bit to be used by the digital error correction logic. The output of each subconverter stage is input to a digital delay line which is controlled by the internal sampling clock. The function of the digital delay line is to time align the digital outputs of the eight identical two-bit subconverter stages with the corresponding output of the ninth stage flash converter before applying the eighteen bit result to the digital error correction logic. The digital error correction logic uses the supplementary bits to correct any error that may exist before generating the final ten bit digital data output of the converter.

Because of the pipeline nature of this converter, the digital data representing an analog input sample is output to the digital data bus following the 6th cycle of the clock after the analog sample is taken (see the timing diagram in Figure 1 on page 8). This time delay is specified as the data latency. After the data latency time, the digital data representing each succeeding analog sample is output during the following clock cycle. The digital output data is provided in offset binary format (see Table 1, A/D Code Table).

Internal Reference Voltage Output, V_{REFOUT}

The HI5762 is equipped with an internal reference voltage generator, therefore, no external reference voltage is required. V_{ROUT} must be connected to V_{RIN} when using the internal reference voltage.

An internal band-gap reference voltage followed by an amplifier/buffer generates the precision +2.5V reference voltage used by the converter. A band-gap reference circuit is used to generate a precision +1.25V internal reference voltage. This voltage is then amplified by a wide-band uncompensated operational amplifier connected in a gain-of-two configuration. An external, user-supplied, 0.1µF capacitor connected from the V_{ROUT} output pin to analog ground is used to set the dominant pole and to maintain the stability of the operational amplifier.

Reference Voltage Input, V_{REFIN}

The HI5762 is designed to accept a +2.5V reference voltage source at the V_{RIN} input pin. Typical operation of the converter requires V_{RIN} to be set at +2.5V. The HI5762 is tested with V_{RIN} connected to V_{ROUT} yielding a fully differential analog input voltage range of ±0.5V.

The user does have the option of supplying an external +2.5V reference voltage. As a result of the high input impedance presented at the V_{RIN} input pin, 1.25kΩ typically, the external reference voltage being used is only required to source 2mA of reference input current. In the situation where an external reference voltage will be used an external 0.1µF capacitor **must** be connected from the V_{ROUT} output pin to analog ground in order to maintain the stability of the internal operational amplifier.

In order to minimize overall converter noise it is recommended that adequate high frequency decoupling be provided at the reference voltage input pin, V_{RIN}.

Analog Input, Differential Connection

The analog input of the HI5762 is a differential input that can be configured in various ways depending on the signal source and the required level of performance. A fully differential connection (Figure 16 and Figure 17) will deliver the best performance from the converter.

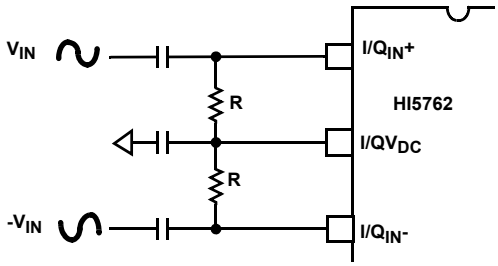


FIGURE 16. AC-COUPLED DIFFERENTIAL INPUT

Since the HI5762 is powered by a single +5V analog supply, the analog input is limited to be between ground and +5V. For the differential input connection this implies the analog input common mode voltage can range from 0.25V to 4.75V. The performance of the ADC does not change significantly with the value of the analog input common mode voltage.

A DC voltage source, I/QV_{DC}, equal to 3.0V (typical), is made available to the user to help simplify circuit design when using an AC-coupled differential input. This low output impedance voltage source is not designed to be a reference but makes an excellent DC bias source and stays well within the analog input common mode voltage range over temperature.

For the AC-coupled differential input (see Figure 16) and with V_{RIN} connected to V_{ROUT}, full scale is achieved when the V_{IN} and $-V_{IN}$ input signals are $0.5V_{P-P}$, with $-V_{IN}$ being 180° out-of-phase with V_{IN}. The converter will be at positive full scale when the $I/Q_{IN}+$ input is at V_{DC} + 0.25V and the $I/Q_{IN}-$ input is at V_{DC} - 0.25V ($I/Q_{IN}+$ - $I/Q_{IN}-$ = +0.5V). Conversely, the converter will be at negative full scale when the $I/Q_{IN}+$ input is equal to V_{DC} - 0.25V and $I/Q_{IN}-$ is at V_{DC} + 0.25V ($I/Q_{IN}+$ - $I/Q_{IN}-$ = -0.5V).

The analog input can be DC coupled (see Figure 17) as long as the inputs are within the analog input common mode voltage range (0.25V ≤ VDC ≤ 4.75V).

The resistors, R, in Figure 17 are not absolutely necessary but may be used as load setting resistors. A capacitor, C, connected from $I/Q_{IN}+$ to $I/Q_{IN}-$ will help filter any high frequency noise on the inputs, also improving performance. Values around 20pF are sufficient and can be used on AC-coupled inputs as well. Note, however, that the value of capacitor C chosen must take into account the highest frequency component of the analog input signal.

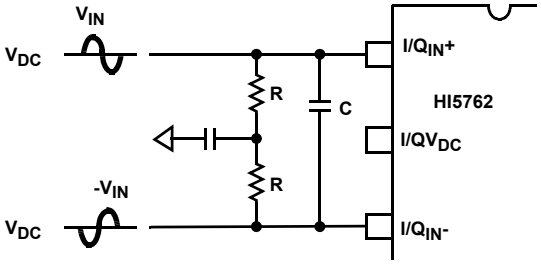


FIGURE 17. DC COUPLED DIFFERENTIAL INPUT

Analog Input, Single-Ended Connection

The configuration shown in Figure 18 may be used with a single-ended AC-coupled input.

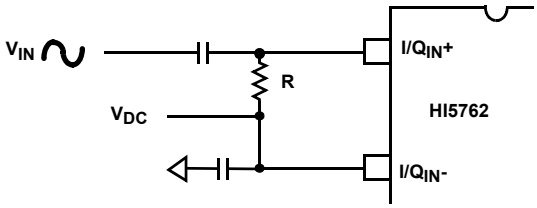


FIGURE 18. AC COUPLED SINGLE-ENDED INPUT

Again, with V_{RIN} connected to V_{ROUT}, if V_{IN} is a $1V_{P-P}$ sinewave, then $I/Q_{IN}+$ is a $1.0V_{P-P}$ sinewave riding on a positive voltage equal to VDC. The converter will be at positive full scale when $I/Q_{IN}+$ is at VDC + 0.5V ($I/Q_{IN}+ - I/Q_{IN}- = +0.5V$) and will be at negative full scale when $I/Q_{IN}+$ is equal to VDC - 0.5V ($I/Q_{IN}+ - I/Q_{IN}- = -0.5V$). Sufficient headroom must be provided such that the input voltage never goes above +5V or below AGND. In this case, VDC could range between 0.5V and 4.5V without a significant change in ADC performance. The simplest way to produce VDC is to use the DC bias source, I/QV_{DC}, output of the HI5762.

The single ended analog input can be DC-coupled (see Figure 19) as long as the input is within the analog input common mode voltage range.

The resistor, R, in Figure 19 is not absolutely necessary but may be used as a load setting resistor. A capacitor, C, connected from $I/Q_{IN}+$ to $I/Q_{IN}-$ will help filter any high frequency noise on the inputs, also improving performance. Values around 20pF are sufficient and can be used on AC-coupled inputs as well. Note, however, that the value of capacitor C chosen must take into account the highest frequency component of the analog input signal.

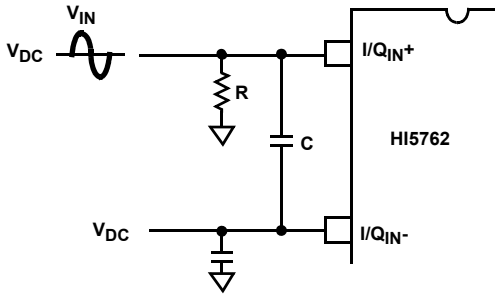


FIGURE 19. DC COUPLED SINGLE ENDED INPUT

A single-ended source may give better overall system performance if it is first converted to differential before driving the HI5762.

Sampling Clock Requirements

The HI5762 sampling clock input provides a standard high-speed interface to external TTL/CMOS logic families.

In order to ensure rated performance of the HI5762, the duty cycle of the clock should be held at 50% ±5%. It must also have low jitter and operate at standard TTL/CMOS levels.

Performance of the HI5762 will only be guaranteed at conversion rates above 1MSPS (Typ). This ensures proper performance of the internal dynamic circuits. Similarly, when power is first applied to the converter, a maximum of 20 cycles at a sample rate above 1MSPS must be performed before valid data is available.

Supply and Ground Considerations

The HI5762 has separate analog and digital supply and ground pins to keep digital noise out of the analog signal path. The digital data outputs also have a separate supply pin, DV_{CC3}, which can be powered from a 3.0V or 5.0V supply. This allows the outputs to interface with 3.0V logic if so desired.

The part should be mounted on a board that provides separate low impedance connections for the analog and digital supplies and grounds. For best performance, the supplies to the HI5762 should be driven by clean, linear regulated supplies. The board should also have good high frequency decoupling capacitors mounted as close as possible to the converter. If the part is powered off a single supply then the analog supply can be isolated by a ferrite bead from the digital supply.

Refer to the application note “Using Intersil High-Speed A/D Converters” (AN9214) for additional considerations when using high-speed converters.

Static Performance Definitions

Offset Error (V_{OS})

The midscale code transition should occur at a level $^1/_4$LSB above half-scale. Offset is defined as the deviation of the actual code transition from this point.

Full-Scale Error (FSE)

The last code transition should occur for an analog input that is $^3/_4$LSB below Positive Full Scale (+FS) with the offset error removed. Full scale error is defined as the deviation of the actual code transition from this point.

Differential Linearity Error (DNL)

DNL is the worst case deviation of a code width from the ideal value of 1LSB.

Integral Linearity Error (INL)

INL is the worst case deviation of a code center from a best fit straight line calculated from the measured data.

Power Supply Sensitivity

Each of the power supplies are moved plus and minus 5% and the shift in the offset and full scale error (in LSBs) is noted.

Dynamic Performance Definitions

Fast Fourier Transform (FFT) techniques are used to evaluate the dynamic performance of the HI5762. A low distortion sine wave is applied to the input, it is coherently sampled, and the output is stored in RAM. The data is then transformed into the frequency domain with an FFT and analyzed to evaluate the dynamic performance of the A/D. The sine wave input to the part is typically -0.5dB down from full scale for all these tests.

SNR and SINAD are quoted in dB. The distortion numbers are quoted in dBc (decibels with respect to carrier) and **DO NOT** include any correction factors for normalizing to full scale.

The Effective Number of Bits (ENOB) is calculated from the SINAD data by Equation 1:

$$ENOB = (SINAD - 1.76 + V_{CORR})/6.02 \quad \text{(EQ. 1)}$$

where: V_{CORR} = 0.5dB (Typ).

V_{CORR} adjusts the SINAD, and hence the ENOB, for the amount the analog input signal is backed off from full scale.

Signal To Noise and Distortion Ratio (SINAD)

SINAD is the ratio of the measured RMS signal to RMS sum of all the other spectral components below the Nyquist frequency, $f_S/2$, excluding DC.

Signal To Noise Ratio (SNR)

SNR is the ratio of the measured RMS signal to RMS noise at a specified input and sampling frequency. The noise is the RMS sum of all of the spectral components below $f_S/2$ excluding the fundamental, the first five harmonics and DC.

Total Harmonic Distortion (THD)

THD is the ratio of the RMS sum of the first 5 harmonic components to the RMS value of the fundamental input signal.

2nd and 3rd Harmonic Distortion

This is the ratio of the RMS value of the applicable harmonic component to the RMS value of the fundamental input signal.

Spurious Free Dynamic Range (SFDR)

SFDR is the ratio of the fundamental RMS amplitude to the RMS amplitude of the next largest spectral component in the spectrum below $f_S/2$.

Intermodulation Distortion (IMD)

Nonlinearities in the signal path will tend to generate intermodulation products when two tones, f_1 and f_2, are present at the inputs. The ratio of the measured signal to the distortion terms is calculated. The terms included in the calculation are (f_1+f_2), (f_1-f_2), ($2f_1$), ($2f_2$), ($2f_1+f_2$), ($2f_1-f_2$), (f_1+2f_2), (f_1-2f_2). The ADC is tested with each tone 6dB below full scale.

Transient Response

Transient response is measured by providing a full-scale transition to the analog input of the ADC and measuring the number of cycles it takes for the output code to settle within 10-bit accuracy.

Over-Voltage Recovery

Over-Voltage Recovery is measured by providing a full-scale transition to the analog input of the ADC which overdrives the input by 200mV, and measuring the number of cycles it takes for the output code to settle within 10-bit accuracy.

Full Power Input Bandwidth (FPBW)

Full power input bandwidth is the analog input frequency at which the amplitude of the digitally reconstructed output has decreased 3dB below the amplitude of the input sine wave. The input sine wave has an amplitude which swings from -FS to +FS. The bandwidth given is measured at the specified sampling frequency.

I/Q Channel Crosstalk

I/Q Channel Crosstalk is a measure of the amount of channel separation or isolation between the two A/D converter cores contained within the dual converter package. The measurement consists of stimulating one channel of the converter with a fullscale input signal and then measuring the amount that signal is below, in dBc, a fullscale signal on the opposite channel.

Timing Definitions

Refer to Figure 1 and Figure 2 for these definitions.

Aperture Delay (t_{AP})

Aperture delay is the time delay between the external sample command (the falling edge of the clock) and the time at which the signal is actually sampled. This delay is due to internal clock path propagation delays.

Aperture Jitter (t_{AJ})

Aperture jitter is the RMS variation in the aperture delay due to variation of internal clock path delays.

Data Hold Time (t_H)

Data hold time is the time to where the previous data (N - 1) is no longer valid.

Data Output Delay Time (t_{OD})

Data output delay time is the time to where the new data (N) is valid.

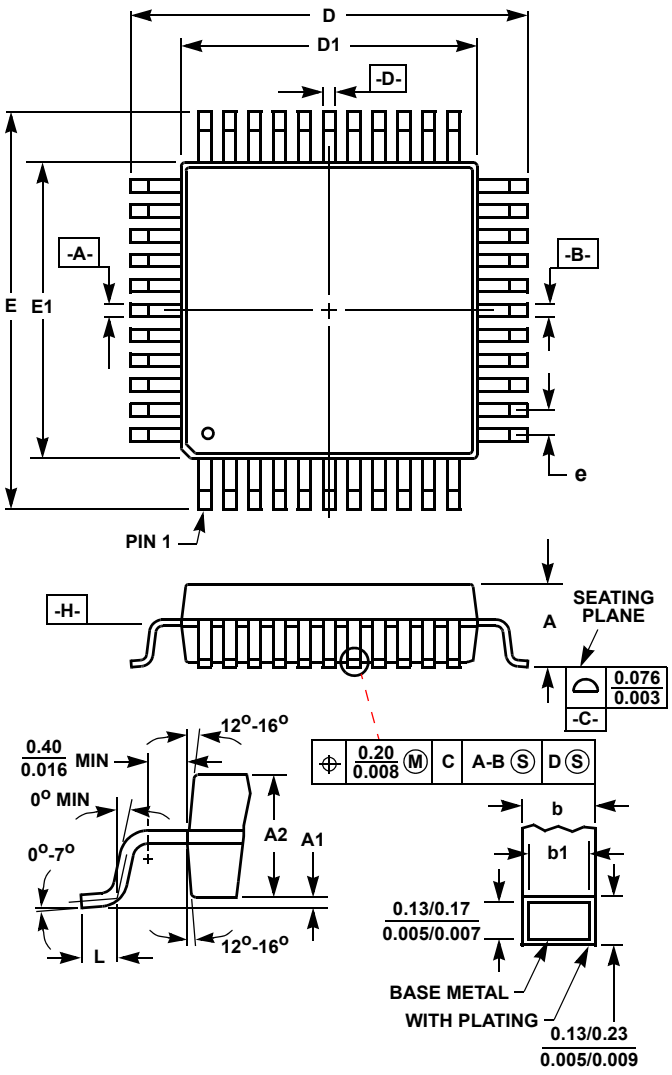
Data Latency (t_{LAT})

After the analog sample is taken, the digital data representing an analog input sample is output to the digital data bus following the 6th cycle of the clock after the analog sample is taken. This is due to the pipeline nature of the converter where the analog sample has to ripple through the internal subconverter stages. This delay is specified as the data latency. After the data latency time, the digital data representing each succeeding analog sample is output during the following clock cycle. The digital data lags the analog input sample by 6 sample clock cycles.

Power-Up Initialization

This time is defined as the maximum number of clock cycles that are required to initialize the converter at power-up. The requirement arises from the need to initialize the dynamic circuits within the converter.

Metric Plastic Quad Flatpack Packages (MQFP)



Q44.10x10 (JEDEC MS-022AB ISSUE B)
44 LEAD METRIC PLASTIC QUAD FLATPACK PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.096	-	2.45	-
A1	0.004	0.010	0.10	0.25	-
A2	0.077	0.083	1.95	2.10	-
b	0.012	0.018	0.30	0.45	6
b1	0.012	0.016	0.30	0.40	-
D	0.515	0.524	13.08	13.32	3
D1	0.389	0.399	9.88	10.12	4, 5
E	0.516	0.523	13.10	13.30	3
E1	0.390	0.398	9.90	10.10	4, 5
L	0.029	0.040	0.73	1.03	-
N	44		44		7
e	0.032 BSC		0.80 BSC		-

Rev. 2 4/99

NOTES:

1. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.
2. All dimensions and tolerances per ANSI Y14.5M-1982.
3. Dimensions D and E to be determined at seating plane -C-.
4. Dimensions D1 and E1 to be determined at datum plane -H-.
5. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25mm (0.010 inch) per side.
6. Dimension b does not include dambar protrusion. Allowable dambar protrusion shall be 0.08mm (0.003 inch) total.
7. “N” is the number of terminal positions.

© Copyright Intersil Americas LLC 1999-2010. All Rights Reserved.
All trademarks and registered trademarks are the property of their respective owners.

For additional products, see www.intersil.com/en/products.html

Intersil products are manufactured, assembled and tested utilizing ISO9001 quality systems as noted in the quality certifications found at www.intersil.com/en/support/qualandreliability.html

Intersil products are sold by description only. Intersil may modify the circuit design and/or specifications of products at any time without notice, provided that such modification does not, in Intersil's sole judgment, affect the form, fit or function of the product. Accordingly, the reader is cautioned to verify that datasheets are current before placing orders. Information furnished by Intersil is believed to be accurate and reliable. However, no responsibility is assumed by Intersil or its subsidiaries for its use; nor for any infringements of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of Intersil or its subsidiaries.

For information regarding Intersil Corporation and its products, see www.intersil.com