8-Lane 5-Port PCI Express® Switch

89HPES8T5
Data Sheet

Device Overview

The 89HPES8T5 is a member of the IDT PRECISE™ family of PCI Express switching solutions. The PES8T5 is an 8-lane, 5-port peripheral chip that performs PCI Express packet switching with a feature set optimized for high performance applications such as servers, storage and communications/networking. It provides connectivity and switching functions between a PCI Express upstream port and up to four downstream ports and supports switching between downstream ports.

Features

- High Performance PCI Express Switch
  - *Eight 2.5 Gbps PCI Express lanes*
  - *Five switch ports*
  - *Upstream port is x4*
  - *Downstream ports are x1*
  - *Low-latency cut-through switch architecture*
  - *Support for Max Payload Size up to 256 bytes*
  - *One virtual channel*
  - *Eight traffic classes*
  - *PCI Express Base Specification Revision 1.1 compliant*
- Flexible Architecture with Numerous Configuration Options
  - *Automatic lane reversal on all ports*
  - *Automatic polarity inversion on all lanes*
  - *Ability to load device configuration from serial EEPROM*
- Legacy Support
  - *PCI compatible INTx emulation*
  - *Bus locking*
- Highly Integrated Solution
  - *Requires no external components*
  - *Incorporates on-chip internal memory for packet buffering and queueing*
  - *Integrates eight 2.5 Gbps embedded SerDes with 8B/10B encoder/decoder (no separate transceivers needed)*
- Reliability, Availability, and Serviceability (RAS) Features
  - *Supports ECRC and Advanced Error Reporting*
  - *Internal end-to-end parity protection on all TLPs ensures data integrity even in systems that do not implement end-to-end CRC (ECRC)*
  - *Supports PCI Express Native Hot-Plug, Hot-Swap capable I/O*
  - *Compatible with Hot-Plug I/O expanders used on PC and server motherboards*
- Power Management
  - *Utilizes advanced low-power design techniques to achieve low typical power consumption*
  - *Supports PCI Power Management Interface specification (PCI-PM 1.1)*
    - *Supports device power management states: D0, $D3_{hot}$ and $D3_{cold}$*
  - *Unused SerDes are disabled*

Block Diagram

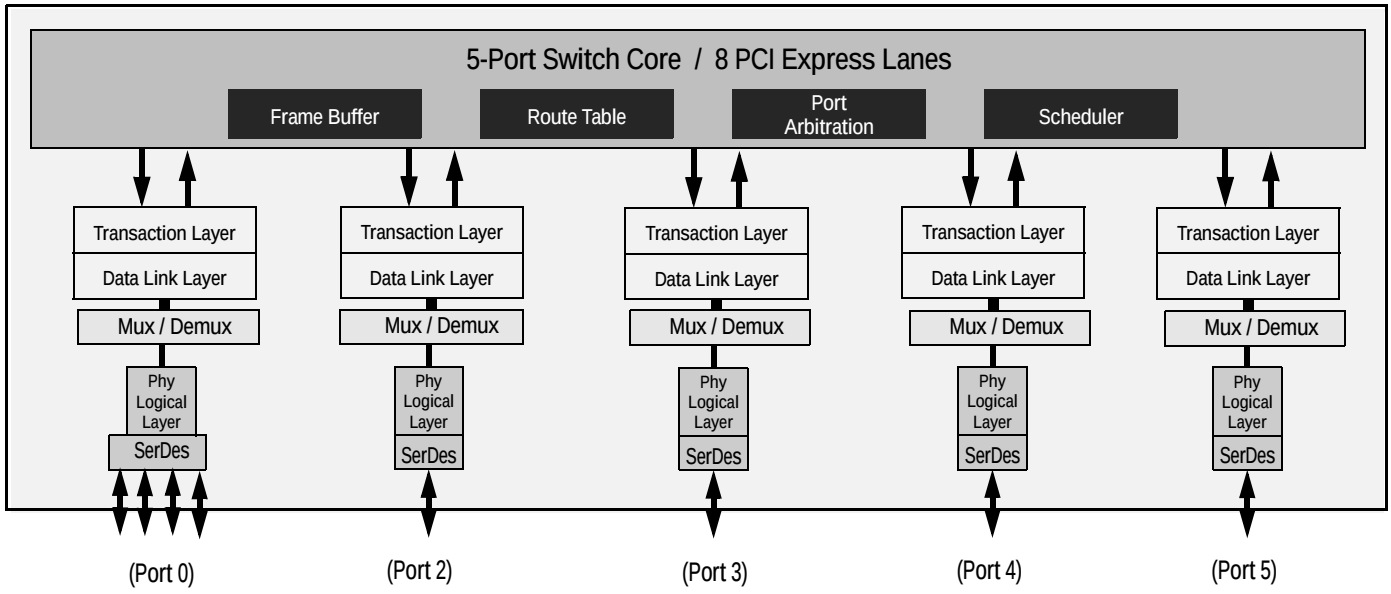


Figure 1 Internal Block Diagram

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- Testability and Debug Features
  - *Ability to read and write any internal register via the SMBus*
- Eleven General Purpose Input/Output pins
  - *Each pin may be individually configured as an input or output*
  - *Each pin may be individually configured as an interrupt input*
  - *Some pins have selectable alternate functions*
- Packaged in 19mm x 19mm 324-ball BGA with 1mm ball spacing

Product Description

Utilizing standard PCI Express interconnect, the PES8T5 provides the most efficient I/O connectivity solution for applications requiring high throughput, low latency, and simple board layout with a minimum number of board layers. It provides connectivity for up to 5 ports across 8 integrated serial lanes. Each lane provides 2.5 Gbps of bandwidth in both directions and is fully compliant with PCI Express Base specification revision 1.1.

The PES8T5 is based on a flexible and efficient layered architecture. The PCI Express layer consists of SerDes, Physical, Data Link and Transaction layers. The PES8T5 can operate either as a store and forward switch or a cut-through switch and is designed to switch memory and I/O transactions. It supports eight Traffic Classes (TCs) and one Virtual Channel (VC) with sophisticated resource management to allow efficient switching for applications requiring additional narrow port connectivity.

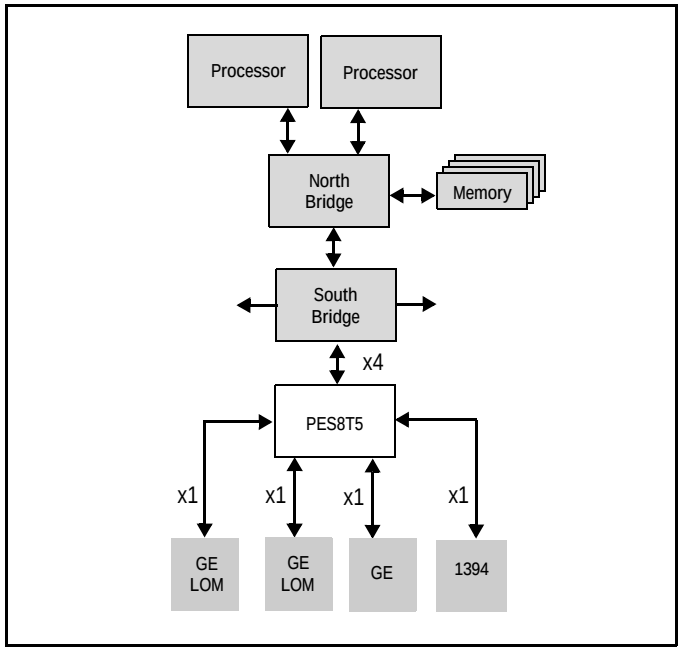


Figure 2 I/O Expansion Application

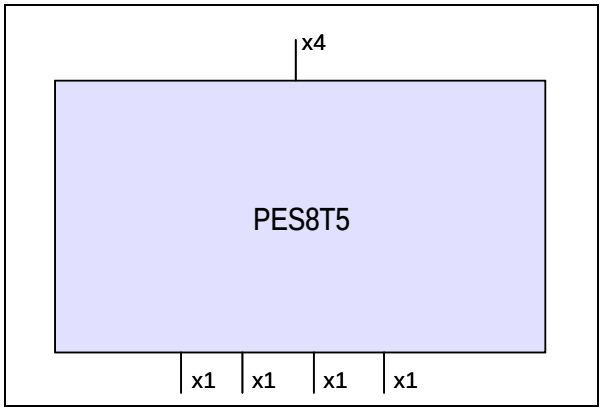


Figure 3 Configuration Option

SMBus Interface

The PES8T5 contains two SMBus interfaces. The slave interface provides full access to the configuration registers in the PES8T5, allowing every configuration register in the device to be read or written by an external agent. The master interface allows the default configuration register values of the PES8T5 to be overridden following a reset with values programmed in an external serial EEPROM. The master interface is also used by an external Hot-Plug I/O expander.

Six pins make up each of the two SMBus interfaces. These pins consist of an SMBus clock pin, an SMBus data pin, and 4 SMBus address pins. In the slave interface, these address pins allow the SMBus address to which the device responds to be configured. In the master interface, these address pins allow the SMBus address of the serial configuration EEPROM from which data is loaded to be configured. The SMBus address is set up on negation of PERSTN by sampling the corresponding address pins. When the pins are sampled, the resulting address is assigned as shown in Table 1.

Bit	Slave SMBus Address	Master SMBus Address
1	SSMBADDR[1]	MSMBADDR[1]
2	SSMBADDR[2]	MSMBADDR[2]
3	SSMBADDR[3]	MSMBADDR[3]
4	0	MSMBADDR[4]
5	SSMBADDR[5]	1
6	1	0
7	1	1

Table 1 Master and Slave SMBus Address Assignment

As shown in Figure 4, the master and slave SMBuses may be used in a unified or split configuration. In the unified configuration, shown in Figure 4(a), the master and slave SMBuses are tied together and the PES8T5 acts both as a SMBus master as well as a SMBus slave on this bus. This requires that the SMBus master or processor that has access to PES8T5 registers supports SMBus arbitration. In some systems, this SMBus master interface may be implemented using general purpose I/O pins on a processor or micro controller, and may not support SMBus arbitration. To support these systems, the PES8T5 may be configured to operate in a split configuration as shown in Figure 4(b).

In the split configuration, the master and slave SMBuses operate as two independent buses and thus multi-master arbitration is never required. The PES8T5 supports reading and writing of the serial EEPROM on the master SMBus via the slave SMBus, allowing in system programming of the serial EEPROM.

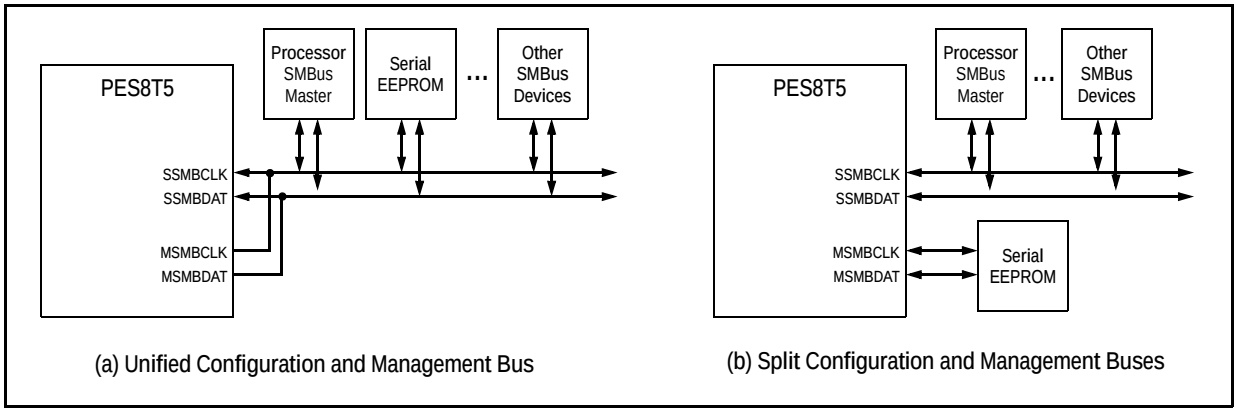


Figure 4 SMBus Interface Configuration Examples

Hot-Plug Interface

The PES8T5 supports PCI Express Hot-Plug on each downstream port. To reduce the number of pins required on the device, the PES8T5 utilizes an external I/O expander, such as that used on PC motherboards, connected to the SMBus master interface. Following reset and configuration, whenever the state of a Hot-Plug output needs to be modified, the PES8T5 generates an SMBus transaction to the I/O expander with the new value of all of the outputs. Whenever a Hot-Plug input changes, the I/O expander generates an interrupt which is received on the IOEXPINTN input pin (alternate function of GPIO) of the PES8T5. In response to an I/O expander interrupt, the PES8T5 generates an SMBus transaction to read the state of all of the Hot-Plug inputs from the I/O expander.

General Purpose Input/Output

The PES8T5 provides 11 General Purpose Input/Output (GPIO) pins that may be used by the system designer as bit I/O ports. Each GPIO pin may be configured independently as an input or output through software control. Some GPIO pins are shared with other on-chip functions. These alternate functions may be enabled via software, SMBus slave interface, or serial configuration EEPROM.

Pin Description

The following tables lists the functions of the pins provided on the PES8T5. Some of the functions listed may be multiplexed onto the same pin. The active polarity of a signal is defined using a suffix. Signals ending with an “N” are defined as being active, or asserted, when at a logic zero (low) level. All other signals (including clocks, buses, and select lines) will be interpreted as being active, or asserted, when at a logic one (high) level.

Note: In the PES8T5, the 4 downstream ports are labeled ports 2 through 5. There is no port 1.

Signal	Type	Name/Description
PE0RP[3:0] PE0RN[3:0]	I	**PCI Express Port 0 Serial Data Receive.** Differential PCI Express receive pairs for port 0.
PE0TP[3:0] PE0TN[3:0]	O	**PCI Express Port 0 Serial Data Transmit.** Differential PCI Express transmit pairs for port 0.
PE2RP[0] PE2RN[0]	I	**PCI Express Port 2 Serial Data Receive.** Differential PCI Express receive pairs for port 2.
PE2TP[0] PE2TN[0]	O	**PCI Express Port 2 Serial Data Transmit.** Differential PCI Express transmit pairs for port 2.
PE3RP[0] PE3RN[0]	I	**PCI Express Port 3 Serial Data Receive.** Differential PCI Express receive pair for port 3.
PE3TP[0] PE3TN[0]	O	**PCI Express Port 3 Serial Data Transmit.** Differential PCI Express transmit pair for port 3.

Table 2 PCI Express Interface Pins (Part 1 of 2)

Signal	Type	Name/Description
PE4RP[0] PE4RN[0]	I	**PCI Express Port 4 Serial Data Receive.** Differential PCI Express receive pair for port 4.
PE4TP[0] PE4TN[0]	O	**PCI Express Port 4 Serial Data Transmit.** Differential PCI Express transmit pair for port 4.
PE5RP[0] PE5RN[0]	I	**PCI Express Port 5 Serial Data Receive.** Differential PCI Express receive pair for port 5.
PE5TP[0] PE5TN[0]	O	**PCI Express Port 5 Serial Data Transmit.** Differential PCI Express transmit pair for port 5.
PEREFCLKP[2:1] PEREFCLKN[2:1]	I	**PCI Express Reference Clock.** Differential reference clock pair input. This clock is used as the reference clock by on-chip PLLs to generate the clocks required for the system logic and on-chip SerDes. The frequency of the differential reference clock is determined by the REFCLKM signal.
REFCLKM	I	**PCI Express Reference Clock Mode Select.** This signal selects the frequency of the reference clock input. 0x0 - 100 MHz 0x1 - 125 MHz

Table 2 PCI Express Interface Pins (Part 2 of 2)

Signal	Type	Name/Description
MSMBADDR[4:1]	I	**Master SMBus Address.** These pins determine the SMBus address of the serial EEPROM from which configuration information is loaded.
MSMBCLK	I/O	**Master SMBus Clock.** This bidirectional signal is used to synchronize transfers on the master SMBus. It is active and generating the clock only when the EEPROM or I/O Expanders are being accessed.
MSMBDAT	I/O	**Master SMBus Data.** This bidirectional signal is used for data on the master SMBus.
SSMBADDR[5,3:1]	I	**Slave SMBus Address.** These pins determine the SMBus address to which the slave SMBus interface responds.
SSMBCLK	I/O	**Slave SMBus Clock.** This bidirectional signal is used to synchronize transfers on the slave SMBus.
SSMBDAT	I/O	**Slave SMBus Data.** This bidirectional signal is used for data on the slave SMBus.

Table 3 SMBus Interface Pins

Signal	Type	Name/Description
GPIO[0]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. Alternate function pin name: P2RSTN Alternate function pin type: Output Alternate function: Reset output for downstream port 2
GPIO[1]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. Alternate function pin name: P4RSTN Alternate function pin type: Output Alternate function: Reset output for downstream port 4
GPIO[2]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. Alternate function pin name: IOEXPINTN0 Alternate function pin type: Input Alternate function: I/O Expander interrupt 0 input
GPIO[3]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. Alternate function pin name: IOEXPINTN1 Alternate function pin type: Input Alternate function: I/O Expander interrupt 1 input
GPIO[4]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. Alternate function pin name: IOEXPINTN2 Alternate function pin type: Input Alternate function: I/O Expander interrupt 2 input
GPIO[5]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin.
GPIO[6]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin.
GPIO[7]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. Alternate function pin name: GPEN Alternate function pin type: Output Alternate function: General Purpose Event (GPE) output
GPIO[8]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin.
GPIO[9]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. Alternate function pin name: P3RSTN Alternate function pin type: Output Alternate function: Reset output for downstream port 3
GPIO[10]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. Alternate function pin name: P5RSTN Alternate function pin type: Output Alternate function: Reset output for downstream port 5

Table 4 General Purpose I/O Pins

Signal	Type	Name/Description
CCLKDS	I	**Common Clock Downstream.** When the CCLKDS pin is asserted, it indicates that a common clock is being used between the downstream device and the downstream port.
CCLKUS	I	**Common Clock Upstream.** When the CCLKUS pin is asserted, it indicates that a common clock is being used between the upstream device and the upstream port.
MSMBSMODE	I	**Master SMBus Slow Mode.** The assertion of this pin indicates that the master SMBus should operate at 100 KHz instead of 400 kHz. This value may not be overridden.
PERSTN	I	**Fundamental Reset.** Assertion of this signal resets all logic inside the PES8T5 and initiates a PCI Express fundamental reset.
RSTHALT	I	**Reset Halt.** When this signal is asserted during a PCI Express fundamental reset, the PES8T5 executes the reset procedure and remains in a reset state with the Master and Slave SMBuses active. This allows software to read and write registers internal to the device before normal device operation begins. The device exits the reset state when the RSTHALT bit is cleared in the SWCTL register by an SMBus master.
SWMODE[3:0]	I	**Switch Mode.** These configuration pins determine the PES8T5 switch operating mode. These pins should be static and not change after the negation of PERSTN. 0x0 - Normal switch mode 0x1 - Normal switch mode with Serial EEPROM initialization 0x2 - through 0xF Reserved

Table 5 System Pins

Signal	Type	Name/Description
JTAG_TCK	I	**JTAG Clock**. This is an input test clock used to clock the shifting of data into or out of the boundary scan logic or JTAG Controller. JTAG_TCK is independent of the system clock with a nominal 50% duty cycle.
JTAG_TDI	I	**JTAG Data Input**. This is the serial data input to the boundary scan logic or JTAG Controller.
JTAG_TDO	O	**JTAG Data Output**. This is the serial data shifted out from the boundary scan logic or JTAG Controller. When no data is being shifted out, this signal is tri-stated.
JTAG_TMS	I	**JTAG Mode**. The value on this signal controls the test mode select of the boundary scan logic or JTAG Controller.
JTAG_TRST_N	I	**JTAG Reset**. This active low signal asynchronously resets the boundary scan logic and JTAG TAP Controller. An external pull-up on the board is recommended to meet the JTAG specification in cases where the tester can access this signal. However, for systems running in functional mode, one of the following should occur: 1) actively drive this signal low with control logic 2) statically drive this signal low with an external pull-down on the board

Table 6 Test Pins

Signal	Type	Name/Description
V_{DD}CORE	I	**Core VDD.** Power supply for core logic.
V_{DD}IO	I	**I/O VDD.** LVTTL I/O buffer power supply.
V_{DD}PE	I	**PCI Express Digital Power.** PCI Express digital power used by the digital power of the SerDes.
V_{DD}APE	I	**PCI Express Analog Power.** PCI Express analog power used by the PLL and bias generator.
V_{TT}PE	I	**PCI Express Termination Power.**
V_{SS}	I	**Ground.**

Table 7 Power and Ground Pins

Pin Characteristics

Note: Some input pads of the PES8T5 do not contain internal pull-ups or pull-downs. Unused inputs should be tied off to appropriate levels. This is especially critical for unused control signal inputs which, if left floating, could adversely affect operation. Also, any input pin left floating can cause a slight increase in power consumption.

Function	Pin Name	Type	Buffer	I/O Type	Internal Resistor[1]	Notes
PCI Express Interface	PE0RN[3:0]	I	CML	Serial Link		
	PE0RP[3:0]	I				
	PE0TN[3:0]	O				
	PE0TP[3:0]	O				
	PE2RN[0]	I				
	PE2RP[0]	I				
	PE2TN[0]	O				
	PE2TP[0]	O				
	PE3RN[0]	I				
	PE3RP[0]	I				
	PE3TN[0]	O				
	PE3TP[0]	O				
	PE4RN[0]	I				
	PE4RP[0]	I				
	PE4TN[0]	O				
	PE4TP[0]	O				
	PE5RN[0]	I				
	PE5RP[0]	I				
	PE5TN[0]	O				
	PE5TP[0]	O				
	PEREFCLKN[2:1]	I	LVPECL/ CML	Diff. Clock Input		Refer toTable 9
	PEREFCLKP[2:1]	I				
	REFCLKM	I	LVTTL	Input	pull-down	
SMBus	MSMBADDR[4:1]	I	LVTTL	Input	pull-up	
	MSMBCLK	I/O		STI[2]		pull-up on board
	MSMBDAT	I/O		STI		pull-up on board
	SSMBADDR[5,3:1]	I		Input	pull-up	
	SSMBCLK	I/O		STI		pull-up on board
	SSMBDAT	I/O		STI		pull-up on board
General Purpose I/O	GPIO[10:0]	I/O	LVTTL	High Drive	pull-up	

Table 8 Pin Characteristics (Part 1 of 2)

Function	Pin Name	Type	Buffer	I/O Type	Internal Resistor[1]	Notes
System Pins	CCLKDS	I	LVTTL	Input	pull-up	
	CCLKUS	I			pull-up	
	MSMBSMODE	I			pull-down	
	PERSTN	I				
	RSTHALT	I			pull-down	
	SWMODE[3:0]	I			pull-down	
EJTAG / JTAG	JTAG_TCK	I	LVTTL	STI	pull-up	
	JTAG_TDI	I		STI	pull-up	
	JTAG_TDO	O				
	JTAG_TMS	I		STI	pull-up	
	JTAG_TRST_N	I		STI	pull-up	External pull-down

Table 8 Pin Characteristics (Part 2 of 2)

1. Internal resistor values under typical operating conditions are 54K Ω for pull-up and 251K Ω for pull-down.

2. Schmitt Trigger Input (STI).

Logic Diagram — PES8T5

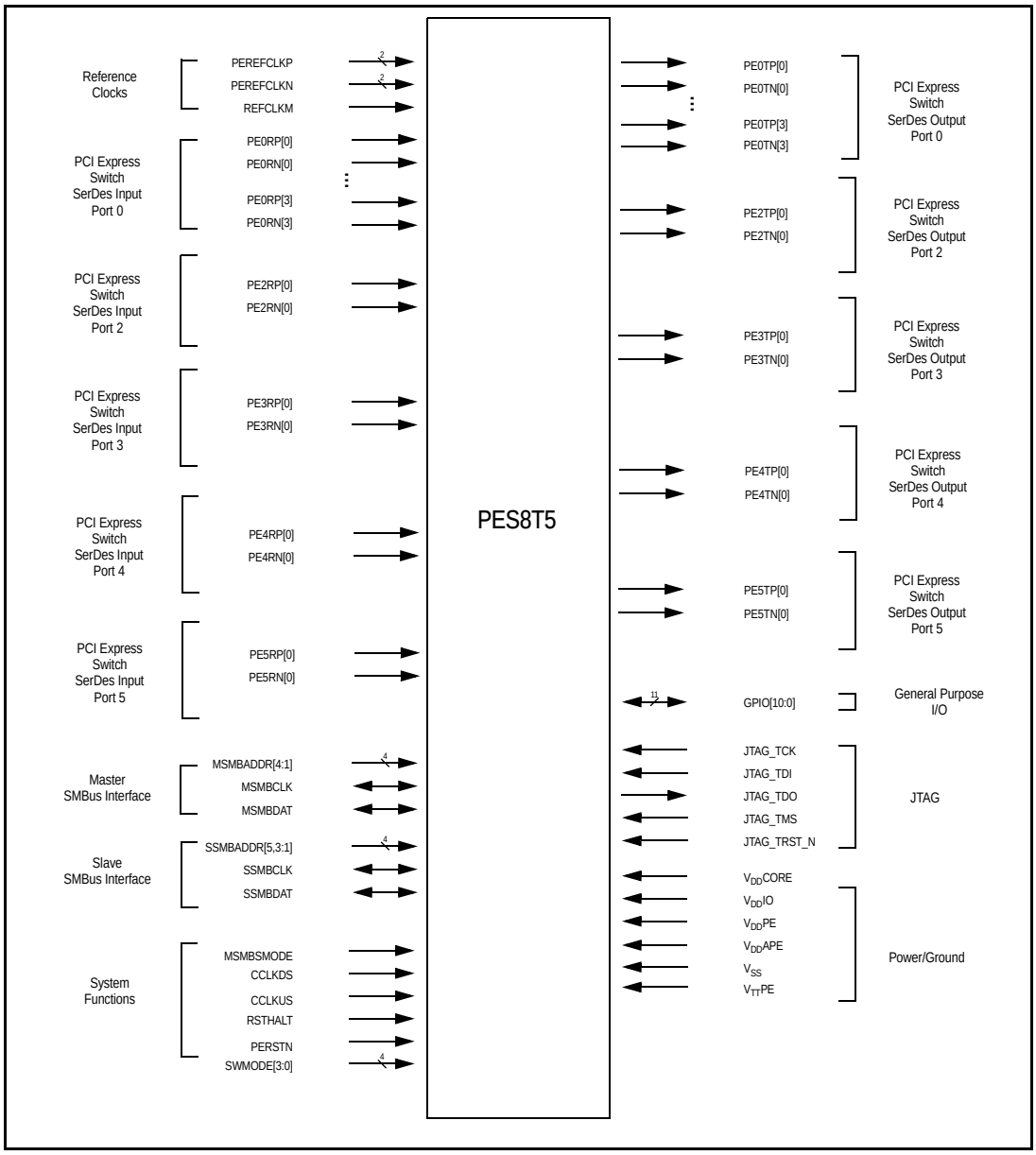


Figure 5 PES8T5 Logic Diagram

System Clock Parameters

Values based on systems running at recommended supply voltages and operating temperatures, as shown in Tables 13 and 14.

Parameter	Description	Min	Typical	Max	Unit
PEREFCLK					
$Refclk_{FREQ}$	Input reference clock frequency range	100		125[1]	MHz
$Refclk_{DC}$[2]	Duty cycle of input clock	40	50	60	%
T_R, T_F	Rise/Fall time of input clocks			0.2*RCUI	RCUI[3]
V_{SW}	Differential input voltage swing[4]	0.6		1.6	V
T_{jitter}	Input clock jitter (cycle-to-cycle)			125	ps
R_T	Termination Resistor		110		Ohms

Table 9 Input Clock Requirements

1. The input clock frequency will be either 100 or 125 MHz depending on signal REFCLKM.
2. ClkIn must be AC coupled. Use 0.01 — 0.1 µF ceramic capacitors.
3. RCUI (Reference Clock Unit Interval) refers to the reference clock period.
4. AC coupling required.

AC Timing Characteristics

Parameter	Description	Min[1]	Typical[1]	Max[1]	Units
PCIe Transmit					
UI	Unit Interval	399.88	400	400.12	ps
T_{TX-EYE}	Minimum Tx Eye Width	0.7	.9		UI
$T_{TX-EYE-MEDIAN-to-MAX-JITTER}$	Maximum time between the jitter median and maximum deviation from the median			0.15	UI
$T_{TX-RISE}$, $T_{TX-FALL}$	D+ / D- Tx output rise/fall time	50	90		ps
$T_{TX- IDLE-MIN}$	Minimum time in idle	50			UI
$T_{TX-IDLE-SET-TO-IDLE}$	Maximum time to transition to a valid Idle after sending an Idle ordered set			20	UI
$T_{TX-IDLE-TO-DIFF-DATA}$	Maximum time to transition from valid idle to diff data			20	UI
$T_{TX-SKEW}$	Transmitter data skew between any 2 lanes		500	1300	ps
PCIe Receive					
UI	Unit Interval	399.88	400	400.12	ps
T_{RX-EYE} (with jitter)	Minimum Receiver Eye Width (jitter tolerance)	0.4			UI
$T_{RX-EYE-MEDIUM TO MAX JITTER}$	Max time between jitter median & max deviation			0.3	UI
$T_{RX-IDLE-DET-DIFF-ENTER TIME}$	Unexpected Idle Enter Detect Threshold Integration Time			10	ms
$T_{RX-SKEW}$	Lane to lane input skew			20	ns

Table 10 PCIe AC Timing Characteristics

1. Minimum, Typical, and Maximum values meet the requirements under PCI Specification 1.1

Signal	Symbol	Reference Edge	Min	Max	Unit	Timing Diagram Reference
GPIO						
GPIO[10:0][1]	Tpw_13b[2]	None	50	—	ns	See Figure 6.

Table 11 GPIO AC Timing Characteristics

1. GPIO signals must meet the setup and hold times if they are synchronous or the minimum pulse width if they are asynchronous.

2. The values for this symbol were determined by calculation, not by testing.

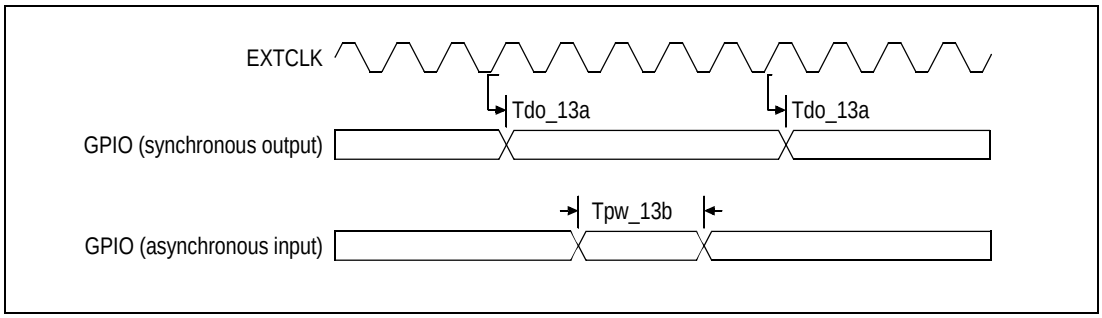


Figure 6 GPIO AC Timing Waveform

Signal	Symbol	Reference Edge	Min	Max	Unit	Timing Diagram Reference
JTAG						
JTAG_TCK	Tper_16a	none	50.0	—	ns	See Figure 7.
	Thigh_16a, Tlow_16a		10.0	25.0	ns	
JTAG_TMS[1], JTAG_TDI	Tsu_16b	JTAG_TCK rising	2.4	—	ns	
	Thld_16b		1.0	—	ns	
JTAG_TDO	Tdo_16c	JTAG_TCK falling	—	20	ns	
	Tdz_16c[2]		—	20	ns	
JTAG_TRST_N	Tpw_16d[2]	none	25.0	—	ns	

Table 12 JTAG AC Timing Characteristics

1. The JTAG specification, IEEE 1149.1, recommends that JTAG_TMS should be held at 1 while the signal applied at JTAG_TRST_N changes from 0 to 1. Otherwise, a race may occur if JTAG_TRST_N is deasserted (going from low to high) on a rising edge of JTAG_TCK when JTAG_TMS is low, because the TAP controller might go to either the Run-Test/Idle state or stay in the Test-Logic-Reset state.

2. The values for this symbol were determined by calculation, not by testing.

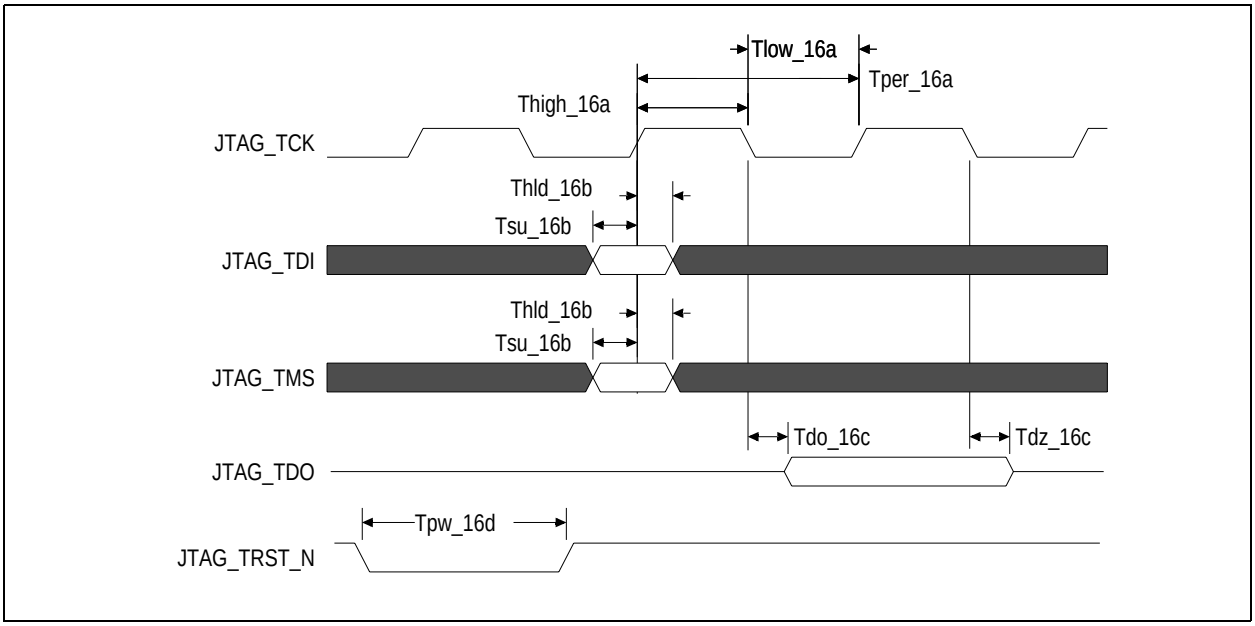


Figure 7 JTAG AC Timing Waveform

Recommended Operating Supply Voltages

Symbol	Parameter	Minimum	Typical	Maximum	Unit
V_{DD}CORE	Internal logic supply	0.9	1.0	1.1	V
V_{DD}I/O	I/O supply except for SerDes LVPECL/CML	3.0	3.3	3.6	V
V_{DD}PE	PCI Express Digital Power	0.9	1.0	1.1	V
V_{DD}APE	PCI Express Analog Power	0.9	1.0	1.1	V
V_{TT}PE	PCI Express Serial Data Transmit Termination Voltage	1.425	1.5	1.575	V
V_{SS}	Common ground	0	0	0	V

Table 13 PES8T5 Operating Voltages

Power-Up Sequence

This section describes the sequence in which various voltages must be applied to the part during power-up to ensure proper functionality. For the PES8T5, the power-up sequence must be as follows:

1. V_{DD}I/O — 3.3V
2. V_{DD}Core, V_{DD}PE, V_{DD}APE — 1.0V
3. V_{TT}PE — 1.5V

When powering up, each voltage level must ramp and stabilize prior to applying the next voltage in the sequence to ensure internal latch-up issues are avoided. There are no maximum time limitations in ramping to valid power levels. The power-down sequence must be in the reverse order of the power-up sequence.

Recommended Operating Temperature

Grade	Temperature
Commercial	0°C to +70°C Ambient

Table 14 PES8T5 Operating Temperatures

Power Consumption

Typical power is measured under the following conditions: 25°C Ambient, 35% total link usage on all ports, typical voltages defined in Table 13 (and also listed below).

Maximum power is measured under the following conditions: 70°C Ambient, 85% total link usage on all ports, maximum voltages defined in Table 13 (and also listed below).

Number of active Lanes per Port		Core Supply		PCIe Digital Supply		PCIe Analog Supply		PCIe Termination Supply		I/O Supply		Total	
		Typ 1.0V	Max 1.1V	Typ 1.0V	Max 1.1V	Typ 1.0V	Max 1.1V	Typ 1.5V	Max 1.575V	Typ 3.3V	Max 3.6V	Typ Power	Max Power
4/1/1/1/1	mA	641	792	637	732	331	352	201	225	1	1	1.9W	2.4W
	Watts	0.641	0.871	0.637	0.805	0.331	0.387	0.302	0.354	0.003	0.004		
1/1/1/1/1	mA	632	744	574	668	325	346	137	155	1	1	1.75W	2.2W
	Watts	0.632	0.818	0.574	0.735	0.325	0.381	0.206	0.244	0.003	0.0035		

Table 15 PES8T5 Power Consumption

Thermal Considerations

This section describes thermal considerations for the PES8T5 (19mm^2 BCG324 package). The data in Table 16 below contains information that is relevant to the thermal performance of the PES8T5 switch.

Symbol	Parameter	Value	Units	Conditions
$T_{J(max)}$	Junction Temperature	125	^{0}C	Maximum
$T_{A(max)}$	Ambient Temperature	70	^{0}C	Maximum for commercial-rated products
$\theta_{JA(effective)}$	Effective Thermal Resistance, Junction-to-Ambient	21.8	^{0}C/W	Zero air flow
		15.1	^{0}C/W	1 m/S air flow
		13.9	^{0}C/W	2 m/S air flow
θ_{JB}	Thermal Resistance, Junction-to-Board	11.4	^{0}C/W	
θ_{JC}	Thermal Resistance, Junction-to-Case	5.1	^{0}C/W	
P	Power Dissipation of the Device	2.4	Watts	Maximum

Table 16 Thermal Specifications for PES8T5, 19x19 mm BCG324 Package

Note: The parameter $\theta_{JA(eff)}$ is not the *absolute* thermal resistance for the package as defined by JEDEC (JESD-51). Because resistance can vary with the number of board layers, size of the board, and airflow, $\theta_{JA(eff)}$ is the *effective* thermal resistance. The values for effective θ_{JA} given above are based on a 10-layer, standard height, full length (4.3"x12.2") PCIe add-in card.

Heat Sink

Table 17 lists heat sink requirements for the PES8T5 under two common usage scenarios. As shown in this table, a heat sink is not required in most cases.

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Air Flow	Board Size	Board Layers	Heat Sink Requirement
Zero	Any	6 or more	No heat sink required
1 m/S or more	Any	Any	No heat sink required

Table 17 Heat Sink Requirements Based on Air Flow and Board Characteristics

Thermal Usage Examples

The junction-to-ambient thermal resistance is a measure of a device's ability to dissipate heat from the die to its surroundings in the absence of a heat sink. The general formula to determine θ_{JA} is:

$$\theta_{JA} = (T_J - T_A)/P$$

Thermal reliability of a device is generally assured when the actual value of T_J in the specific system environment being considered is less than the maximum T_J specified for the device. Using an ambient temperature of 70^oC and assuming a system with 1m/S airflow, the actual value of T_J is:

$$T_{J(actual)} = T_A + P * \theta_{JA(eff)} = 70^oC + 2.4W * 9.9W/^oC = 94^oC$$

The actual T_J of 94^oC is well below the maximum T_J of 125^oC specified for the device (shown in Table 16). Therefore, no heat sink is needed in this scenario. The formula is also useful from a system design perspective. It can be used to determine if a heat sink should be added to the device based on some desired value of T_J. For example, if for reliability purposes the desired T_J is 100^oC, then the maximum allowable T_A is:

$$T_{A(allowed)} = T_{J(desired)} - (P * \theta_{JA(effective)})$$
$$T_{A(allowed)} = 100^oC - (2.4W * 9.9W/^oC) = 100^oC - 24^oC = 76^oC$$

An appropriate level of increased air flow and/or a heat sink can be added to achieve this lower ambient temperature. Please contact ssdhelp@idt.com for further assistance.

DC Electrical Characteristics

Values based on systems running at recommended supply voltages, as shown in Table 13.

Note: See Table 8, Pin Characteristics, for a complete I/O listing.

I/O Type	Parameter	Description	Min[1]	Typ[1]	Max[1]	Unit	Conditions
Serial Link	PCIe Transmit						
	$V_{TX-DIFFp-p}$	Differential peak-to-peak output voltage	800		1200	mV	
	$V_{TX-DE-RATIO}$	De-emphasized differential output voltage	-3		-4	dB	
	$V_{TX-DC-CM}$	DC Common mode voltage	-0.1	1	3.7	V	
	$V_{TX-CM-ACP}$	RMS AC peak common mode output voltage			20	mV	
	$V_{TX-CM-DC-active-idle-delta}$	Abs delta of DC common mode voltage between L0 and idle			100	mV	
	$V_{TX-CM-DC-line-delta}$	Abs delta of DC common mode voltage between D+ and D-			25	mV	
	$V_{TX-Idle-DiffP}$	Electrical idle diff peak output			20	mV	
	$V_{TX-RCV-Detect}$	Voltage change during receiver detection			600	mV	
	$RL_{TX-DIFF}$	Transmitter Differential Return loss	12			dB	
	RL_{TX-CM}	Transmitter Common Mode Return loss	6			dB	
	$Z_{TX-DEFF-DC}$	DC Differential TX impedance	80	100	120	Ω	
	Z_{OSE}	Single ended TX Impedance	40	50	60	Ω	
	Transmitter Eye Diagram	TX Eye Height (De-emphasized bits)	505	650		mV	
	Transmitter Eye Diagram	TX Eye Height (Transition bits)	800	950		mV	
	PCIe Receive						
	$V_{RX-DIFFp-p}$	Differential input voltage (peak-to-peak)	175		1200	mV	
	$V_{RX-CM-AC}$	Receiver common-mode voltage for AC coupling			150	mV	
	$RL_{RX-DIFF}$	Receiver Differential Return Loss	15			dB	
	RL_{RX-CM}	Receiver Common Mode Return Loss	6			dB	
	$Z_{RX-DIFF-DC}$	Differential input impedance (DC)	80	100	120	Ω	
	$Z_{RX-COMM-DC}$	Single-ended input impedance	40	50	60	Ω	
	$Z_{RX-COMM-HIGH-Z-DC}$	Powered down input common mode impedance (DC)	200k	350k		Ω	
	$V_{RX-IDLE-DET-DIFFp-p}$	Electrical idle detect threshold	65		175	mV	
PCIe REFCLK							
	C_{IN}	Input Capacitance	1.5	—		pF	

Table 18 DC Electrical Characteristics (Part 1 of 2)

I/O Type	Parameter	Description	Min[1]	Typ[1]	Max[1]	Unit	Conditions
Other I/Os							
LOW Drive Output	I_{OL}		—	2.5	—	mA	V_{OL} = 0.4v
	I_{OH}		—	-5.5	—	mA	V_{OH} = 1.5V
High Drive Output	I_{OL}		—	12.0	—	mA	V_{OL} = 0.4v
	I_{OH}		—	-20.0	—	mA	V_{OH} = 1.5V
Schmitt Trigger Input (STI)	V_{IL}		-0.3	—	0.8	V	—
	V_{IH}		2.0	—	V_{DD}IO + 0.5	V	—
Input	V_{IL}		-0.3	—	0.8	V	—
	V_{IH}		2.0	—	V_{DD}IO + 0.5	V	—
Capacitance	C_{IN}		—	—	8.5	pF	—
Leakage	Inputs		—	—	± 10	µA	V_{DD}I/O (max)
	$I/O_{LEAK\ W/O}$ Pull-ups/downs		—	—	± 10	µA	V_{DD}I/O (max)
	$I/O_{LEAK\ WITH}$ Pull-ups/downs		—	—	± 80	µA	V_{DD}I/O (max)

Table 18 DC Electrical Characteristics (Part 2 of 2)

1. Minimum, Typical, and Maximum values meet the requirements under PCI Specification 1.1.

Package Pinout — 324-BGA Signal Pinout for PES8T5

The following table lists the pin numbers and signal names for the PES8T5 device.

Pin	Function	Alt	Pin	Function	Alt	Pin	Function	Alt	Pin	Function	Alt
A1	V_{SS}		B17	V_{DD}CORE		D15	V_{DD}CORE		F13	V_{SS}	
A2	V_{SS}		B18	V_{DD}CORE		D16	SWMODE_1		F14	V_{SS}	
A3	PE0RP03		C1	V_{SS}		D17	SWMODE_0		F15	V_{DD}CORE	
A4	V_{DD}CORE		C2	CCLKUS		D18	CCLKDS		F16	V_{SS}	
A5	PE0TN03		C3	SSMBDAT		E1	SSMBADDR_3		F17	GPIO_00	1
A6	V_{DD}CORE		C4	V_{DD}CORE		E2	SSMBADDR_2		F18	GPIO_01	1
A7	PE0TP02		C5	V_{SS}		E3	MSMBDAT		G1	MSMBADDR_2	
A8	V_{DD}CORE		C6	V_{TT}PE		E4	V_{SS}		G2	JTAG_TRST_N	
A9	PE0RN02		C7	V_{SS}		E5	V_{DD}CORE		G3	MSMBADDR_1	
A10	V_{DD}CORE		C8	V_{TT}PE		E6	V_{DD}PE		G4	V_{SS}	
A11	PE0RP01		C9	V_{SS}		E7	V_{SS}		G5	V_{DD}IO	
A12	V_{DD}CORE		C10	V_{TT}PE		E8	V_{DD}PE		G6	V_{SS}	
A13	PE0TP01		C11	V_{SS}		E9	V_{SS}		G7	V_{SS}	
A14	V_{DD}CORE		C12	V_{TT}PE		E10	V_{DD}PE		G8	V_{SS}	
A15	V_{DD}CORE		C13	V_{DD}CORE		E11	V_{SS}		G9	V_{SS}	
A16	PE0TN00		C14	PE0RN00		E12	V_{DD}PE		G10	V_{DD}IO	
A17	V_{SS}		C15	PE0RP00		E13	V_{SS}		G11	V_{SS}	
A18	V_{SS}		C16	V_{DD}CORE		E14	V_{DD}CORE		G12	V_{DD}CORE	
B1	V_{DD}IO		C17	V_{DD}IO		E15	SWMODE_2		G13	V_{SS}	
B2	V_{DD}IO		C18	V_{DD}IO		E16	SWMODE_3		G14	V_{DD}IO	
B3	PE0RN03		D1	SSMBCLK		E17	RSTHALT		G15	V_{SS}	
B4	V_{SS}		D2	SSMBADDR_5		E18	PERSTN		G16	GPIO_04	1
B5	PE0TP03		D3	SSMBADDR_1		F1	MSMBADDR_3		G17	GPIO_03	1
B6	V_{SS}		D4	V_{DD}CORE		F2	MSMBADDR_4		G18	GPIO_02	1
B7	PE0TN02		D5	V_{SS}		F3	MSMBCLK		H1	JTAG_TDO	
B8	V_{SS}		D6	V_{DD}APE		F4	V_{DD}CORE		H2	JTAG_TMS	
B9	PE0RP02		D7	V_{SS}		F5	V_{SS}		H3	JTAG_TCK	
B10	V_{SS}		D8	V_{DD}APE		F6	V_{DD}CORE		H4	V_{DD}CORE	
B11	PE0RN01		D9	V_{SS}		F7	V_{SS}		H5	V_{DD}IO	
B12	V_{SS}		D10	V_{DD}APE		F8	V_{DD}CORE		H6	V_{SS}	
B13	PE0TN01		D11	V_{SS}		F9	V_{SS}		H7	V_{DD}CORE	
B14	V_{SS}		D12	V_{DD}APE		F10	V_{DD}CORE		H8	V_{SS}	
B15	V_{SS}		D13	V_{SS}		F11	V_{SS}		H9	V_{DD}CORE	
B16	PE0TP00		D14	V_{DD}CORE		F12	V_{SS}		H10	V_{DD}CORE	

Table 19 PES8T5 324-pin Signal Pin-Out (Part 1 of 3)

Pin	Function	Alt	Pin	Function	Alt	Pin	Function	Alt	Pin	Function	Alt
H11	V_{SS}		K12	V_{SS}		M13	V_{DD}CORE		P14	GPIO_09	1
H12	V_{DD}CORE		K13	V_{SS}		M14	V_{SS}		P15	V_{DD}APE	
H13	V_{SS}		K14	V_{SS}		M15	V_{DD}PE		P16	V_{DD}PE	
H14	V_{DD}IO		K15	V_{DD}PE		M16	V_{SS}		P17	V_{SS}	
H15	V_{DD}CORE		K16	V_{SS}		M17	V_{SS}		P18	V_{SS}	
H16	GPIO_07	1	K17	V_{SS}		M18	V_{SS}		R1	PE3RN00	
H17	GPIO_06		K18	V_{DD}CORE		N1	V_{DD}CORE		R2	PE3RP00	
H18	GPIO_05		L1	PE2TP00		N2	V_{DD}CORE		R3	V_{DD}PE	
J1	PE2RN00		L2	PE2TN00		N3	V_{TT}PE		R4	V_{DD}APE	
J2	PE2RP00		L3	V_{TT}PE		N4	V_{DD}APE		R5	V_{DD}IO	
J3	JTAG_TDI		L4	V_{DD}PE		N5	V_{SS}		R6	V_{DD}PE	
J4	V_{SS}		L5	V_{SS}		N6	V_{SS}		R7	V_{SS}	
J5	V_{DD}IO		L6	V_{DD}CORE		N7	V_{SS}		R8	V_{DD}PE	
J6	V_{DD}CORE		L7	V_{DD}CORE		N8	V_{SS}		R9	V_{SS}	
J7	V_{SS}		L8	V_{DD}CORE		N9	V_{SS}		R10	V_{DD}PE	
J8	V_{SS}		L9	V_{DD}CORE		N10	V_{SS}		R11	V_{SS}	
J9	V_{DD}CORE		L10	V_{DD}CORE		N11	V_{SS}		R12	V_{DD}PE	
J10	V_{DD}CORE		L11	V_{DD}CORE		N12	V_{SS}		R13	V_{DD}IO	
J11	V_{SS}		L12	V_{DD}CORE		N13	V_{SS}		R14	GPIO_10	1
J12	V_{SS}		L13	V_{DD}CORE		N14	GPIO_08		R15	REFCLKM	
J13	V_{DD}CORE		L14	V_{SS}		N15	V_{DD}APE		R16	V_{DD}PE	
J14	V_{DD}IO		L15	V_{DD}PE		N16	V_{TT}PE		R17	PE4TP00	
J15	V_{SS}		L16	V_{TT}PE		N17	V_{DD}CORE		R18	PE4TN00	
J16	V_{SS}		L17	PE5RN00		N18	V_{DD}CORE		T1	V_{DD}CORE	
J17	PE5TP00		L18	PE5RP00		P1	V_{SS}		T2	V_{SS}	
J18	PE5TN00		M1	V_{SS}		P2	V_{SS}		T3	V_{DD}APE	
K1	V_{DD}CORE		M2	V_{SS}		P3	V_{DD}PE		T4	V_{SS}	
K2	V_{SS}		M3	V_{SS}		P4	V_{DD}APE		T5	V_{DD}CORE	
K3	V_{SS}		M4	V_{DD}PE		P5	V_{SS}		T6	V_{SS}	
K4	V_{DD}PE		M5	V_{SS}		P6	V_{SS}		T7	V_{SS}	
K5	V_{DD}CORE		M6	V_{DD}CORE		P7	V_{SS}		T8	V_{DD}APE	
K6	V_{SS}		M7	V_{SS}		P8	V_{DD}CORE		T9	V_{SS}	
K7	V_{SS}		M8	V_{SS}		P9	V_{DD}IO		T10	V_{DD}APE	
K8	V_{SS}		M9	V_{DD}CORE		P10	V_{DD}CORE		T11	V_{SS}	
K9	V_{SS}		M10	V_{DD}CORE		P11	V_{DD}CORE		T12	V_{SS}	
K10	V_{SS}		M11	V_{SS}		P12	V_{SS}		T13	V_{SS}	
K11	V_{SS}		M12	V_{SS}		P13	V_{DD}IO		T14	V_{DD}IO	

Table 19 PES8T5 324-pin Signal Pin-Out (Part 2 of 3)

Pin	Function	Alt	Pin	Function	Alt	Pin	Function	Alt	Pin	Function	Alt
T15	MSMBSMODE		U7	V_{SS}		U17	PE4RN00		V9	V_{SS}	
T16	V_{DD}APE		U8	V_{TT}PE		U18	PE4RP00		V10	V_{SS}	
T17	V_{SS}		U9	V_{SS}		V1	V_{SS}		V11	V_{SS}	
T18	V_{DD}CORE		U10	V_{TT}PE		V2	V_{SS}		V12	V_{SS}	
U1	PE3TP00		U11	V_{SS}		V3	PEREFCLKP1		V13	V_{SS}	
U2	PE3TN00		U12	V_{SS}		V4	PEREFCLKN1		V14	V_{SS}	
U3	V_{DD}PE		U13	V_{SS}		V5	V_{SS}		V15	PEREFCLKP2	
U4	V_{SS}		U14	V_{SS}		V6	V_{SS}		V16	PEREFCLKN2	
U5	V_{SS}		U15	V_{DD}APE		V7	V_{SS}		V17	V_{SS}	
U6	V_{SS}		U16	V_{DD}PE		V8	V_{SS}		V18	V_{SS}	

Table 19 PES8T5 324-pin Signal Pin-Out (Part 3 of 3)

Alternate Signal Functions

Pin	GPIO	Alternate
F17	GPIO_00	P2RSTN
F18	GPIO_01	P4RSTN
G18	GPIO_02	IOEXPINTN0
G17	GPIO_03	IOEXPINTN1
G16	GPIO_04	IOEXPINTN2
H16	GPIO_07	GPEN
P14	GPIO_09	P3RSTN
R14	GPIO_10	P5RSTN

Table 20 PES8T5 Alternate Signal Functions

Power Pins

V_{DD}Core	V_{DD}Core	V_{DD}Core	V_{DD}IO	V_{DD}PE	V_{DD}APE	V_{TT}PE
A4	F10	L10	B1	E6	D6	C6
A6	F15	L11	B2	E8	D8	C8
A8	G12	L12	C17	E10	D10	C10
A10	H4	L13	C18	E12	D12	C12
A12	H7	M6	G5	K4	N4	L3
A14	H9	M9	G10	K15	N15	L16
A15	H10	M10	G14	L4	P4	N3
B17	H12	M13	H5	L15	P15	N16
B18	H15	N1	H14	M4	R4	U8
C4	J6	N2	J5	M15	T3	U10
C13	J9	N17	J14	P3	T8	
C16	J10	N18	P9	P16	T10	
D4	J13	P8	P13	R3	T16	
D14	K1	P10	R5	R6	U15	
D15	K5	P11	R13	R8		
E5	K18	T1	T14	R10		
E14	L6	T5		R12		
F4	L7	T18		R16		
F6	L8			U3		
F8	L9			U16		

Table 21 PES8T5 Power Pins

Ground Pins

V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}
A1	F7	K3	N6	T17
A2	F9	K6	N7	U4
A17	F11	K7	N8	U5
A18	F12	K8	N9	U6
B4	F13	K9	N10	U7
B6	F14	K10	N11	U9
B8	F16	K11	N12	U11
B10	G4	K12	N13	U12
B12	G6	K13	P1	U13
B14	G7	K14	P2	U14
B15	G8	K16	P5	V1
C1	G9	K17	P6	V2
C5	G11	L5	P7	V5
C7	G13	L14	P12	V6
C9	G15	M1	P17	V7
C11	H6	M2	P18	V8
D5	H8	M3	R7	V9
D7	H11	M5	R9	V10
D9	H13	M7	R11	V11
D11	J4	M8	T2	V12
D13	J7	M11	T4	V13
E4	J8	M12	T6	V14
E7	J11	M14	T7	V17
E9	J12	M16	T9	V18
E11	J15	M17	T11	
E13	J16	M18	T12	
F5	K2	N5	T13	

Table 22 PES8T5 Ground Pins

Signals Listed Alphabetically

Signal Name	I/O Type	Location	Signal Category
CCLKDS	I	D18	System
CCLKUS	I	C2	
GPIO_00	I/O	F17	General Purpose Input/Output
GPIO_01	I/O	F18	
GPIO_02	I/O	G18	
GPIO_03	I/O	G17	
GPIO_04	I/O	G16	
GPIO_05	I/O	H18	
GPIO_06	I/O	H17	
GPIO_07	I/O	H16	
GPIO_08	I/O	N14	
GPIO_09	I/O	P14	
GPIO_10	I/O	R14	
JTAG_TCK	I	H3	JTAG
JTAG_TDI	I	J3	
JTAG_TDO	O	H1	
JTAG_TMS	I	H2	
JTAG_TRST_N	I	G2	
MSMBADDR_1	I	G3	SMBus
MSMBADDR_2	I	G1	
MSMBADDR_3	I	F1	
MSMBADDR_4	I	F2	
MSMBCLK	I/O	F3	
MSMBDAT	I/O	E3	
MSMBSMODE	I	T15	System
PE0RN00	I	C14	PCI Express
PE0RN01	I	B11	
PE0RN02	I	A9	
PE0RN03	I	B3	
PE0RP00	I	C15	
PE0RP01	I	A11	
PE0RP02	I	B9	
PE0RP03	I	A3	
PE0TN00	O	A16	

Table 23 89PES8T5 Alphabetical Signal List (Part 1 of 3)

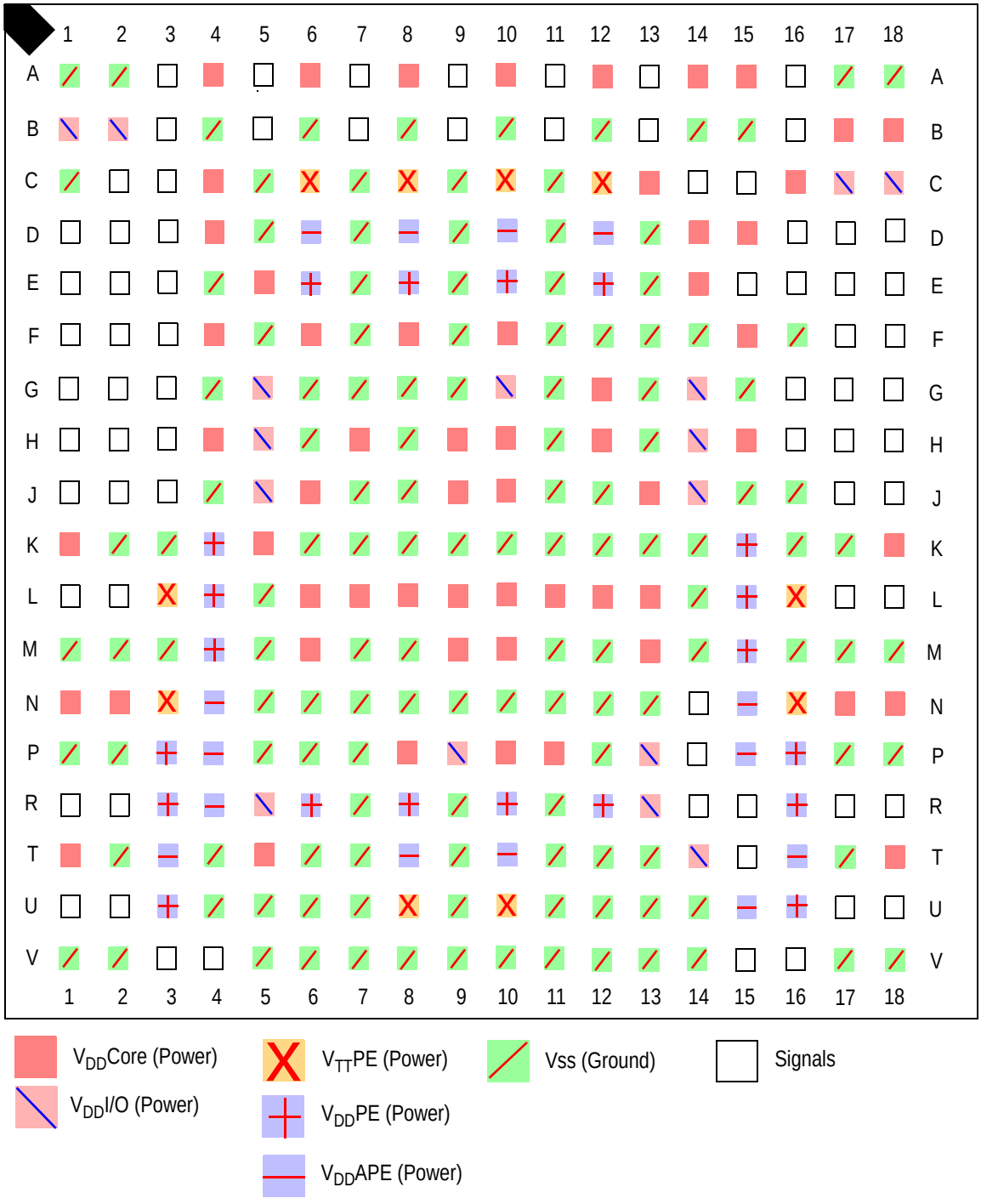
Signal Name	I/O Type	Location	Signal Category
PE0TN01	O	B13	PCI Express (cont.)
PE0TN02	O	B7	
PE0TN03	O	A5	
PE0TP00	O	B16	
PE0TP01	O	A13	
PE0TP02	O	A7	
PE0TP03	O	B5	
PE2RN00	I	J1	
PE2RP00	I	J2	
PE2TN00	O	L2	
PE2TP00	O	L1	
PE3RN00	I	R1	
PE3RP00	I	R2	
PE3TN00	O	U2	
PE3TP00	O	U1	
PE4RN00	I	U17	
PE4RP00	I	U18	
PE4TN00	O	R18	
PE4TP00	O	R17	
PE5RN00	I	L17	
PE5RP00	I	L18	
PE5TN00	O	J18	
PE5TP00	O	J17	
PEREFCLKN1	I	V4	
PEREFCLKN2	I	V16	
PEREFCLKP1	I	V3	
PEREFCLKP2	I	V15	
PERSTN	I	E18	System
REFCLKM	I	R15	PCI Express
RSTHALT	I	E17	System
SSMBADDR_1	I	D3	SMBus
SSMBADDR_2	I	E2	
SSMBADDR_3	I	E1	
SSMBADDR_5	I	D2	
SSMBCLK	I/O	D1	
SSMBDAT	I/O	C3	

Table 23 89PES8T5 Alphabetical Signal List (Part 2 of 3)

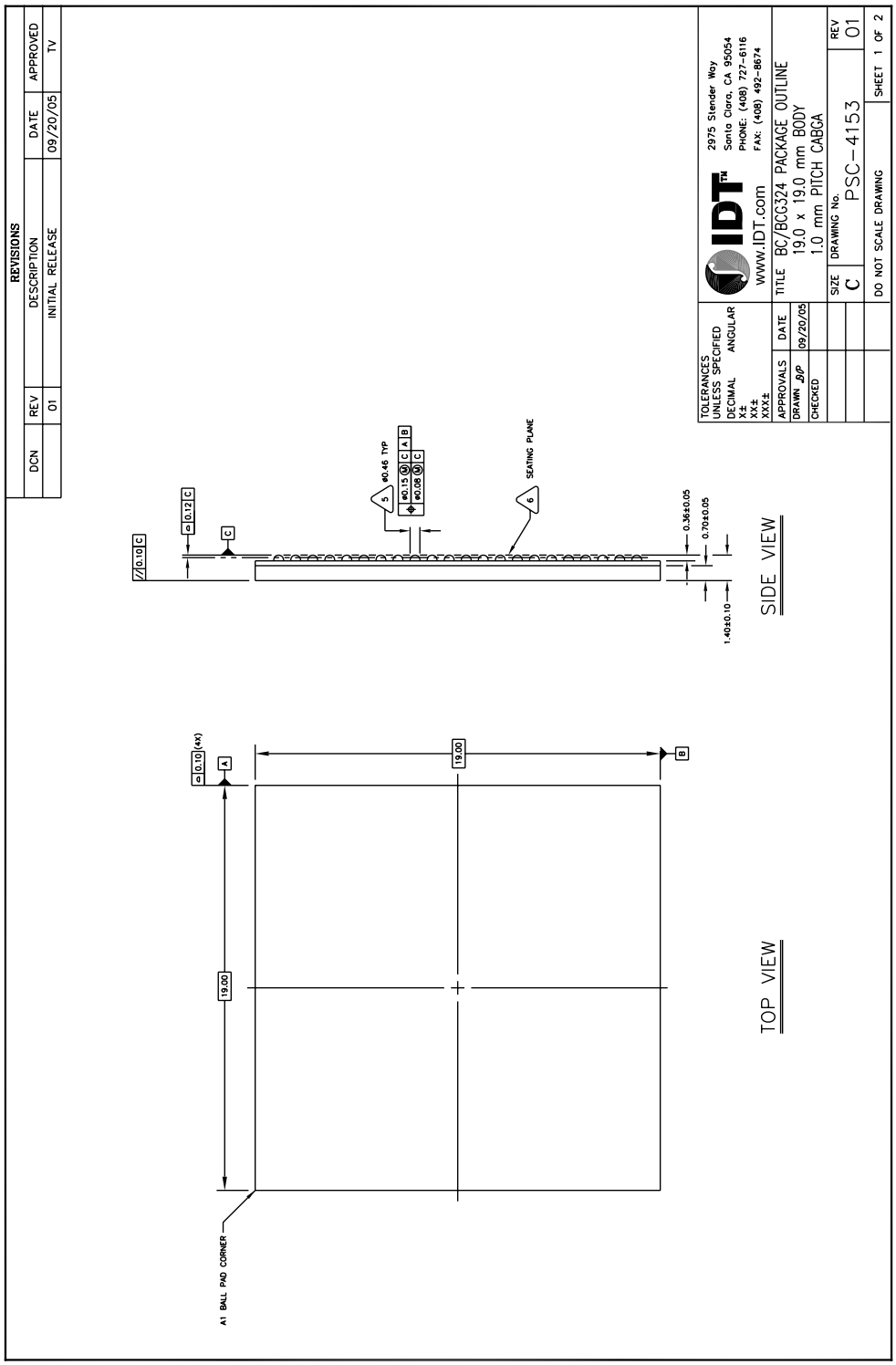
Signal Name	I/O Type	Location	Signal Category
SWMODE_0	I	D17	System
SWMODE_1	I	D16	
SWMODE_2	I	E15	
SWMODE_3	I	E16	
V_{DD}CORE, V_{DD}APE, V_{DD}IO, V_{DD}PE, V_{TT}PE	See Table 21 for a listing of power pins.		
V_{SS}	See Table 22 for a listing of ground pins.		

Table 23 89PES8T5 Alphabetical Signal List (Part 3 of 3)

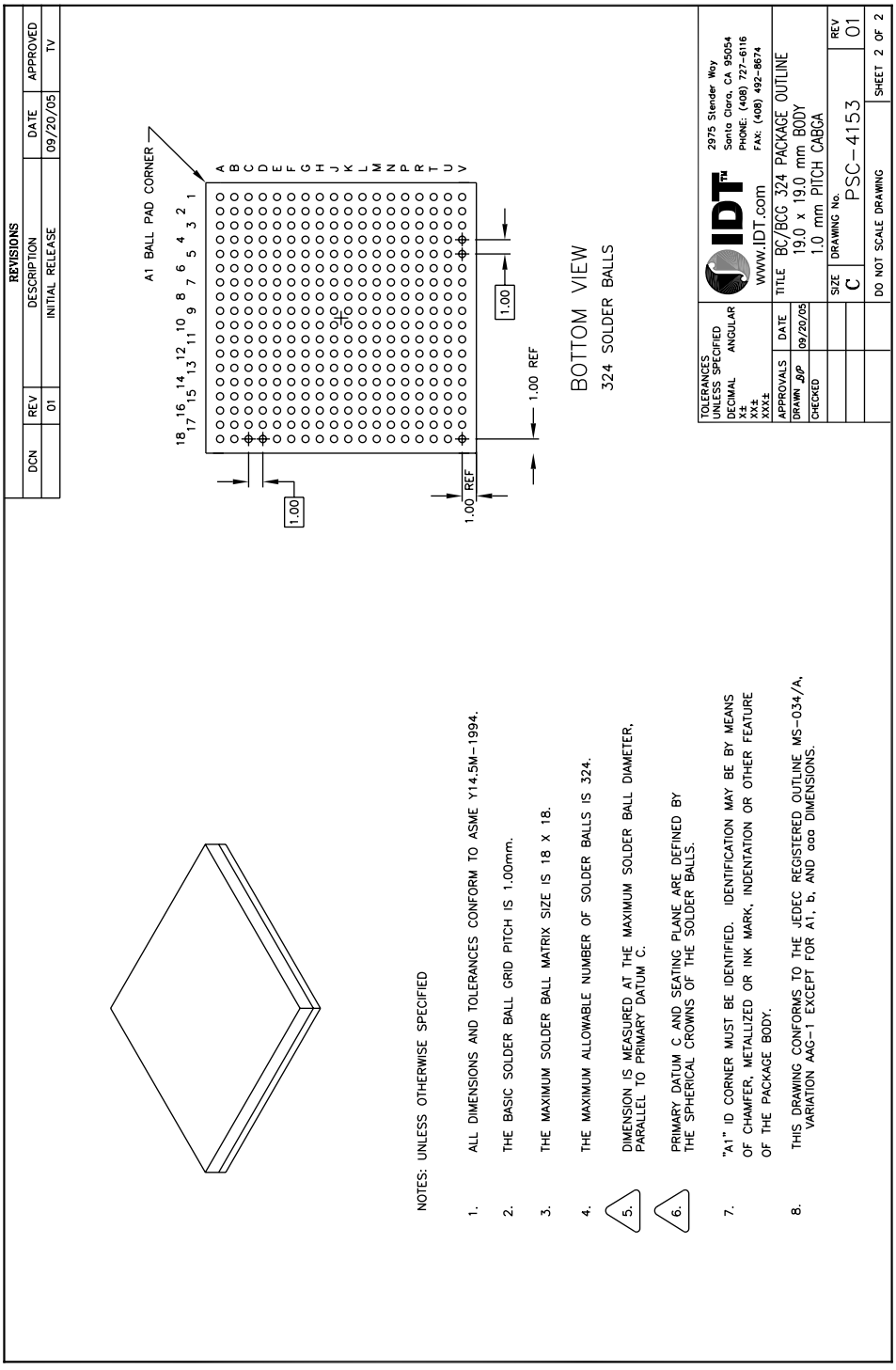
PES8T5 Pinout — Top View



PES8T5 Package Drawing — 324-Pin BC324/BCG324



PES8T5 Package Drawing — Page Two



Revision History

February 8, 2007: Initial publication.

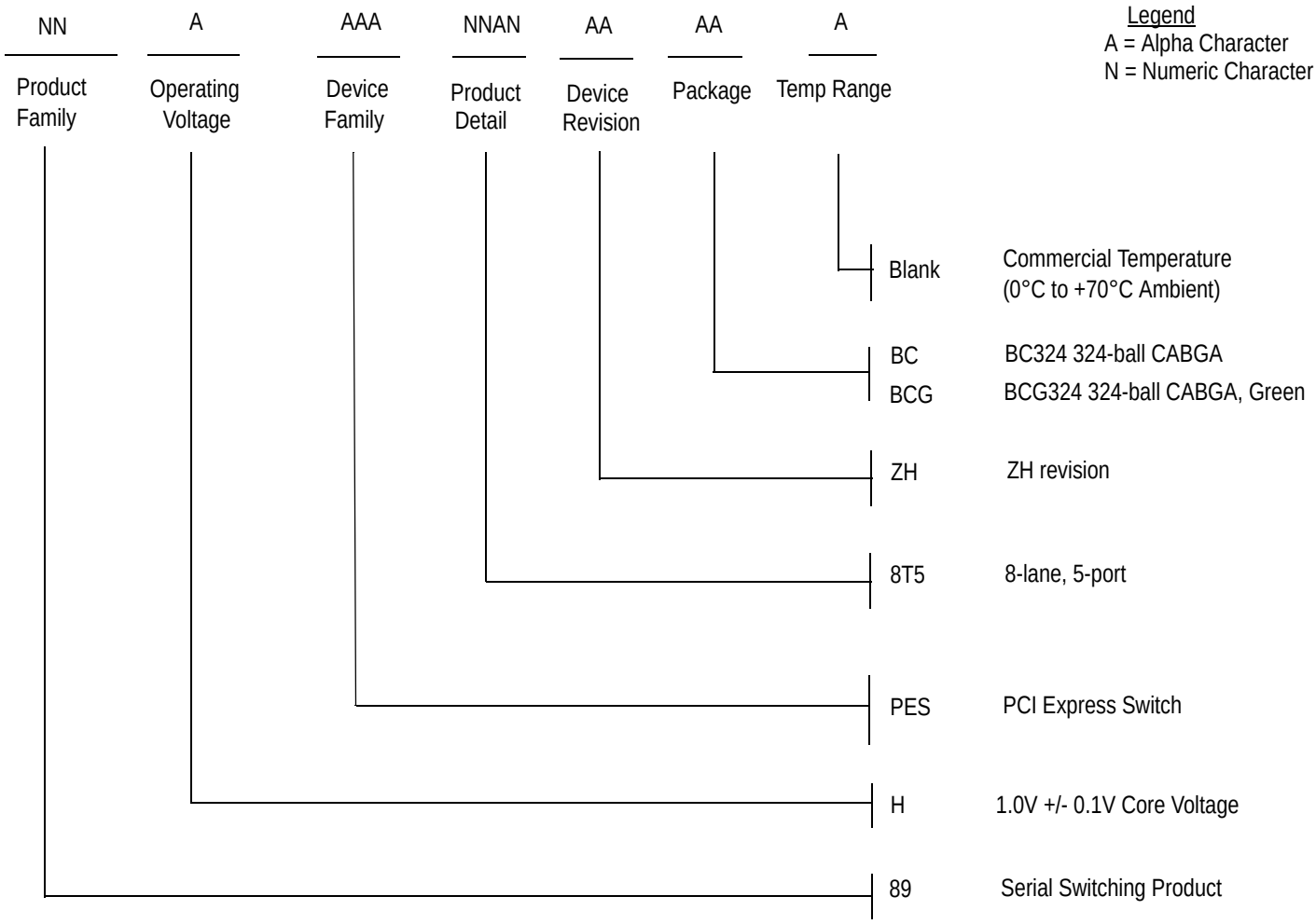
April 4, 2007: In Table 3, revised description for MSMBCLK signal.

May 30, 2007: Changed device revision in Ordering Information from ZD to ZH.

November 14, 2007: Added new parameter, Termination Resistor, to Table 9, Input Clock Requirements.

March 27, 2008: In Table 16, Thermal Specifications, added θ_{JB} and θ_{JC} parameters and revised the values for θ_{JA}.

Ordering Information



Valid Combinations

89HPES8T5ZHBC	324-pin BC324 package, Commercial Temperature
89HPES8T5ZHBCG	324-pin Green BCG324 package, Commercial Temperature

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